General Description

EZ-PD™ CCG4M is a USB Type-C dual port controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4M provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks and PCs. EZ-PD CCG4M uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors R_P and R_D as well as a 6:4 mux for USB 3.0 and DisplayPort signals.

Applications

- Notebooks and PCs

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM
- In-system reprogrammable

Integrated Digital Blocks

- Four integrated timers or counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable I^{2}C, SPI, or UART functionality

Integrated 6:4 Mux

- Six differential channels to 4 differential channels
- Multiplexes USB 3.0 (5 Gbps) and DisplayPort 1.2 (5.4 Gbps) signals to the USB Type-C connector
- With DisplayPort 1.2, AUX signals are multiplexed to SBU pins

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Type-C Support

- Two integrated transceivers (baseband PHY)
- Integrated UFP (R_D) and current sources for DFP (R_P) on both Type-C ports
- Integrated dead battery termination for DRP applications
- Supports two USB Type-C ports

Low-Power Operation

- 2.7-V to 5.5-V operation
- Integrated VCONN FETs to power EMCA cables
- Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os

System-Level ESD on CC Pins

- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C
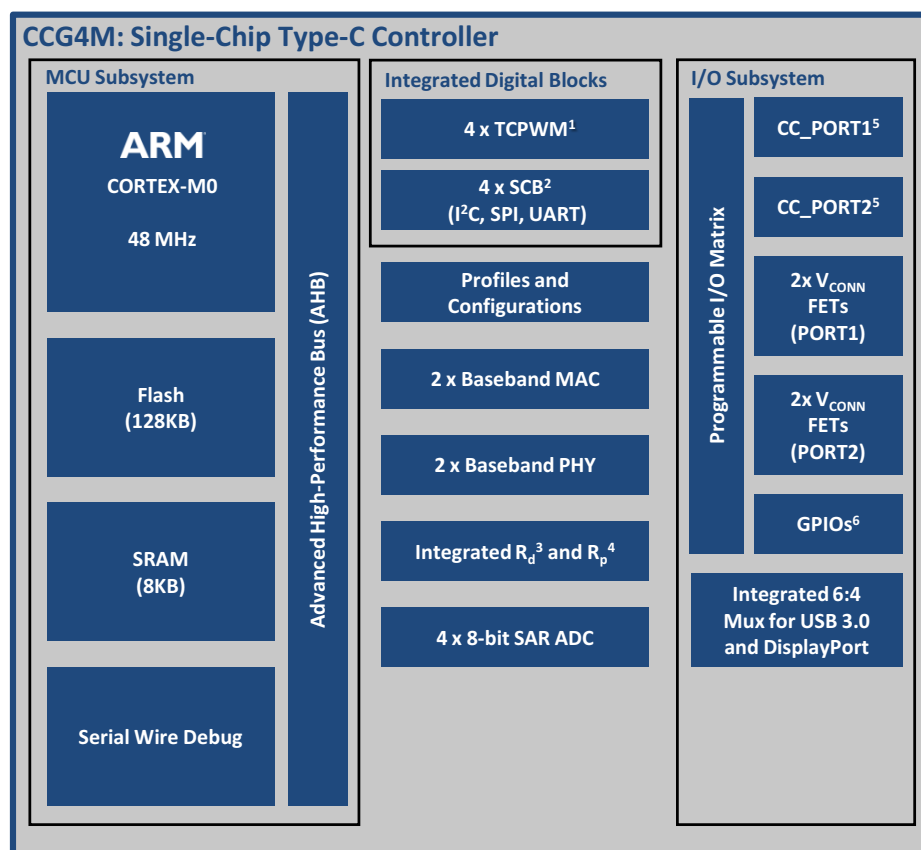
Hot Swappable I/Os

- Port 1 I2C pins and CC1, CC2 pins are hot-swappable

Packages

- 6.0 mm × 6.0 mm, 0.5 mm, 96-ball BGA
- Supports industrial temperature range (–40 °C to +85 °C)

Logic Block Diagram

CCG4M: Single-Chip Type-C Controller

MCU Subsystem

ARM
CORTEX-M0
48 MHz

Flash (128KB)

SRAM (8KB)

Serial Wire Debug

Advanced High-Performance Bus (AHB)

Integrated Digital Blocks

4 x TCPWM[1]

4 x SCB[2] (I^2C, SPI, UART)

Profiles and Configurations

2 x Baseband MAC

2 x Baseband PHY

Integrated R_d[3] and R_p[4]

4 x 8-bit SAR ADC

I/O Subsystem

Programmable I/O Matrix

CC_PORT1[5]

CC_PORT2[5]

2x V_{CONN} FETs (PORT1)

2x V_{CONN} FETs (PORT2)

GPIOs[6]

Integrated 6:4 Mux for USB 3.0 and DisplayPort

[1] Timer, counter, pulse-width modulation block
[2] Serial communication block configurable as UART, SPI, or I^2C
[3] Termination resistor denoting a UFP
[4] Current source to indicate a DFP
[5] Configuration Channel
[6] General-purpose input/output

Contents

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG4M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG4M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG4M device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz and with 0-WS access time at 16 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG4M has a USB-PD subsystem consisting of two USB Type-C baseband transceivers and physical-layer logic. These transceivers perform the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V analog front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG4M solution. R_D is used to identify EZ-PD CCG4M as a UFP in a DRP application. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the USB Type-C spec. EZ-PD CCG4M responds to all USB-PD communication.

The USB-PD sub-system contains two 8-bit SAR (Successive Approximation Register) ADC per port for analog to digital conversions. The ADC includes a 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global Analog Multiplex Busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux busses.

Figure 1. USB-PD Subsystem
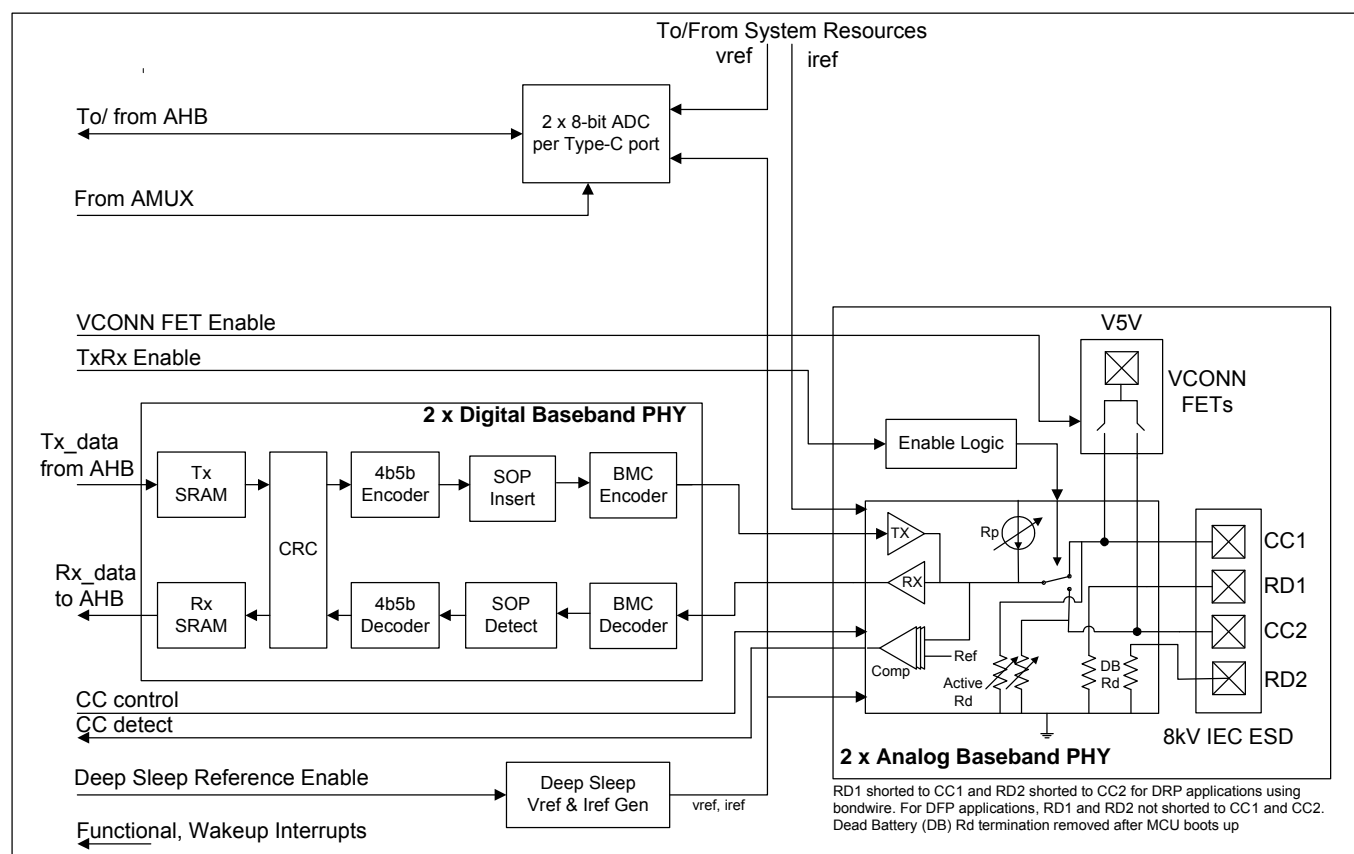
System Resources

Power System

The power system is described in detail in the section "Power" on page 16. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). EZ-PD CCG4M can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG4M provides Sleep and Deep Sleep low-power modes.

Clock System

The clock system for EZ-PD CCG4M consists of the Internal Main Oscillator (IMO) and the Internal Low-power Oscillator (ILO).

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG4M has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a master or a slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG4M and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB2, SCB3, and SCB4 blocks of EZ-PD CCG4M are not completely compliant with the I^2C spec in the following:

■ The GPIO cells for SCB2, SCB3, and SCB4 I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

■ Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.

■ Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG4M has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG4M has 30 GPIOs that includes the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from only SCB 1 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

■ Seven drive strength modes:
   ❏ Input only
   ❏ Weak pull-up with strong pull-down
   ❏ Strong pull-up with weak pull-down
   ❏ Open drain with strong pull-down
   ❏ Open drain with strong pull-up
   ❏ Strong pull-up with strong pull-down
   ❏ Weak pull-up with weak pull-down

■ Input threshold select (CMOS or LVTTL)

■ Individual control of input and output buffer enabling/disabling in addition to the drive strength modes

■ Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)

■ Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Mux

EZ-PD CCG4M integrates a 6:4 differential channel mux used for switching USB 3.0 and/or DP 1.2 signals through the USB Type-C connector. CCG4M can mux the following signals to the USB Type-C connector:

■ USB 3.0 signals only

■ One lane of USB 3.0 signals and two lanes of DP 1.2 signals

■ Four lanes of DP 1.2 signals

In addition, the AUX signals are also multiplexed to the SBU pins. The insertion loss is –1.2 dB and the return loss –21 dB at 5-Gbps USB 3.0 speed.

Pinouts

Table 1. Pinout for CYPD4255-96BZXI

Group	Name	Ball Location	Description
USB Type-C Port 1	CC1_P1	K2	USB PD connector detect/Configuration Channel 1
	CC2_P1	H2	USB PD connector detect/Configuration Channel 2
USB Type-C Port 2	CC1_P2	K9	USB PD connector detect/Configuration Channel 1
	CC2_P2	K10	USB PD connector detect/Configuration Channel 2
Mux	TX_P	L11	Differential USB 3.0 transmit signal
	TX_M	K11	Differential USB 3.0 transmit signal
	RX_P	H11	Differential USB 3.0 receive signal
	RX_M	G11	Differential USB 3.0 receive signal
	TX1_P	A8	Differential transmit signal 1
	TX1_M	A7	Differential transmit signal 1
	RX1_P	A11	Differential receive signal 1
	RX1_M	A10	Differential receive signal 1
	TX2_P	A4	Differential transmit signal 2
	TX2_M	A5	Differential transmit signal 2
	RX2_P	A1	Differential receive signal 2
	RX2_M	A2	Differential receive signal 2
	AUX_P	F11	Auxiliary signal for DisplayPort
	AUX_M	E11	Auxiliary signal for DisplayPort
	DP0_P	C1	Differential DisplayPort 0 signal
	DP0_M	D1	Differential DisplayPort 0 signal
	DP1_P	F1	Differential DisplayPort 1 signal
	DP1_M	G1	Differential DisplayPort 1 signal
	DP2_P	J1	Differential DisplayPort 2 signal
	DP2_M	K1	Differential DisplayPort 2 signal
	DP3_P	L2	Differential DisplayPort 3 signal
	DP3_M	L3	Differential DisplayPort 3 signal
	SBU1	B11	Sideband Use signal
	SBU2	C11	Sideband Use signal31
VBUS Control	VBUS_P_CTRL_P1/ P1.6	K3	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 1
	VBUS_C_CTRL_P1/P1.7	K4	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 1 or SCB1 (see Table 3 through Table 6)
	VBUS_DISCHARGE_P1/P2.5	K8	I/O used for discharging VBUS line during voltage change
	VBUS_P_CTRL_P2/P4.2	B4	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 2
	VBUS_C_CTRL_P2/P4.1	B5	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 2
	VBUS_DISCHARGE_P2/P4.3	B3	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P1/VSEL_1_P1/P2.4	L7	Monitor VCONN for UVP condition on port 1 or GPIO or Voltage selection control for VBUS on port 1
	SCL_3/VCONN_MON_P2/ VSEL_1_P2/P2.7	L10	SCB3 (see Table 3 through Table 6) or Monitor VCONN for UVP condition on port 2 or Voltage selection control for VBUS on port 2
Overvoltage Protection (OVP)	OVP_TRIP_P1/VSEL_2_P1/P2.1	K5	VBUS overvoltage output indicator for port 1 or voltage selection control for VBUS on port 1 or SCB1 (see Table 3 through Table 6)
	OVP_TRIP_P2/P3.0	L8	VBUS overvoltage output indicator for port 2 or SCB3 (see Table 3 through Table 6)

Table 1. Pinout for CYPD4255-96BZXI *(continued)*

Group	Name	Ball Location	Description
GPIOs and Serial Interfaces	VBUS_MON_P1/P2.0	L4	VBUS overvoltage protection monitoring signal or GPIO
	VBUS_MON_P2/P4.0	B6	VBUS overvoltage protection monitoring signal
	HPD_P1/P2.3	K7	Hot Plug Detect I/O for port 1/GPIO
	HPD_P2/P3.4	E10	Hot Plug Detect I/O for port 2/GPIO
	MUX_CTRL_3_P2/P3.5	B9	Mux control for port 2 /GPIO
	MUX_CTRL_2_P2/P3.6	B8	Mux control for port 2/GPIO/SCB4 (see Table 3 through Table 6)
	MUX_CTRL_1_P2/P3.7	B7	Mux control for port 2 or GPIO or SCB4 (see Table 3 through Table 6)
	VSEL_2_P2/P3.1	H10	Voltage selection control for VBUS on port 2/GPIO
	I2C_SCL_SCB1_EC/P0.1	L6	SCB1 (see Table 3 through Table 6)
	I2C_SDA_SCB1_EC/P0.0	K6	SCB1 (see Table 3 through Table 6) or SCB3 (see Table 3 through Table 6)
	I2C_INT_EC/P2.2	L5	I2C interrupt line
	I2C_SCL_SCB2_AR/P1.0	E2	SCB2 (see Table 3 through Table 6) or GPIO
	I2C_SDA_SCB2_AR/P1.3	D2	SCB2 (see Table 3 through Table 6) or GPIO
	I2C_INT_AR_P1/P1.4	F2	I2C interrupt line
	I2C_INT_AR_P2/P1.5	G2	I2C interrupt line or SCB2 (see Table 3 through Table 6)
	SDA_3/P2.6	J10	SCB3 (see Table 3 through Table 6) or GPIO
	SCL_4/P3.3	F10	SCB4 (see Table 3 through Table 6)
	SDA_4/P3.2	G10	SCB4 (see Table 3 through Table 6)
	SWD_IO/AR_RST#/P1.1	B2	Serial Wire Debug I/O or SCB2 (see Table 3 through Table 6)
	SWD_CLK/I2C_CFG_EC/P1.2	C2	SWD Clock or I2C config line
Reset	XRES	H6	Reset input
Power	VDDM	A3	3.0-V to 3.6-V supply for integrated mux
	VDDM	A6	3.0-V to 3.6-V supply for integrated mux
	VDDM	A9	3.0-V to 3.6-V supply for integrated mux
	VDDM	B1	3.0-V to 3.6-V supply for integrated mux
	VDDM	D11	3.0-V to 3.6-V supply for integrated mux
	VDDM	E1	3.0-V to 3.6-V supply for integrated mux
	VDDM	H1	3.0-V to 3.6-V supply for integrated mux
	VDDM	J11	3.0-V to 3.6-V supply for integrated mux
	VDDM	L1	3.0-V to 3.6-V supply for integrated mux
	VDDD	D10	VDDD supply input/output (2.7-V to 5.5-V)
	VCCD	B10	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDIO	C10	1.71-V to 5.5-V supply for I/Os
	V5V_P1	J2	2.7-V to 5.5-V supply for VCONN FET of Type-C port 1
	V5V_P2	L9	2.7-V to 5.5-V supply for VCONN FET of Type-C port 2

Table 1. Pinout for CYPD4255-96BZXI *(continued)*

Group	Name	Ball Location	Description
Ground	GND	D5	Ground
	GND	D6	Ground
	GND	D7	Ground
	GND	D8	Ground
	GND	E4	Ground
	GND	E5	Ground
	GND	E6	Ground
	GND	E7	Ground
	GND	E8	Ground
	GND	F4	Ground
	GND	F5	Ground
	GND	F6	Ground
	GND	F7	Ground
	GND	F8	Ground
	GND	G4	Ground
	GND	G5	Ground
	GND	G6	Ground
	GND	G7	Ground
	GND	H7	Ground
No Connect	NC	G8	No connect
	NC	H4	No connect
	NC	H5	No connect
	NC	H8	No connect

Figure 2. 96-Ball BGA Map for CYPD4255-96BZXI

	1	2	3	4	5	6	7	8	9	10	11
A	RX2_P	RX2_M	VDDM	TX2_P	TX2_M	VDDM	TX1_M	TX1_P	VDDM	RX1_M	RX1_P
B	VDDM	SWD_IO/AR_RST#/P1.1	VBUS_DISCHARGE_P2/P4.3	VBUS_P_CTRL_P2/P4.2	VBUS_C_CTRL_P2/P4.1	VBUS_MON_P2/P4.0	MUX_CTRL_1_P2/P3.7	MUX_CTRL_2_P2/P3.6	MUX_CTRL_3_P2/P3.5	VCCD	SBU1
C	DP0_P	SWD_CLK/I2C_CFG_EC/P1.2								VDDIO	SBU2
D	DP0_M	I2C_SDA_SCB2_AR/P1.3		GND	GND	GND	GND			VDDD	VDDM
E	VDDM	I2C_SCL_SCB2_AR/P1.0		GND	GND	GND	GND	GND		HPD_P2/P3.4	AUX_M
F	DP1_P	I2C_INT_AR_P1/P1.4		GND	GND	GND	GND	GND		SCL_4/P3.3	AUX_P
G	DP1_M	I2C_INT_AR_P2/P1.5		GND	GND	GND	GND	NC		SDA_4/P3.2	RX_M
H	VDDM	CC2_P1		NC	NC	XRES	GND	NC		VSEL_2_P2/P3.1	RX_P
J	DP2_P	V5V_P1								SDA_3/P2.6	VDDM
K	DP2_M	CC1_P1	VBUS_P_CTRL_P1/P1.6	VBUS_C_CTRL_P1/P1.7	OVP_TRIP_P1/VSEL_2_P1/P2.1	I2C_SDA_SCB1_EC/P0.0	HPD_P1/P2.3	VBUS_DISCHARGE_P1/P2.5	CC1_P2	CC2_P2	TX_M
L	VDDM	DP3_P	DP3_M	VBUS_MON_P1/P2.0	I2C_INT_EC/P2.2	I2C_SCL_SCB1_EC/P0.1	VCONN_MON_P1/VSEL_1_P1/P2.4	OVP_TRIP_P2/P3.0	V5V_P2	SCL_3/VCONN_MON_P2/VSEL_1_P2/P2.7	TX_P

Table 2. Pinout for CYPD4155-96BZXI

Group	Name	Ball Location	Description
USB Type-C Port 1	CC1_P1	K2	USB PD connector detect/Configuration Channel 1
	CC2_P1	H2	USB PD connector detect/Configuration Channel 2
Mux	TX_P	L11	Differential USB 3.0 transmit signal
	TX_M	K11	Differential USB 3.0 transmit signal
	RX_P	H11	Differential USB 3.0 receive signal
	RX_M	G11	Differential USB 3.0 receive signal
	TX1_P	A8	Differential transmit signal 1
	TX1_M	A7	Differential transmit signal 1
	RX1_P	A11	Differential receive signal 1
	RX1_M	A10	Differential receive signal 1
	TX2_P	A4	Differential transmit signal 2
	TX2_M	A5	Differential transmit signal 2
	RX2_P	A1	Differential receive signal 2
	RX2_M	A2	Differential receive signal 2
	AUX_P	F11	Auxiliary signal for DisplayPort
	AUX_M	E11	Auxiliary signal for DisplayPort
	DP0_P	C1	Differential DisplayPort 0 signal
	DP0_M	D1	Differential DisplayPort 0 signal
	DP1_P	F1	Differential DisplayPort 1 signal
	DP1_M	G1	Differential DisplayPort 1 signal
	DP2_P	J1	Differential DisplayPort 2 signal
	DP2_M	K1	Differential DisplayPort 2 signal
	DP3_P	L2	Differential DisplayPort 3 signal
	DP3_M	L3	Differential DisplayPort 3 signal
	SBU1	B11	Sideband Use signal
	SBU2	C11	Sideband Use signal
VBUS Control	VBUS_P_CTRL_P1/P1.6	K3	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 1
	VBUS_C_CTRL_P1/P1.7	K4	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 1 or SCB1 (see Table 3 through Table 6)
	VBUS_DISCHARGE_P1/P2.5	K8	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P1/VSEL_1_P1/P2.4	L7	Monitor VCONN for UVP condition on port 1 or GPIO or Voltage selection control for VBUS on port 1
Overvoltage Protection (OVP)	OVP_TRIP_P1/VSEL_2_P1/P2.1	K5	VBUS overvoltage output indicator for port 1 or Voltage selection control for VBUS on port 1 or SCB1 (see Table 3 through Table 6)

Table 2. Pinout for CYPD4155-96BZXI *(continued)*

Group	Name	Ball Location	Description
GPIOs and Serial Interfaces	VBUS_MON_P1/P2.0	L4	VBUS overvoltage protection monitoring signal or GPIO
	HPD_P1/P2.3	K7	Hot Plug Detect I/O for port 1 or GPIO
	SCL_3/P2.7	L10	SCB3 (see Table 3 through Table 6) or GPIO
	SDA_3/P2.6	J10	SCB3 (see Table 3 through Table 6) or GPIO
	SCL_4/P3.3	F10	SCB4 (see Table 3 through Table 6)
	SDA_4/P3.2	G10	SCB4 (see Table 3 through Table 6)
	I2C_SCL_SCB1_EC/P0.1	L6	SCB1 (see Table 3 through Table 6)
	I2C_SDA_SCB1_EC/P0.0	K6	SCB1 (see Table 3 through Table 6) or SCB3 (see Table 3 through Table 6)
	I2C_INT_EC/P2.2	L5	I2C interrupt line
	I2C_SCL_SCB2_AR/P1.0	E2	SCB2 (see Table 3 through Table 6) or GPIO
	I2C_SDA_SCB2_AR/P1.3	D2	SCB2 (see Table 3 through Table 6) or GPIO
	I2C_INT_AR_P1/P1.4	F2	I2C interrupt line
	P4.3	B3	GPIO
	P4.2	B4	GPIO
	P4.1	B5	GPIO
	P4.0	B6	GPIO
	P3.7	B7	GPIO or SCB4 (see Table 3 through Table 6)
	P3.6	B8	GPIO or SCB4 (see Table 3 through Table 6)
	P3.5	B9	GPIO
	P3.4	E10	GPIO
	P1.5	G2	GPIO or SCB2 (seeTable 3 through Table 6)
	P3.1	H10	GPIO
	P3.0	L8	GPIO or SCB3 (see Table 3 through Table 6)
	SWD_IO/AR_RST#/P1.1	B2	Serial Wire Debug I/O or SCB2 (see Table 3 through Table 6)
	SWD_CLK/I2C_CFG_EC/P1.2	C2	SWD Clock or I2C config line
Reset	XRES	H6	Reset input
Power	VDDM	A3	3.0-V to 3.6-V supply for integrated mux
	VDDM	A6	3.0-V to 3.6-V supply for integrated mux
	VDDM	A9	3.0-V to 3.6-V supply for integrated mux
	VDDM	B1	3.0-V to 3.6-V supply for integrated mux
	VDDM	D11	3.0-V to 3.6-V supply for integrated mux
	VDDM	E1	3.0-V to 3.6-V supply for integrated mux
	VDDM	H1	3.0-V to 3.6-V supply for integrated mux
	VDDM	J11	3.0-V to 3.6-V supply for integrated mux
	VDDM	L1	3.0-V to 3.6-V supply for integrated mux
	VDDD	D10	VDDD supply input/output (2.7-V to 5.5-V)
	VCCD	B10	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDIO	C10	1.71-V to 5.5-V supply for I/Os
	V5V_P1	J2	2.7-V to 5.5-V supply for VCONN FET of Type-C port 1

Table 2. Pinout for CYPD4155-96BZXI *(continued)*

Group	Name	Ball Location	Description
Ground	GND	D5	Ground
	GND	D6	Ground
	GND	D7	Ground
	GND	D8	Ground
	GND	E4	Ground
	GND	E5	Ground
	GND	E6	Ground
	GND	E7	Ground
	GND	E8	Ground
	GND	F4	Ground
	GND	F5	Ground
	GND	F6	Ground
	GND	F7	Ground
	GND	F8	Ground
	GND	G4	Ground
	GND	G5	Ground
	GND	G6	Ground
	GND	G7	Ground
	GND	H7	Ground
No Connect	NC	G8	No connect
	NC	H4	No connect
	NC	H5	No connect
	NC	H8	No connect
	NC	K9	No connect
	NC	K10	No connect
	NC	L9	No connect

Figure 3. 96-Ball BGA Ball Map for CYPD4155-96BZXI

	1	2	3	4	5	6	7	8	9	10	11
A	RX2_P	RX2_M	VDDM	TX2_P	TX2_M	VDDM	TX1_M	TX1_P	VDDM	RX1_M	RX1_P
B	VDDM	SWD_IO/AR_RST#/P1.1	P4.3	P4.2	P4.1	P4.0	P3.7	P3.6	P3.5	VCCD	SBU1
C	DP0_P	SWD_CLK/I2C_CFG_EC/P1.2								VDDIO	SBU2
D	DP0_M	I2C_SDA_SCB2_AR/P1.3			GND	GND	GND	GND		VDDD	VDDM
E	VDDM	I2C_SCL_SCB2_AR/P1.0		GND	GND	GND	GND	GND		P3.4	AUX_M
F	DP1_P	I2C_INT_AR_P1/P1.4		GND	GND	GND	GND	GND		SCL_4/P3.3	AUX_P
G	DP1_M	P1.5		GND	GND	GND	GND	NC		SDA_4/P3.2	RX_M
H	VDDM	CC2_P1		NC	NC	XRES	GND	NC		P3.1	RX_P
J	DP2_P	V5V_P1								SDA_3/P2.6	VDDM
K	DP2_M	CC1_P1	VBUS_P_CTRL_P1/P1.6	VBUS_C_CTRL_P1/P1.7	OVP_TRIP_P1/VSEL_2_P1/P2.1	I2C_SDA_SCB1_EC/P0.0	HPD_P1/P2.3	VBUS_DISCHARGE_P1/P2.5	NC	NC	TX_M
L	VDDM	DP3_P	DP3_M	VBUS_MON_P1/P2.0	I2C_INT_EC/P2.2	I2C_SCL_SCB1_EC/P0.1	VCONN_MON_P1/VSEL_1_P1/P2.4	P3.0	NC	SCL_3/P2.7	TX_P

Table 3. Serial Communication Block (SCB1) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
K4	UART_TX_SCB1	SPI_MOSI_SCB1	SPI_MOSI_SCB1	VBUS_C_CTRL_P1	VBUS_C_CTRL_P1
K5	UART_RX_SCB1	SPI_CLK_SCB1	SPI_CLK_SCB1	VSEL_2_P1/ VCONN_MON_P1	VSEL_2_P1/ VCONN_MON_P1
L6	UART_RTS_SCB1	SPI_MISO_SCB1	SPI_MISO_SCB1	I2C_SDA_SCB1	I2C_SDA_SCB1
K6	UART_CTS_SCB1	SPI_SEL_SCB1	SPI_SEL_SCB1	I2C_SCL_SCB1	I2C_SCL_SCB1

Table 4. Serial Communication Block (SCB2) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
E2	UART_TX_SCB2	SPI_CLK_SCB2	SPI_CLK_SCB2	I2C_SCL_SCB2	I2C_SCL_SCB2
D2	UART_RX_SCB2	SPI_MISO_SCB2	SPI_MISO_SCB2	I2C_SDA_SCB2	I2C_SDA_SCB2
G2	UART_RTS_SCB2	SPI_SEL_SCB2	SPI_SEL_SCB2	GPIO	GPIO
B2	UART_CTS_SCB2	SPI_MOSI_SCB2	SPI_MOSI_SCB2	SWD_IO	SWD_IO

Table 5. Serial Communication Block (SCB3) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
J10	UART_TX_SCB3	SPI_MISO_SCB3	SPI_MISO_SCB2	I2C_SDA_SCB3	I2C_SDA_SCB3
L10	UART_RX_SCB3	SPI_MOSI_SCB3	SPI_MOSI_SCB3	I2C_SCL_SCB3	I2C_SCL_SCB3
K6	UART_RTS_SCB3	SPI_SEL_SCB3	SPI_SEL_SCB3	I2C_SCL_SCB1	I2C_SCL_SCB1
L8	UART_CTS_SCB3	SPI_CLK_SCB3	SPI_CLK_SCB3	AR_RST#	AR_RST#

Table 6. Serial Communication Block (SCB4) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
G10	UART_TX_SCB4	SPI_MOSI_SCB4	SPI_MOSI_SCB4	I2C_SDA_SCB4	I2C_SDA_SCB4
F10	UART_RX_SCB4	SPI_MISO_SCB4	SPI_MISO_SCB4	I2C_SCL_SCB4	I2C_SCL_SCB4
B7	UART_RTS_SCB4	SPI_SEL_SCB4	SPI_SEL_SCB4	GPIO	GPIO
B8	UART_CTS_SCB4	SPI_CLK_SCB4	SPI_CLK_SCB4	GPIO	GPIO

Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD CCG4M.

CCG4M shall be able to operate from three possible external supply sources: V5V_P1 for first Type-C port, V5V_P2 for second Type- C port and VDDD.

CCG4M has the power supply input V5V_P1 and V5V_P2 pins for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG4M per Type-C port to power either CC1 or CC2 pin. These FETs are capable of providing a minimum of 1W on the CC1 and CC2 pins for the EMCA cables. In USB-PD applications, the valid levels on V5V_P1 and V5V_P2 supplies can range from 4.85 – 5.5 V.

The chip's internal operating power supply is derived from VDDD. In UFP mode, CCG4M operates in 2.7 – 5.5V. In DFP and DRP modes, it operates at 3.0 – 5.5V range.

A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the V5V_P1 or V5V_P2 and VDDD pins.

The VCCD output of EZ-PD CCG4M must be bypassed to ground via an external capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

Bypass capacitors must be used from VDDD and V5V_P1 or V5V_P2 pins to ground; typical practice for systems in this frequency range is to use a 0.1-µF capacitor on VDDD, V5V_P1 and V5V_P2. Note that these are simply rules of thumb and that for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 4 shows an example of the power supply bypass capacitors.

Figure 4. EZ-PD CCG4M Power and Bypass Scheme Example
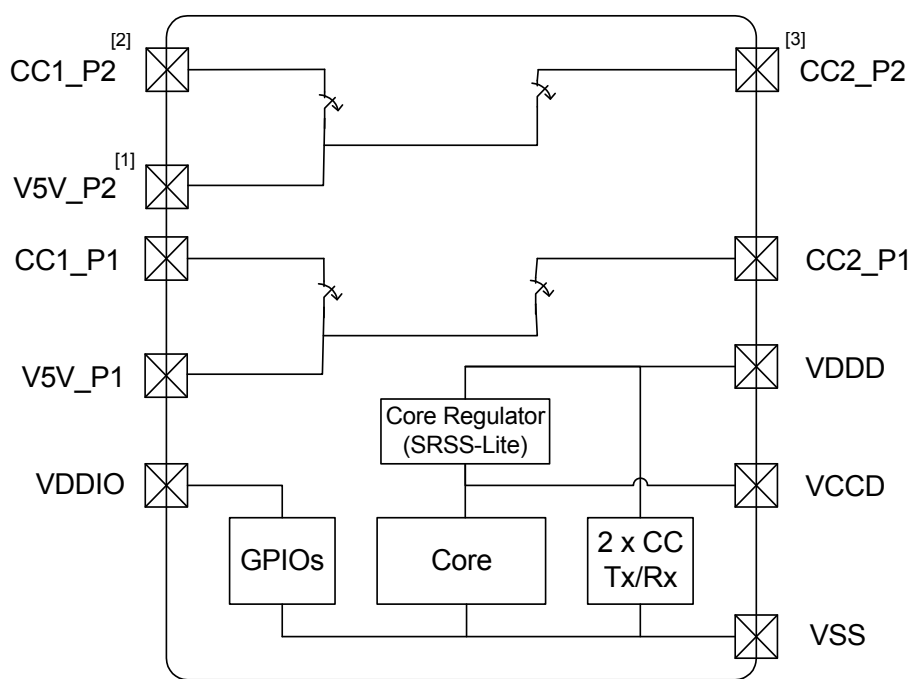
Note
1. V5V_P1 denoted power supply input for Type-C port 1
   V5V_P2 denoted power supply input for Type-C port 2
2. CC1_1:USB PD connector detect/Configuration Channel 1 for Type-C port 1
   CC1_2:USB PD connector detect/Configuration Channel 1 for Type-C port 2
3. CC2_1:USB PD connector detect/Configuration Channel 2 for Type-C port 1
   CC2_2:USB PD connector detect/Configuration Channel 2 for Type-C port 2

Figure 5. Dual Port Notebook Application Using CCG4M (CYD4255-96BZXI)

Figure 6. Single Port Notebook Application Using CCG4M (CYD4155-96BZXI)
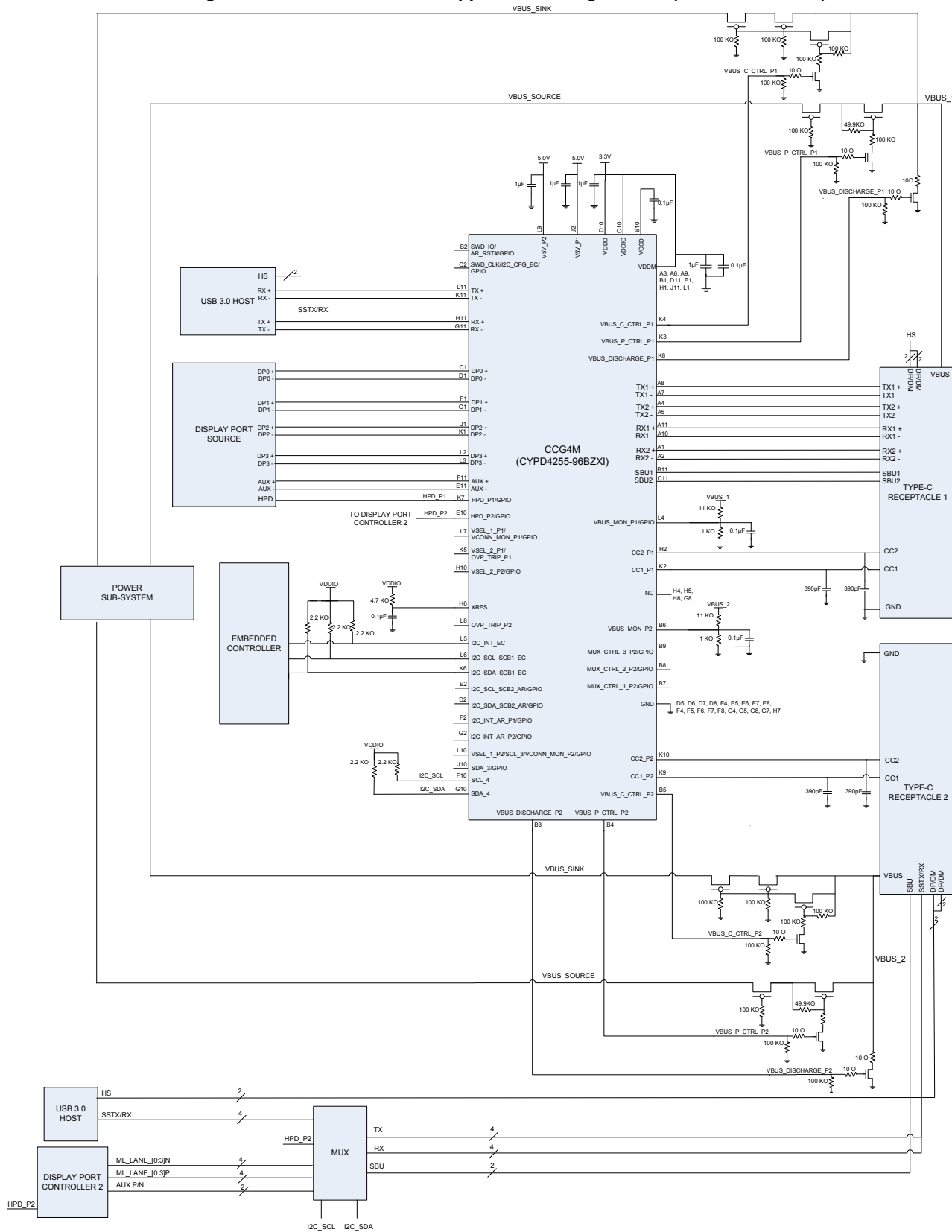
Electrical Specifications

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings[4]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{DDM_MAX}	Mux supply relative to V_{SS}	–0.3	–	4.3	V	Absolute max
V5V_P1	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V5V_P2	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute Max
V_{MUX_ABS}	Mux USB/DP signal voltage	– 0.3	–	1.2	V	Absolute Max
V_{AUX_ABS}	Mux AUX signal voltage	– 0.35	–	V_{DDM}	V	Absolute Max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1, CC2

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 8. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP Applications
SID.PWR#1_A	V_{DDD}	Power supply input voltage	3.0	–	5.5	V	DFP/DRP Applications
SID.PWR#26	V5V_P1, V5V_P2	Power supply input voltage	4.85	–	5.5	V	–
SID.VDDM	V_{DDM}	Mux power supply input voltage	3.0	3.3	3.6	V	
SID.IDDM	I_{DDM}	V_{DDM} current supply	–	300	350	µA	
PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	–
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	0.8	1	–	µF	X5R ceramic or better

Note
4. Usage above the absolute maximum conditions listed in Table 7 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 8. DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#27	C_{EXV}	Power Supply Decoupling Capacitor on V5V_P1 and V5V_P2	–	0.1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID.PWR#4	I_{DD12}	Supply current	–	10	–	mA	V5V_P1 and V5V_P2 = 5 V, T_A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active
Sleep Mode, V_{DDD} = 2.7 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup WDT ON IMO at 48 MHz	–	2.5	4.0	mA	V_{DDD} = 3.3 V, T_A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current
Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on)							
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V I^2C wakeup and WDT ON	–	360	–	µA	V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	32.5	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled
SID_DS1	I_{DD_DS1}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	130	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P and R_D connected at 70 ms intervals by CPU. R_P, R_D connection should be enabled for both PD ports.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 9. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	3.0 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO. Guaranteed by characterization.
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to "Ready to accept I2C / CC command"	–	5	25	ms	Guaranteed by characterization

MUX

Table 10. Mux Specifications

Spec ID	Parameter	Min	Typ	Max	Units	Details/Conditions
C_{OFF}	USB 3.0/DP switch OFF capacitance	–	1.2	–	pF	V_{IOM} = GND f = 1 MHz
C_{ON}	USB 3.0/DP switch ON capacitance	–	2.3	–	pF	V_{IOM} = GND f = 1 MHz
C_{OFF}	AUX+/AUX– switch OFF capacitance	–	4.0	–	pF	V_{IOM} = GND f = 1 MHz
C_{ON}	AUX+/AUX– switch ON capacitance	–	7.0	–	pF	V_{IOM} = GND f = 1 MHz
I_{OZL}	I/O leakage for TX_to_TX1/TX2, RX_toRX1/RX2, DPx_to_TX/RX (x = 0,1, 2, 3), AUX_to_SBUy (y = 1, 2)	–	1	5	µA	V_{DDM} = 3.6 V V_{IOM} (USB 3.0) = 0 V V_{IOM} (DP) = 0 V V_{IOM} (AUX) = 0 V
I_{OZH}	I/O leakage for TX_to_TX1/TX2, RX_toRX1/RX2, DPx_to_TX/RX (x = 0,1, 2, 3), AUX_to_SBUy (y = 1, 2)	–	1	15	µA	V_{DDM} = 3.6 V V_{IOM} (USB 3.0) = 1.2 V V_{IOM} (DP) = 1.2 V V_{IOM} (AUX) = 4.0 V
R_{ON}	Switch on resistance USB 3.0/DP	–	7.0 9.0	10.0 12.0	Ω	V_{DDM} = min, I_{ON} = –40 mA V_{IN} = 0 V V_{IN} = 1.2 V
	AUX Switch	–	3.5 4.5	5.0 7.0	Ω	V_{DDM} = min, I_{IN} = –40 mA V_{IN} = 0 V V_{IN} = 3.0 V
Linear region for analog switch						
VP_IO	Linear region for analog switch TX_to_TX1/TX2, RX_to_RX1/RX2, DPx_to_TX/RX (x = 0, 1, 2, 3)	1.4	1.6	–	V	V_{DDM} = 3.3 V I_{PASS} = 10 mA
VP_IOSB	Linear region for analog switch AUX_to_SBUx (x = 1, 2)	4.0	4.2	–	V	V_{DDM} = 3.3 V I_{PASS} = 10 mA

Table 11. Dynamic Mux Characteristics

Min and max apply for T_A between –40 °C to 85 °C. Typical values are referenced to T_A = 25 °C.

Spec ID	Parameter	Min	Typ	Max	Units	Details/Conditions
tstartup	Startup time	–	10	20	µs	Supply voltage valid or the device is powered up and the channel is turned on to its specified characteristics V_{DDM} = 3 V
tpd	Propagation delay 1	–	80	–	ps	From input port to output port USB/DP
	Propagation delay 2	–	150	–	ps	From input port to output port AUX
tsk	Skew time 1	–	10	–	ps	From input port to output USB/DP. Bit to bit skew
	Skew time 2	–	20	–	ps	From input port to output AUX. Bit to bit skew
VI_sub_dp	USB/DP input signal	–0.3	–	1.2	V	USB/DP switch analog signal
VI_aux	AUX+/AUX– input signal	–0.35	–	V_{DDM}	V	AUX switch analog signal

Table 12. Mux Switch AC Electrical Characteristics

Min and max apply for T_A between –40 °C to 85 °C and T_J up to +125 °C (unless otherwise noted). Typical values are referenced to T_A = 25 °C, V_{DDM} = 3.3 V.

Spec ID	Parameter	Frequency		Min	Typ	Max	Units	Details/Conditions
BW_usb	–3 dB bandwidth of USB 3.0			–	6	–	GHz	
I_L	Differential insertion loss	2.5/2.7 GHz		–	–1.2/–1.3	–	dB	Vcom = 0 V
R_L	Differential return loss	2.5/2.7 GHz		–	–21/–20	–	dB	Vcom = 0 V
Xtalk	Differential crosstalk	2.5/2.7 GHz	USB	–	–38/–37	–	dB	Vcom = 0 V
			DP		–25/–24		dB	Vcom = 0 V
Xoff	Off isolation	2.5/2.7 GHz		–	–23/–22	–	dB	Vcom = 0 V

I/O

Table 13. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH}[5]	Input voltage HIGH threshold	$0.7 \times V_{DDIO}$	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DDIO}$	V	CMOS input
SID.GIO#39	V_{IH}[5]	LVTTL input, V_{DDIO} < 2.7 V	$0.7 \times V_{DDIO}$	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	$0.3 \times V_{DDIO}$	V	–
SID.GIO#41	V_{IH}[5]	LVTTL input, $V_{DDIO} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, $V_{DDIO} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	$V_{DDIO} - 0.6$	–	–	V	I_{OH} = 4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	$V_{DDIO} - 0.5$	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDIO} \geq$ 2.7 V. Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDIO}$	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization

Table 14. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF

Note
5. V_{IH} must not exceed V_{DDIO} + 0.2 V.

XRES

Table 15. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	$0.7 \times V_{DDIO}$	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DDIO}$	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	$0.05 \times V_{DDIO}$	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 16. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 17. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kbps	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kbps	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 18. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 19. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbit/sec	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbit/sec	–	–	312	µA	–

Table 20. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 21. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbit/sec	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbit/sec	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbit/sec	–	–	600	µA	–

Table 22. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 23. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 24. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$48 + 3 * T_{SCB}$	ns	$T_{SCB} = T_{CPU} = 1/24$ MHz
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 25. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#4	$T_{ROWWRITE}$[6]	Row (block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	$T_{ROWERASE}$[6]	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$[6]	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$[6]	Bulk erase time (128 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$[6]	Total device program time	–	–	25	seconds	Guaranteed by characterization
SID.MEM#6	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET1}	Flash retention. $T_A \leq 55\,°C$, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET2}	Flash retention. $T_A \leq 85\,°C$, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

System Resources

Power-on-Reset (POR) with Brown Out

Table 26. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 27. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5	V	Guaranteed by characterization

SWD Interface

Table 28. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\,V \leq V_{DDIO} \leq 5.5\,V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\,V \leq V_{DDIO} \leq 3.3\,V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Note
6. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Internal Main Oscillator

Table 29. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 30. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	–
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 31. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 32. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO Frequency	20	40	80	kHz	–

Power Down

Table 33. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 0.6 V applied at CC1 or CC2. Applicable for DRP applications only.
SID.PD.15	Vdrop_V5V_CC1	Voltage drop from V5V_P1 and V5V_P2 pins to CC1 pin while sourcing 215 mA	–	–	100	mV	–
SID.PD.16	Vdrop_V5V_CC2	Voltage drop from V5V_P1 and V5V_P2 pins to CC2 pin while sourcing 215 mA	–	–	100	mV	–

Analog to Digital Converter

Table 34. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.0	–	1.0	LSB	–

Table 35. ADC AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Ordering Information

The EZ-PD CCG4M part numbers and features are listed in Table 36.

Table 36. EZ-PD CCG4M Ordering Information

Part Number	Application	Type-C Ports	Dead Battery Termination	Termination Resistor	Role	Package
CYPD4255-96BZXI	Notebooks, Desktops	2	Yes	R_P[7], R_D[8]	DRP	96-ball BGA
CYPD4155-96BZXI	Notebooks, Desktops	1	Yes	R_P[7], R_D[8]	DRP	96-ball BGA

Ordering Code Definitions

CY PD 4 1/2 0 X - XX XX X I T

T = Tape and Reel

Temperature Grade:
I = Industrial

Pb-free

Package Type: XX = BZ
BZ = BGA

Number of pins in the package: XX = 96

Device Role: Unique combination of role and termination:
X = 2 or 3 or 4 or 5

Feature: Unique Applications

Number of Type-C Ports: 1 = 1 Port, 2 = 2 Ports

Product Type: 4 = Fourth-generation product family

Marketing Code: PD = Power Delivery product family

Company ID: CY = Cypress

Notes
7. Termination resistor denoting an accessory or downstream facing port.
8. Termination resistor denoting a upstream facing port.

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Packaging

Table 37. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (96-ball BGA)	–	–	62	–	°C/W
T_{JC}	Package θ_{JC} (96-ball BGA)	–	–	23	–	°C/W

Table 38. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
96-ball BGA	245 °C	30 seconds

Table 39. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
96-ball BGA	MSL 3

Figure 7. 96-Ball BGA(6 × 6 × 0.5 mm), 002-10631

TOP VIEW

BOTTOM VIEW

DETAIL A

SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	96		
∅ b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.00		
SE	0.00		
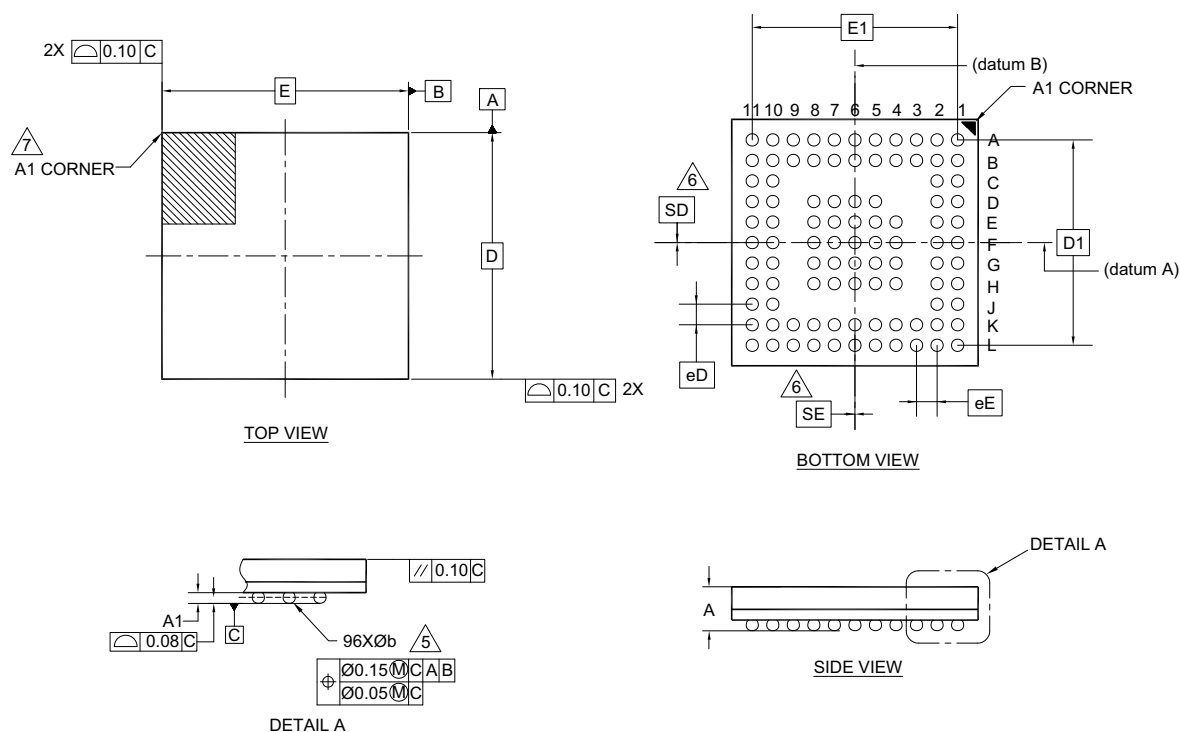
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.

3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.

4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.

7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

9. JEDEC SPECIFICATION NO. REF. : MO-225.

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Acronyms

Table 40. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I²C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 40. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I²C serial clock
SDA	I²C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG4M pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 41. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: EZ-PD™ CCG4M, USB Type-C Dual Port Controller with USB 3.1 Gen 1/DP1.2 Mux Document Number: 002-11084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5131574	VGT	02/18/2016	New datasheet
*A	5626232	VGT	02/10/2017	Updated Copyright and Disclaimer. Updated Sales, Solutions, and Legal Information.
*B	5768666	VGT	06/15/2017	Updated logo and Copyright. Updated Packaging: Spec 002-10631 changed revision from ** to *A. Removed "Preliminary" in the document.
*C	5842990	VGT	08/03/2017	Updated GPIO related information in Table 1, Table 2, Figure 2, and Figure 3.

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