

## Contents

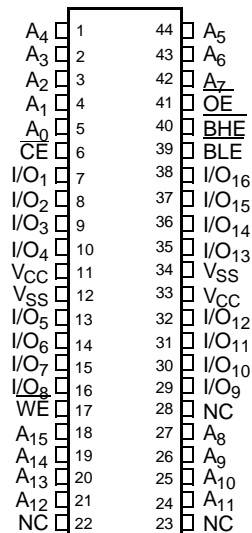
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## Selection Guide

Description		CY7C10211B-10	CY7C1021B-12	CY7C1021B-15
Maximum access time (ns)		10	12	15
Maximum operating current (mA)	Commercial/Industrial	150	140	130
	Automotive-A	-	-	130
	Automotive-E	-	-	130
Maximum CMOS standby current (mA)	Commercial/Industrial	10	10	10
	Commercial/Industrial (L version)	0.5	0.5	0.5
	Automotive-A (L version)	-	-	0.5
	Automotive-E	-	-	15

## Pin Configuration

Figure 1. 44-Pin SOJ/TSOP II (Top View)



## Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>15</sub>	1–5, 18–21, 24–27, 42–44	Input	Address inputs used to select one of the address locations.
I/O <sub>1</sub> –I/O <sub>16</sub>	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	Write enable input, active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{\text{CE}}$	6	Input/Control	Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
BHE, BLE	40, 39	Input/Control	Byte enable select inputs, active LOW. BHE controls I/O <sub>16</sub> –I/O <sub>9</sub> , BLE controls I/O <sub>8</sub> –I/O <sub>1</sub> .
$\overline{\text{OE}}$	41	Input/Control	Output enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	Power supply inputs to the device.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to GND<sup>[2]</sup> ..... -0.5 V to +7.0 V

DC voltage applied to outputs in High Z state<sup>[2]</sup> ..... -0.5 V to  $V_{CC}+0.5$  V

DC input voltage<sup>[2]</sup> ..... -0.5 V to  $V_{CC}+0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V  
(per MIL-STD-883, Method 3015)

Latch-up current ..... >200 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ ) <sup>[3]</sup>	$V_{CC}$
Commercial	0 °C to +70 °C	5 V $\pm$ 10%
Industrial	-40 °C to +85 °C	
Automotive-A	-40 °C to +85 °C	
Automotive-E	-40 °C to +125 °C	

## Electrical Characteristics Over the operating range

Parameter	Description	Test Conditions	-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}$ , $I_{OH} = -4.0$ mA	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}$ , $I_{OL} = 8.0$ mA	-	0.4	-	0.4	-	0.4	V
$V_{IH}$	Input HIGH voltage		2.2	6.0	2.2	6.0	2.2	6.0	V
$V_{IL}$	Input LOW voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	Commercial/Industrial		-1	+1	-1	+1	$\mu$ A
			Automotive-A		-	-	-	+1	$\mu$ A
			Automotive-E		-	-	-4	+4	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	Commercial/Industrial		-1	+1	-1	+1	$\mu$ A
			Automotive-A		-	-	-1	+1	$\mu$ A
			Automotive-E		-	-	-4	+4	$\mu$ A
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$	Commercial/Industrial		-	150	-	140	mA
			Automotive-A		-	-	-	130	
			Automotive-E		-	-	-	130	
$I_{SB1}$	Automatic CE power down current—TTL inputs	Max $V_{CC}$ , $CE \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Commercial/Industrial		-	40	-	40	mA
			Automotive-A		-	-	-	40	
			Automotive-E		-	-	-	50	
$I_{SB2}$	Automatic CE power down current—CMOS inputs	Max $V_{CC}$ , $CE \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$	Commercial/Industrial		-	10	-	10	mA
			Commercial/Industrial (L)		-	0.5	-	0.5	
			Automotive-A (L)		-	-	-	0.5	
			Automotive-E		-	-	-	15	

### Notes

- $V_{IL}$  (min.) = -2.0 V and  $V_{IH}$  (max) =  $V_{CC} + 0.5$  V for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.

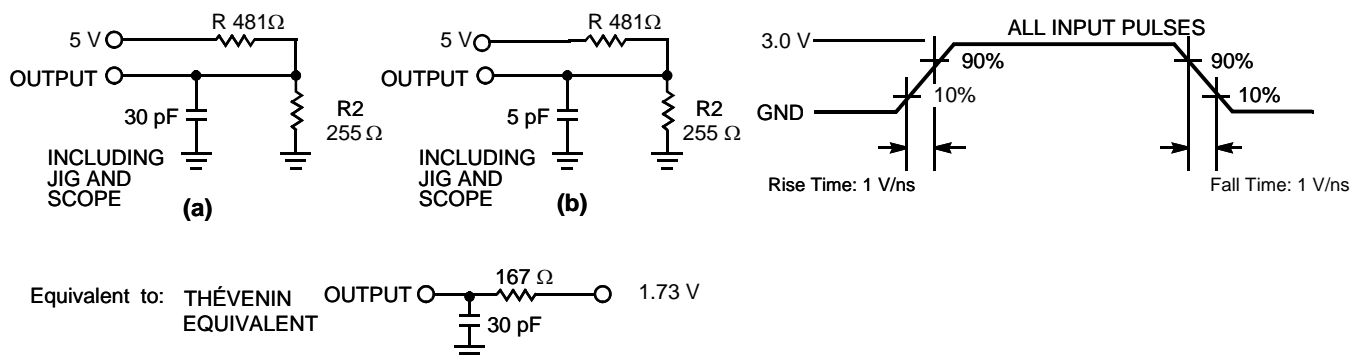
## Capacitance

Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[4]</sup>	Description	Test Conditions	44-Pin SOJ	44-Pin TSOP-II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	64.32	76.89	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		31.03	14.28	$^{\circ}\text{C/W}$

Figure 2. AC Test Loads and Waveforms



### Note

4. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup>** Over the operating range

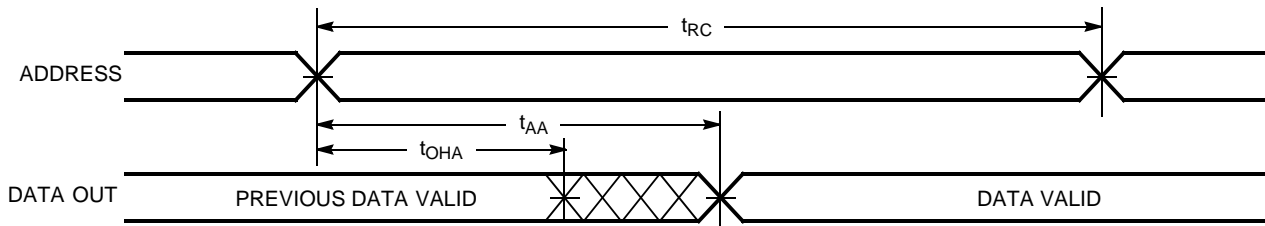
Parameter	Description	CY7C10211B-10		CY7C1021B-12		CY7C1021B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t <sub>RC</sub>	Read cycle time	10	-	12	-	15	-	ns
t <sub>AA</sub>	Address to data valid	-	10	-	12	-	15	ns
t <sub>OHA</sub>	Data hold from address change	3	-	3	-	3	-	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	-	10	-	12	-	15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	-	5	-	6	-	7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[5]</sup>	0	-	0	-	0	-	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[6, 7]</sup>	-	5	-	6	-	7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[6]</sup>	3	-	3	-	3	-	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[6, 7]</sup>	-	5	-	6	-	7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power up	0	-	0	-	0	-	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power down	-	10	-	12	-	15	ns
t <sub>DBE</sub>	Byte enable to data valid	-	5	-	6	-	7	ns
t <sub>LZBE</sub>	Byte enable to low Z <sup>[6]</sup>	0	-	0	-	0	-	ns
t <sub>HZBE</sub>	Byte disable to high Z <sup>[6, 7]</sup>	-	5	-	6	-	7	ns
Write Cycle <sup>[8]</sup>								
t <sub>WC</sub>	Write cycle time	10	-	12	-	15	-	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	8	-	9	-	10	-	ns
t <sub>AW</sub>	Address setup to write end	7	-	8	-	10	-	ns
t <sub>HA</sub>	Address hold from write end	0	-	0	-	0	-	ns
t <sub>SA</sub>	Address setup to write start	0	-	0	-	0	-	ns
t <sub>SD</sub>	Data setup to write end	5	-	6	-	8	-	ns
t <sub>HD</sub>	Data hold from write end	0	-	0	-	0	-	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[6]</sup>	3	-	3	-	3	-	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[6, 7]</sup>	-	5	-	6	-	7	ns
t <sub>BW</sub>	Byte enable to write end	7	-	8	-	9	-	ns

**Notes**

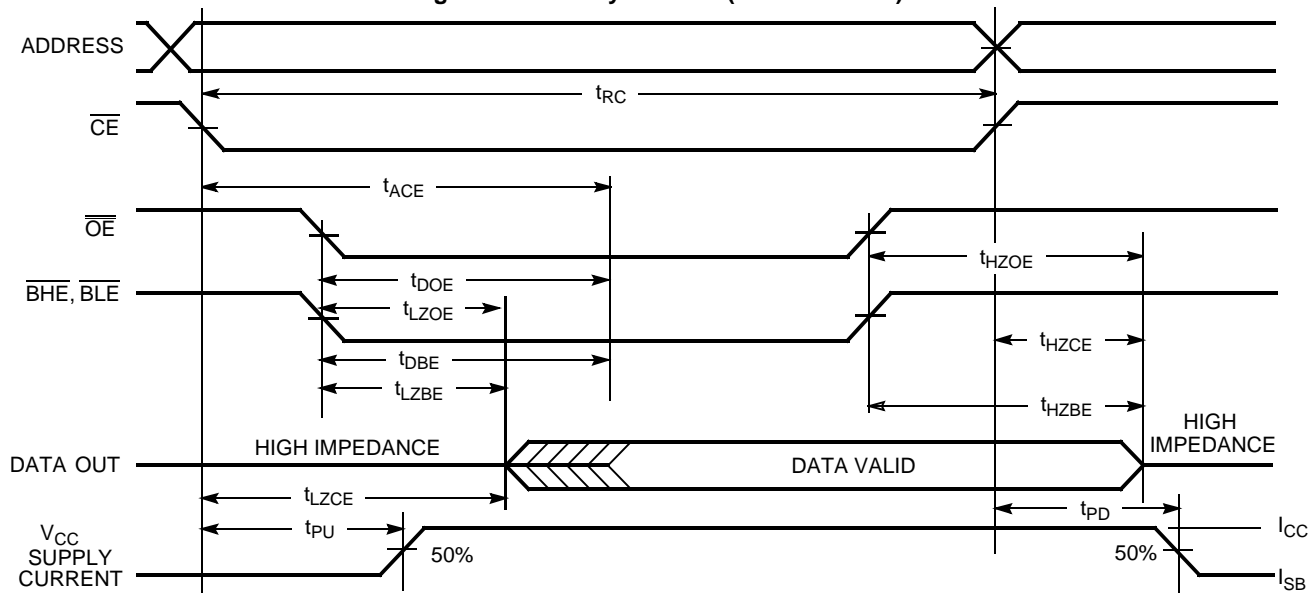
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW, and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.

## Switching Waveforms

**Figure 3. Read Cycle No. 1<sup>[9, 10]</sup>**



**Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

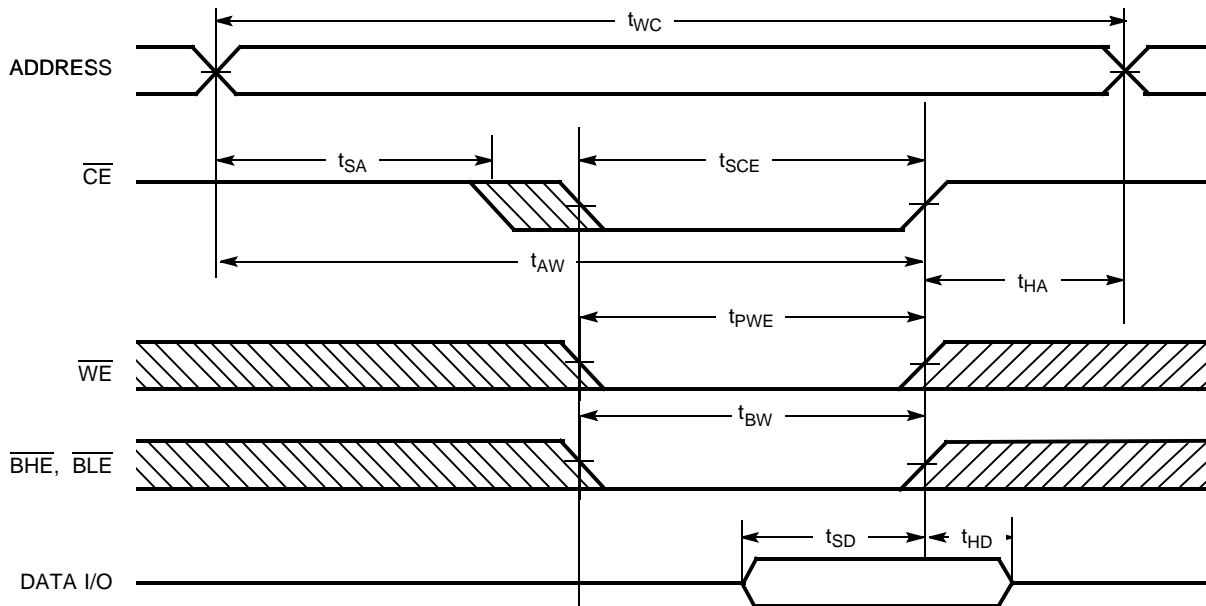
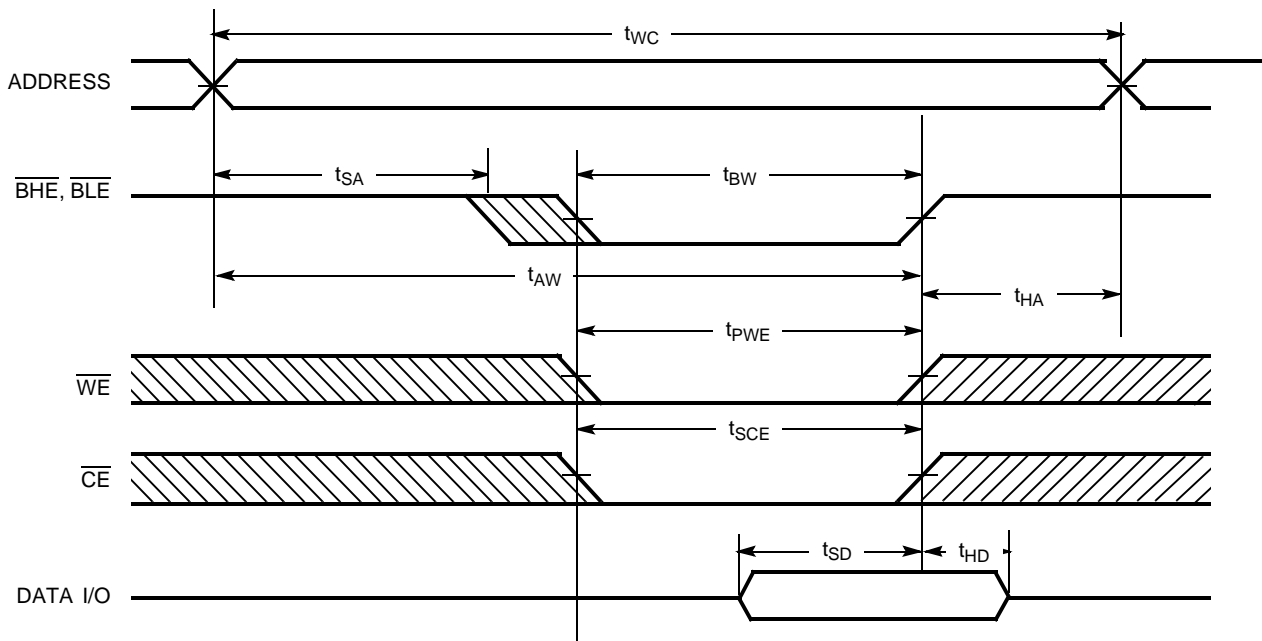


### Notes

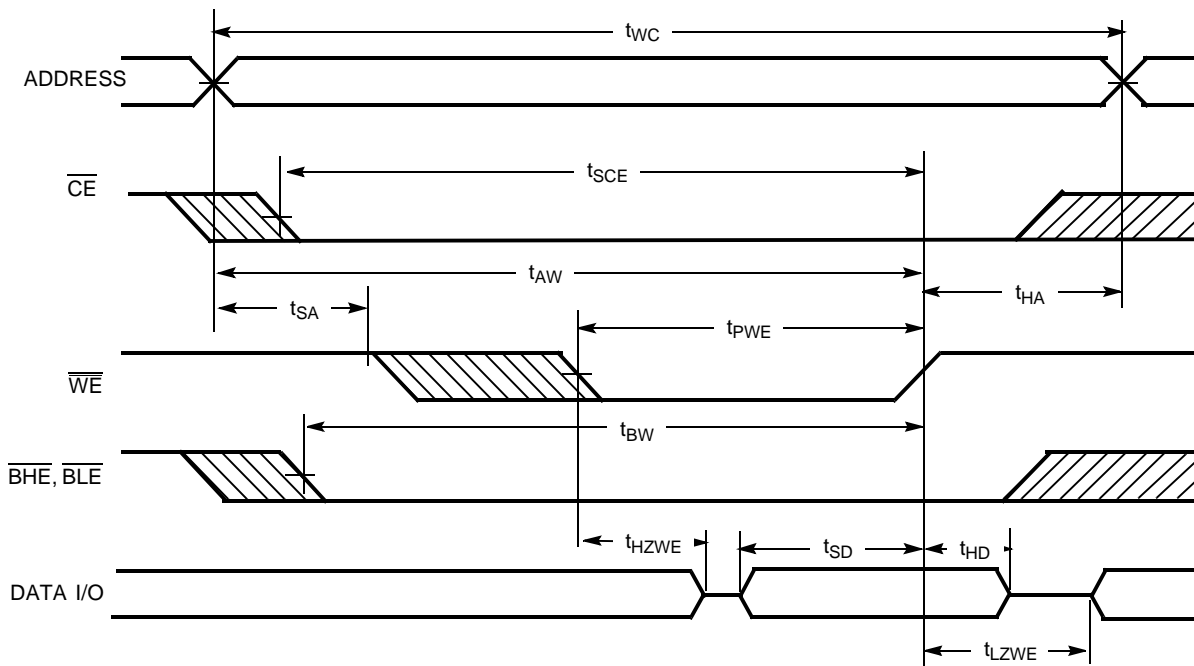
9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and  $\overline{BLE}$  =  $V_{IL}$ .

10.  $\overline{WE}$  is HIGH for read cycle.

11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[12, 13]</sup>**

**Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes**

12. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .  
 13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

**Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)**

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>1</sub> –I/O <sub>8</sub>	I/O <sub>9</sub> –I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby ( $I_{\text{SB}}$ )
L	L	H	L	L	Data out	Data out	Read - All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data out	High Z	Read - Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data out	Read - Upper bits only	Active ( $I_{\text{CC}}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{\text{CC}}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{\text{CC}}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{\text{CC}}$ )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )



## Ordering Information

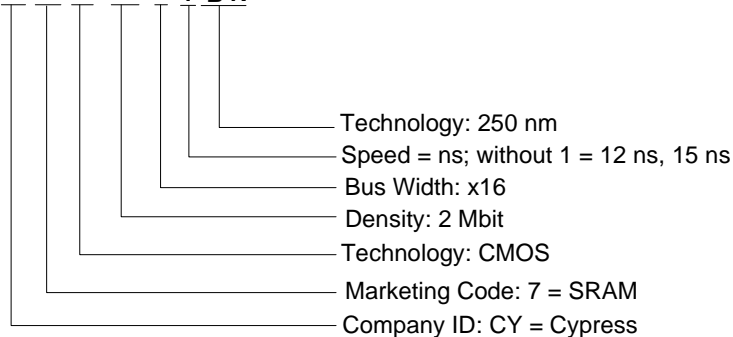
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Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1021BN-12ZXC	51-85082	44-pin TSOP type II (Pb-free)	Commercial
15	CY7C1021BNL-15VXC	51-85082	44-pin (400-mil) molded SOJ (Pb-free)	Commercial
	CY7C1021BN-15ZXC	51-85087	44-pin TSOP type II (Pb-free)	Commercial
	CY7C1021BN-15ZXI	51-85087	44-pin TSOP type II (Pb-free)	Industrial
	CY7C1021BNL-15ZXI	51-85087	44-pin TSOP type II (Pb-free)	Industrial
	CY7C1021BNL-15ZSXA	51-85087	44-pin TSOP type II (Pb-free)	Automotive-A
	CY7C1021BN-15VXE	51-85082	44-pin (400-mil) molded SOJ (Pb-free)	Automotive-E
	CY7C1021BN-15ZSXE	51-85087	44-pin TSOP type II (Pb-free)	Automotive-E

## Ordering Code Definition

**CY 7 C 10 2 1 1 B N**



## Package Diagrams

Figure 8. 44-Pin (400-Mil) Molded SOJ

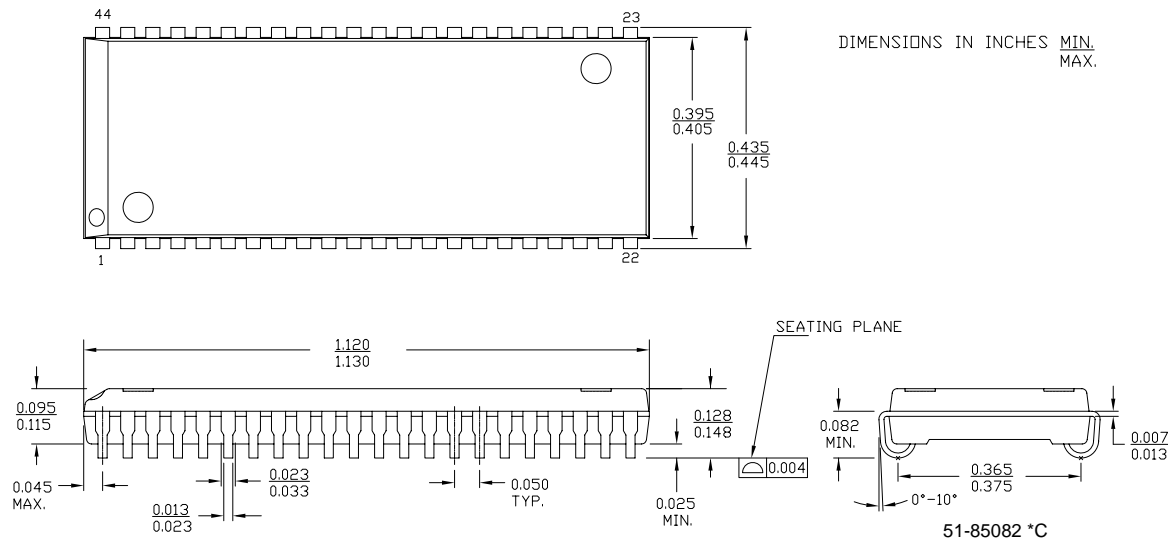
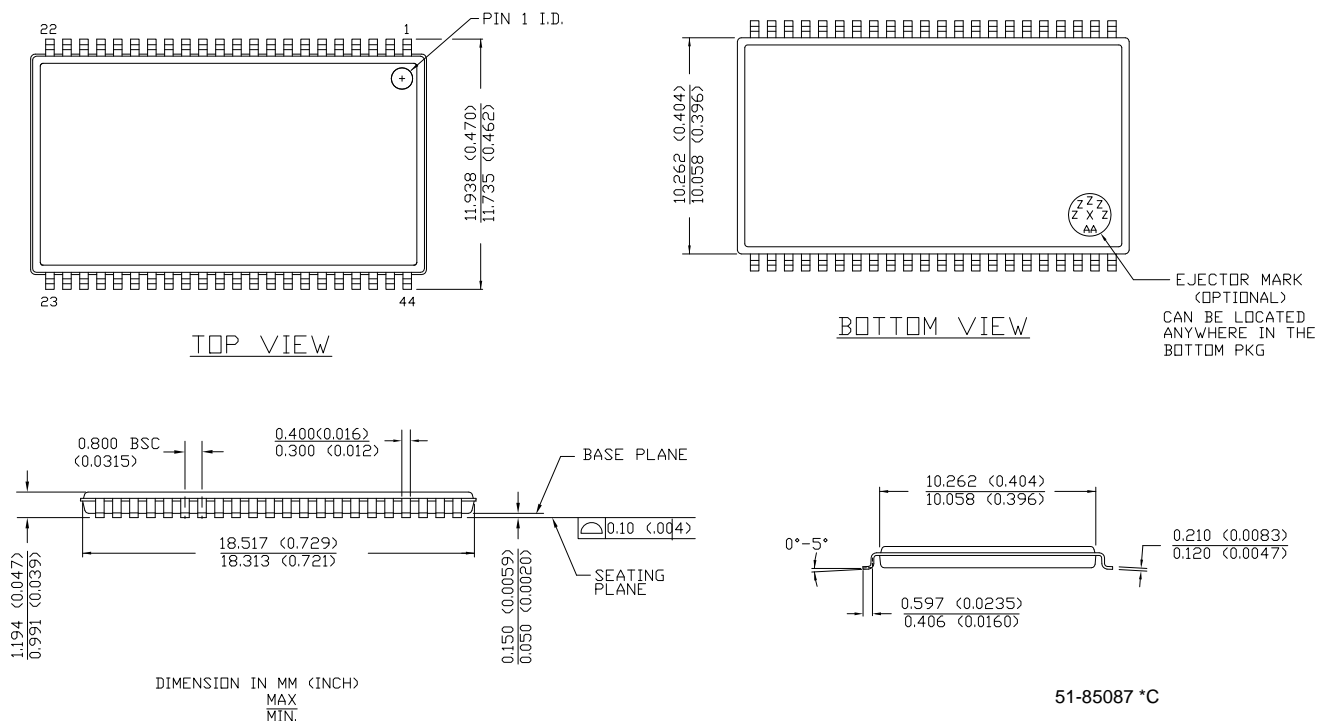


Figure 9. 44-Pin TSOP II



## Acronyms

**Table 1. Acronyms Used in this Document**

Acronym	Description
BHE	Byte high enable
BLE	Byte low enable
CE	Chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	Output enable
SRAM	Static random access memory
TSOP	Thin small outline package
WE	Write enable

## Document History Page

Document Title: CY7C1021BN, CY7C10211BN 1 Mbit (64K x 16) Static RAM Document Number: 001-06494				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New datasheet
*A	505726	See ECN	NXR	Removed I <sub>OS</sub> parameter from DC Electrical Characteristics table. Added Automotive products Updated ordering Information table
*B	2897061	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*C	2947254	06/08/10	RAME	Corrected 'Byte write select inputs' to 'Byte Enable select inputs' on page 2. Added ohm ( $\Omega$ ) symbol in Thevenin equivalent circuit on page 4. Included T <sub>HZBE</sub> and T <sub>LZBE</sub> to Switching Characteristics table footnote 2 Included operating range for CY7C1021BNL-15ZXI in ordering information table.

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