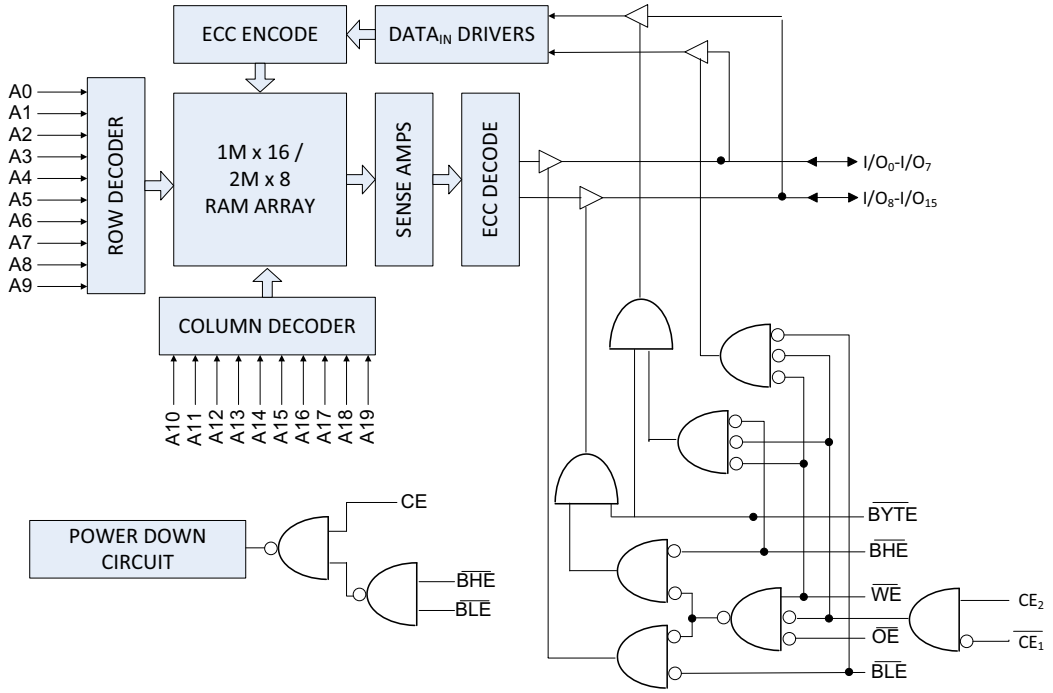
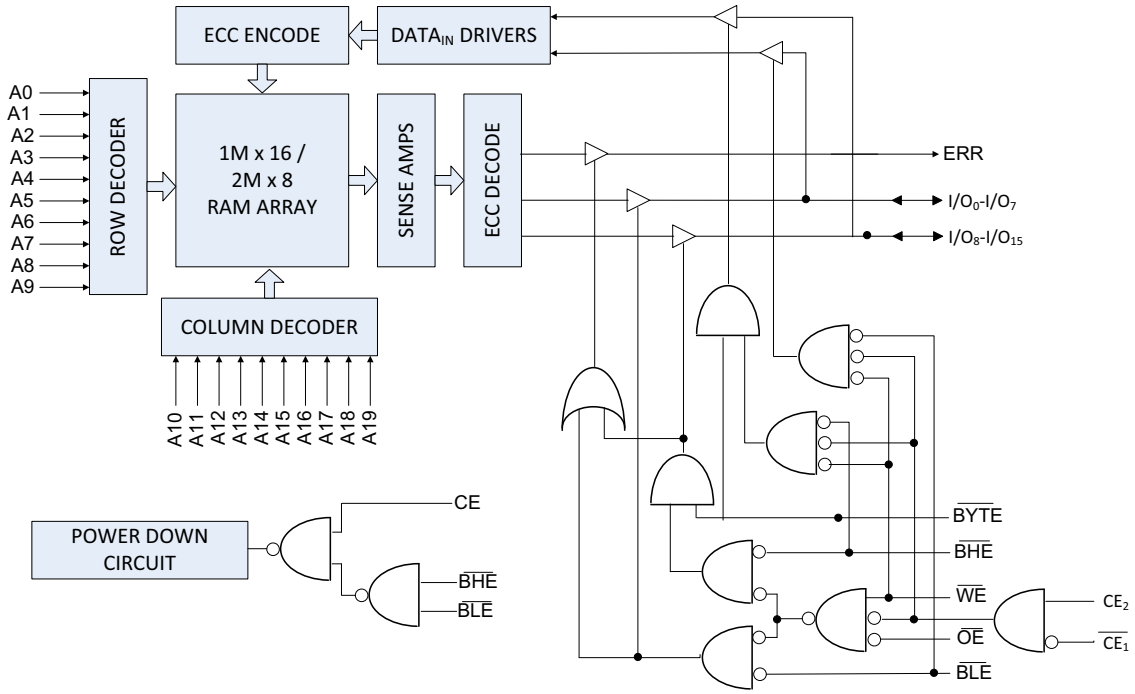
Logic Block Diagram – CY62167G



Logic Block Diagram – CY62167GE



Contents

Pin Configuration – CY62167G

Figure 1. 48-ball VFBGA Pinout (Dual Chip Enable without ERR) – CY62167G [5]

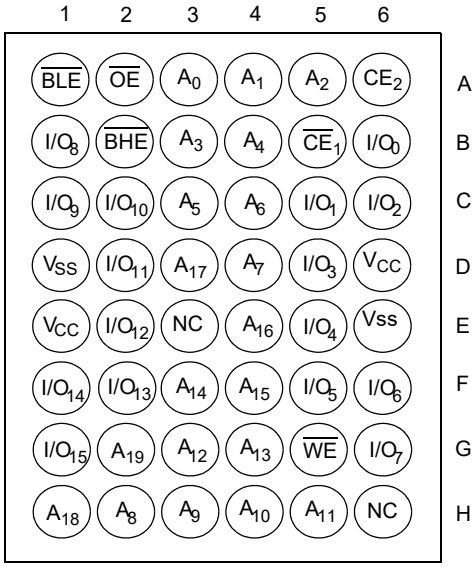
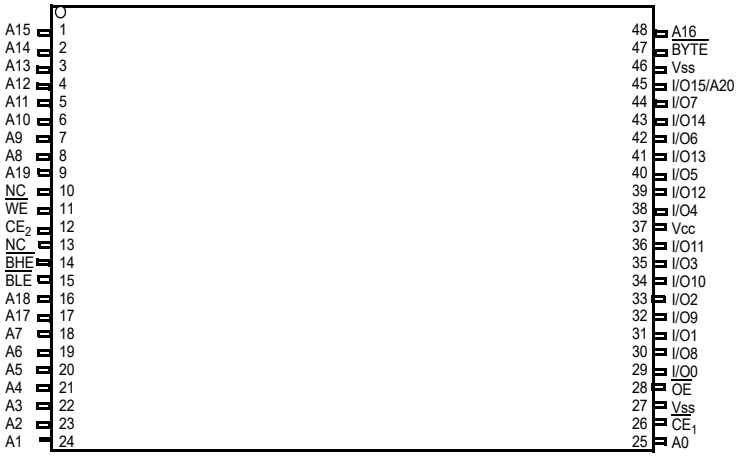


Figure 2. 48-pin TSOP I Pinout (Dual Chip Enable without ERR) – CY62167G [5, 6]



Notes

5. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
6. Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M × 8 configuration, pin 45 is the extra address line A20, while BHE, BLE, and I/O_8 to I/O_{14} pins are not used and can be left floating.

Pin Configuration – CY62167GE

Figure 3. 48-ball VFBGA Pinout (Single Chip Enable with ERR) – CY62167GE [7, 8]

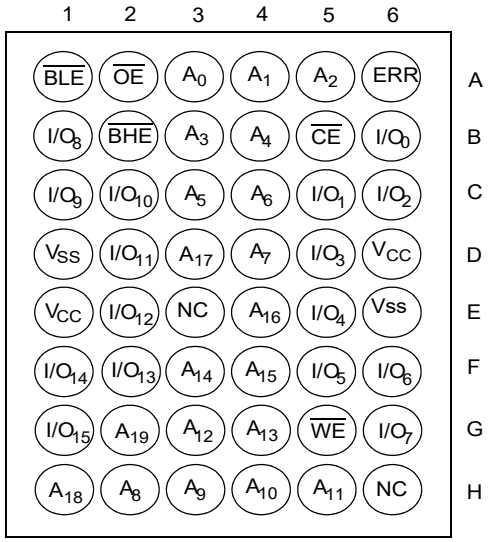
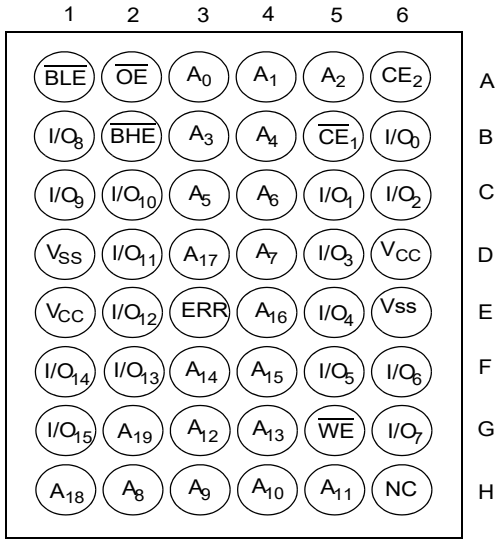


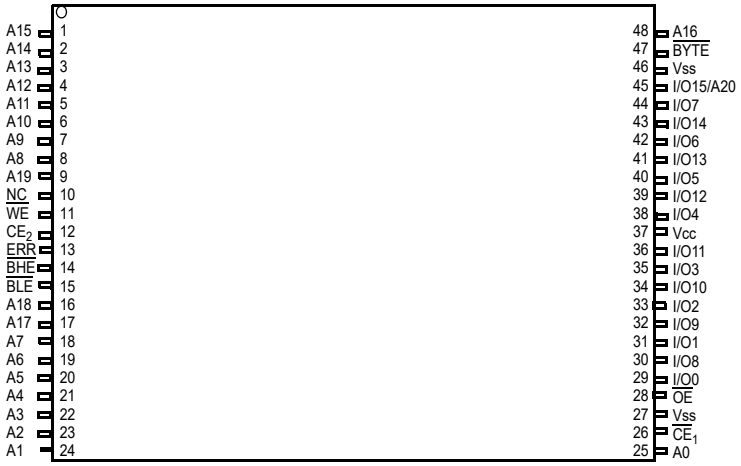
Figure 4. 48-ball VFBGA Pinout (Dual Chip Enable with ERR) – CY62167GE [7, 8]



Note
7. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
8. ERR is an Output pin. If not used, this pin should be left floating.

Pin Configuration – CY62167GE (continued)

Figure 5. 48-pin TSOP I Pinout (Dual Chip Enable with ERR) – CY62167GE [9, 10]



Notes

9. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
10. Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M × 8 configuration, pin 45 is the extra address line A20, while the BHE, BLE, and I/O_8 to I/O_{14} pins are not used and can be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in High Z state[11] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage[11] ..... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}[12]
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V[15,16], 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		45/55 ns			Unit
					Min	Typ [13]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V[15,16]	V_{CC} = Min, I_{OH} = –0.1 mA		2.0	–	–	
		2.7 V to 3.6 V[15,16]	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.4[14]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	
		2.2 V to 2.7 V[15,16]	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	
		2.7 V to 3.6 V[15,16]	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage[11]	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	
		2.2 V to 2.7 V[15,16]	–		1.8	–	V_{CC} + 0.3	
		2.7 V to 3.6 V[15,16]	–		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW voltage[11]	1.65 V to 2.2 V	–		–0.2	–	0.4	
		2.2 V to 2.7 V[15,16]	–		–0.3	–	0.6	
		2.7 V to 3.6 V[15,16]	–		–0.3	–	0.8	
		4.5 V to 5.5 V	–		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	29.0	36.0	mA
				f = 18.18 MHz (55 ns)	–	29.0	32.0	
				f = 1 MHz	–	7.0	9.0	

Notes

11. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
12. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 200-µs wait time after V_{CC} stabilizes to its operational value.
13. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
14. This parameter is guaranteed by design and is not tested.
15. The 3V Typical V_{CC} device is offered with improved I_{CC}, I_{SB1} and I_{SB2} specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress Sales representative.
16. For next version of this 3V Typical V_{CC} device, kindly refer here. Further details about improvement and comparison between current and new versions can be found in the PCN193805.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns			Unit
				Min	Typ [13]	Max	
I_{SB1}[17]	Automatic Power-down Current – CMOS Inputs; V_{CC} = 2.2 V to 3.6 V[18, 19] and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	5.5	16.0	µA
	Automatic Power-down Current – CMOS Inputs V_{CC} = 1.65 V to 2.2 V			–	7.0	26.0	
I_{SB2}[17]	Automatic Power-down Current – CMOS Inputs V_{CC} = 2.2 V to 3.6 V[18, 19] and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$	25 °C	–	5.5	6.5[20]	
			40 °C	–	6.3	8.0[20]	
			70 °C	–	8.4	12.0[20]	
			85 °C	–	12.0	16.0	
	Automatic Power-down Current – CMOS Inputs V_{CC} = 1.65 V to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	7.0	26.0	

Notes

17. Chip enables ($\overline{CE}_1$ and CE_2) and $\overline{BYTE}$ must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
18. The 3V Typical V_{CC} device is offered with improved I_{CC}, I_{SB1} and I_{SB2} specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress Sales representative.
19. For next version of this 3V Typical V_{CC} device, kindly refer here. Further details about improvement and comparison between current and new versions can be found in the PCN193805.
20. The I_{SB2} maximum limits at 25 °C, 40 °C, and 70 °C are guaranteed by design and not 100% tested.

Capacitance

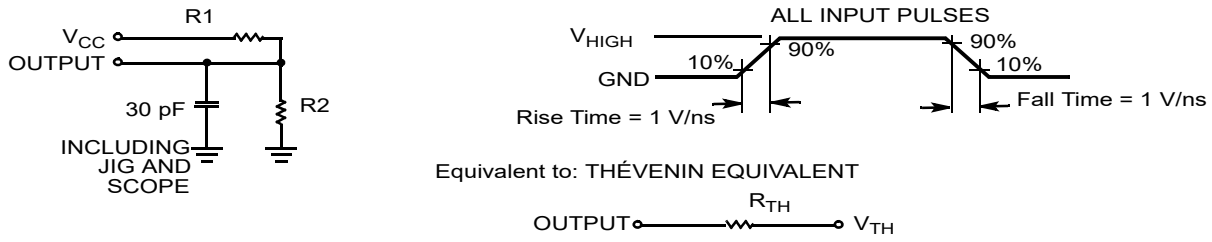
Parameter [21]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10.0	pF
C_{OUT}	Output capacitance		10.0	pF

Thermal Resistance

Parameter [21]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V
V_{HIGH}	1.8	2.5	3.0	5.0	V

Note
21. Tested initially and after any design or process changes that may affect these parameters.

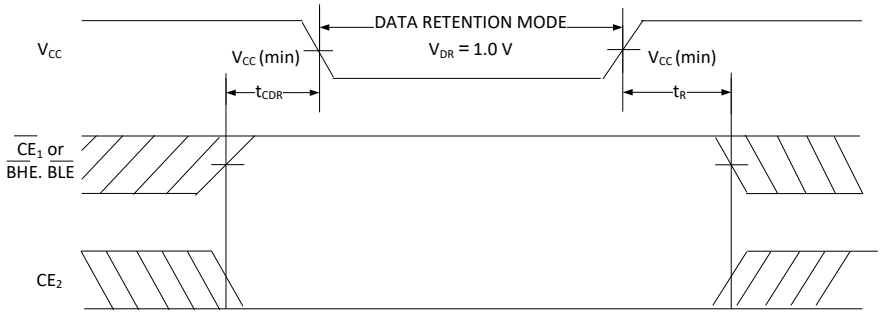
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [22]	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	–	V
I_{CCDR}[23, 24]	Data retention current	1.2 V ≤ V_{CC} ≤ 2.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	7.0	26.0	µA
		2.2 V < V_{CC} ≤ 3.6 V[25, 26] or 4.5 V ≤ V_{CC} ≤ 5.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	5.5	16.0	µA
t_{CDR}[27]	Chip deselect to data retention time	–	0.0	–	–	–
t_R[27, 28]	Operation recovery time	–	45/55	–	–	ns

Data Retention Waveform

Figure 7. Data Retention Waveform [29]



Notes

22. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
23. Chip enables ($\overline{CE}_1$ and CE_2) and $\overline{BYTE}$ must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
24. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
25. The 3V Typical V_{CC} device is offered with improved I_{CC}, I_{SB1} and I_{SB2} specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress Sales representative.
26. For next version of this 3V Typical V_{CC} device, kindly refer here. Further details about improvement and comparison between current and new versions can be found in the PCN193805.
27. These parameters are guaranteed by design and are not tested.
28. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
29. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [30]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45.0	–	55.0	–	ns
t_{AA}	Address to data valid/Address to ERR valid	–	45.0	–	55.0	ns
t_{OHA}	Data hold from address change/ERR hold from address change	10.0	–	10.0	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45.0	–	55.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid/$\overline{OE}$ LOW to ERR valid	–	22.0	–	25.0	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[31, 32]	5.0	–	5.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[31, 32, 33]	–	18.0	–	18.0	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[31, 32]	10.0	–	10.0	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[31, 32, 33]	–	18.0	–	18.0	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up[34]	0.0	–	0.0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down[34]	–	45.0	–	55.0	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	45.0	–	55.0	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[31]	5.0	–	5.0	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[31, 33]	–	18.0	–	18.0	ns
Write Cycle [35, 36]						
t_{WC}	Write cycle time	45.0	–	55.0	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35.0	–	40.0	–	ns
t_{AW}	Address setup to write end	35.0	–	40.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35.0	–	40.0	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35.0	–	40.0	–	ns
t_{SD}	Data setup to write end	25.0	–	25.0	–	ns
t_{HD}	Data hold from write end	0.0	–	0.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[31, 32, 33]	–	18.0	–	20.0	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[31, 32]	10.0	–	10.0	–	ns

Notes

30. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in Figure 6 on page 9, unless specified otherwise.
31. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
32. Tested initially and after any design or process changes that may affect these parameters.
33. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
34. These parameters are guaranteed by design and are not tested.
35. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
36. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 8. Read Cycle No. 1 of CY62167G (Address Transition Controlled) [37, 38]

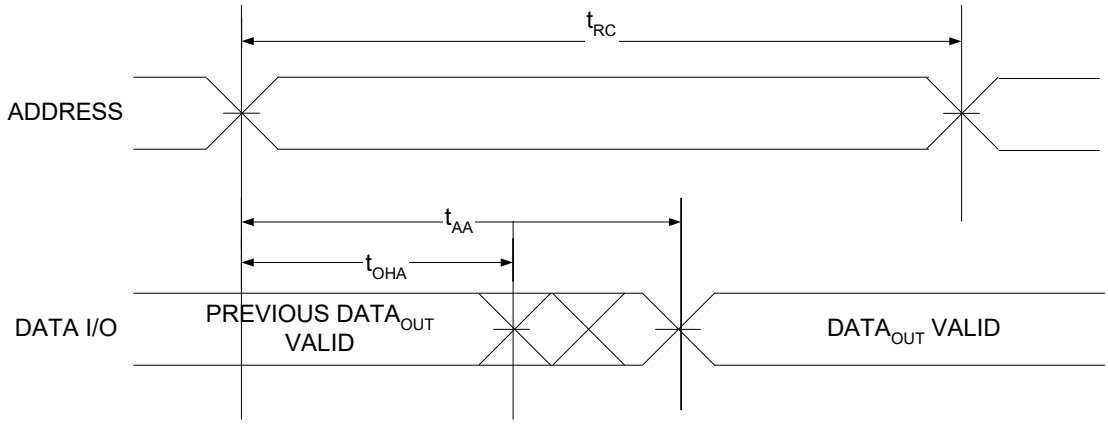
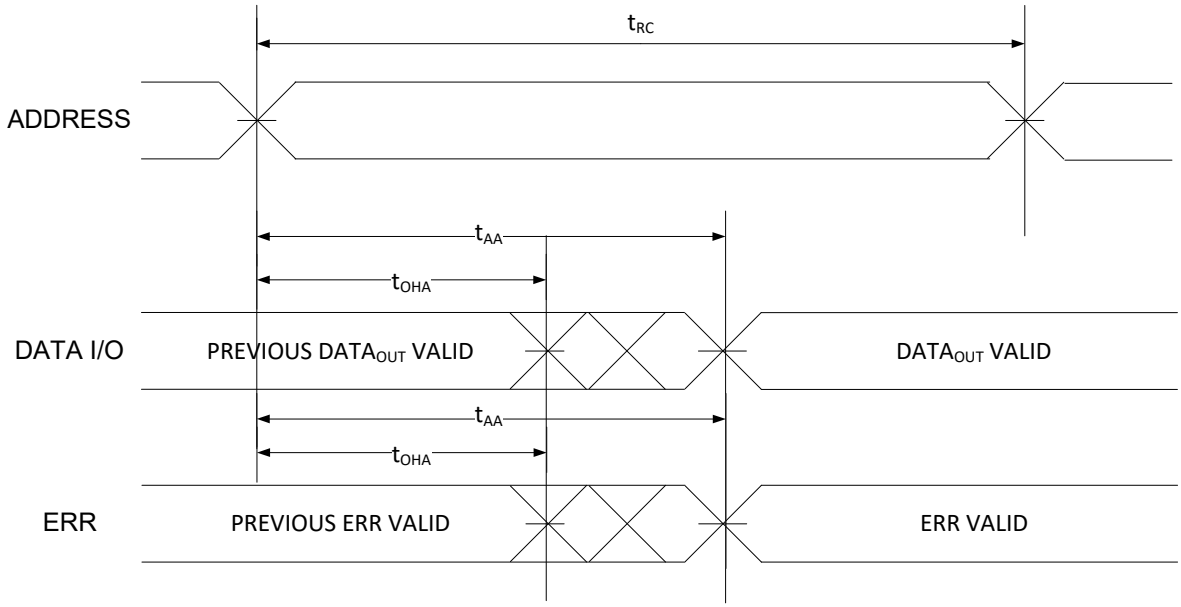


Figure 9. Read Cycle No. 1 of CY62167GE (Address Transition Controlled) [37, 38]



Notes
37. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$, or both = V_{IL}.
38. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 10. Read Cycle No. 2 (OE Controlled) [39, 40, 41, 43]

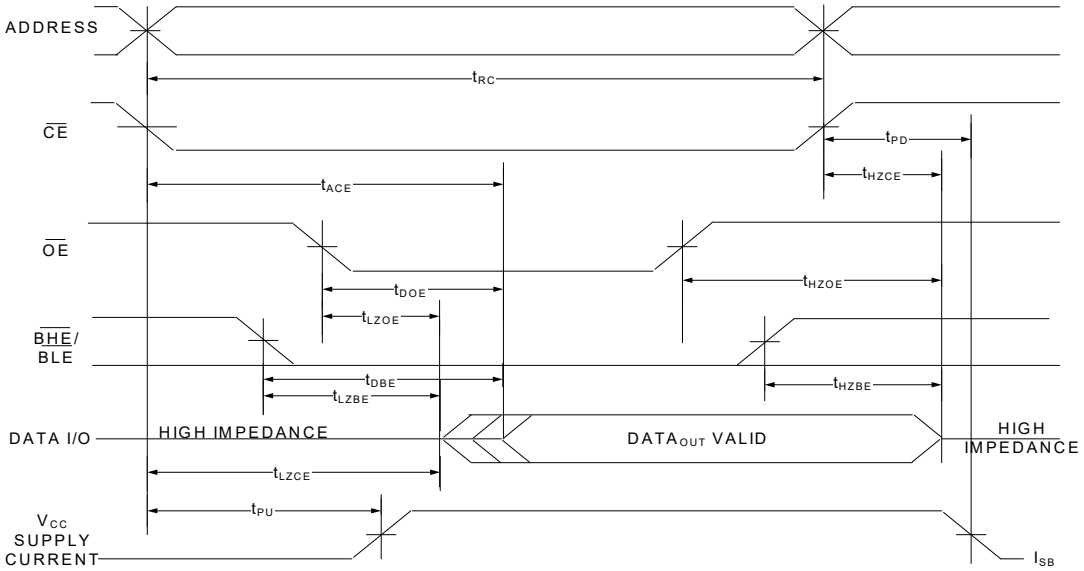
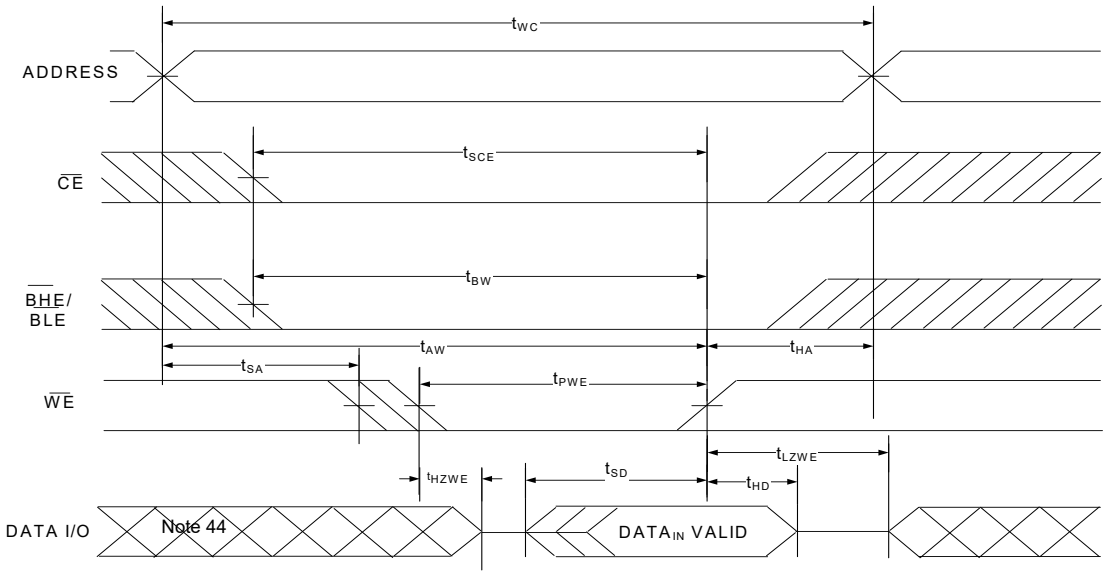


Figure 11. Write Cycle No. 1 (WE Controlled, OE LOW) [40, 42, 43, 33]

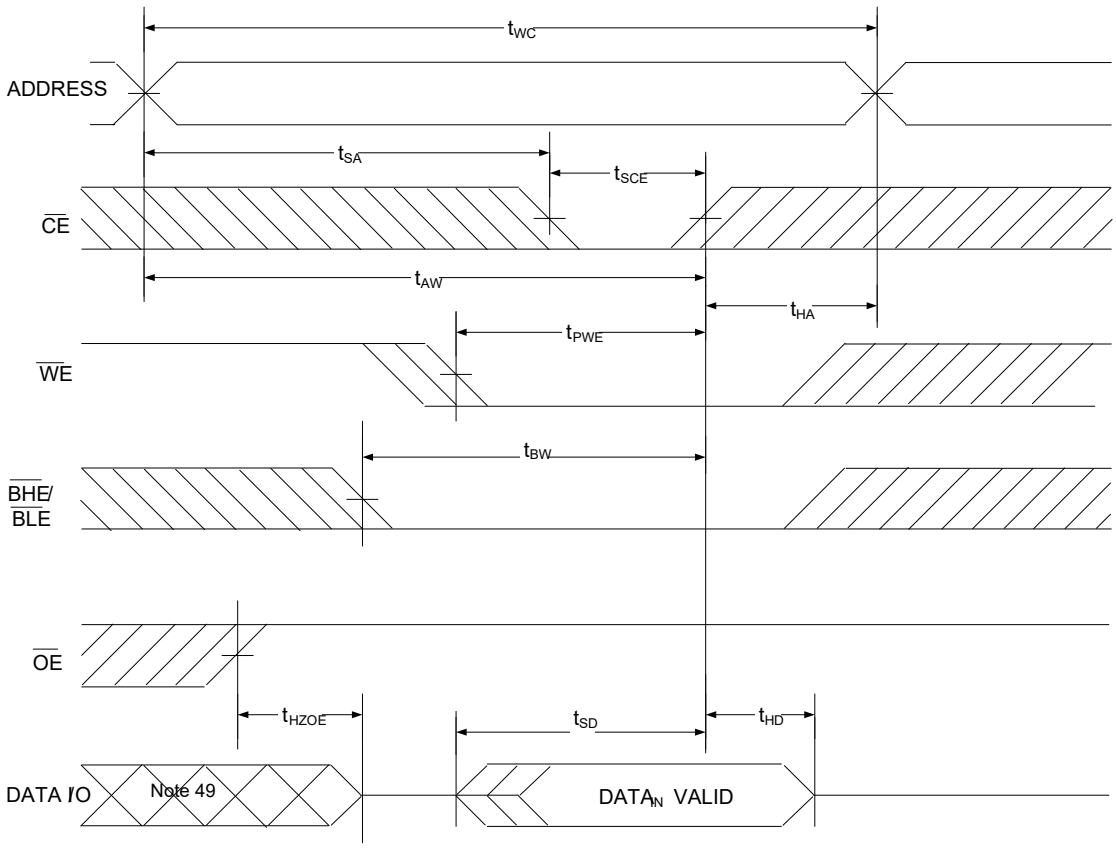


Notes

39. WE is HIGH for read cycle.
40. For all dual chip enable devices, CE is the logical combination of CE_1 and CE_2. When CE_1 is LOW and CE_2 is HIGH, CE is LOW; when CE_1 is HIGH or CE_2 is LOW, CE is HIGH.
41. Address valid prior to or coincident with CE LOW transition.
42. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE_1 = V_{IL}, BHE or BLE, or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
43. Data I/O is in the high-impedance state if CE = V_{IH}, or OE = V_{IH}, or BHE, and/or BLE = V_{IH}.
44. During this period, the I/Os are in the output state. Do not apply input signals.
45. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 2 ($\overline{CE}$ Controlled) [46, 47, 48]



Notes

46. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
47. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
48. Data I/O is in the high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
49. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [50, 51, 52]

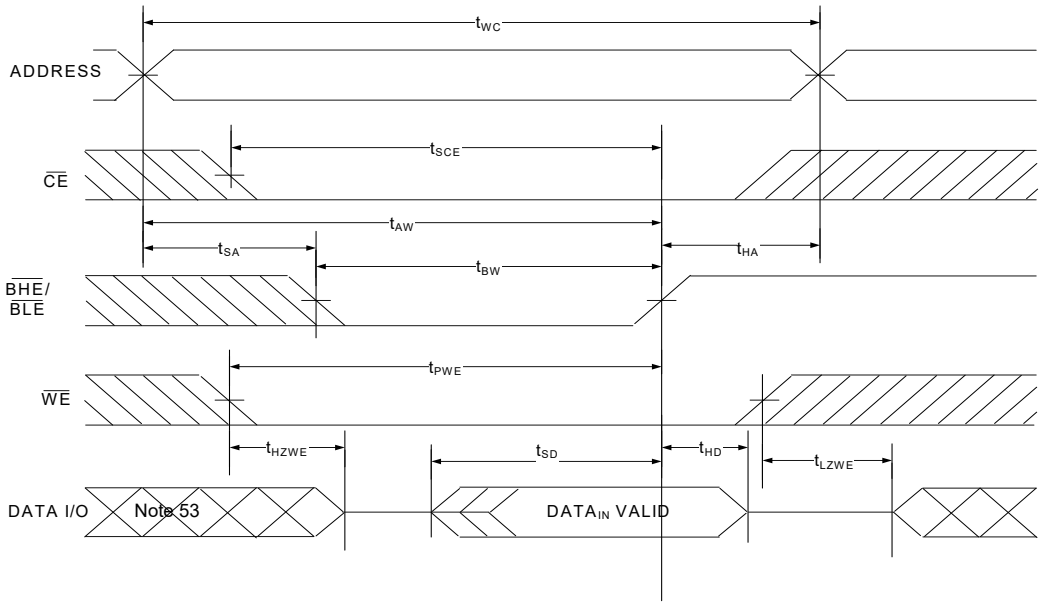
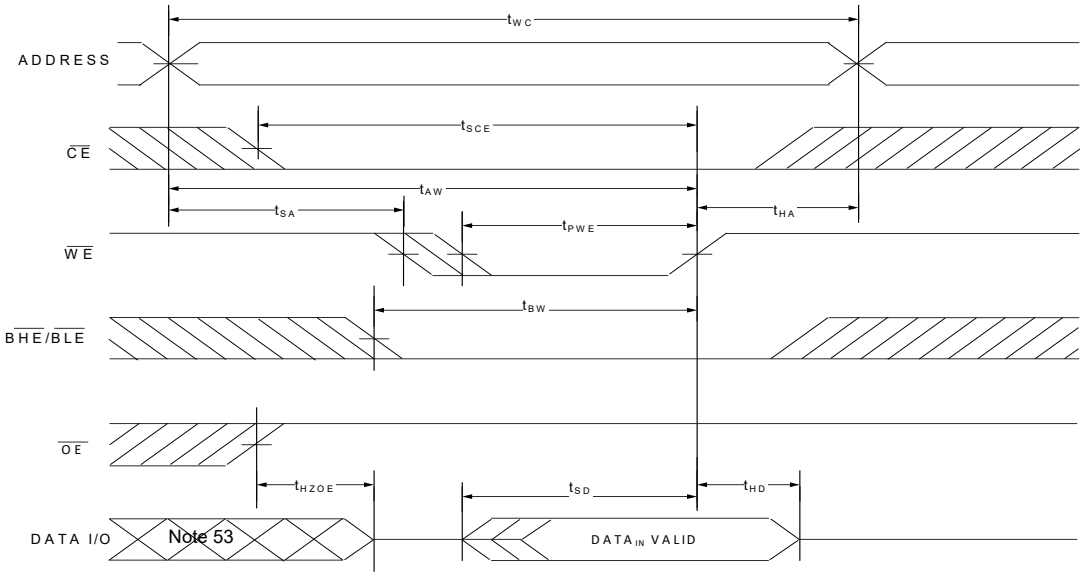


Figure 14. Write Cycle No. 5 (WE Controlled) [50, 51, 52]



Notes

50. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
51. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
52. Data I/O is in the high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
53. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table – CY62167G/CY62167GE

$\overline{BYTE}$ [54]	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power	Configuration
X[55]	H	X[55]	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	2M × 8/1M × 16
X	X[55]	L	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	2M × 8/1M × 16
X	X[55]	X[55]	X	X	H	H	High-Z	Deselect/Power-down	Standby (I_{SB})	1M × 16
H	L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})	1M × 16
H	L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})	1M × 16
H	L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})	1M × 16
H	L	H	H	H	L	H	High-Z	Output disabled	Active (I_{CC})	1M × 16
H	L	H	H	H	H	L	High-Z	Output disabled	Active (I_{CC})	1M × 16
H	L	H	H	H	L	L	High-Z	Output disabled	Active (I_{CC})	1M × 16
H	L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})	1M × 16
H	L	H	L	X	H	L	Data In (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})	1M × 16
H	L	H	L	X	L	H	High-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})	1M × 16
L	L	H	H	L	X	X	Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})	2M × 8
L	L	H	H	H	X	X	High-Z	Output disabled	Active (I_{CC})	2M × 8
L	L	H	L	X	X	X	Data In (I/O_0–I/O_7)	Write	Active (I_{CC})	2M × 8

ERR Output – CY62167GE

Output[56]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

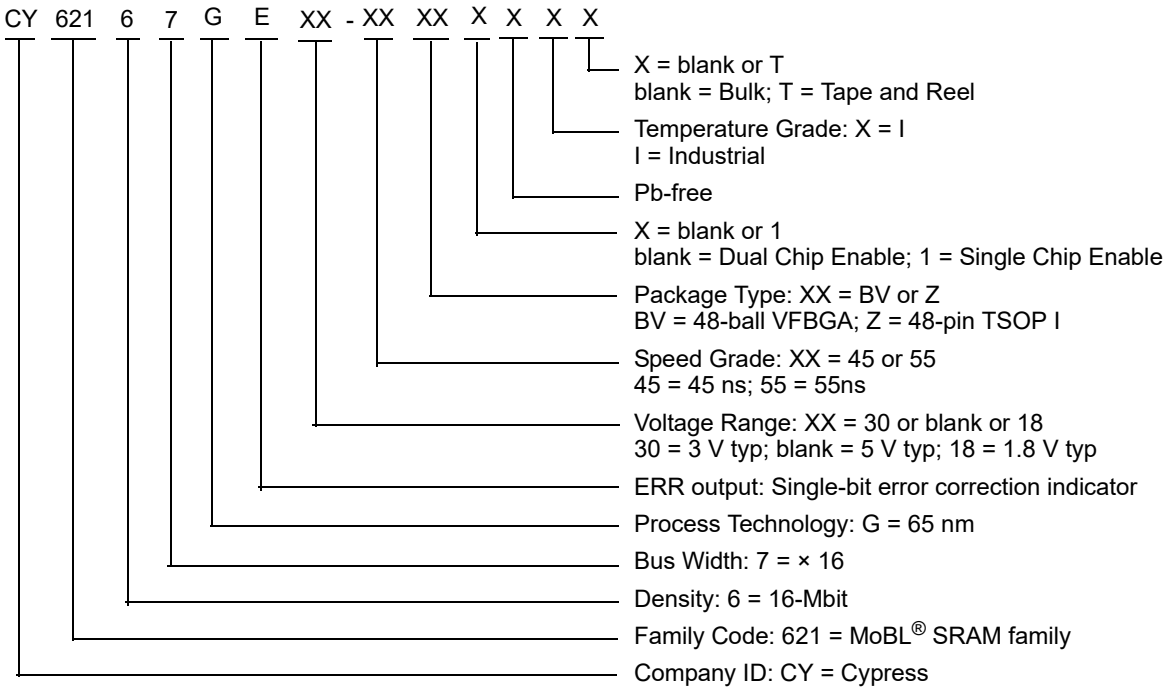
Notes

54. This pin is available only in the 48-pin TSOP I package. Tie the $\overline{BYTE}$ to V_{CC} to configure the device in the 1M × 16 option. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}.
55. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.
56. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

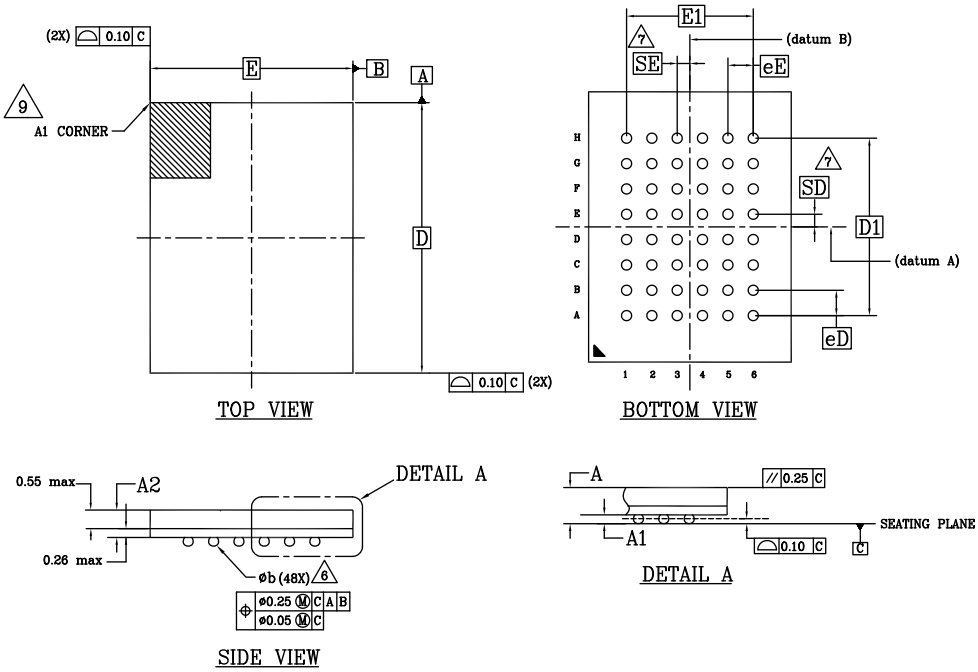
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	ERR Pin / Ball	Operating Range
45	2.2 V–3.6 V	CY62167GE30-45BV1XI	51-85150	48-ball VFBGA	Sing Chip Enable	Yes	Industrial
		CY62167GE30-45BV1XIT					
		CY62167GE30-45BVXI			Dual Chip Enable	Yes	
		CY62167GE30-45BVXIT					
		CY62167G30-45BVXI				No	
		CY62167G30-45BVXIT					
		CY62167GE30-45ZXI	51-85183	48-pin TSOP I	Dual Chip Enable	Yes	
		CY62167GE30-45ZXIT					
		CY62167G30-45ZXI				No	
		CY62167G30-45ZXIT					
	4.5 V–5.5 V	CY62167G-45BVXI	51-85150	48-ball VFBGA	Dual Chip Enable	No	
		CY62167G-45BVXIT					
		CY62167G-45ZXI	51-85183	48-pin TSOP I	Dual Chip Enable	No	
		CY62167G-45ZXIT					
		CY62167GE-45ZXI				Yes	
		CY62167GE-45ZXIT					
55	1.65 V–2.2 V	CY62167GE18-55BVXI	51-85150	48-ball VFBGA	Dual Chip Enable	Yes	
		CY62167GE18-55BVXIT					
		CY62167G18-55BVXI				No	
		CY62167G18-55BVXIT					
		CY62167G18-55ZXI	51-85183	48-pin TSOP I		No	
		CY62167G18-55ZXIT					

Ordering Code Definitions



Package Diagrams

Figure 15. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

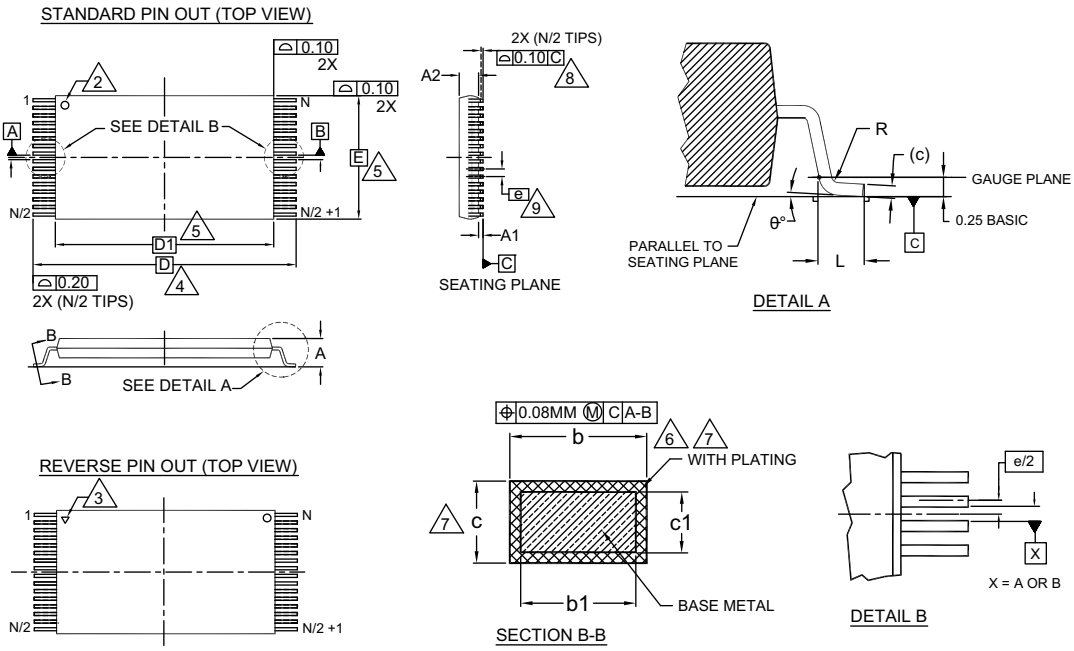
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALLIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 16. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [-C-] . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SRAM	Static random access memory
TSOP	Thin small outline package
VFBGA	Very fine-pitch ball grid array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167G/CY62167GE MoBL, 16-Mbit (1M words × 16-bit/2M words × 8-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81537			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*M	4791835	06/15/2015	Changed status from Preliminary to Final.
*N	5027105	11/25/2015	Updated DC Electrical Characteristics: Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –1.0 mA”.
*O	5439177	09/16/2016	Updated DC Electrical Characteristics: Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Note 11 (Replaced 2 ns with 20 ns). Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated to new template.
*P	5751153	05/26/2017	Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*Q	6607623	09/23/2019	Updated Product Portfolio: Added Notes 3 and 4; and referred the same notes in CY62167G(E)30. Updated DC Electrical Characteristics: Added Notes 15 and 16; and referred the same notes in “2.2 V to 2.7 V”, “2.7 V to 3.6 V” in “Description” column corresponding to V_{OH}, V_{OL}, V_{IH}, V_{IL} parameters. Added Notes 18 and 19; and referred the same notes in “V_{CC} = 2.2 V to 3.6 V” in “Description” column corresponding to I_{SB1}, I_{SB2} parameters. Updated Data Retention Characteristics: Added Notes 25 and 26; and referred the same notes in “2.2 V < V_{CC} ≤ 3.6 V” in “Conditions” column corresponding to I_{CCDR} parameter. Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template. Completing Sunset Review.

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