

Description

The AUIRS2184(4)S are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Feature Comparison: AUIRS2181(4)/AUIRS2183(4)/AUIRS2184(4)

Part	Input Logic	Cross-Conduction Prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	160/200 ns
21814				V_{SS}/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 500ns	COM	160/200 ns
21834			Programmable 0.4 – 5 us	V_{SS}/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 500ns	COM	600/230 ns
21844			Programmable 0.4 – 5 us	V_{SS}/COM	

Qualification Information†

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8	MSL3†† 260°C (per IPC/JEDEC J-STD-020)
		SOIC14N	
ESD	Machine Model	Class M1 (Pass +/-100V) (per AEC-Q100-003)	
	Human Body Model	Class H1C (Pass +/-1500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A††† (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

††† IN, SD, DT Class II Level B at 40mA per JESD78.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition		Min	Max	Units
V_B	High-side floating absolute voltage		-0.3	620	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20†	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable deadtime pin voltage		V_{SS} -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} -0.3	V_{CC} + 0.3	
V_{SS}	Logic ground		V_{CC} - 20	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	(8-lead SOIC)	—	0.625	W
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead SOIC)	—	200	°C/W
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min	Max	Units
V_B	High-side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	(††)	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$) (†††)	V_{SS}	V_{CC}	
DT	Programmable deadtime pin voltage	V_{SS}	V_{CC}	
V_{SS}	Logic ground	-5	5	
T_A	Ambient temperature	-40	125	°C

†† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to Design Tip DT97-3 for more details).

††† HIN and LIN are internally clamped with a 5.2 V zener diode.

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	600	900	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	230	400		V_S = 0 V or 600 V
t_{sd}	Shut-down propagation delay	—	220	350		
MT_{on}	Delay matching, HS & LS turn-on	—	3	90		
MT_{off}	Delay matching , HS & LS turn-off	—	15	40		
t_r	Turn-on rise time	—	15	60		V_S = 0 V
t_f	Turn-off fall time	—	12	35		
DT	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	280	375	520		R_{DT} = 0 Ω
		3.9	5	6	µs	R_{DT} = 200 kΩ
MDT	Deadtime matching DT_{LO-HO} - DT_{HO-LO}	—	0	50	ns	R_{DT} = 0 Ω
		—	0	600		R_{DT} = 200 kΩ

Static Electrical Characteristics

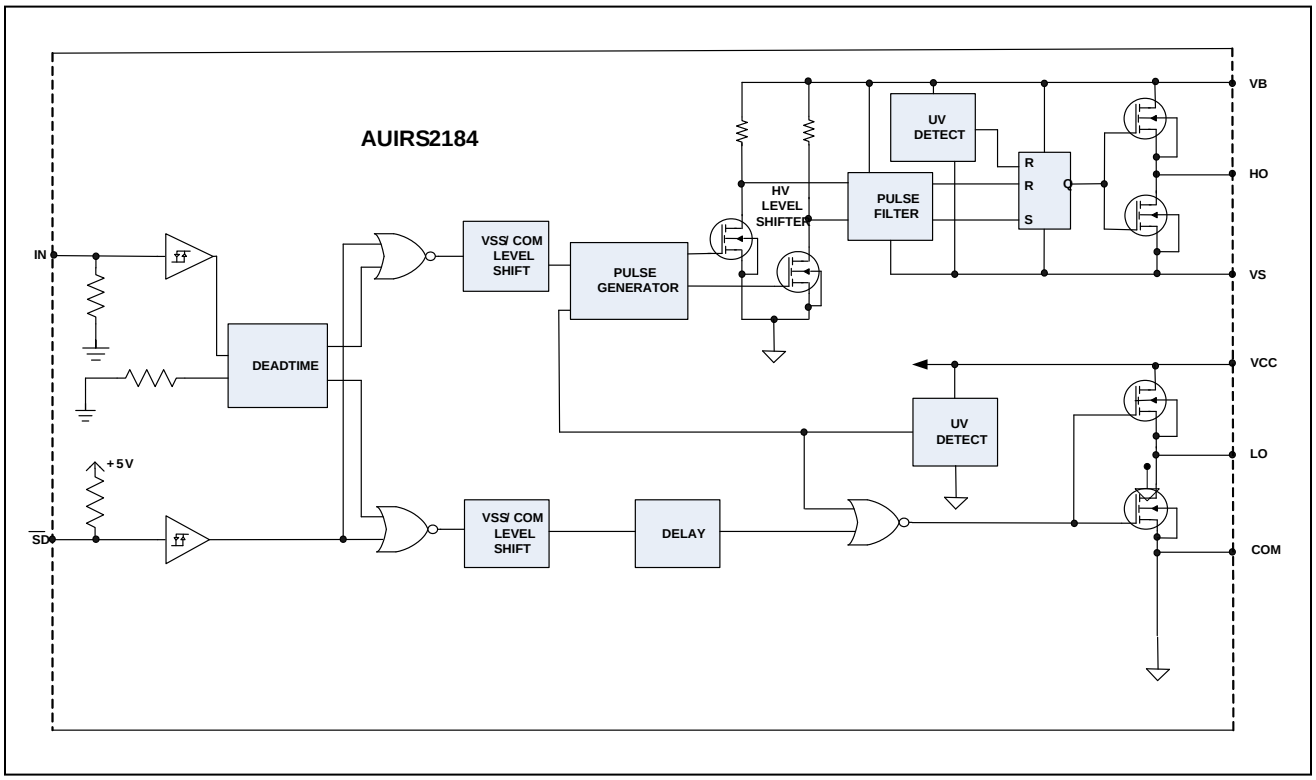
Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM. The $V_{IL,}$ V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: IN and $\overline{SD}$. The $V_{O,}$ I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

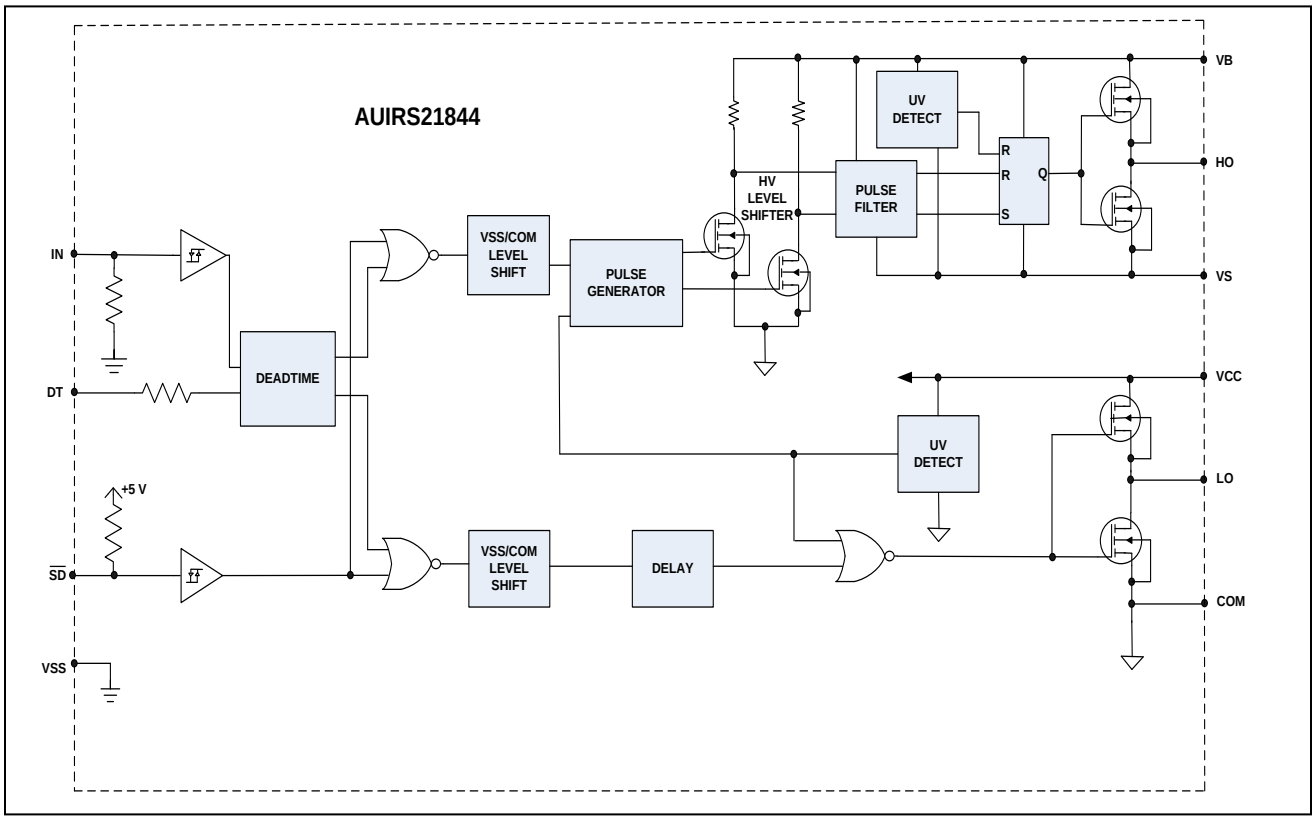
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.5	—	—		
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.5		I_O = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.2		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	10	50	130		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.3	mA	
I_{IN+}	Logic "1" input bias current	—	25	60	µA	IN = 5 V, $\overline{SD}$ = 0 V
I_{IN-}	Logic "0" input bias current	—	—	5.0		IN = 0 V, $\overline{SD}$ = 5 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O25+} (†)	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0V, PW ≤ 10us, T_J = 25°C
I_{O25-} (†)	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V, PW ≤ 10us, T_J = 25°C
I_{O+} (†) (††)	Output high short circuit pulsed current	1.2	—	—		V_O = 0 V, PW ≤ 10 µs
I_{O-} (†) (††)	Output low short circuit pulsed current	1.5	—	—		V_O = 15 V, PW ≤ 10 µs

(†) Guaranteed by design

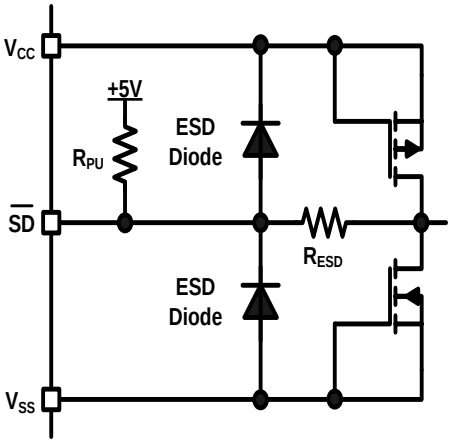
(††) I_{O+} and I_{O-} decrease with rising temperature

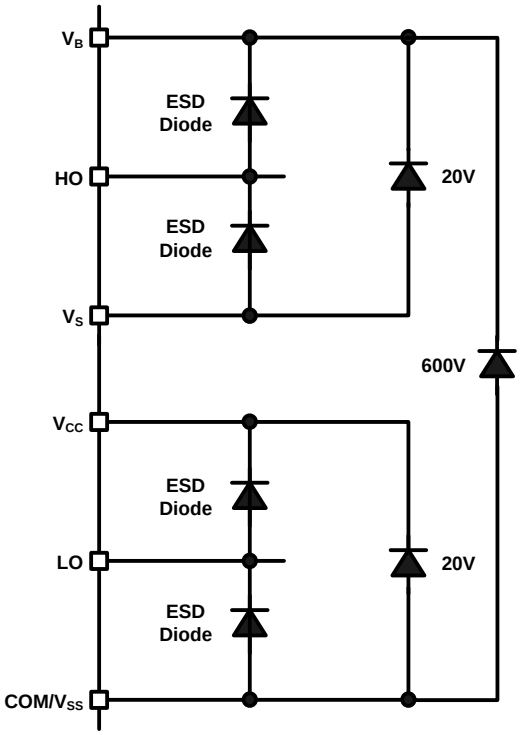
Functional Block Diagram: AUIRS2184, AUIRS21844

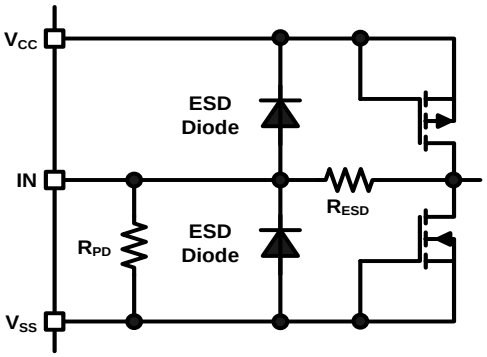


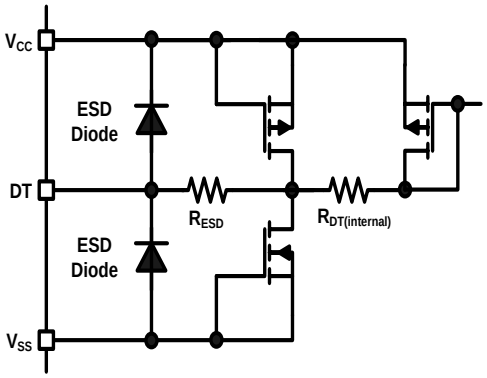


Input/Output Pin Equivalent Circuit Diagrams: AUIRS2184S

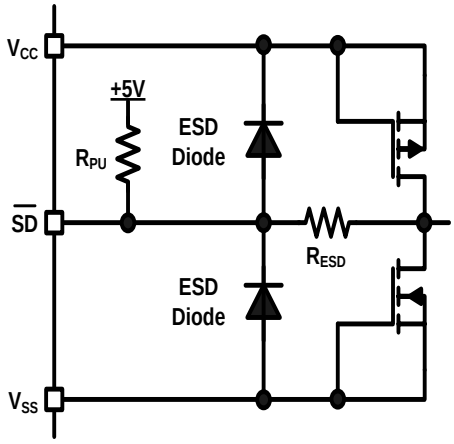


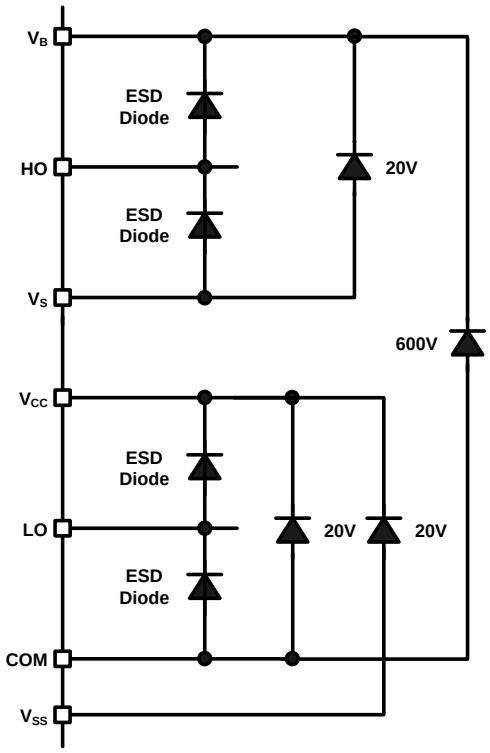


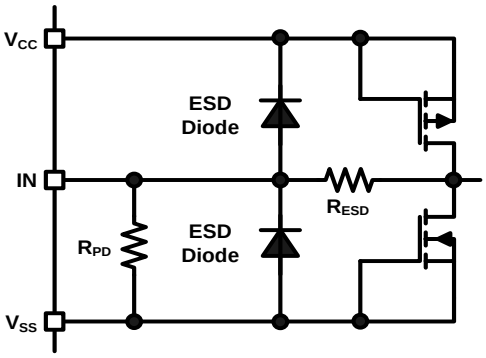


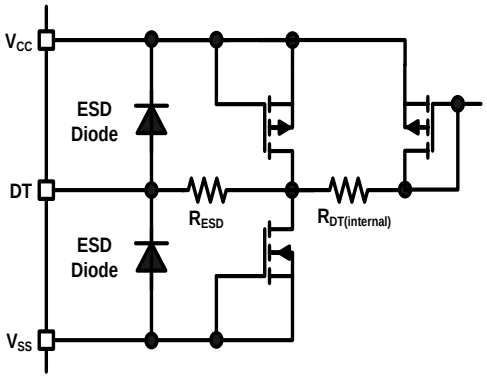


Input/Output Pin Equivalent Circuit Diagrams: AUIRS21844S





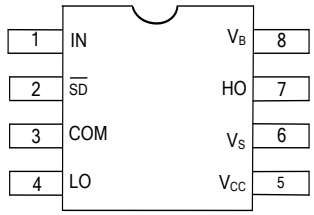




Lead Definitions

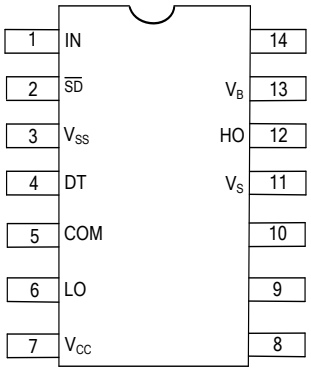
Symbol	Description
IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to COM for AUIRS2184 and V_{SS} for AUIRS21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for AUIRS2184 and V_{SS} for AUIRS21844)
DT	Programmable deadtime lead, referenced to V_{SS} (AUIRS21844 only)
V_{SS}	Logic ground (AUIRS21844 only)
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments: AUIRS2184(4)S



8-Lead SOIC

AUIRS2184(S)



14-Lead SOIC
Narrow Body

AUIRS21844(S)

Application Information and Additional Details

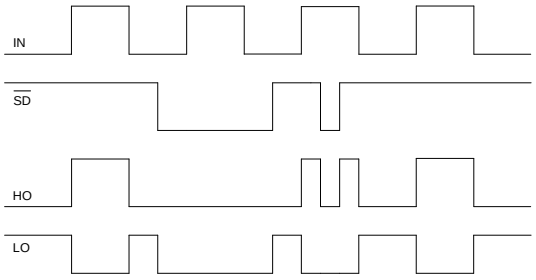


Figure 1: Input/Output Timing Diagram

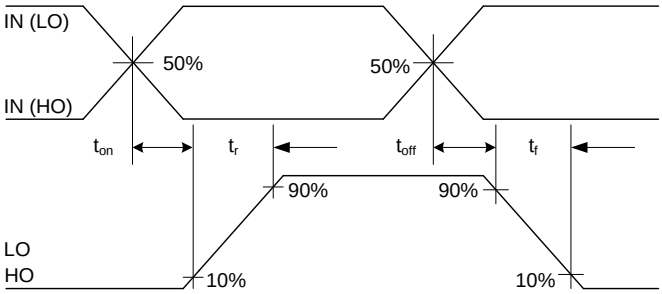


Figure 2: Switching Time Waveform Definitions

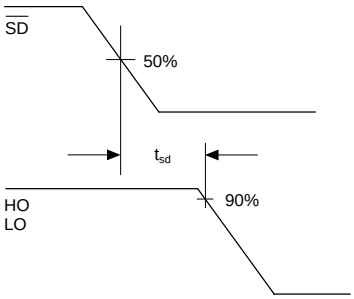


Figure 3: Shutdown Waveform Definitions

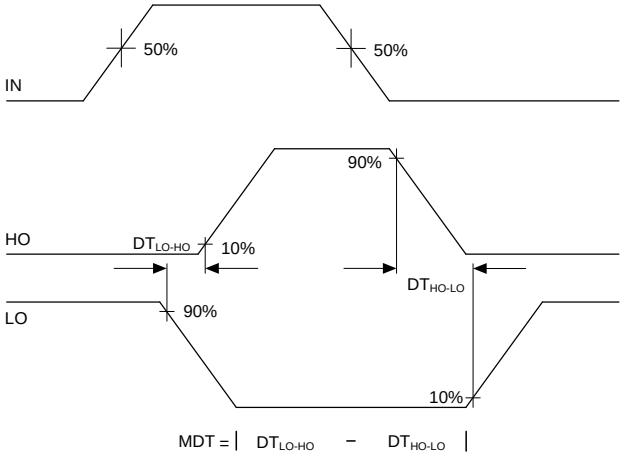


Figure 4: Deadtime Waveform Definitions

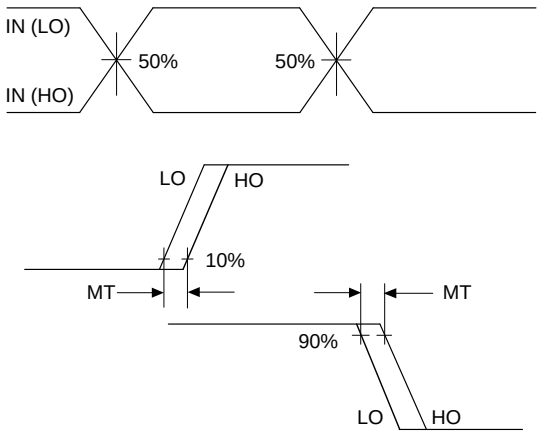


Figure 5: Delay Matching Waveform Definitions

Tolerability to Negative VS Transients

The AUIRS21844S has been seen to withstand negative V_S transient conditions on the order of -20V for a period of 400 ns.
An illustration of the AUIRS21844S performance can be seen in Figure 7, where points above the lines represent pulses that the circuit can withstand (with V_{CC}=V_{BS}= 15V).
Two curves are present in figure 7: one refers to ambient temperature T_A=25 °C, the other refers to tests performed at T_A=-40 °C, 25 °C and 125 °C.
Even though the AUIRS21844S has been shown able to handle these negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

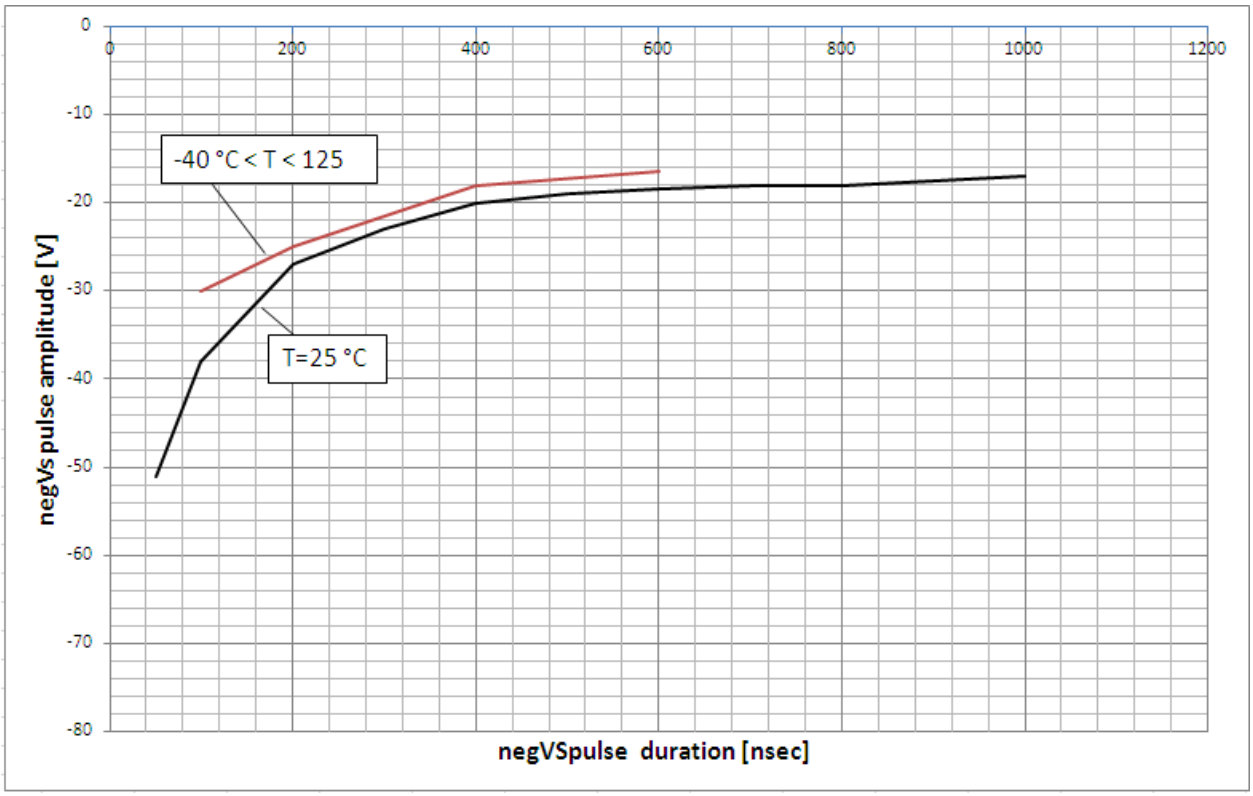


Figure 7: -Vs Transient results

Parameter Trends vs. Temperature and vs. Supply Voltage

Figures of this chapter provide information on the experimental performance of the AUIRS2184(4)S HVIC. The line plotted in each figure is generated from actual lab data.

A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

A different set of individual samples was used to generate curves of parameter trends vs. supply voltage.

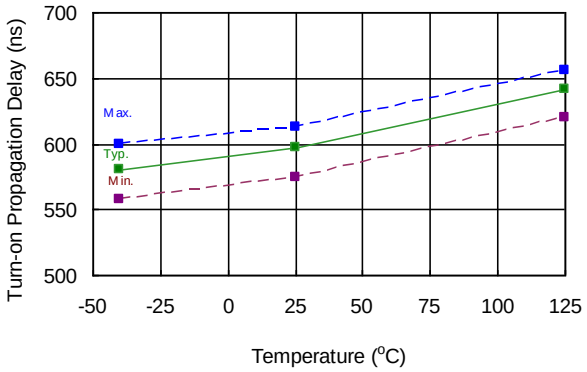


Figure 6A. Turn-on Propagation Delay vs. Temperature

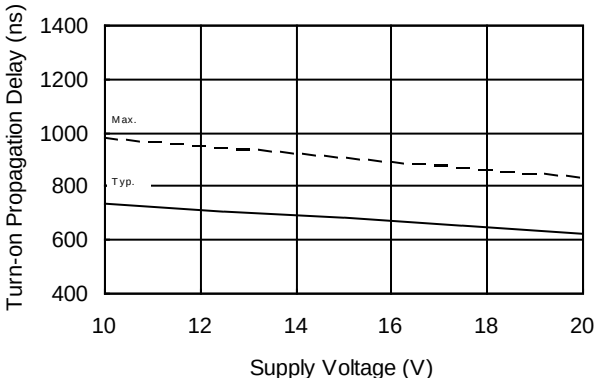


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

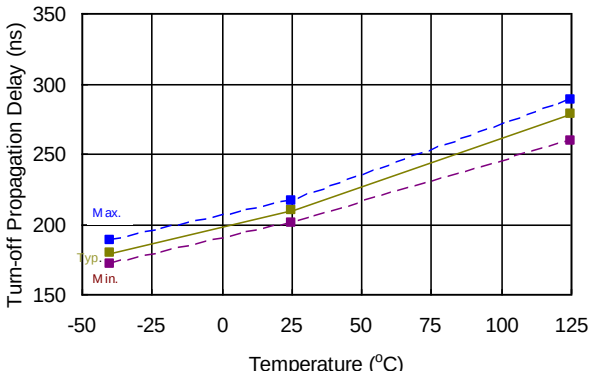


Figure 7A. Turn-off Propagation Delay vs. Temperature

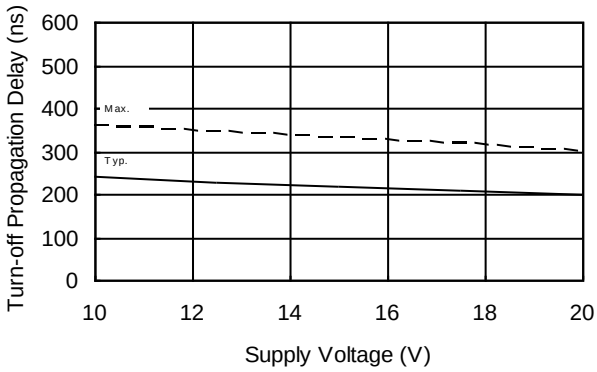


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

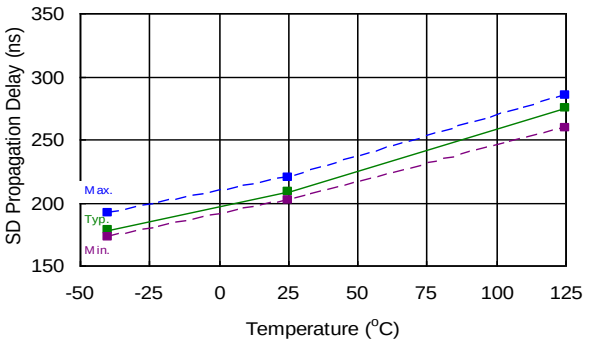


Figure 8A. SD Propagation Delay vs. Temperature

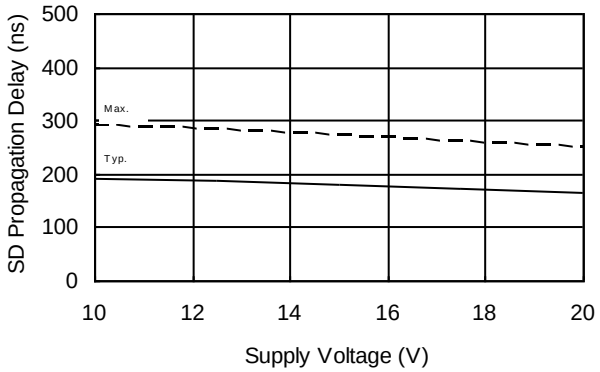


Figure 8B. SD Propagation Delay vs. Supply Voltage

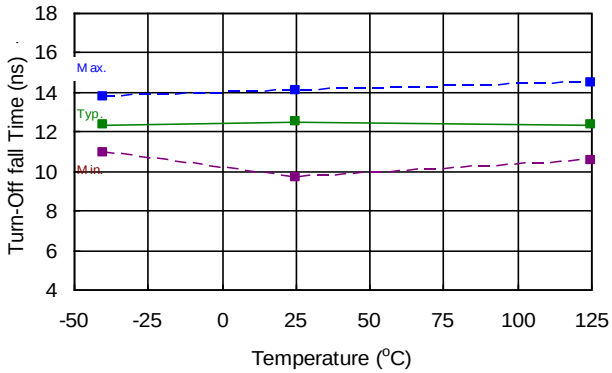


Figure 9A. Turn-off Fall Time vs. Temperature

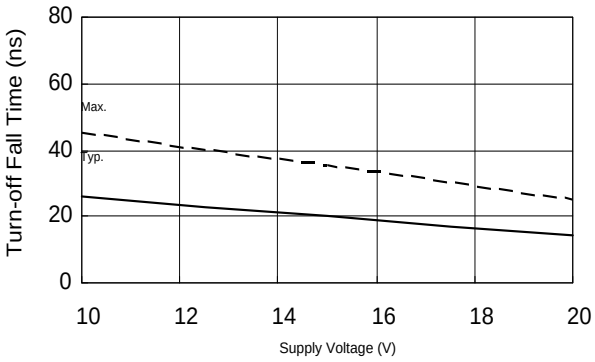


Figure 10B. Turn-off Fall Time vs. Supply Voltage

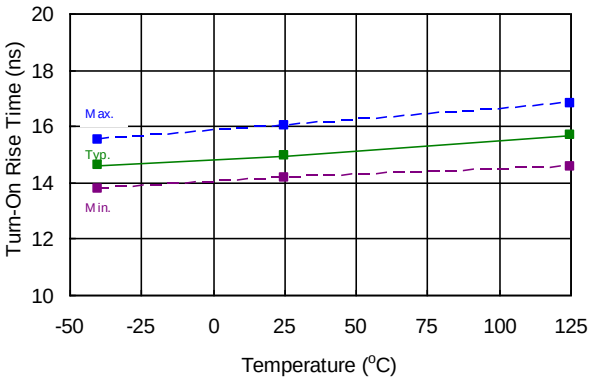


Figure 10. Turn-on Rise Time vs. Temperature

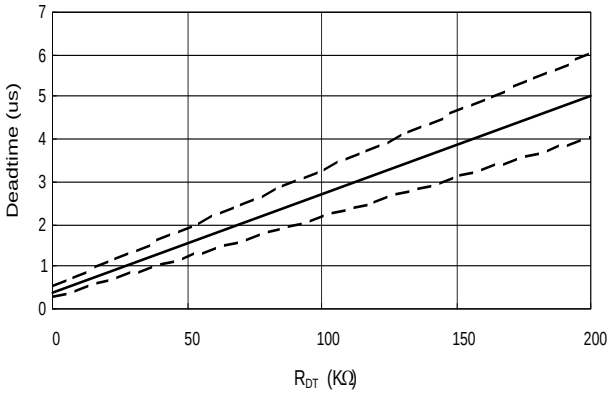


Figure 11. Deadtime vs R_{DT}

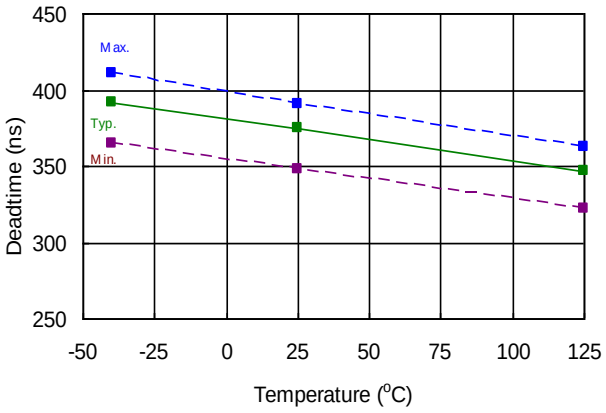


Figure 12A. Deadtime vs Temperature

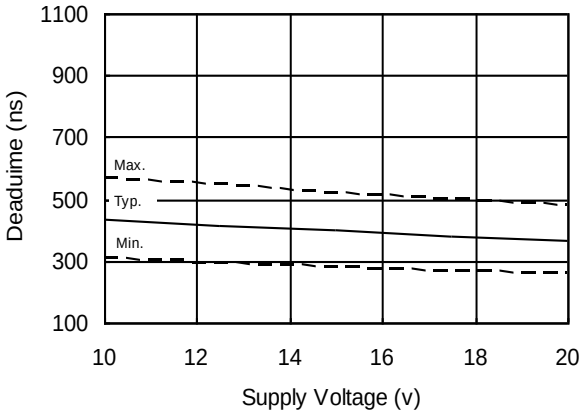


Figure 12B. Deadtime vs. Supply Voltage

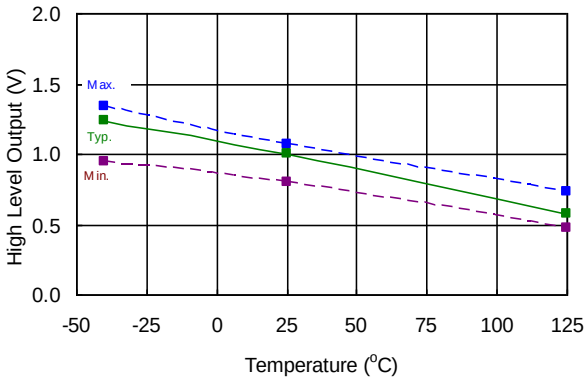


Figure 13. High Level Output vs. Temperature (I_O = 0 mA)

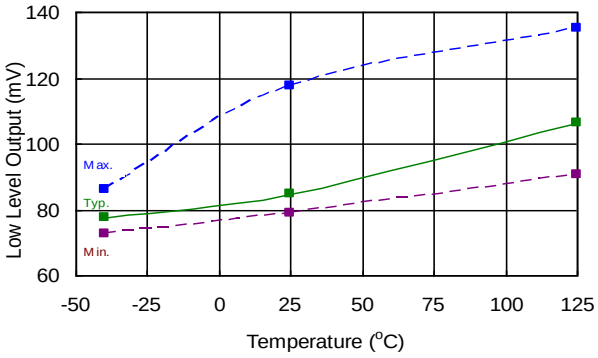


Figure 14. Low Level Output vs. Temperature

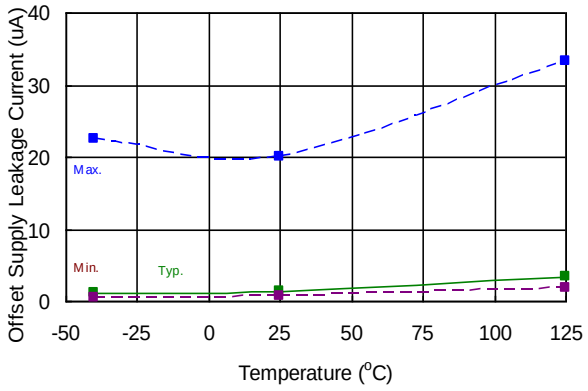


Figure 15. Offset Supply Leakage Current vs. Temperature

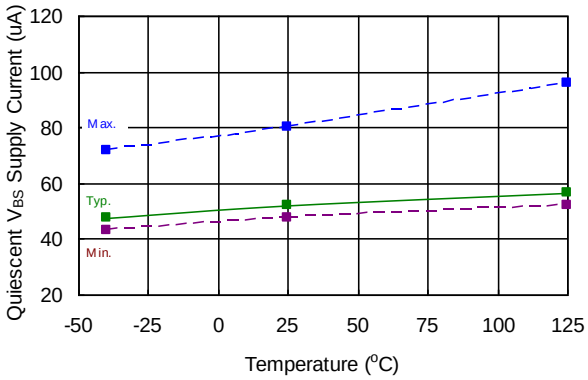


Figure 16. V_{BS} Supply Current vs. Temperature

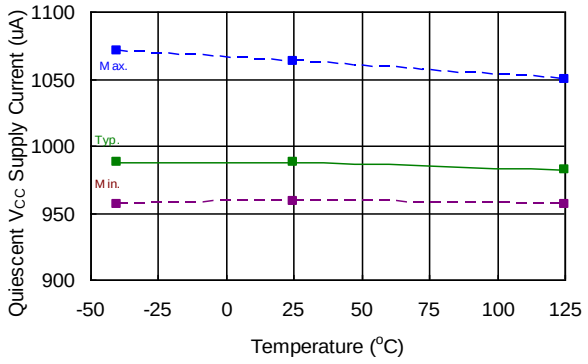


Figure 17A. V_{cc} Supply Current vs. Temperature

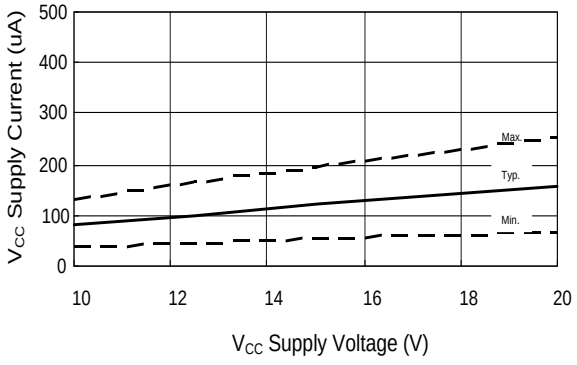


Figure 17B. V_{CC} Supply Current vs. V_{CC} Supply Voltage (V)

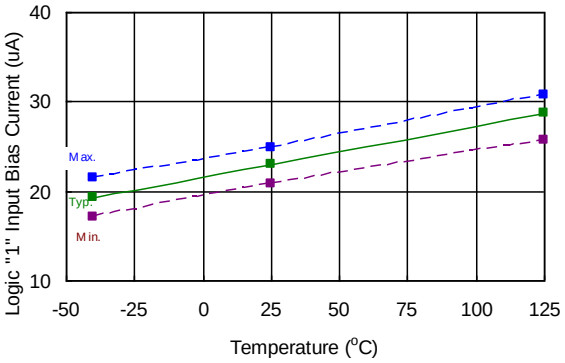


Figure 18. Logic "1" Input Bias Current vs. Temperature

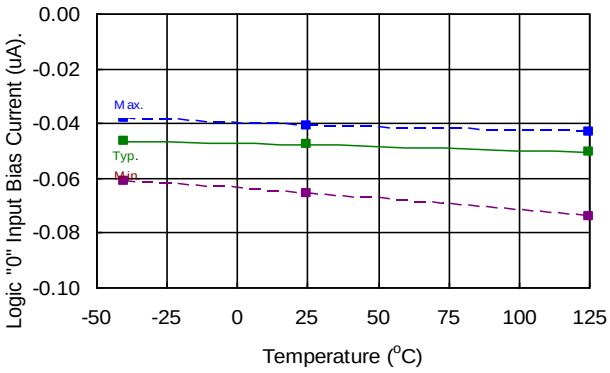


Figure 19. Logic "0" Input Bias Current vs. Temperature

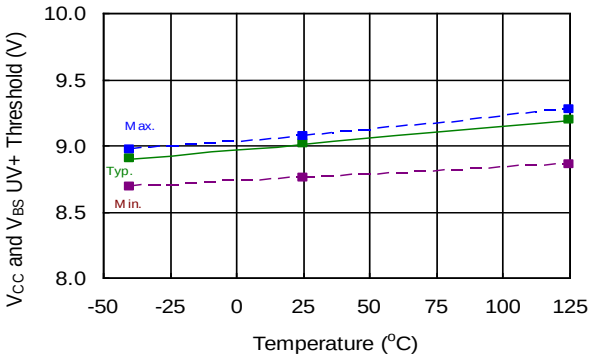


Figure 20. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

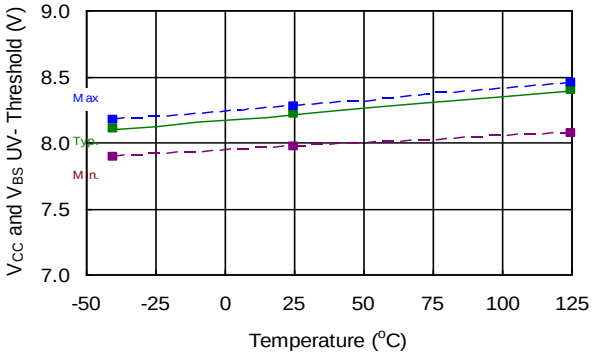


Figure 21. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

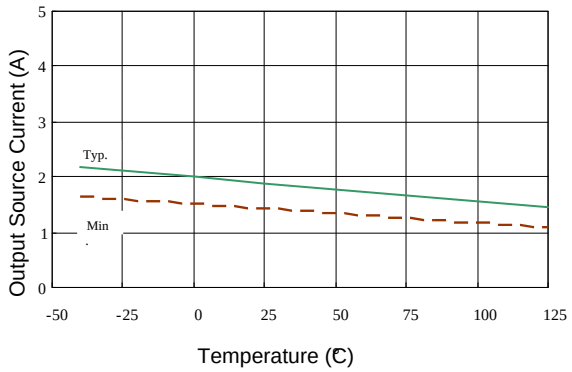


Figure 22. Output Source Current (A) vs. Temperature

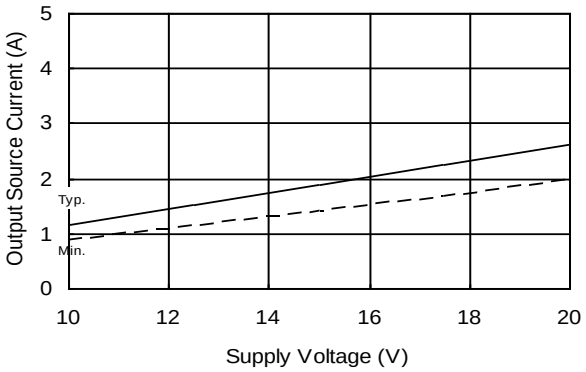


Figure 22A. Output Source Current (A) vs. Supply Voltage (V)

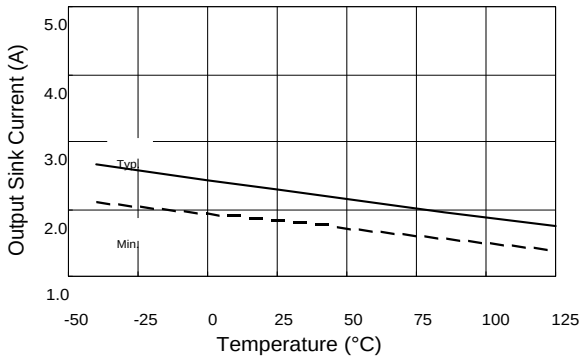


Figure 23. Output Sink Current (A) vs. Temperature

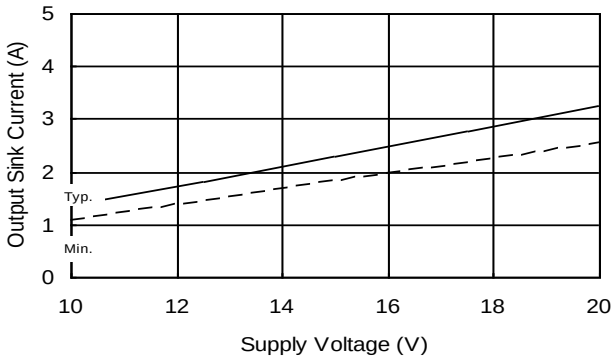
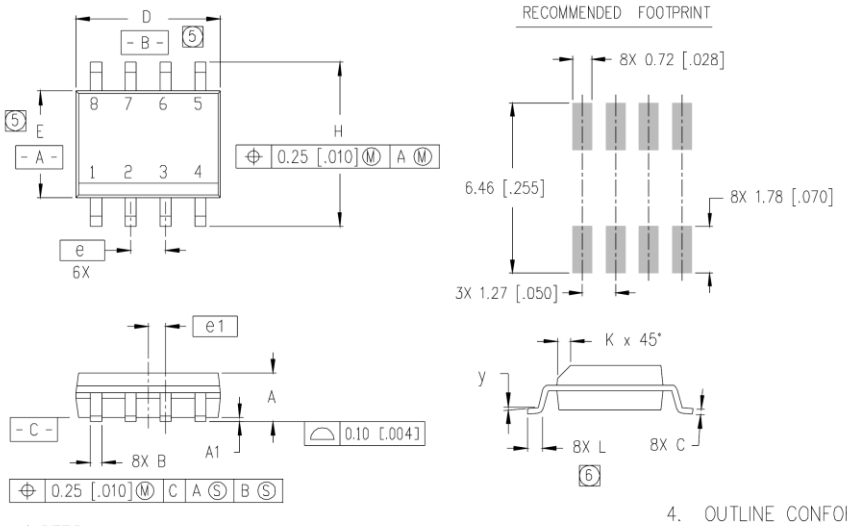


Figure 23A. Output Sink Current (A) vs. Supply Voltage (V)

Package Details: SOIC8



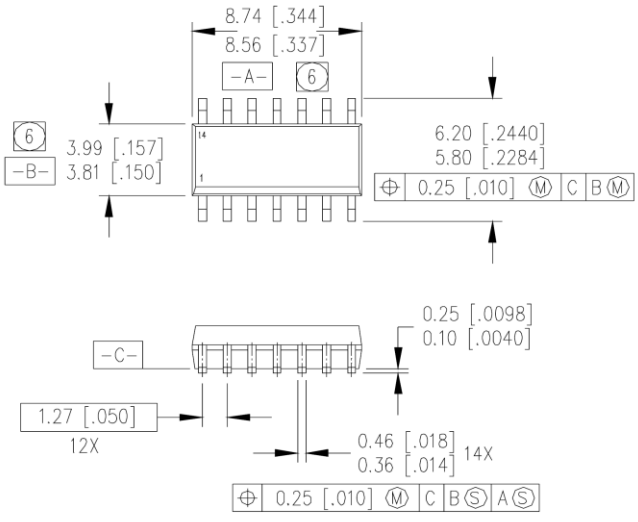
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

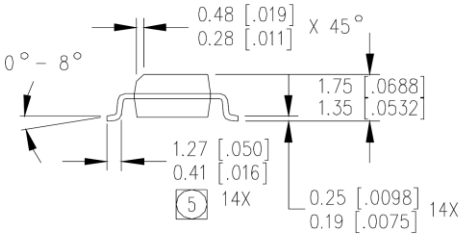
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

Package Details: SOIC14N



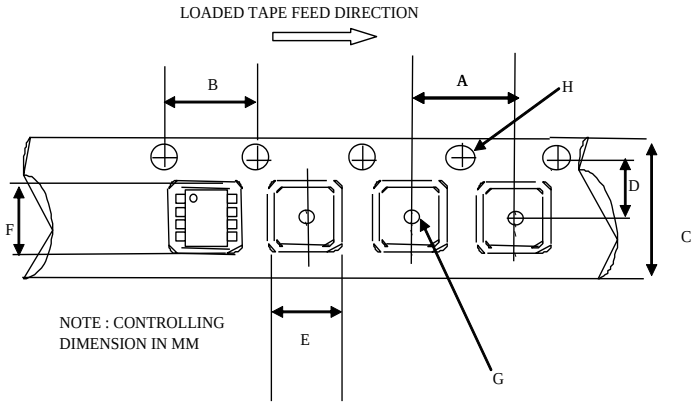


NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

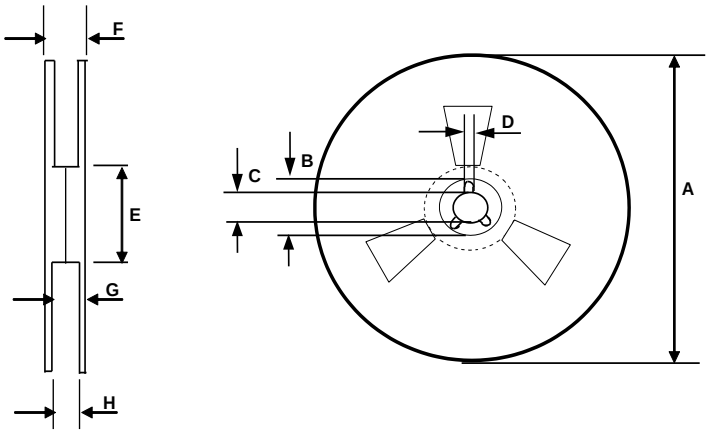
14 Lead SOIC (narrow body)

Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

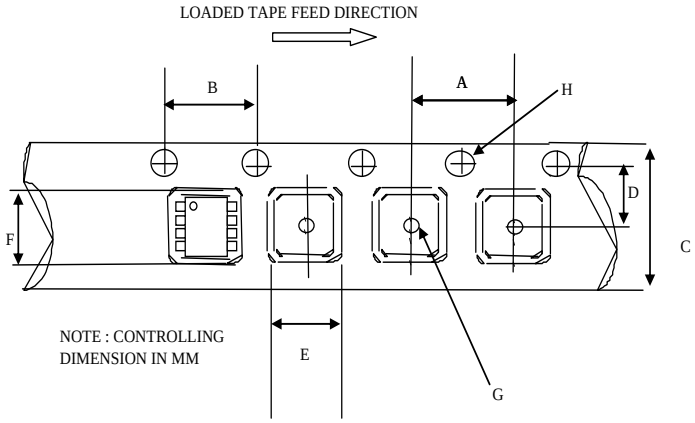
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

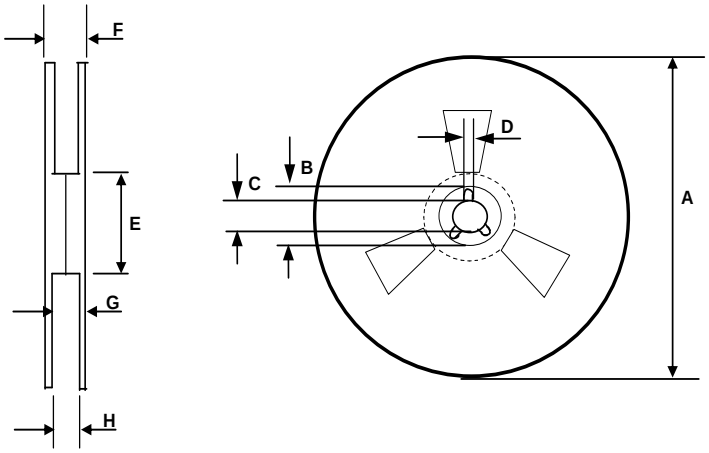
	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Tape and Reel Details: SOIC14N



CARRIER TAPE DIMENSION FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

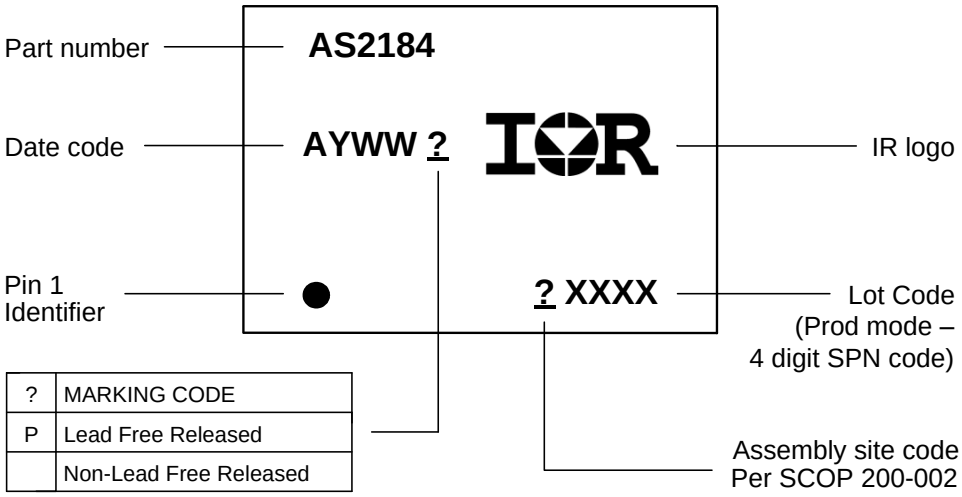


REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

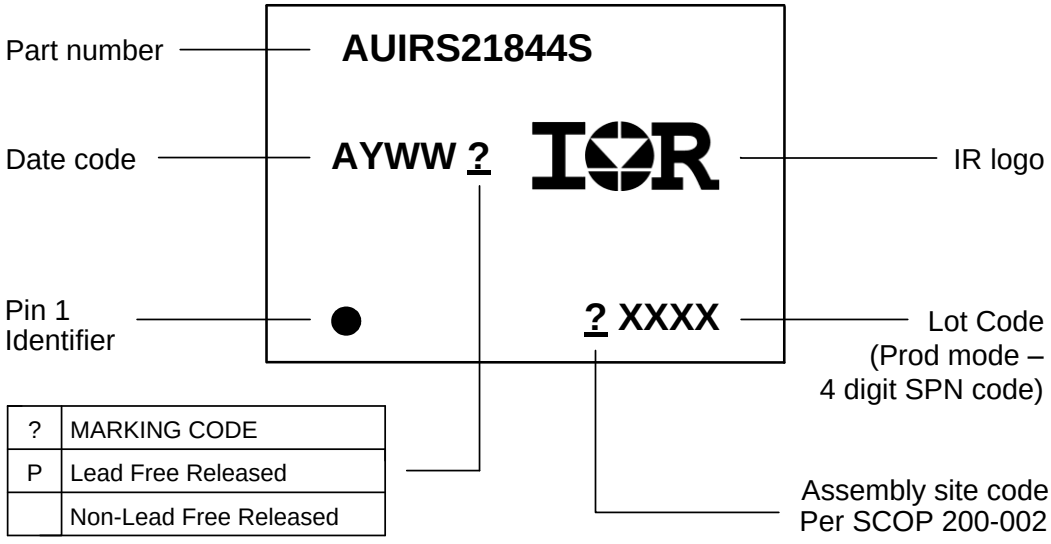
Part Marking Information

SOIC8:



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

SOIC14N:



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2184S	SOIC8	Tube/Bulk	55	AUIRS2184S
		Tape and Reel	***2500***	AUIRS2184STR
AUIRS21844S	SOIC14N	Tube/Bulk	55	AUIRS21844S
		Tape and Reel	***2500***	AUIRS21844STR

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233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

Date	Comment
04/29/08	Draft
5/6/08	Converted to automotive format
5/13/08	Corrected various formatting issues and typos (e.g. /SD) Corrected typical application dwg
5/16/08	Inserted figures 1-5
5/22/08	Added graphs for parameter temperature trends
5/26/08	Added missing graphs, added note on PbF and auto qualification on features list
5/28/08	Added date
9/30/08	Reviewed and updated various missing information
10/01/08	Inserted Input/Output Pin Equivalent Circuit Diagram
Feb13th, 2009	Typ application changes
6/04/09	Updated package information, qualification information, and tri-temp waveforms
8/4/09	Updated qualification information; graphs 27-42 changed 2181(4) to 2184(4)
8/6/09	Removed characterization graphs 27-42.
8/11/09	Updated package type and marking info
9/15/09	Corrected chapter with Parameter Trends SD max propagation delay changed from 270ns to 300ns Turn on rise time typ value changed from 40nsec to 20nsec
9/19/09	Rearranged temperature characteristic graphs and added actual part number on marking drawings
9/21/09	Added ESD passing voltages, updated table of contents.
9/22/09	Typ application section updated
9/23/09	Added note 1 for Vcc under Abs Max rating
12/17/09	Front page: changed ton/toff typ. to 600ns/230ns, Page6: changed Ton typ.=600ns; toff typ.=230ns; tsd typ.=220ns, max=350ns; MTon typ.=3ns; MToff typ.=15ns; tr typ=15ns; tf typ=12ns, DT (R_{DT}@200Kohms) min=3.9uS; DT (0-ohm) typ=375ns; VOH max.=1.5V; iqbs min.=10uA, typ=50uA, max=130uA; Iqcc max.=1.3mA; added Important Notice page
12/22/09	Corrected MSL level on qual info page to MSL3 and updated MM ESD passing voltage to +/-100V instead of +/-150V.
02/24/2010	Updated disclaimer under Abs. Max. Rating Page 6: Added I_{O25+} and I_{O25-} specification and the note
Jul. 27, 2010	clamp diode values changed from 25V into 20V (in-out pin eq. circ. diagrams)
Aug 29th, 2011	AUIRS2184 Functional Block diagram: COM no more shorted to Vss.
Dec 22nd, 2012	Added paragraph “Tolerability to Negative VS Transients”
July 22, 2014	Page 4: Removed note II from AEC-Q100

