

### Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	75			V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temp. Coefficient		0.09		V/°C	Reference to 25°C, $I_D$ = 5mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		2.5	3.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 140A ⑤
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0		4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
gfs	Forward Trans conductance	230			S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 140A
R <sub>G</sub>	Gate Resistance		1.2		Ω	
1	Drain to Course Lookage Current			20		$V_{DS} = 75V, V_{GS} = 0V$
I <sub>DSS</sub>	Drain-to-Source Leakage Current			250	μA	$V_{DS} = 75V, V_{GS} = 0V$ $V_{DS} = 75V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I <sub>GSS</sub>	Gate-to-Source Forward Leakage			100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage			-100	ПА	V <sub>GS</sub> = -20V

### Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

-			,		
$Q_{g}$	Total Gate Charge	 160	240		I <sub>D</sub> = 140A
$Q_{gs}$	Gate-to-Source Charge	 38			V <sub>DS</sub> = 38V
$Q_{gd}$	Gate-to-Drain Charge	 54		nC	V <sub>GS</sub> = 10V⑤
Q <sub>sync</sub>	Total Gate Charge Sync. (Qg - Qgd)	 106			
t <sub>d(on)</sub>	Turn-On Delay Time	 19			V <sub>DD</sub> = 49V
tr	Rise Time	 110			I <sub>D</sub> = 140A
t <sub>d(off)</sub>	Turn-Off Delay Time	 99		ns	R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	 100			V <sub>GS</sub> = 10V⑤
C <sub>iss</sub>	Input Capacitance	 9370			V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	 840			V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	 580		pF	f = 1.0MHz, See Fig. 5
Coss eff.(ER)	Effective Output Capacitance (Energy Related)	 1130		-	$V_{GS}$ = 0V, $V_{DS}$ = 0V to 60V $\odot$
Coss eff.(TR)	Effective Output Capacitance (Time Related)	 1500			$V_{GS}$ = 0V, $V_{DS}$ = 0V to 60V®

### **Diode Characteristics**

	Parameter	Min.	Тур.	Max.	Units	C	onditions
ls	Continuous Source Current			230①		MOSFET sy	
I <sub>SM</sub>	(Body Diode) Pulsed Source Current			900	A	showing the integral reve	erse ett
V <sub>SD</sub>	(Body Diode) ② Diode Forward Voltage			1.3	V	p-n junction T <sub>J</sub> = 25°C,I <sub>S</sub>	<u>alode.</u> = 140A,V <sub>GS</sub> = 0V ©
t <sub>rr</sub>	Reverse Recovery Time		54		ns	T <sub>J</sub> = 25°C	V <sub>DD</sub> = 64V
41			60		113	T <sub>J</sub> = 125°C	l <sub>F</sub> = 140A, di/dt = 100A/µs⑤
Q <sub>rr</sub>	Reverse Recovery Charge		103		nC	T <sub>J</sub> = 25°C	
Qrr	The verse mecovery charge		132			T <sub>J</sub> = 125°C	
I <sub>RRM</sub>	Reverse Recovery Current		3.6		Α	T <sub>J</sub> = 25°C	
t <sub>on</sub>	Forward Turn-On Time	Intrinsio	turn-or	n time is	negligi	ble (turn-on is	dominated by L <sub>S</sub> +L <sub>D</sub> )

#### Notes:

Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

 $\odot$  Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.045mH, R<sub>G</sub> = 25 $\Omega$ , I<sub>AS</sub> = 140A, V<sub>GS</sub> =10V. Part not recommended for use above this value.

 $\label{eq:ISD} \textcircled{$ I_{SD} \leq 140A, \, di/dt \leq 1380A/\mu s, \, V_{DD} \leq V_{(BR)DSS}, \, T_J \leq 175^\circ C. $ }$ 

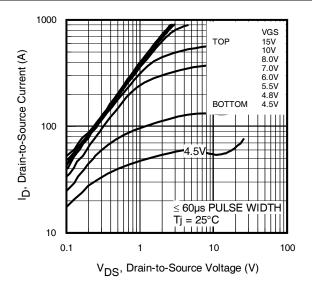
© Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 80% VDSS.

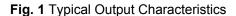
 $\odot$  C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.

- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

 $@ \ R_{\theta JC}$  value shown is at time zero







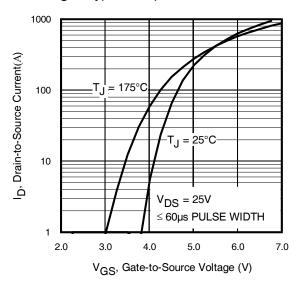


Fig. 3 Typical Transfer Characteristics

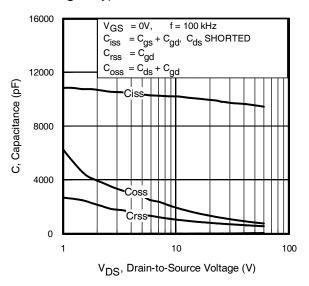


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

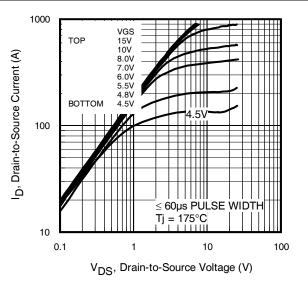


Fig. 2 Typical Output Characteristics

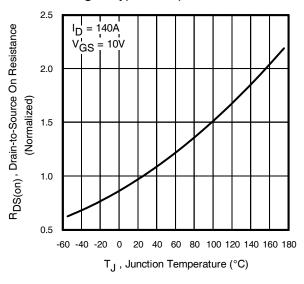


Fig. 4 Normalized On-Resistance vs. Temperature

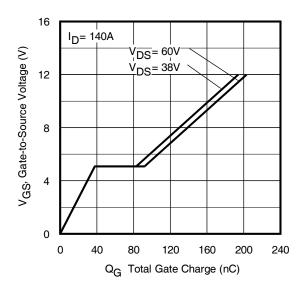
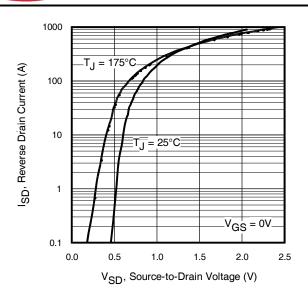
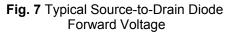


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage







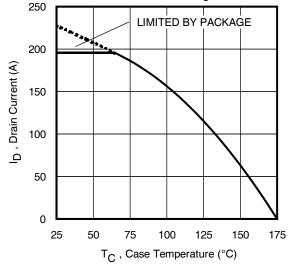


Fig 9. Maximum Drain Current vs. Case Temperature

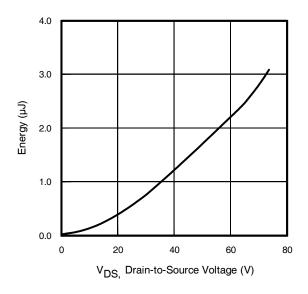


Fig 11. Typical Coss Stored Energy

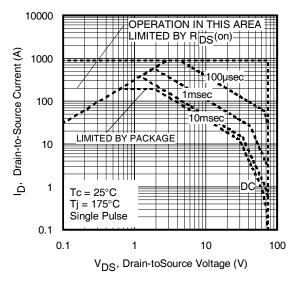


Fig 8. Maximum Safe Operating Area

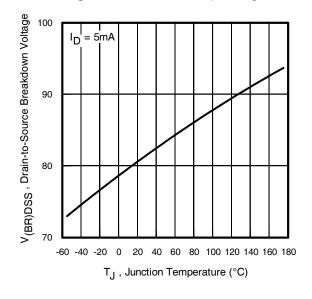


Fig 10. Drain-to-Source Breakdown Voltage

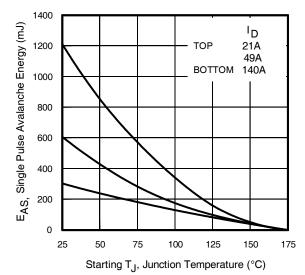


Fig 12. Maximum Avalanche Energy vs. Drain Current



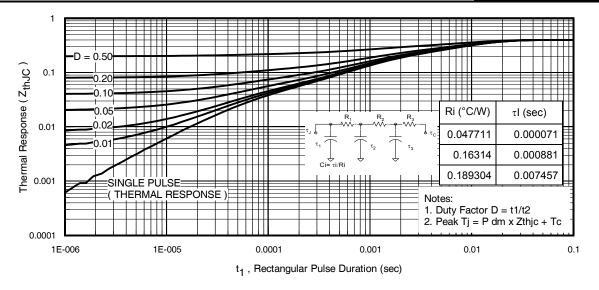


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

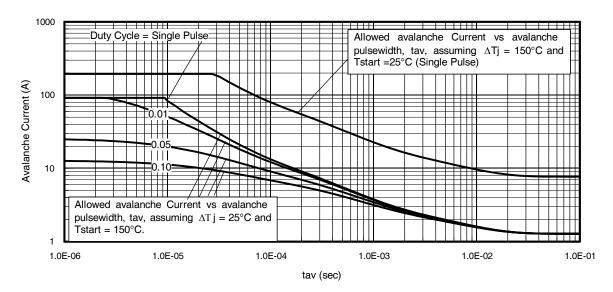
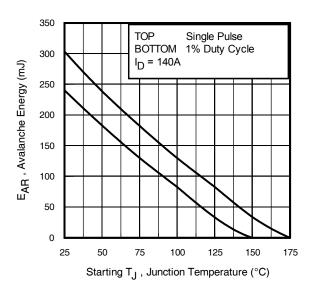


Fig 14. Avalanche Current vs. Pulse width



Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>jmax</sub>. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. Iav = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed T<sub>jmax</sub> (assumed as 25°C in Figure 13, 14).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$\begin{split} \mathsf{P}_{\mathsf{D}\;(\mathsf{ave})} &= \mathsf{1}/\mathsf{2}\;(\;\mathsf{1.3}\cdot\mathsf{BV}\cdot\mathsf{I}_{\mathsf{av}}) = \Delta\mathsf{T}/\;\mathsf{Z}_{\mathsf{thJC}}\\ \mathsf{I}_{\mathsf{av}} &= \mathsf{2}\Delta\mathsf{T}/\;[\mathsf{1.3}\cdot\mathsf{BV}\cdot\mathsf{Z}_{\mathsf{th}}]\\ \mathsf{E}_{\mathsf{AS}\;(\mathsf{AR})} &= \mathsf{P}_{\mathsf{D}\;(\mathsf{ave})}\cdot\mathsf{t}_{\mathsf{av}} \end{split}$$

### Fig 15. Maximum Avalanche Energy vs. Temperature



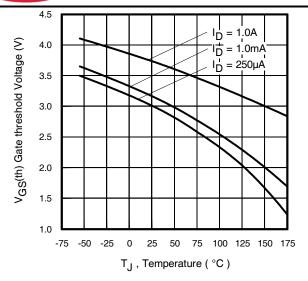


Fig 16. Threshold Voltage vs. Temperature

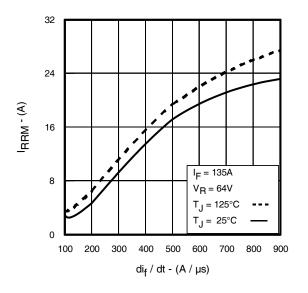


Fig. 18 - Typical Recovery Current vs. dif/dt

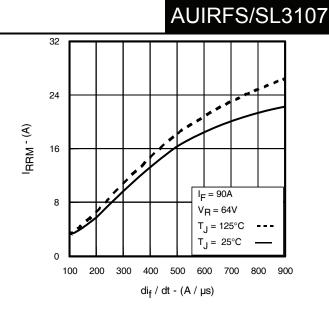


Fig. 17 - Typical Recovery Current vs. dif/dt

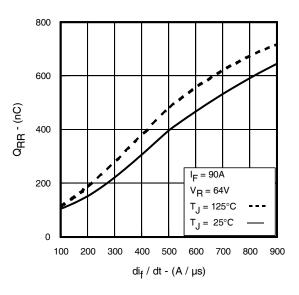


Fig. 19 - Typical Stored Charge vs. dif/dt

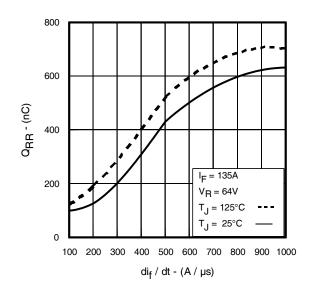
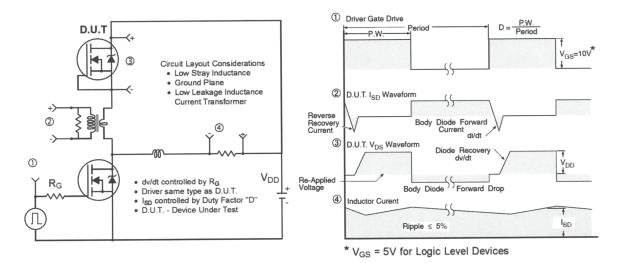
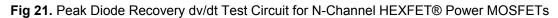


Fig. 20 - Typical Stored Charge vs. dif/dt







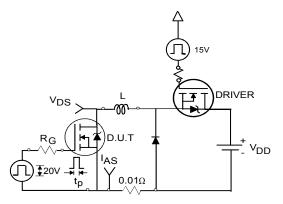


Fig 22a. Unclamped Inductive Test Circuit

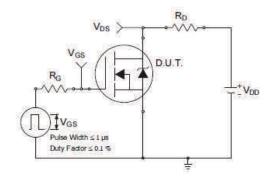


Fig 23a. Switching Time Test Circuit

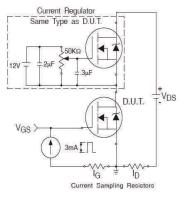


Fig 24a. Gate Charge Test Circuit

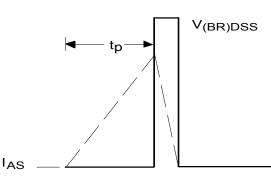
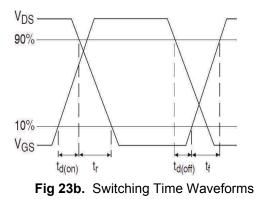


Fig 22b. Unclamped Inductive Waveforms



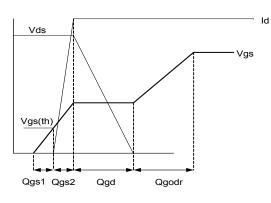
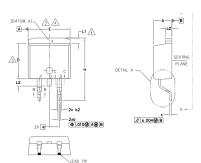


Fig 24b. Gate Charge Waveform



### D<sup>2</sup> Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION 61, 63 AND c1 APPLY TO BASE METAL ONLY.

6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

7. CONTROLLING DIMENSION: INCH.

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

<u>\_\_\_\_\_6</u> |--−b1, b3---| -BASE METAL PLATING  $\triangle$ 1 🛆 —(b, b2)ţţ SECTION B-B & C-C SCALE: NONE VIEW A-A н DETAIL "A" ROTATED 90° CW SCALE 8:1 B SEATING PLANE A1\_ 13

S Y M	DIMENSIONS					
B O	MILLIM	ETERS	INC	O T E S		
L	MIN.	MAX.	MIN.	MAX.	E S	
А	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
Ь	0.51	0.99	.020	.039		
Ь1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
С	0.38	0.74	.015	.029		
с1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	_	.270	—	4	
Е	9.65	10.67	.380	.420	3,4	
Ε1	6.22	_	.245	—	4	
е	2.54	BSC	.100 BSC			
Н	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
∟1	_	1.68	-	.066	4	
L2	_	1.78	-	.070		
L3	0.25	25 BSC .010 BSC		BSC		

LEAD ASSIGNMENTS

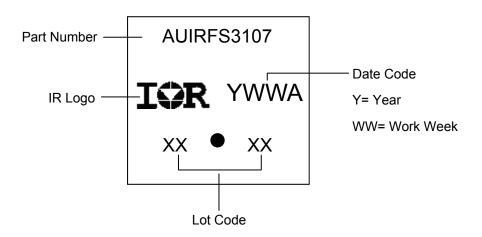
HEXFET

1.- GATE 2, 4.- DRAIN 3.- SOURCE

DIODES 1.- ANODE (TWO DIE) / OPEN (ONE DIE) 2. 4.- CATHODE 3.- ANODE

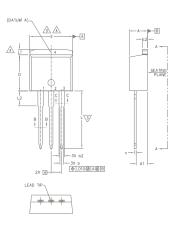
I<u>GBTs, CoPACK</u> 1.- GATE 2, 4.- COLLECTOR 3.- EMITTER

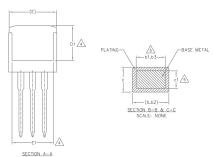
### D<sup>2</sup> Pak (TO-263AB) Part Marking Information





### TO-262 Package Outline (Dimensions are shown in millimeters (inches)





NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED C.127 [.OGS"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- 5. DIMENSION 61 AND c1 APPLY TO BASE METAL ONLY.
- 6. CONTROLLING DIMENSION: INCH.
- 7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

#### LEAD ASSIGNMENTS

IGBTs.	CoPACK

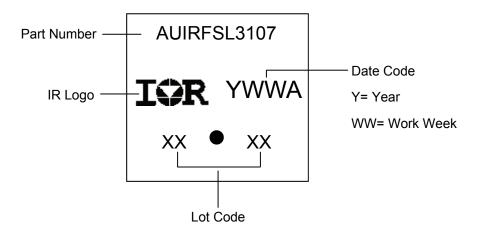
- 1.- GATE 2.- COLLECTOR 3.- EMITTER 4.- COLLECTOR

HEXFET DIODES

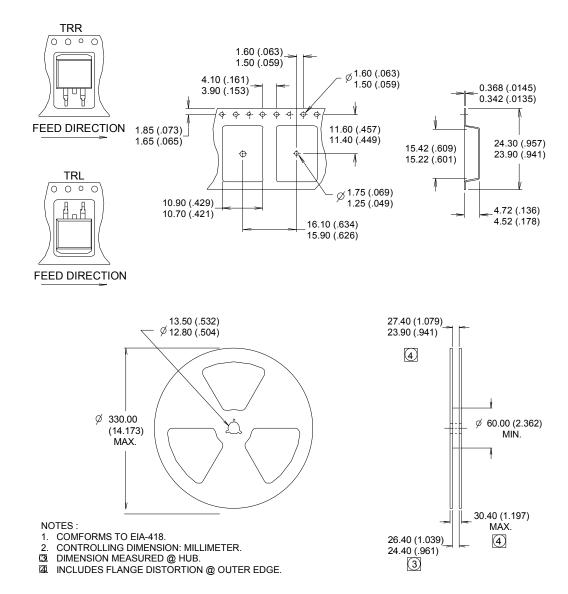
- 1.- GATE
  - 1.- ANODE (TWO DIE) / OPEN (ONE DIE) 2, 4.- CATHODE 3.- ANODE
- 2.- DRAIN 3.- SOURCE
- 4.- DRAIN

S Y		N			
MB	MILLIMETERS INCHES				O T E S
0 L	MIN.	MAX.	MIN.	MAX.	S
Α	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
С	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245		4
е	2.54	BSC	.100		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

### **TO-262 Part Marking Information**



### D<sup>2</sup> Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))





### **Qualification Information**

	Comments: Thi						
	Comments: This part number(s) passed Automotive qualification. Infineon's						
	Industrial and Consumer qualification level is granted by extension of the higher						
		Automotive level.					
Moisture Sensitivity Level		MSL1					
lachina Madal	Class M4 (+/- 800V) <sup>†</sup>						
Machine Model	AEC-Q101-002						
Human Body Model	Class H3A (+/- 6000V) <sup>†</sup>						
	AEC-Q101-001						
Charged Device Model	Class C5 (+/- 2000V) <sup>†</sup>						
	AEC-Q101-005						
RoHS Compliant		Yes					
	ivity Level achine Model uman Body Model harged Device Model	Automotive leve   D <sup>2</sup> -Pak   TO-262   achine Model   uman Body Model   harged Device Model					

† Highest passing voltage.

### **Revision History**

Date	Comments		
10/08/2015	<ul><li>Updated datasheet with corporate template</li><li>Corrected ordering table on page 1.</li></ul>		
10/11/2017	Corrected typo error on part marking on page 8,9.		

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