- Complete Firmware Upgrade OTA
- Integrated Flash Memory for System Software
  - 4 Mb Flash - ATWINC1500B
  - 8 Mb Flash - ATWINC1510B
- SPI Host Interface
- Power Save Modes:
  - <4 µA Power Down mode typical at 3.3V I/O
  - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)[1]
  - On-chip low-power sleep oscillator
  - Fast host wake up from the Doze mode by a pin or host I/O transaction
- Fast Boot Options:
  - On-chip boot ROM (firmware instant boot)
  - SPI Flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables
  - Fast AP re-association (150 ms)
- On-Chip Network Stack to Offload MCU:
  - Integrated network IP stack to minimize host CPU requirements
  - Network features: TCP, UDP, DHCP, ARP, HTTP, TLS, and DNS
- Hardware Accelerators for Wi-Fi and TLS Security to Improve Connection Time
- Hardware Accelerator for IP Checksum
- Hardware Accelerators for OTA Security

Note:

1. For more details on module power modes, see Power Consumption section.
2. For more information on software feature, refer to *Wi-Fi Network Controller Software Design Guide* (DS00002389).

Table of Contents

1. Ordering Information and IC Marking

The following table provides the ordering information for the ATWINC1500B and ATWINC1510B.

Table 1-1. Ordering Details

Ordering Code[1]	Package Type	Package Size	IC Marking
ATWINC1500B-MU-ABCD	QFN in Tray, Tape and Reel	5 mm x 5 mm	ATWINC1500B
ATWINC1510B-MU-ABCD	QFN in Tape and Reel	5 mm x 5 mm	ATWINC1510B

Note:

1. ABCD interprets as:
   "A" can be "Y" indicating Tray, or "T" indicating Tape and Reel.

   "BCD" equals to "042" for part assigned with MAC ID and blank for part with no MAC ID.

   The following table lists possible combinations for ordering the ATWINC1500B and ATWINC1510B.

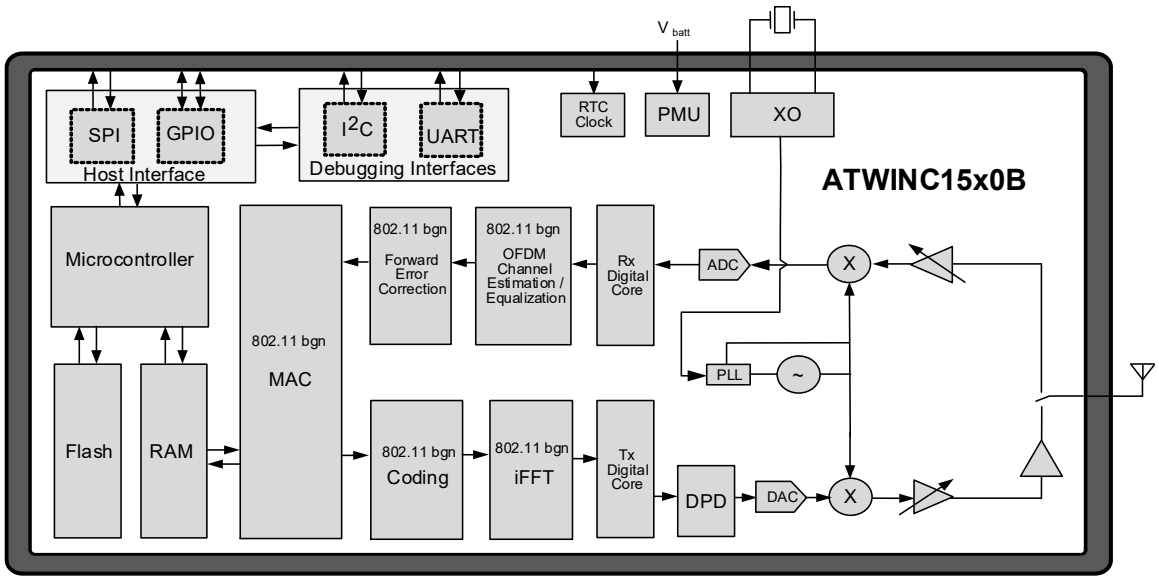
Ordering Code	Description
ATWINC1500B-MU-T	4 Mb Flash with no MAC ID and ship in Tape and Reel
ATWINC1500B-MU-Y	4 Mb Flash with no MAC ID and ship in Tray
ATWINC1500B-MU-Y042	4 Mb Flash with MAC ID assigned and ship in Tray
ATWINC1500B-MU-T042	4 Mb Flash with MAC ID assigned and ship in Tape and Reel
ATWINC1510B-MU-T	8 Mb Flash with no MAC ID and ship in Tape and Reel
ATWINC1510B-MU-Y	8 Mb Flash with no MAC ID and ship in Tray
ATWINC1510B-MU-Y042	8 Mb Flash with MAC ID assigned and ship in Tray
ATWINC1510B-MU-T042	8 Mb Flash with MAC ID assigned and ship in Tape and Reel

2. Functional Overview

2.1 Block Diagram

The ATWINC15x0B block diagram is shown in the following figure.

Figure 2-1. ATWINC15x0B Block Diagram

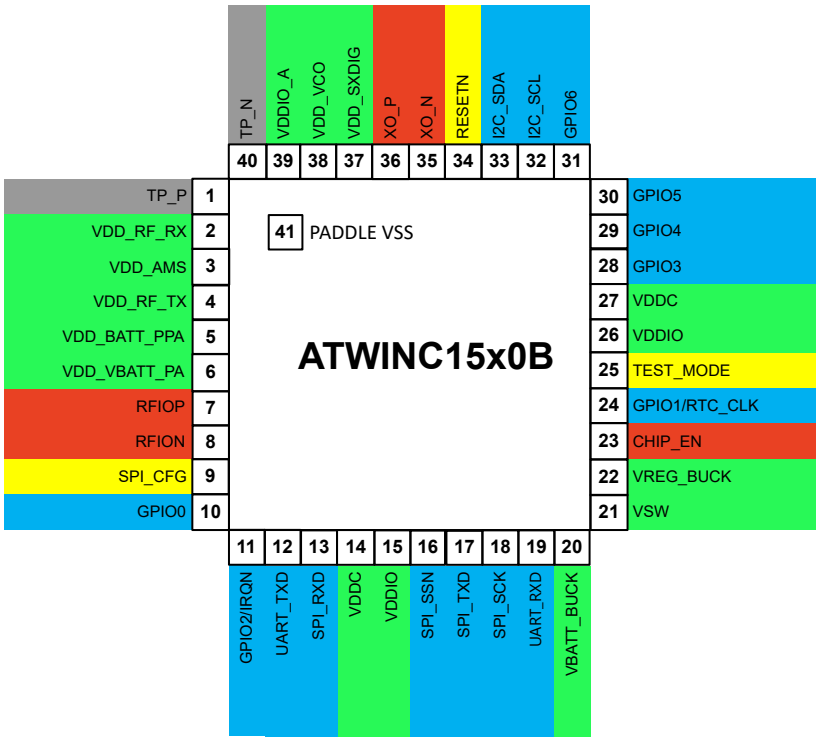


2.2 Pinout Information

The ATWINC15x0B is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in the following figure. The color shading is used to indicate the pin type as follows:

- Green – power
- Red – analog
- Blue – digital I/O
- Yellow – digital input
- Grey – unconnected or reserved

Figure 2-2. ATWINC15x0B Pin Assignment



2.3 Pinout Description

The ATWINC15x0B pins with default peripheral mapping are described in the following table.

Table 2-1. ATWINC15x0B Pin Description

Pin Number	Pin Name	Pin Type	Description
1	TP_P	Analog	Test pin/no connect
2	VDD_RF_RX	Power	Tuner RF supply (see Section 9.1)
3	VDD_AMS	Power	Tuner BB supply (see Section 9.1)
4	VDD_RF_TX	Power	Tuner RF supply (see Section 9.1)
5	VDD_BATT_PPA	Power	PA 1st stage supply (see Section 9.1)
6	VDD_VBATT_PA	Power	PA 2nd stage supply (see Section 9.1)
7	RFIOP	Analog	Positive RF differential I/O
8	RFION	Analog	Negative RF differential I/O
9	SPI_CFG	Digital Input	Tie to High
10	GPIO0	Digital I/O, Programmable Pull-Up	GPIO0

.....continued

Pin Number	Pin Name	Pin Type	Description
11	GPIO2/IRQN	Digital I/O, Programmable Pull-Up	GPIO2/Device interrupt
12	UART_TXD	Digital I/O, Programmable Pull-Up	UART data transmit
13	SPI_RXD	Digital I/O, Programmable Pull-Up	SPI data receive
14	VDDC	Power	Digital core power supply (see Section 9.1)
15	VDDIO	Power	Digital I/O power supply (see Section 9.1)
16	SPI_SSN	Digital I/O, Programmable Pull-Up	SPI slave select
17	SPI_TXD	Digital I/O, Programmable Pull-Up	SPI data TX
18	SPI_SCK	Digital I/O, Programmable Pull-Up	SPI clock
19	UART_RXD	Digital I/O, Programmable Pull-Up	UART data receive
20	VBATT_BUCK	Power	Battery supply for DC/DC converter (see Section 9.1)
21	VSW	Power	Switching output of DC/DC converter (see Section 9.1)
22	VREG_BUCK	Power	• Core power from DC/DC converter (see Section 9.1) • Decouple with 10 µF and 0.01 µF capacitor to GND
23	CHIP_EN	Analog	PMU enable
24	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-Up	GPIO1/32 kHz clock input
25	TEST_MODE	Digital Input	Test mode – User must tie this pin to GND
26	VDDIO	Power	Digital I/O power supply (see Section 9.1)
27	VDDC	Power	Digital core power supply (see Section 9.1)
28	GPIO3	Digital I/O, Programmable Pull-Up	GPIO3
29	GPIO4	Digital I/O, Programmable Pull-Up	GPIO4

.....continued

Pin Number	Pin Name	Pin Type	Description
30	GPIO5	Digital I/O, Programmable Pull-Up	GPIO5
31	GPIO6	Digital I/O, Programmable Pull-Up	GPIO6
32	I2C_SCL	Digital I/O, Programmable Pull-Up	I^2C slave clock (high-drive pad, see ATWINC15x0B Electrical Characteristics Table)
33	I2C_SDA	Digital I/O, Programmable Pull-Up	I^2C slave data (high-drive pad, see ATWINC15x0B Electrical Characteristics Table)
34	RESETN	Digital Input	Active-low hard Reset
35	XO_N	Analog	Crystal oscillator N
36	XO_P	Analog	Crystal oscillator P
37	VDD_SXDIG	Power	SX power supply (see Section 9.1)
38	VDD_VCO	Power	VCO power supply (see Section 9.1)
39	VDDIO_A	Power	Tuner VDDIO power supply (see Section 9.1)
40	TP_N	Analog	Test pin/no connect
41	PADDLE VSS	Power	Connect to system board ground

2.4 Package Description

The following table provides information on the physical details of the ATWINC15x0B devices.

Table 2-2. ATWINC15x0B QFN Package Information

Parameter	Value	Units	Tolerance
Package size	5x5	mm	±0.1mm
QFN pad count	40	mm	-
Total thickness	0.85	mm	+0.15/-0.05
QFN pad pitch	0.40	mm	-
Pad width	0.20	mm	-
Exposed pad size	3.85x3.85	mm	-

For drawing details, see 9.1 Package Outline Drawing.

3. Clocking

This section details the clocking sources of the ATWINC15x0B.

3.1 Crystal Oscillator

The following table provides the values of the ATWINC15x0B crystal oscillator parameters.

Table 3-1. ATWINC15x0B Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Unit
Crystal resonant frequency	-	26	-	MHz
Crystal equivalent series resistance	-	50	150	Ω
Stability – Initial offset(1)	-100	-	100	ppm

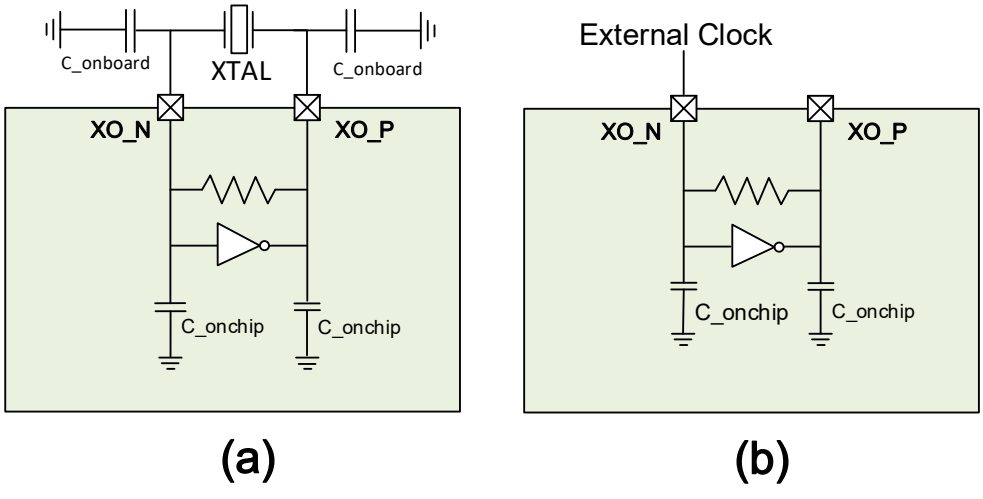
Note:

1. The initial offset must be calibrated to maintain ±25 ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in the following figure (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal as shown the following figure (b).

The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. This internal capacitance must be considered when calculating the external loading capacitance, c_onboard, for the XTAL.

Figure 3-1. ATWINC15x0B XO Connections



(a) Crystal Oscillator is Used

(b) Crystal Oscillator is Bypassed

The following table specifies the electrical and performance requirements for the external clock.

Table 3-2. ATWINC15x0B Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillator frequency	-	26	-	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.5	-	1.2	Vpp	Must be AC coupled
Stability – Temperature and aging	-25	-	+25	ppm	-
Phase noise	-	-	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	-	-	<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

3.2 Low-Power Oscillator

The ATWINC15x0B has an internal 32 kHz clock to provide timing information to various Sleep functions. Alternatively, the ATWINC15x0B allows an 32 kHz external clock for this purpose, which is provided through pin 24 (RTC_CLK). The software is used to select between internal clock and external clock.

The internal low-power clock is a ring-oscillator and has accuracy within 10,000 ppm. When using the internal low-power clock, the advance wake-up time in the beacon monitoring mode must be increased to 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wake-up time must be increased by 1 ms. For any application with low-power consumption, an external 32 kHz RTC clock must be used.

4. CPU and Memory Subsystem

This chapter describes about the Cortus APS3 32-bit processor and memory subsystem of the ATWINC15x0B.

4.1 Processor

The ATWINC15x0B has a Cortus APS3 32-bit processor. The processor performs MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as Station (STA) and Access Point (AP) modes.

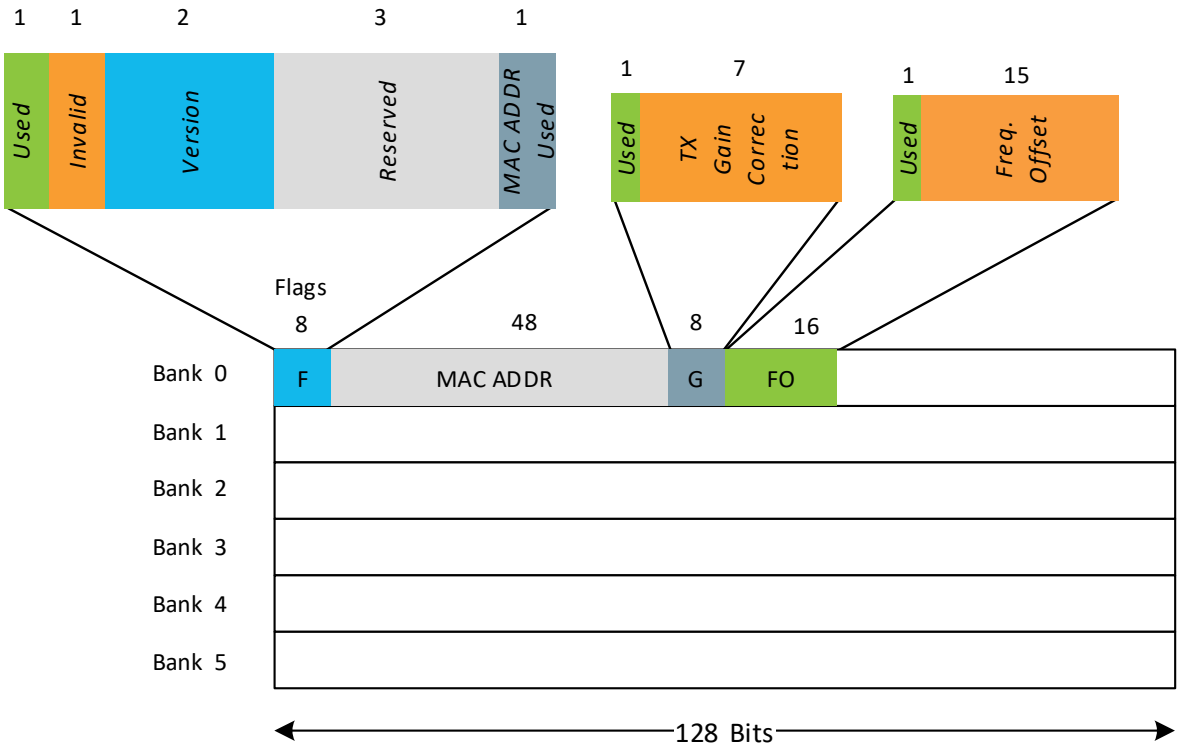
4.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. The ATWINC15x0B devices are populated with either 4 Mb or 8 Mb of Flash memory depending on the model that is ordered. This memory can be used for system software. For more information, see the Ordering Details table. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

4.3 Non-volatile Memory (eFuse)

The ATWINC15x0B IC have 768 bits of non-volatile eFuse memory that can be read by the CPU after device Reset. This non-volatile One-Time-Programmable (OTP) memory can be used to store customer-specific parameters such as MAC address, and various calibration information such as TX power, crystal frequency offset, and so on, and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bitmap (see the following figure). The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, ie., updating MAC address.

Figure 4-1. ATWINC15x0B eFuse Bitmap



5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

5.1 MAC

The ATWINC15x0B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES.

The control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, beacon TX control, interframe spacing, and so on.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

5.1.1 Features

The ATWINC15x0B IEEE802.11 MAC supports the Following Functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF Multiple Access Categories Traffic Scheduling
- Advanced IEEE 802.11n Features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA Security with Key Management
  - WEP 64/128

  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced Power Management
  - Standard 802.11 power save mode
  - Wi-Fi alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-Self Support
- Supports Either STA or AP Mode in the Infrastructure Basic Service Set Mode

5.2 PHY

The ATWINC15x0B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth. Advanced algorithms are employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment, and automatic gain control.

5.2.1 Features

The ATWINC15x0B IEEE802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- Supports IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5, 11 Mbps
- Supports IEEE 802.11g OFDM Modulation: 6, 9, 12,18, 24, 36, 48, 54 Mbps
- Supports IEEE 802.11n HT Modulations MCS0-7, 20 MHz, and 400 ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2 Mbps
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery, and Frame Detection

5.3 Radio

This section describes the properties and characteristics of ATWINC15x0B and Wi-Fi radio transmit, and receive performance capabilities of the IC.

The performance measurements are taken at the RF pin assuming 50 Ω differential; the RF performance is guaranteed for room temperature of 25ºC with a derating of 2 dB to 3 dB at boundary conditions.

Measurements are taken under typical conditions: VBATT=3.3 V; VDDIO=3.3 V; temperature: +25ºC

Table 5-1. Features and Properties

Feature	Description
Part number	ATWINC15x0B-MU
WLAN standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host interface	SPI
Frequency range	2.412GHz ~ 2.472GHz (2.4GHz ISM Band)

.....continued	
Feature	**Description**
Number of channels	11 for North America, and 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK
Data rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20 MHz, normal GI, 800 ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20 MHz, short GI, 400 ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Operating temperature	-40 to +85ºC
Storage temperature	-40 to +125 ºC
Humidity	Operating humidity 10% to 95% Non-condensing Storage humidity 5% to 95% Non-condensing

5.3.1 Receiver Performance

The following table shows the typical Receiver performance for the ATWINC15x0B.

Table 5-2. ATWINC15x0B Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,484	MHz
Sensitivity 802.11b (8% PER)	1 Mbps DSS	-	-95	-	dBm
	2 Mbps DSS	-	-90	-	
	5.5 Mbps DSS	-	-92	-	
	11 Mbps DSS	-	-86	-	
Sensitivity 802.11g (10% PER)	6 Mbps OFDM	-	-90	-	dBm
	9 Mbps OFDM	-	-89	-	
	12 Mbps OFDM	-	-88	-	
	18 Mbps OFDM	-	-85	-	
	24 Mbps OFDM	-	-83	-	
	36 Mbps OFDM	-	-80	-	
	48 Mbps OFDM	-	-76	-	
	54 Mbps OFDM	-	-74	-	

.....continued					
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
Sensitivity 802.11n (10% PER) (BW=20 MHz)	MCS 0	-	-89	-	dBm
	MCS 1	-	-87	-	
	MCS 2	-	-85	-	
	MCS 3	-	-82	-	
	MCS 4	-	-77	-	
	MCS 5	-	-74	-	
	MCS 6	-	-72	-	
	MCS 7	-	-70.5	-	
Maximum receive signal level	1-11 Mbps DSS	-	0	-	dBm
	6-54 Mbps OFDM	-	0	-	
	MCS 0 – 7	-	0	-	
Adjacent channel rejection	1 Mbps DSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	
Cellular blocker immunity	776-794 MHz CDMA	-	-14	-	dBm
	824-849 MHz GSM	-	-10	-	
	880-915 MHz GSM	-	-10	-	
	1710-1785 MHz GSM	-	-15	-	
	1850-1910 MHz GSM	-	-15	-	
	1850-1910 MHz WCDMA	-	-24	-	
	1920-1980 MHz WCDMA	-	-24	-	

5.3.2 Transmitter Performance

The following table explains the ATWINC15x0B Transmitter performance.

Table 5-3. ATWINC15x0BTransmitter Performance (1)

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412		2,484	MHz

.....continued

Parameter	Description	Min.	Typ.	Max.	Unit
Output power (1, 2, 3) ON_Transmit	802.11b 1 Mbps	-	17.5	-	dBm/MHz
	802.11b 11 Mbps	-	18.5	-	
	802.11g 6 Mbps	-	17.5	-	
	802.11g 54 Mbps	-	16.0	-	
	802.11n MCS 0	-	17.0	-	
	802.11n MCS 7	-	14.5	-	
TX power accuracy	-	-	±1.5 (3)	-	dB
Carrier suppression	-	-	30.0	-	dBc
Harmonic output power	2nd	-	-	-41	dBm/MHz
	3rd	-	-	-41	

Note:

1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network.
3. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

6. External Interfaces

The ATWINC15x0B external interfaces include:

- I²C slave for control
- SPI slave for control and data transfer
- One UART for debug
- General Purpose Input/Output (GPIO) pins

6.1 I²C Slave Interface

The I²C slave interface is a two-wire serial interface consisting of a serial data line (SDA, pin 33) and a serial clock (SCL, pin 32). The I²C interface is used for RF testing; the pins must not be connected to the host interface. It must be pinned out for easy control by an I²C controller. It responds to the seven bit address value 0x60. The ATWINC15x0B supports I²C bus Version 2.1 - 2000 and can operate in the Standard mode (with data rates up to 100 Kb/s) and Fast mode (with data rates up to 400 Kb/s).

The I²C slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I2C -Bus Specification, Version 2.1”.

The I²C slave timing information is provided in the following figure and table:

Figure 6-1. ATWINC15x0B I²C Slave Timing Diagram

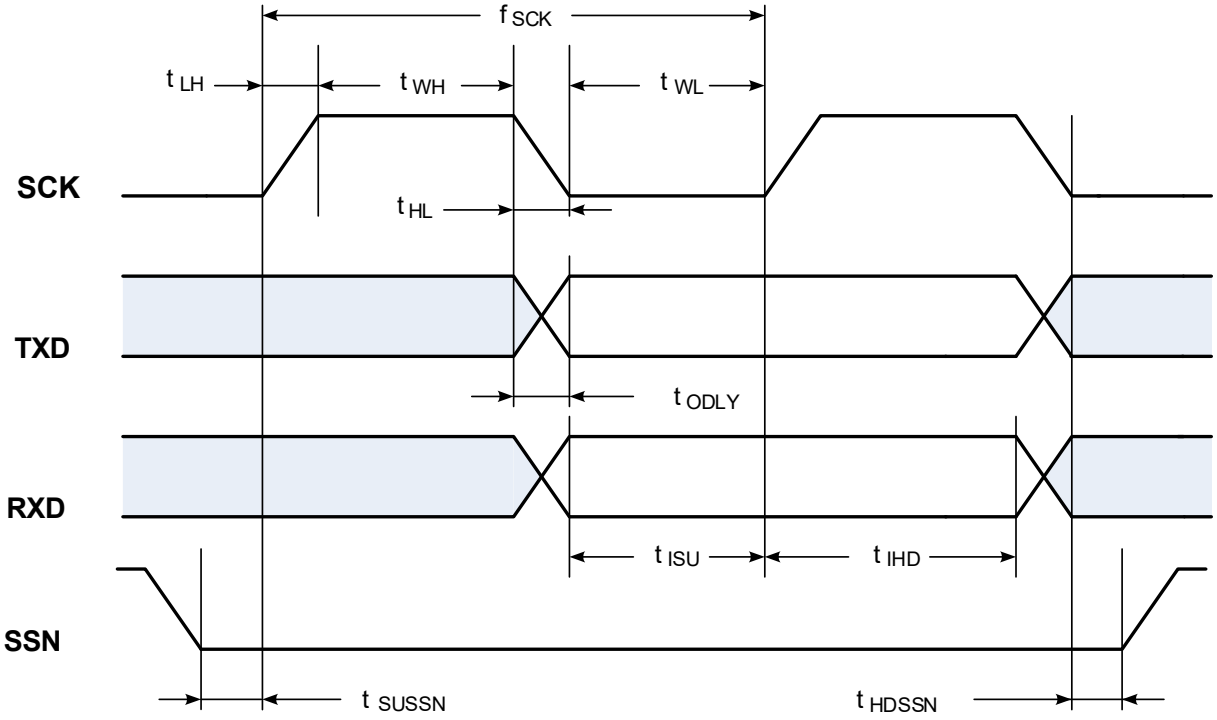


Table 6-1. ATWINC15x0B Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	-
SCL low pulse width	t_{WL}	1.3	-	µs	-
SCL high pulse width	t_{WH}	0.6	-		-
SCL, SDA fall time	t_{HL}	-	300	ns	-
SCL, SDA rise time	t_{LH}	-	300		This is dictated by external components
START setup time	t_{SUSTA}	0.6	-	µs	-
START hold time	t_{HDSTA}	0.6	-		-
SDA setup time	t_{SUDAT}	100		ns	
SDA hold time	t_{HDDAT}	0	-		Slave and Master Default
		40	-		Master Programming Option
STOP setup time	t_{SUSTO}	0.6	-	µs	-
Bus free time between STOP and START	t_{BUF}	1.3	-		-
Glitch pulse reject	t_{PR}	0	50	ns	-

6.2 SPI Slave Interface

The ATWINC15x0B provides a Serial Peripheral Interface (SPI) that operates as an SPI slave. This is the main interface to the host. The SPI slave interface can be used to control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in the following table. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available following Reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 6-2. ATWINC15x0B SPI Slave Interface Pin Mapping

Pin Number	Pin Name	SPI Function
9	SDIO_SPI_CFG	Must be tied to VDDIO
16	SSN	Active low slave select
18	SPI_SCK	Serial clock
13	SPI_RXD	Serial data receive (MOSI)
17	SPI_TXD	Serial data transmit (MISO)

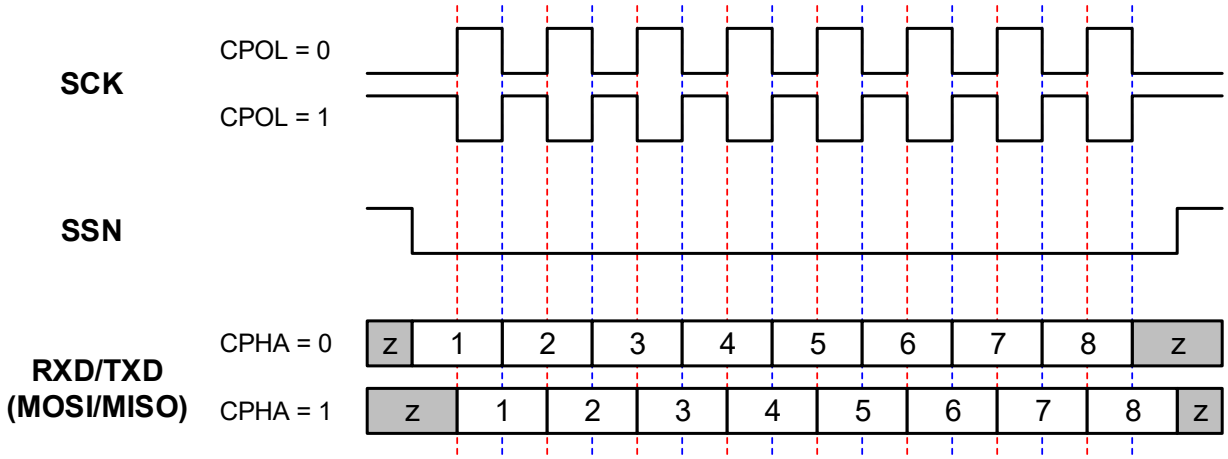
When the SPI is not selected, that is, when SSN is high, the SPI interface does not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiates DMA transfer.

The SPI slave interface supports four Standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 6-2. ATWINC15x0B SPI Slave Clock Polarity and Clock Phase Timing



The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 6-3. ATWINC15x0BSPI Slave Timing Diagram

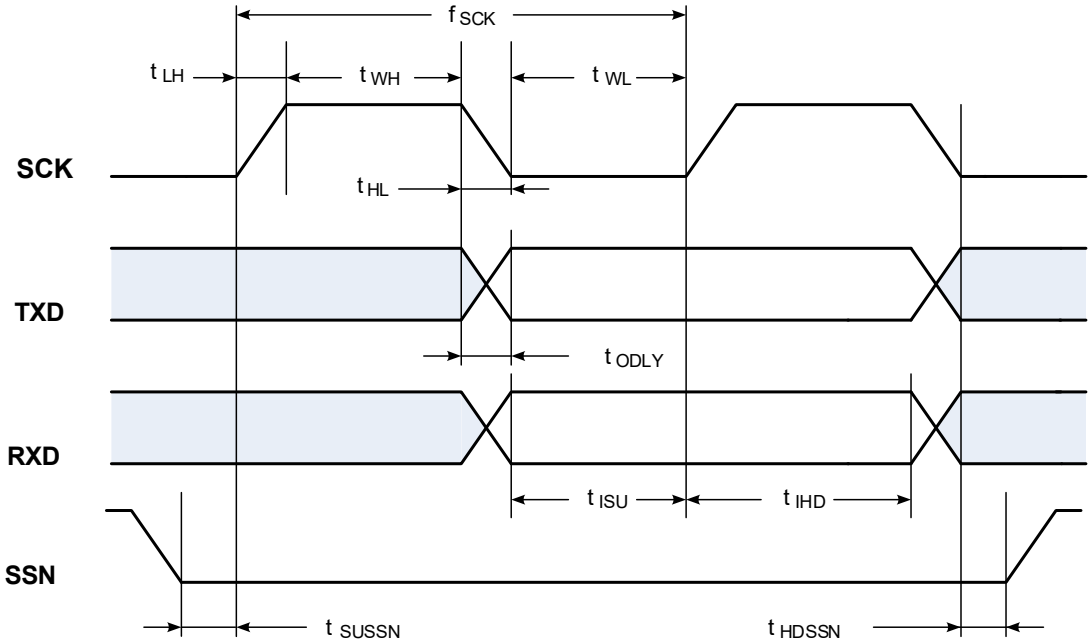


Table 6-3. ATWINC15x0B SPI Slave Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Units
Clock input frequency(2)	f_{SCK}		48	MHz
Clock low pulse width	t_{WL}	4		ns
Clock high pulse width	t_{WH}	5		
Clock rise time	t_{LH}	0	7	
Clock fall time	t_{HL}	0	7	
TXD output delay(3)	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD input setup time	t_{ISU}	1		
RXD input hold time	t_{IHD}	5		
SSN input setup time	t_{SUSSN}	3		
SSN input hold time	t_{HDSSN}	5.5		

Note:

1. Timing is applicable to all the SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design. Actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading.

6.3 UART Interface

The ATWINC15x0B supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface should be used for debug purposes only. The UART is available on pins 12 and 19. It is recommended to add test points for these pins. The UART is compatible with the RS-232 standard, and the ATWINC15x0-MR210xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

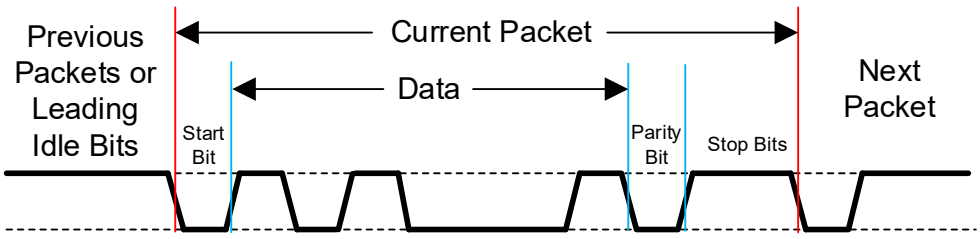
The following is the default configuration for accessing the UART interface of the ATWINC15x0-MR210xB:

- Baud rate: 460800
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 6-4. Example of UART RX or TX Packet



6.4 GPIO Pins

Seven General Purpose Input/Output (GPIO) pins, labeled GPIO 0 to 6, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input.

7. Power Management

7.1 Power Architecture

The ATWINC15x0B uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. The following table shows the typical values for the digital and RF/AMS core voltages. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

Figure 7-1. ATWINC15x0B Power Architecture

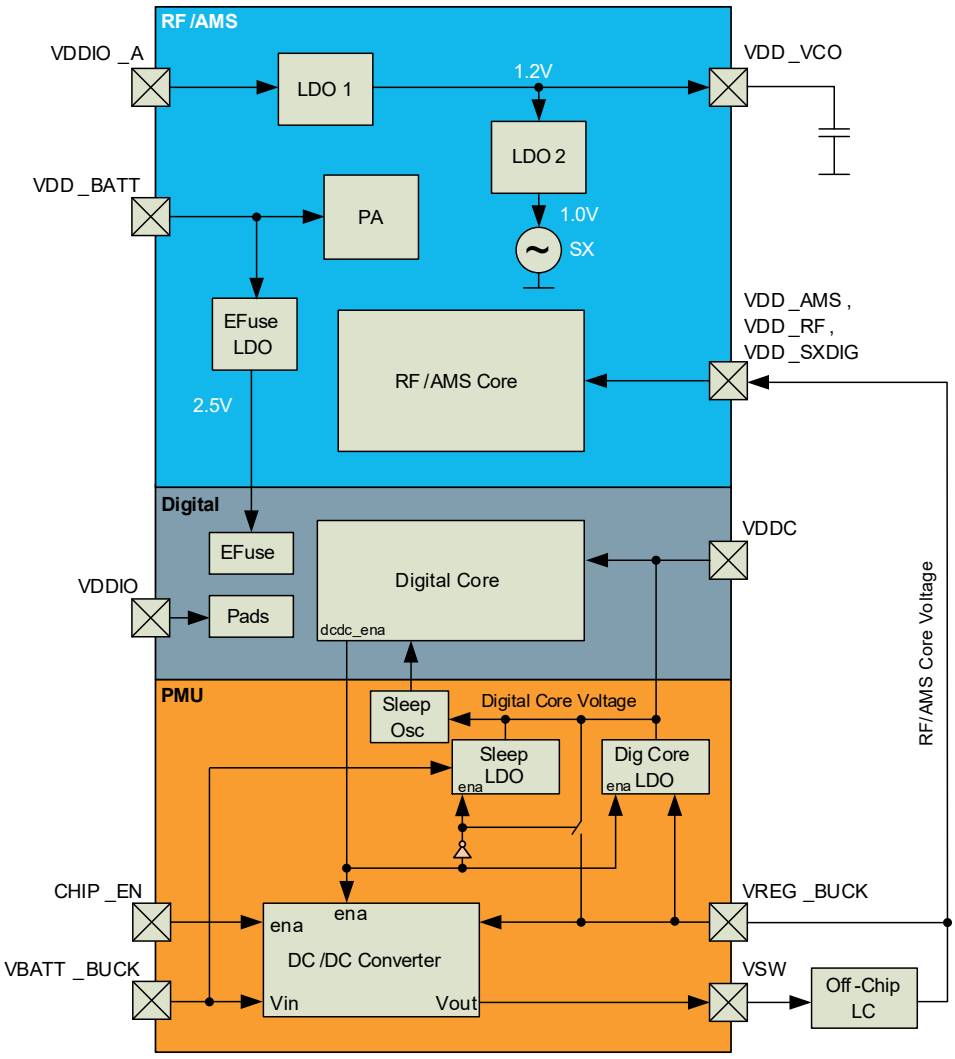


Table 7-1. ATWINC15x0B Power Consumption

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.25V
Digital Core Voltage (VDDC)	1.10V

The power connections in Figure 7-1 provide a conceptual framework for understanding the ATWINC15x0B power architecture. For more details on reference design, see section 11 for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

7.2 Power Consumption

7.2.1 Description of Device States

The ATWINC15x0B has several device states:

- ON_Transmit – device is actively transmitting an 802.11 signal with highest output power and nominal current consumption
- ON_Receive – device is actively receiving an 802.11 signal with lowest sensitivity and nominal current consumption
- ON_Doze – device is ON but is neither transmitting nor receiving
- Power_Down – device core supply off (leakage)
- IDLE connect – device is connected with one DTIM beacon interval

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – device pin (pin 23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is OFF and CHIP_EN is low, the chip is powered off with no leakage (see also: Section 8.2.3).

7.2.2 Current Consumption in Various Device States

The following table provides the current consumption of ATWINC15x0B in various device states.

Table 7-2. ATWINC15x0B Current Consumption

Device State	Code Rate	Output Power, dBm	Current Consumption (1)	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1 Mbps	17.5	268 mA	22 mA
	802.11b 11 Mbps	18.5	264 mA	22 mA
	802.11g 6 Mbps	17.5	269 mA	22 mA
	802.11g 54 Mbps	16.0	266 mA	22 mA
	802.11n MCS 0	17.0	268 mA	22 mA
	802.11n MCS 7	14.5	265 mA	22 mA

.....continued

Device State	Code Rate	Output Power, dBm	Current Consumption (1)	
			IVBATT	IVDDIO
ON_Receive	802.11b 1 Mbps	N/A	61 mA	22 mA
	802.11b 11 Mbps	N/A	61 mA	22 mA
	802.11g 6 Mbps	N/A	61 mA	22 mA
	802.11g 54 Mbps	N/A	61 mA	22 mA
	802.11n MCS 0	N/A	61 mA	22 mA
	802.11n MCS 7	N/A	61 mA	22 mA
ON_Doze	N/A	N/A	380 µA	<10 µA
Power_Down	N/A	N/A	<0.5 µA	<3.5 µA

Note:

1. Conditions: VBATT =3.3V, VDDIO=3.3V, and at 25°C

7.2.3 Restrictions for Power States

When no power is supplied to the device, that is, the DC/DC Converter output and VDDIO are OFF (at ground potential), a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode turns on when a voltage higher than one diode-drop is supplied to the pin.

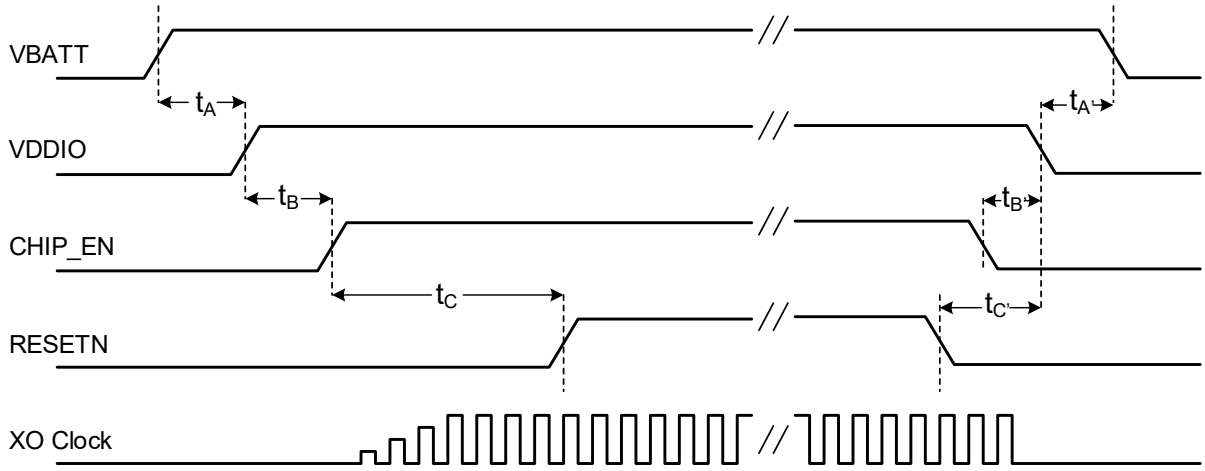
If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

7.3 Power Up/Power Down Sequence

The power up and power down sequence for ATWINC15x0B is shown in the following figure.

Figure 7-2. ATWINC15x0B Power Up/Down Sequence



The following table lists the parameters for the timing.

Table 7-3. ATWINC15x0B Power Up/Power Down Sequence

Symbol	Min.	Max.	Unit	Description	Condition
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5			CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0			CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0			RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

7.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents digital I/O pin states corresponding to the device power modes.

Table 7-4. ATWINC15x0B Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input driver	Pull-Up/Down Resistor (1)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

Note:

1. The pull-up/pull-down resistor value used is 96 kΩ ±10%.

7.5 Chip Reset

If a chip reset is performed on the ATWINC15x0B, the RESETN signal must be pulsed low for a minimum of 1 µs to reset the device successfully.

8. Electrical Specifications

8.1 Absolute Maximum Ratings

The values listed in this section are the ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Table 8-1. ATWINC15x0B Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Core supply voltage	V_{DDC}	-0.3	1.5	V
I/O supply voltage	V_{DDIO}	-0.3	4.2	
Battery supply voltage	V_{BATT}	-0.3	5.0	
Digital input voltage	V_{IN}	-0.3	VDDIO	
Analog input voltage	V_{AIN}	-0.3	1.5	
ESD Human Body Model	V_{ESDHBM}	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
Storage Temperature	TA	-40	125	ºC
Junction Temperature	-	-	125	
RF input power max	-	-	23	dBm

Note:

1. V_{IN} corresponds to all the digital pins
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins are all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

⚠ CAUTION Stresses listed in the above table may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

8.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for ATWINC15x0B.

Table 8-2. ATWINC15x0B Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit
I/O supply voltage	VDDIO	2.7	3.3	3.6	V
Battery supply voltage	VBATT	3.0	3.3	4.2	V
Operating temperature	-	-40	25	85	ºC

Note:

1. I/O supply voltage is applied to VDDIO_A, and VDDIO pins.
2. Battery supply voltage is applied to VDD_BATT_PPA, VDD_BATT_PA, and VBATT_BUCK pins.
3. For more details on power connections, see 7. Power Management and Table 8.3.

8.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWINC15x0B digital pads.

Table 8-3. ATWINC15x0B Electrical Characteristics

Characteristic	Min.	Typ.	Max.	Unit
Input low voltage (V_{IL})	-0.30	-	0.65	V
Input high voltage (V_{IH})	VDDIO-0.60	-	VDDIO+0.30	
Output low voltage (V_{OL})	-	-	0.45	
Output high voltage (V_{OH})	VDDIO-0.50	-	-	
Output loading	-	-	20	pF
Digital input load	-	-	6	
Pad drive strength (regular pads(1))	8	13.5	-	mA
Pad drive strength (high-drive pads(1))	16	27	-	

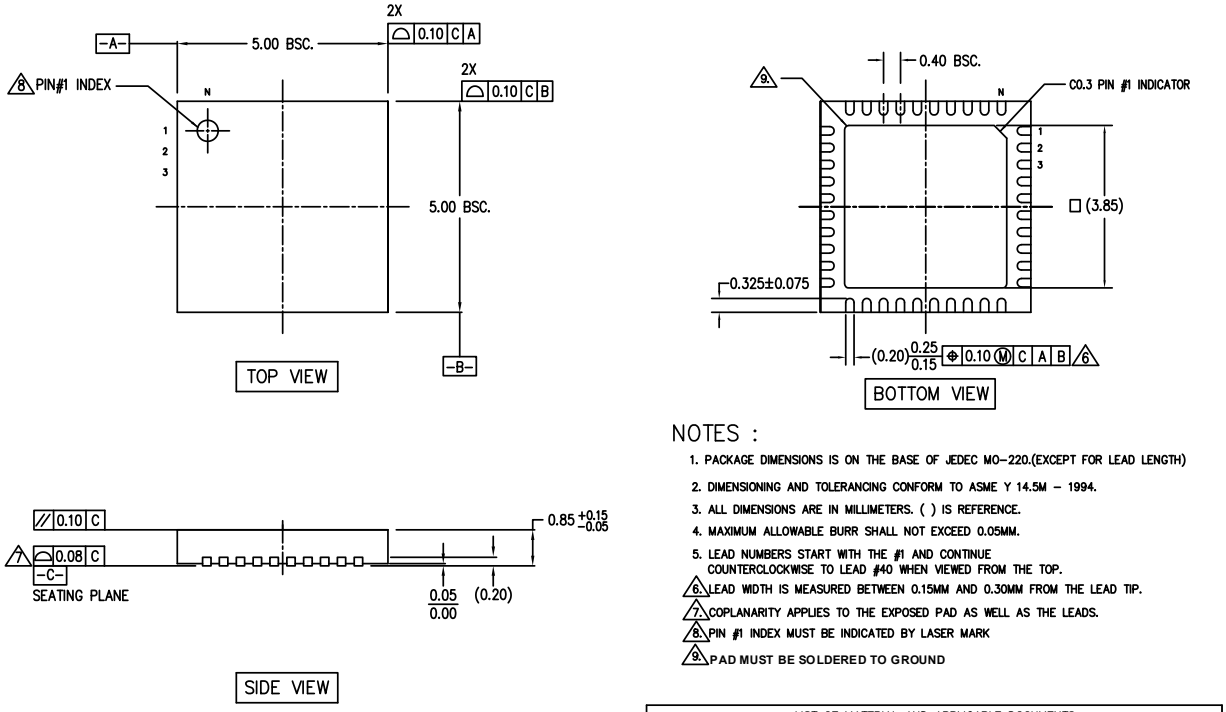
Note:

1. The I2C_SCL, and I2C_SDA are high-drive pads and all other pads are regular.

9. Appendix A: IC Outline and References

9.1 Package Outline Drawing

Figure 9-1. ATWINC15x0B QFN Package Outline Drawing



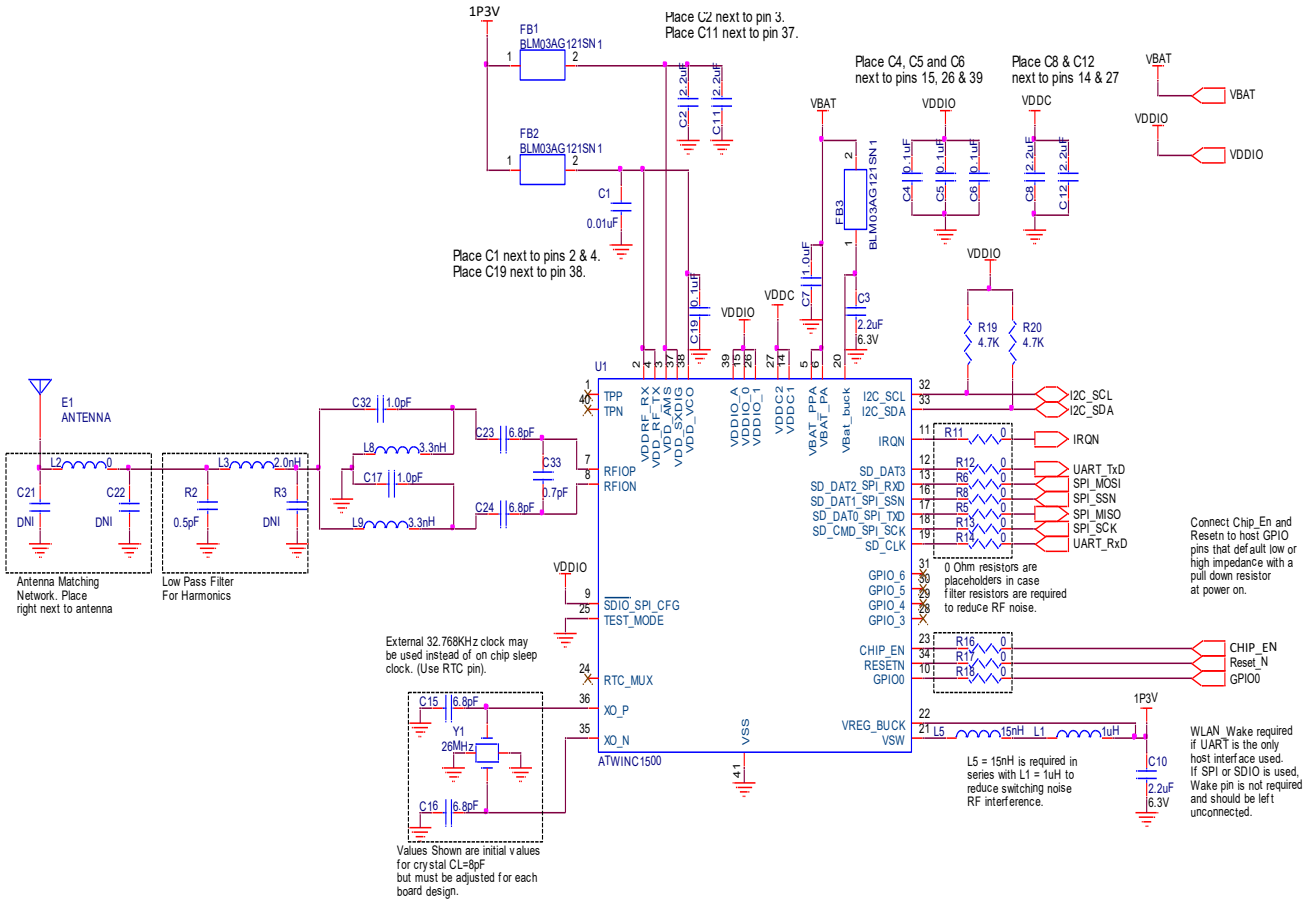
NOTES :

1. PACKAGE DIMENSIONS IS ON THE BASE OF JEDEC MO-220.(EXCEPT FOR LEAD LENGTH)
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y 14.5M – 1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ( ) IS REFERENCE.
4. MAXIMUM ALLOWABLE BURR SHALL NOT EXCEED 0.05MM.
5. LEAD NUMBERS START WITH THE #1 AND CONTINUE COUNTERCLOCKWISE TO LEAD #40 WHEN VIEWED FROM THE TOP.
6. LEAD WIDTH IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE LEAD TIP.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
8. PIN #1 INDEX MUST BE INDICATED BY LASER MARK
9. PAD MUST BE SOLDERED TO GROUND

LIST OF MATERIAL AND APPLICABLE DOCUMENTS			
SCALE: NONE	DATE: 02/26/13		TITLE: VQFN SAW 5 X 5 MM, 40 LEAD 3.85X3.85 EEP SIZE PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS		
PROJECTION UNLESS SPECIFIED	FRAC: .XX ±0.10 .XXX ±0.05 .XXXX ±0.03 ANGLE ±1°		

9.2 Reference Schematic Design

Figure 9-2. ATWINC15x0B Reference Schematic Design



Note:

1. Add Test points for I2C_SCL, and I2C_SDA pins.
2. Add Test points for UART TxD, and RxD pins.

9.3 Bill of Material

Figure 9-3. ATWINC15x0B Reference Bill of Material

ATWINC1500 Reference Design Revised: Friday, February 20, 2017 - Changed chip to Microchip.
ATWINC1500 Ref Revision: 3

Bill Of Materials February 12,2016 15:50:06

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	C1	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-125C	Murata	GRM033R61A103KA01D	0201
2	6	C2,C3,C8,C10,C11,C12	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K	0402
3	4	C4,C5,C6,C19	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	0201
4	1	C7	1.0uF	CAP,CER,1.0uF,10%,X5R,0402,6.3V,-55-85C	GRM155R60J105KE19D	GRM155R60J105KE19D	0402
5	4	C15,C16,C23,C24	6.8pF	CAP,CER,6.8pF,0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E6R8D030BA	0201
6	2	C17,C32	1.0pF	CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	0201
7	1	C21	DNI	CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	0201
8	2	R3,C22	DNI	CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125C	Murata	500RGRM0335C1ER50BA0	0201
9	1	C33	0.7pF	CAP,CER,0.7pF,0.1pF,NPO,0201,25V,-55-125C	Murata	500RGRM0335C1ER70BA01D07S0R5AV4T	0201
10	1	E1	ANTENNA	Antenna, 50 ohms, ISM Band, 2.4 - 2.5GHz			
11	3	FB1,FB2,FB3	BLM03AG121SN1	FERRITE,120 OHM @100MHz,200mA,0201,-55-125C	Murata	BLM03AG121SN1	0201
12	1	L1	1uH	POWER INDUCTOR,1uH,20%,940mA,0.125ohms,0603,shielded,-40-85c	Murata	LQM18PN1R0MFRL	0603
13	1	L2	0	Inductor,2.0nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S2N0C-T	0201
14	1	L3	2.0nH	Inductor,2.0nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S2N0C-T	0201
15	1	L5	15nH	INDUCTOR,Multilayer,15nH,5%,350mA,Q=8@100MHz,0402	Murata	LQG15HS15NJ02D	0402
16	2	L8,L9	3.3nH	Inductor,3.3nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N3C-T	0201
17	1	R2	0.5pF	CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125C	Murata	500RGRM0335C1ER50BA0	0201
18	10	R5,R6,R8,R11,R12,R13,	0	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
		R14,R16,R17,R18					
19	2	R19,R20	4.7K	RESISTOR,Thick Film,4.7K,5%,0201	Panasonic	ERJ-1GEJ472C	0201
20	1	U1	ATWINC1500	IC, WiFi, 40QFN	Microchip	ATWINC1500	40QFN
21	1	Y1	26MHz	CRYSTAL,26MHz,CL=7.36pF,10ppm,-20-85C,ESR=50,3.2x2.5mm	NDK	NX3225SA-26.000000MHZ-G3	3.2x2.5mm

10. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 10-1. Reference Documents

Title	Content
Platform Getting Started Guide	Details how to evaluate the WINC15X0 Network Controller Module.
Flash Memory Download Procedure	Details the download procedures of firmware, root certificate, gain table values and, so on.
ATWINC1500 Wi-Fi Network Controller Software Design Guide	Integration guide with a clear description of high-level arch, an overview on how to write a networking application, list all API, parameters, and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
Software Programming Guide (ATWINC15x0)	Details the flow chart and how to use each API to implement all generic use cases (for example, start AP, start STA, provisioning, UDP, TCP, HTTP, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.
PCB Mounting Guidelines for Surface Mount Packages Application Note	Guidelines for solder reflow process for successful board mounting of a device.
Solder Reflow Recommendation Application Note	For more information on Reflow process guidelines, refer to *Solder Reflow Recommendation Application Note* (DS00233D).

Note: A Design Files Package is available under NDA. For more details, contact your Microchip sales representative.

For a complete listing of development-support tools and documentation, visit https://www.microchip.com/wwwproducts/en/ATWINC1500, or refer to the customer support section on options to the nearest Microchip field representative.

11. Document Revision History

Note: The datasheet revision is independent of the die revision (Revision bit in the Device Identification register of the Device Service Unit, DSU.DID.REVISION) and the device variant (last letter of the ordering number).

Rev. A - 10/2018

Section	Changes
Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42487 revision B. • Changed document style. • Changed the name to incorporate all the ATWINC15x0B devices. • Removed references to WAPI security.
Ordering Details	• Updated ordering code details.
Pinout Information	• Revised Pin Assignment figure for clarity.
Package Description	• Corrected tolerance in Package Description table. • Revised QFN Package Outline drawing to be clearer.
Power Management	• Added footnote to Digital I/O pin Behavior in Different Device States table. • Updated RF/RMS Core Voltage in PMU Output Voltages table.
External Interfaces	• Added SPI Pin names to SPI Interface Pin Mapping table. • Added section for Chip Reset. • Revised timing parameters in SPI Slave Timing Parameter table.
Clocking	• Revised RTC drawing in XO connections figure.
Radio	• Revised b Mode number in Receiver Performance table. • Revised data and footnotes in Transmit Performance table.
Reflow Profile Information	• Removed Reflow Profile Information chapter from the datasheet.

Atmel Document Revision History
Rev. B - 03/2016

Section	Changes
Package Description	• Updated device drawing to include note to solder the paddle pad to GND in POD Figure 3-2.
Radio Transmit Performance	• Revised table in transmit performance Table 7-2.
Power Management	• Revised Chapter 9 text and current consumption table information in Table 9-2. • Removed preliminary numbers note from performance numbers Table 9-2.
Reference Design	• Updated schematic figure in Figure 10-1.
Reflow Profile Information	• Added Chapter11 Reflow Profile Information.

Rev.A- 07/2015

Section	Changes
Document	• DS update to RevB offering • Changes from WINC1500A (42353D) to WINC1500B: • Miscellaneous minor updates and corrections
Features List	• Added hardware accelerators in feature list (SSL security, IP checksum, OTA security) • Corrected Power Down and Doze mode current in Table 9-2 and in feature list
Pinout and Package Information	• Changed RTC_CLK pad definition from pull-down to pull-up
Electrical Specifications	• Corrected Table 4-3 and added high-drive pads reference in Table 3-1
WLAN Subsystem	• Increased instruction RAM size from 128KB to 160KB • Updated radio performance in Table 7-1 and Table 7-2

.....continued

Section	Changes
External Interfaces	• Fixed typos for SPI Slave interface timing in Table 8-6 • Added second UART, increased UART data rates • Updated pin mux table: added new options for various interfaces • Improved description of Coexistence interface • Changed pin list to add GPIOs 3,4,5,6 - chip pinout identical WINC and WILC • Fixed typos for SPI Slave interface timing in Table 8-6 • Fixed typos for battery supply name: changed from VBAT to VBATT • Corrected Table 8-7
Power Management	• Added VDD_VCO switch and connection in the power architecture • Updated power consumption numbers • Modified sections 9.2.1 and 9.2.2 to add high-power and low-power modes and current consumption numbers • Corrected Power Down and Doze mode current in Table 9-2 and in feature list
Reference Schematic Design	• Updated reference schematic

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