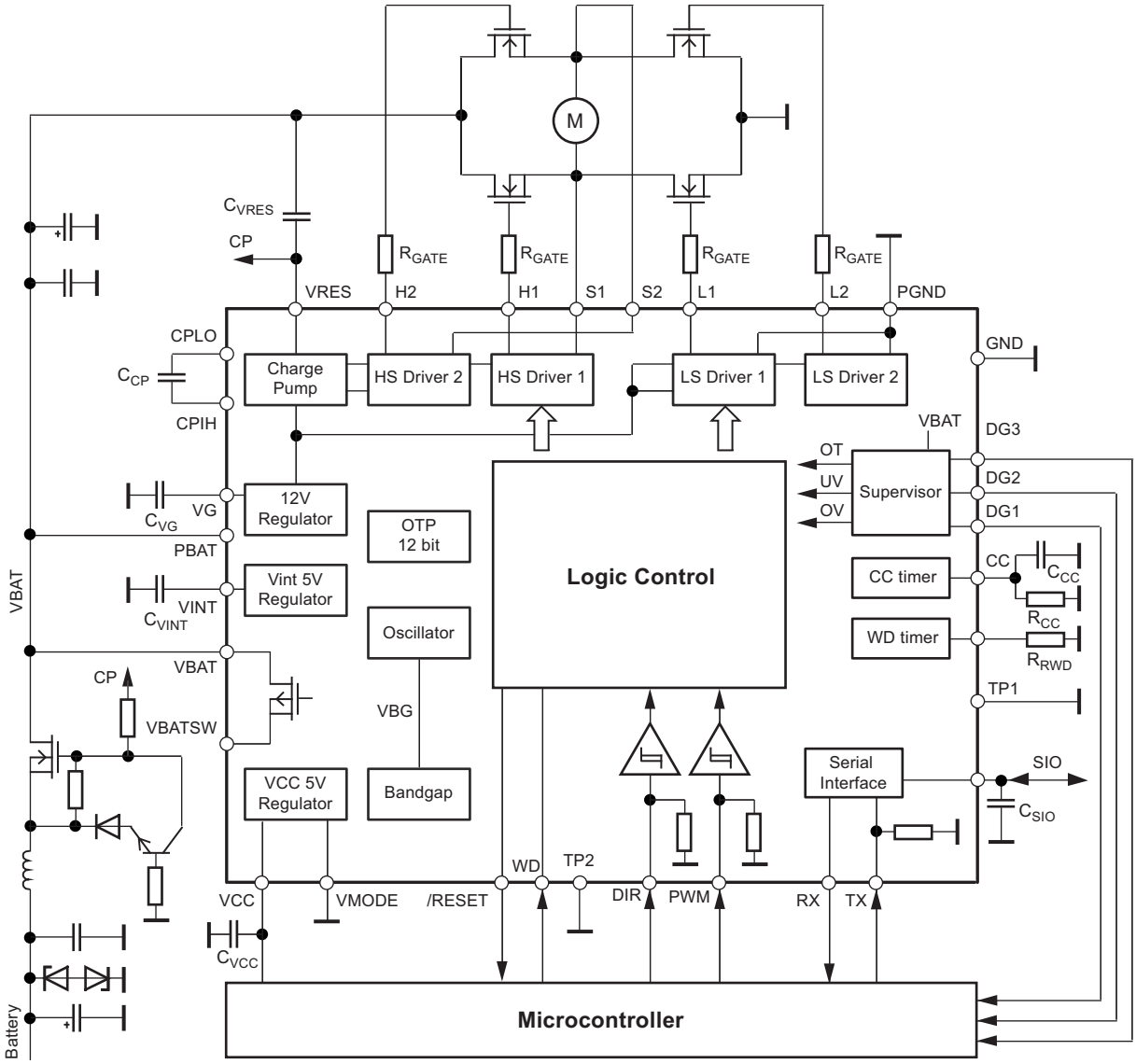
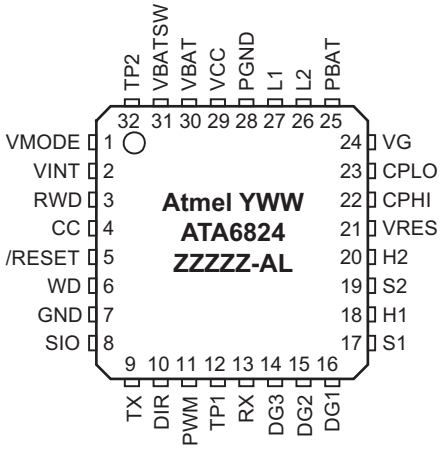
Figure 1. Block Diagram



1. Pin Configuration

Figure 1-1. Pinning TPQFP32



Note:

	YWW	Date code (Y = Year - above 2000, WW = week number)
	ATA6824C	Product name
	ZZZZZ	Wafer lot number
	AL	Assembly sub-lot number

Table 1-1. Pin Description

Pin	Symbol	I/O	Function
1	VMODE	I	Selector for V_{CC} and interface logic voltage level
2	VINT	I/O	Blocking capacitor 220nF/10V/X7R
3	RWD	I	Resistor defining the watchdog interval
4	CC	I/O	RC combination to adjust cross conduction time
5	/RESET	O	Reset signal for microcontroller
6	WD	I	Watchdog trigger signal
7	GND	I	Ground for chip core
8	SIO	I/O	High Voltage (HV) serial interface
9	TX	I	Transmit signal to serial interface from microcontroller
10	DIR	I	Defines the rotation direction for the motor
11	PWM	I	PWM input controls motor speed
12	TP1	–	Test pin to be connected to GND
13	RX	O	Receive signal from serial interface for microcontroller
14	DG3	O	Diagnostic output 3
15	DG2	O	Diagnostic output 2
16	DG1	O	Diagnostic output 1
17	S1	I/O	Source voltage H-bridge, high-side 1
18	H1	O	Gate voltage H-bridge, high-side 1
19	S2	I/O	Source voltage H-bridge, high-side 2
20	H2	O	Gate voltage H-bridge, high-side 2
21	VRES	I/O	Gate voltage for reverse protection NMOS, blocking capacitor 470nF/25V/X7R
22	CPHI	I	Charge pump capacitor 220nF/25V/X7R
23	CPLO	O	

Table 1-1. Pin Description (Continued)

Pin	Symbol	I/O	Function
24	VG	I/O	Blocking capacitor 470nF/25V/X7R
25	PBAT	I	Power supply (after reverse protection) for charge pump and H-bridge
26	L2	O	Gate voltage H-bridge, low-side 2
27	L1	O	Gate voltage H-bridge, low-side 1
28	PGND	I	Power ground for H-bridge and charge pump
29	VCC	O	5V/100 mA supply for microcontroller, blocking capacitor 2.2µF/10V/X7R
30	VBAT	I	Supply voltage for IC core (after reverse protection)
31	VBATSW	O	100Ω PMOS switch from V_{VBAT}
32	TP2	–	Test pin to be connected to GND

2. General Statement and Conventions

- Parameter values given without tolerances are indicative only and not to be tested in production
- Parameters given with tolerances but without a parameter number in the first column of parameter table are “guaranteed by design” (mainly covered by measurement of other specified parameters). These parameters are not to be tested in production. The tolerances are given if the knowledge of the parameter tolerances is important for the application
- The lowest power supply voltage is named GND
- All voltage specifications are referred to GND if not otherwise stated
- Sinking current means that the current is flowing into the pin (value is positive)
- Sourcing current means that the current is flowing out of the pin (value is negative)

2.1 Related Documents

- Qualification of integrated circuits according to Atmel® HNO procedure based on AEC-Q100
- AEC-Q100-004 and JESD78 (Latch-up)
- ESD STM 5.1-1998
- CEI 801-2 (only for information regarding ESD requirements of the PCB)

3. Application

3.1 General Remark

This chapter describes the principal application for which the Atmel® ATA6824C was designed. Because Atmel cannot be considered to understand fully all aspects of the system, application and environment, no warranties of fitness for a particular purpose are given.

Table 3-1. Typical External Components (See also Figure 1 on page 2)

Component	Function	Value	Tolerance
C_{VINT}	Blocking capacitor at VINT	220nF, 10V, X7R	50%
C_{VCC}	Blocking capacitor at VCC	2.2µF, 10V, X7R	50%
C_{CC}	Cross conduction time definition capacitor	Typical 680pF, 100V, COG	
R_{CC}	Cross conduction time definition resistor	Typical 10kΩ	
C_{VG}	Blocking capacitor at VG	Typical 470nF, 25V, X7R	50%
C_{CP}	Charge pump capacitor	Typical 220nF, 25V, X7R	
C_{VRES}	Reservoir capacitor	Typical 470nF, 25V, X7R	
R_{RWD}	Watchdog time definition resistor	Typical 51kΩ	
C_{SIO}	Filter capacitor for SIO	Typical 220pF, 100V	

4. Functional Description

4.1 Power Supply Unit with Supervisor Functions

4.1.1 Power Supply

The IC is supplied by a reverse-protected battery voltage. To prevent it from destruction, proper external protection circuitry has to be added. It is recommended to use at least a capacitor combination of storage and HF caps behind the reverse protection circuitry and closed to the VBAT pin of the IC (see Figure 1 on page 2).

An internal low-power and low drop regulator (V_{INT}), stabilized by an external blocking capacitor, provides the necessary low-voltage supply for all internal blocks except the digital IO pins. This voltage is also needed in the wake-up process. The low-power band gap reference is trimmed and is used for the bigger VCC regulator, too. All internal blocks are supplied by the internal regulator.

The internal supply voltage V_{INT} must not be used for any other supply purpose!

Nothing inside the IC except the logic interface to the microcontroller is supplied by the 5V/3.3V VCC regulator.

A power-good comparator checks the output voltage of the V_{INT} regulator and keeps the whole chip in reset as long as the voltage is too low.

There is a high-voltage switch which brings out the battery voltage to the pin VBATSW for measurement purposes. This switch is switched ON for VCC = HIGH and stays ON in case of a watchdog reset. The signal can be used to switch on external voltage regulators, etc.

4.1.2 Voltage Supervisor

This block is intended to protect the IC and the external power MOS transistors against overvoltage on battery level and to manage undervoltage on it.

Function: in case of both overvoltage alarm (V_{THOV}) and of undervoltage alarm (V_{THUV}) the external NMOS motor bridge transistors will be switched off. The failure state will be flagged via DG2. No other actions will be carried out. The undervoltage comparator is connected to the pin VBAT while the overvoltage comparator is connected to pin PBAT. Both are filtered by a first-order low pass with a corner frequency of typical 15kHz.

4.1.3 Temperature Supervisor

There is a temperature sensor integrated on-chip to prevent the IC from overheating due to a failure in the external circuitry and to protect the external NMOSFET transistors.

In case of detected overtemperature (180°C), the diagnostic pin DG3 will be switched to “H” to signalize overtemperature warning to the microcontroller. It should undertake actions to reduce the power dissipation in the IC. In case of detected overtemperature (200°C), the V_{CC} regulator and all drivers including the serial interface will be switched OFF immediately and /RESET will go LOW.

Both temperature thresholds are correlated. The absolute tolerance is ±15K and there is a built-in hysteresis of about 10K to avoid fast oscillations. After cooling down below the 170°C threshold; the IC will go into Active mode.

The occurrence of overtemperature shutdown is latched in DG3. DG3 stays on high until first WD trigger.

4.2 5V/3.3V VCC Regulator

The 5V/3.3V regulator is fully integrated on-chip. It requires only a 2.2µF ceramic capacitor for stability and has 100 mA current capability. Using the VMODE pin, the output voltage can be selected to either 5V or 3.3V. Switching of the output voltage during operation is not intended to be supported. The VMODE pin must be hard-wired to either VINT for 5V or to GND for 3.3V. The logic HIGH level of the microcontroller interface will be adapted to the VCC regulator voltage.

The output voltage accuracy is in general < ±3%; in the 5V mode with V_{VBAT} < 9V it is limited to < 5%.

To prevent destruction of the IC, the current delivered by the regulator is limited to maximum 100mA to 350mA. The delivered voltage will break down and a reset may occur.

Please note that this regulator is the main heat source on the chip. The maximum output current at maximum battery voltage and high ambient temperature can only guaranteed if the IC is mounted on an efficient heat sink.

A power-good comparator checks the output voltage of the VCC regulator and keeps the external microcontroller in reset as long as the voltage is too low.

Figure 4-1. Voltage Dependence and Timing of VCC Controlled RESET

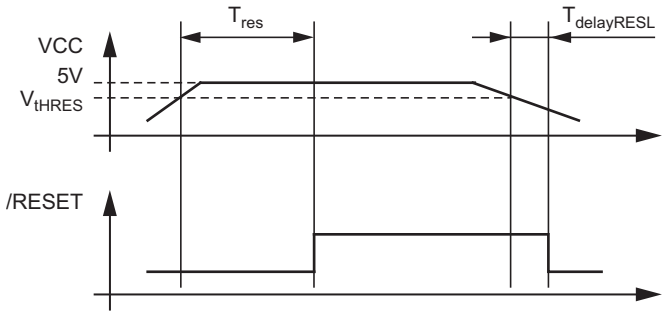
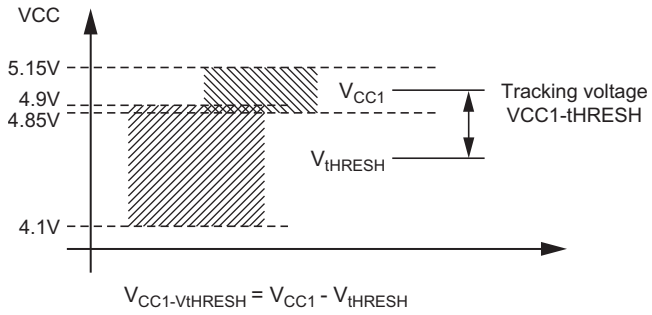


Figure 4-2. Correlation between VCC Output Voltage and Reset Threshold



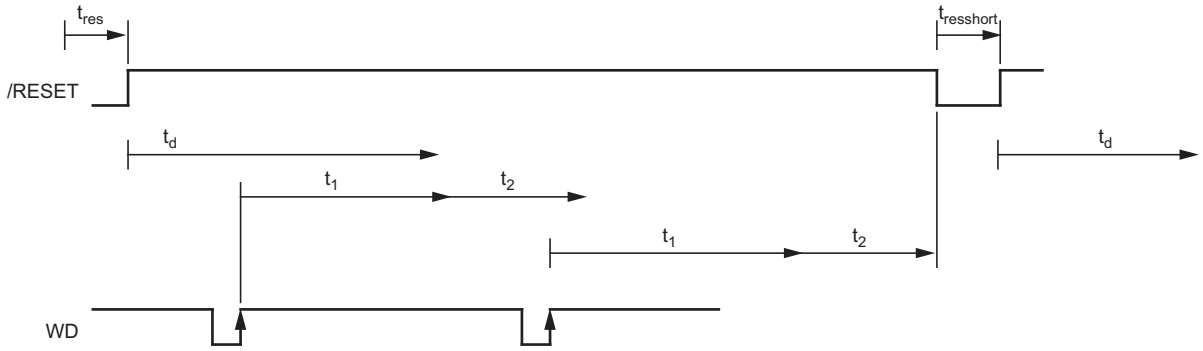
The voltage difference between the regulator output voltage and the upper reset threshold voltage is bigger than 75mV (VMODE = HIGH) and bigger than 50mV (VMODE = LOW).

4.3 Reset and Watchdog Management

The timing basis of the watchdog is provided by the trimmed internal oscillator. Its period T_{OSC} is adjustable via the external resistor R_{WD}.

The watchdog expects a triggering signal (a rising edge) from the microcontroller at the WD input within a period time window of T_{WD}.

Figure 4-3. Timing Diagram of the Watchdog Function



4.3.1 Timing Sequence

For example, with an external resistor R_{WD} = 33 kΩ ±1% we get the following typical parameters of the watchdog.

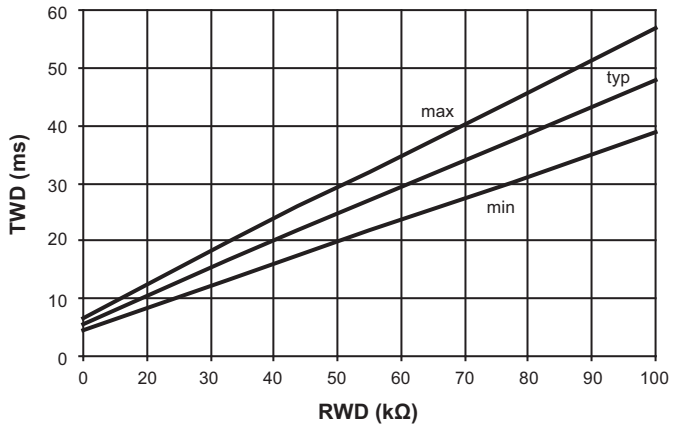
T_{OSC} = 12.32µs, t_1 = 12.1ms, t_2 = 9.61ms, T_{WD} = 16.88ms ±10%

The times t_{res} = 70ms and t_d = 70ms are fixed values with a tolerance of 10%.

After ramp-up of the battery voltage (power-on reset), the V_{CC} regulator is switched on. The reset output, /RESET, stays low for the time t_{res}, then switches to high. For an initial lead time t_d (for setups in the controller) the watchdog waits for a rising edge on WD to start its normal window watchdog sequence. If no rising edge is detected, the watchdog will reset the microcontroller for t_{res} and wait t_d for the rising edge on WD.

Times t_1 (close window) and t_2 (open window) form the window watchdog sequence. To avoid receiving a reset from the watchdog, the triggering signal from the microcontroller must hit the timeframe of t_2 = 9.61ms. The trigger event will restart the watchdog sequence.

Figure 4-4. T_{WD} versus R_{WD}



If triggering fails, /RESET will be pulled to ground for a shortened reset time of typically 2ms. The watchdog start sequence is similar to the power-on reset.

The internal oscillator is trimmed to a tolerance of < ±10%. This means that t_1 and t_2 can also vary by ±10%. The following calculation shows the worst case calculation of the watchdog period T_{wd} which the microcontroller has to provide.

$t_{1min} = 0.90 \times t_1$ = 10.87ms, $t_{1max} = 1.10 \times t_1$ = 13.28ms

$t_{2min} = 0.90 \times t_2$ = 8.65ms, $t_{2max} = 1.10 \times t_2$ = 10.57ms

$T_{wdmax} = t_{1min} + t_{2min}$ = 10.87ms + 8.65ms = 19.52ms

$T_{wdmin} = t_{1max}$ = 13.28ms

T_{wd} = 16.42ms ±3.15ms (±19.1%)

Figure 4-4 on page 8 shows the typical watchdog period T_{WD} depending on the value of the external resistor R_{OSC}.

A reset will be active for $V_{CC} < V_{tHRESx}$; the level V_{tHRESx} is realized with a hysteresis (HYS_{RESth}).

4.4 High Voltage Serial Interface

A bi-directional bus interface is implemented for data transfer between hostcontroller and the local microcontroller (SIO).

The transceiver consists of a low side driver (1.2V at 40mA) with slew rate control, wave shaping, current limitation, and a high-voltage comparator followed by a debouncing unit in the receiver.

4.4.1 Transmit Mode

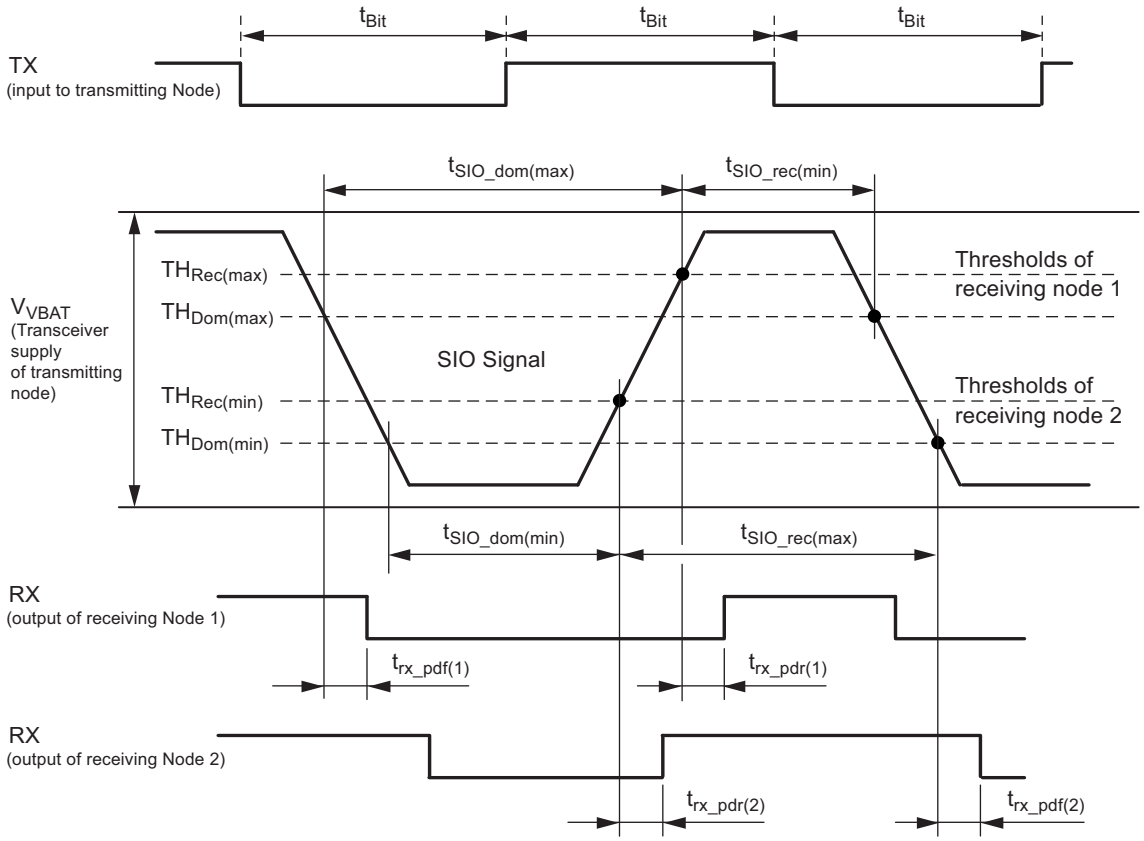
During transmission, the data at the pin TX will be transferred to the bus driver to generate a bus signal on pin SIO. The pin TX has a pull-down resistor included.

To minimize the electromagnetic emission of the bus line, the bus driver has an integrated slew rate control and wave-shaping unit. In transmit mode, transmission will be interrupted in case of overheating at the SIO driver.

4.4.2 Reset Mode

In case of an active reset shown at pin /RESET the pin SIO is switched to low, independent of the temperature. The maximum current is limited to $I_{SIO\_LIM\_RESET}$.

Figure 4-5. Definition of Bus Timing Parameters



The recessive BUS level is generated from the integrated 30 kΩ pull-up resistor in series with an active diode. This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS ($V_{BUS} > V_{SUP}$).

4.5 Control Inputs DIR and PWM

4.5.1 Pin DIR

Logical input to control the direction of the external motor to be controlled by the IC. An internal pull-down resistor is included.

4.5.2 Pin PWM

Logical input for PWM information delivered by external microcontroller. Duty cycle and frequency at this pin are passed through to the H-bridge. An internal pull-down resistor is included.

Table 4-1. Status of the IC Depending on Control Inputs and Detected Failures

Control Inputs			Driver Stage for External Power MOS				Comments
ON	DIR	PWM	H1	L1	H2	L2	
0	X	X	OFF	OFF	OFF	OFF	DG1, DG2 fault or RESET
1	0	PWM	ON	OFF	/PWM	PWM	Motor PWM forward
1	1	PWM	/PWM	PWM	ON	OFF	Motor PWM reverse

The internal signal ON is high when

- At least one valid WD trigger has been accepted
- No short circuit detected
- V_{PBAT} is inside the specified range ($V_{PBAT\_OV} \leq V_{PBAT} \leq V_{THOV}$)
- V_{VBAT} is higher than V_{THUV}
- The device temperature is not above shutdown threshold

In case of a short circuit, the appropriate transistor is switched off after a blanking time of t_{SC} . In order to avoid cross current through the bridge, a cross conduction timer is implemented. Its time constant is programmable by means of an RC combination.

Table 4-2. Status of the Diagnostic Outputs

Device Status						Diagnostic Outputs			Comments
PBAT_UV	SC	VBAT_UV	PBAT_OV	CPOK	OT	DG1	DG2	DG3	
X	X	X	X	X	1	–	–	1	Overtemperature warning
X	X	X	X	0	X	0	1	–	Charge pump failure
X	X	X	1	X	X	0	1	–	Overvoltage PBAT
X	X	1	X	X	X	0	1	–	Undervoltage VBAT
X	1	0	0	1	X	1	0	–	Short circuit
1	0	0	0	1	X	1	1	–	Undervoltage PBAT

Note: X represents: don't care – no effect)
– Status of the diagnostic outputs depends on device status
PBAT_UV: Undervoltage PBAT pin
SC: Short circuit drain source monitoring
VBAT_UV: Undervoltage of VBAT pin
PBAT_OV: Overvoltage of PBAT pin
CPOK: Charge pump OK
OT: Overtemperature warning

4.6 VG Regulator

The VG regulator is used to generate the gate voltage for the low-side driver. Its output voltage will be used as one input for the charge pump, which generates the gate voltage for the high-side driver. The purpose of the regulator is to limit the gate voltage for the external power MOS transistors to 12V. It needs a ceramic capacitor of 470nF for stability. The output voltage is reduced if the supply voltage at VBAT falls below 12V.

4.7 Charge Pump

The integrated charge pump is needed to supply the gates of the external power MOS transistors. It needs a shuffle capacitor of 220nF and a reservoir capacitor of 470nF. Without load, the output voltage on the reservoir capacitor is V_{VBAT} plus VG. The charge pump is clocked with a dedicated internal oscillator of 100KHz. The charge pump is designed to reach a good EMC level. The charge pump will be switched off for $V_{VBAT} > V_{THOV}$.

4.8 Thermal Shutdown

There is a thermal shutdown block implemented. With rising junction temperature, a first warning level will be reached at 180°C. At this point the IC stays fully functional and a warning will be sent to the microcontroller. At junction temperature 200°C the drivers for H1, H2, L1, L2, SIO and the VCC regulator will be switched off and a reset occurs.

4.9 H-bridge Driver

The IC includes two push-pull drivers for control of two external power NMOS used as high-side drivers and two push-pull drivers for control of two external power NMOS used as low-side drivers. The drivers are able to be used with standard and logic-level power NMOS.

The drivers for the high-side control use the charge pump voltage to supply the gates with a voltage of VG above the battery voltage level. The low-side drivers are supplied by VG directly. It is possible to control the external load (motor) in the forward and reverse direction (see Table 4-1 on page 10). The duty cycle of the PMW controls the speed. A duty cycle of 100% is possible in both directions.

4.9.1 Cross Conduction Time

To prevent high peak currents in the H-bridge, a non-overlapping phase for switching the external power NMOS is realized. An external RC combination defines the cross conduction time in the following way:

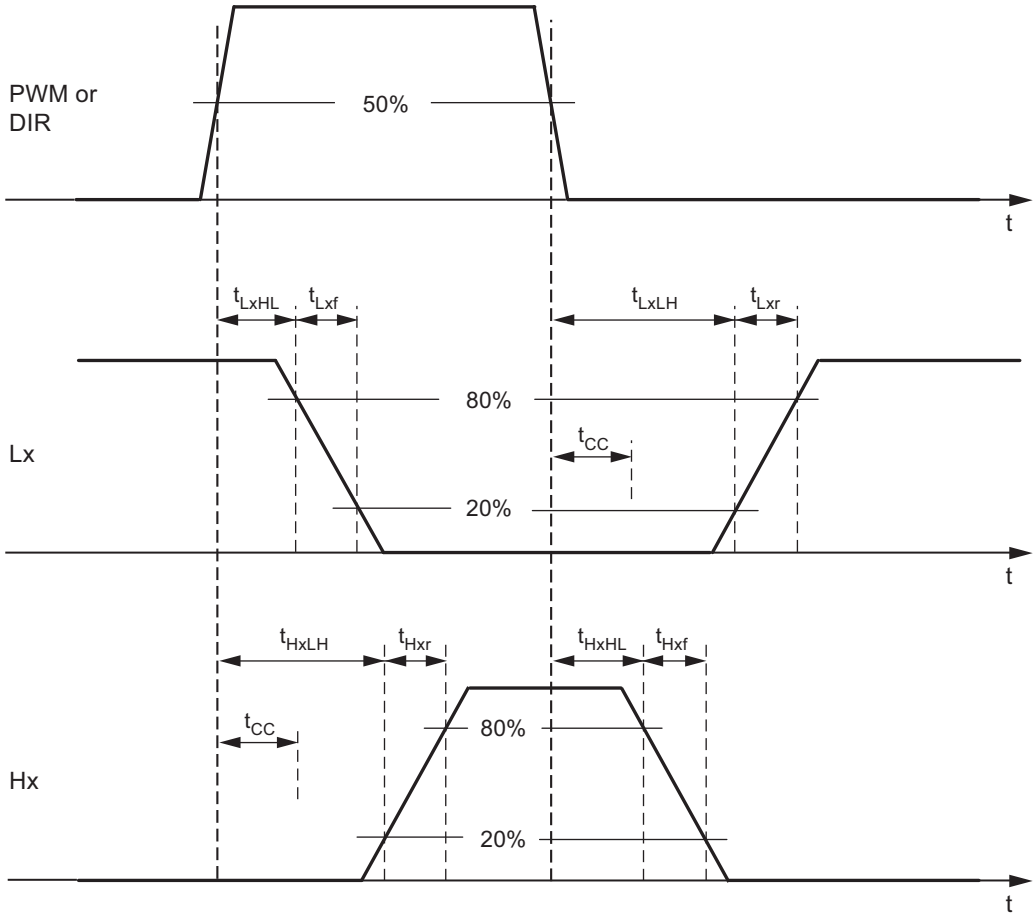
t_{CC} (µs) = 0.41 × R_{CC} (kΩ) × C_{CC} (nF) (tolerance: ±5% ±0.15µs)

The RC combination is charged to 5V and the switching level of the internal comparator is 67% of the start level.

The resistor R_{CC} must be greater than 5kΩ and should be as close as possible to 10kΩ, the C_{CC} value has to be ≤ 5nF. Use of COG capacitor material is recommended.

The time measurement is triggered by the PWM or DIR signal crossing the 50% level.

Figure 4-6. Timing of the Drivers



The delays t_{HxLH} and t_{LxLH} include the cross conduction time t_{CC}.

4.10 Short Circuit Detection

To detect a short in H-bridge circuitry, internal comparators detect the voltage difference between source and drain of the external power NMOS. If the transistors are switched ON and the source-drain voltage difference is higher than the value V_{SC} (4V with tolerances) the diagnosis pin DG1 will be set to ‘H’ and the drivers will be switched off. All gate driver outputs (Hx and Lx) will be set to ‘L’. Releasing the gate driver outputs will set DG1 back to ‘L’. With the next transition on the pin PWM, the corresponding drivers, depending on the DIR pin, will be switched on again.

There is a PBAT supervision block implemented to detect the possible voltage drop on PBAT during a short circuit. If the voltage at PBAT falls under V_{PBAT_OK} the drivers will be switched off and DG1 will be set to “H”. It will be cleared as soon as the PBAT undervoltage condition disappears.

The detection of drain source voltage exceedances is activated after the short circuit blanking time t_{SC}, the short circuit detection of PBAT failures operates immediately.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description	Pin Name	Min	Max	Unit
Ground	GND	0	0	V
Power ground	PGND	–0.3	+0.3	V
Reverse protected battery voltage	VBAT		+40	V
Reverse current out of pin	VBAT	–1		mA
Reverse protected battery voltage	PBAT		+40	V
Reverse current out of pin	PBAT	–20		mA
Digital output	/RESET	–0.3	V_{VCC} + 0.3	V
Digital output	DG1, DG2, DG3	–0.3	V_{VCC} + 0.3	V
4.9V output, external blocking capacitor	VINT	–0.3	+5.5	V
Cross conduction time capacitor/resistor combination	CC	–0.3	V_{VCC} + 0.3	V
Digital input coming from microcontroller	WD	–0.3	V_{VCC} + 0.3	V
Watchdog timing resistor	RWD	–0.3	V_{VCC} + 0.3	V
Digital input direction control	DIR	–0.3	V_{VCC} + 0.3	V
Digital input PWM control + Test mode	PWM	–0.3	V_{VCC} + 0.3	V
5V regulator output	VCC	–0.3	+5.5	V
Digital input	VMODE	–0.3	V_{VINT} + 0.3	V
12V output, external blocking capacitor	VG		+16	V
Digital output	RX	–0.3	V_{VCC} + 0.3	V
Digital input	TX	–0.3	V_{VCC} + 0.3	V
Serial interface data pin	SIO	–27	V_{VBAT} + 2	V
Source external high-side NMOS	S1, S2	(–2)	+30 +40[3]	V
Gates external low-side NMOS	L1, L2	V_{PGND} – 0.3	V_{VG} + 0.3	V
Gates of external high-side NMOS	H1, H2	V_{Sx} – 1[2]	V_{Sx} + 16[2]	V
Charge pump	CPLO		V_{PBAT} + 0.3	V
Charge pump	CPHI		V_{VRES} + 0.3	V
Charge pump output	VRES		+40[4]	V
Switched VBAT	VBATSW	–0.3	V_{VBAT} + 0.3	V
Power dissipation	P_{tot}		1.4[1]	W
Storage temperature	ϑ_{STORE}	–55	+150	°C
Reverse current	CPLO, CPHI, VG, VRES, Sx	–2		mA
	Lx, Hx	–1		mA

Notes:
1. May be additionally limited by external thermal resistance
2. x = 1.2
3. t < 0.5s
4. Load dump of t < 0.5s tolerated

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction to heat slug	R_{thjc}	< 5	K/W
Thermal resistance junction to ambient when heat slug is soldered to PCB	R_{thja}	25	K/W

7. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly.

Parameters	Symbol	Min	Max	Unit
Operating supply voltage(1)	V_{VBAT1}	V_{THUV}	V_{THOV}	V
Operating supply voltage(2)	V_{VBAT2}	6	< V_{THUV}	V
Operating supply voltage(3)	V_{VBAT3}	4.5	< 6	V
Operating supply voltage(4)	V_{VBAT4}	0	< 4.5	V
Operating supply voltage(5)	V_{VBAT5}	> V_{THOV}	40	V
Junction temperature range under bias	T_j	–40	+200	°C
Normal functionality	T_a	–40	+150	°C
Normal functionality, overtemperature warning set	T_j	165	195	°C
Switch-off temperatures of drivers for H1, H2, L1, L2, SIO and of VCC regulator	T_j	185	215	°C

Notes:
1. Full functionality
2. H-bridge drivers are switched off (undervoltage detection)
3. H-bridge drivers are switched off, 5V/3.3V regulator with reduced parameters, RESET works correctly
4. H-bridge drivers are switched off, 5V regulator not working, RESET not correct
5. H-bridge drivers are switched off

8. Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Interference suppression	IEC-CISPR25	Level 5
ESD (Human Body Model)	ESD S 5.1	2kV
CDM (Charge Device Model)	ESD STM5.3.	500V

Note: 1. Test pulse 5: V_{vbmax} = 40V

9. Electrical Characteristics

All parameters given are valid for $V_{THUV} \leq V_{VBAT} \leq V_{THOV}$ and for $-40°C \leq \vartheta_{ambient} \leq 150°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
1	Power Supply and Supervisor Functions								
1.1	Current consumption V_{VBAT}	V_{VBAT} = 13.5V(1)	25, 30	I_{VBAT1}			7	mA	A
1.2	Internal power supply		2	V_{INT}	4.8	4.94	5.1	V	A
1.3	Band gap voltage		3	V_{BG}		1.235		V	A
1.4	Overvoltage threshold Up V_{PBAT}		25	V_{THOV_UP}	21.2		22.7	V	A
1.4.1	Overvoltage threshold Down V_{PBAT}		25	V_{THOV_DOWN}	19.7		21.3	V	A
1.5	Overvoltage threshold hysteresis V_{PBAT}		25	V_{TOVhys}	1		2.4	V	A
1.6	Undervoltage threshold Up V_{VBAT}		30	V_{THUV_UP}	6.8		7.4	V	A
1.6.1	Undervoltage threshold Down V_{VBAT}		30	V_{THUV_DOWN}	6.5		7.0	V	A
1.7	Undervoltage threshold hysteresis V_{VBAT}	Measured during qualification only	30	V_{TUVhys}	0.2		0.6	V	A
1.8	On resistance of V_{VBAT} switch	V_{VBAT} = 13.5V	31	R_{ON_VBATSW}			100	Ω	A
1.9	Undervoltage threshold PBAT	V_{VBAT} = 13.5V	25	V_{PBAT_OK}	6.1		7	V	A
1.10	Undervoltage threshold hysteresis PBAT	V_{VBAT} = 13.5V	25	$V_{PBAT\_OK\_HYST}$	0		100	mV	A
2	5V/3.3V Regulator								
2.1	Regulated output voltage	9V < V_{VBAT} < 40V, I_{load} = 0mA to 100mA	29	V_{CC1}	4.85 (3.2)		5.15 (3.4)	V	A
2.2	Regulated output voltage	6V < $V_{VBAT} \leq$ 9V I_{load} = 0mA to 100mA	29	V_{CC2}	4.75 (3.2)		5.25 (3.4)	V	A
2.2a	Regulated output voltage	6V < $V_{VBAT} \leq$ 9V I_{load} = 0mA to 80mA T_a > 125°C	29	V_{CC2}	4.75 (3.2)		5.25 (3.4)	V	A
2.3	Line regulation	I_{load} = 0mA to 100mA	29	DC line regulation		<1	50	mV	A

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6. Tested during characterization only
7. Supplied by charge pump
8. See Section 4.9.1 “Cross Conduction Time” on page 11
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10. The short-circuit message will never be generated for switch-on time < t_{sc}
11. See Figure 4-5 on page 9 “Definition of Bus Timing Parameters”

9. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \leq V_{VBAT} \leq V_{THOV}$ and for $-40°C \leq \vartheta_{ambient} \leq 150°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
2.4	Load regulation	I_{load} = 0mA to 100mA	29	DC load regulation		<10	50	mV	A
2.5	Output current limitation	V_{VBAT} > 6V	29	I_{OS1}	100		350	mA	A
2.6	Serial inductance to C_{VCC} including PCB		29	ESL	1		20	nH	D
2.7	Serial resistance to C_{VCC} including PCB		29	ESR	0		0.5	Ω	D
2.8	Blocking cap at VCC	(2), (3)	29	C_{VCC}	1.1		3.3	µF	D
2.9	HIGH threshold VMODE		1	VMODE H			4.0	V	A
2.10	LOW threshold VMODE		1	VMODE L	0.7			V	A
3	VG Regulator								
3.1	Regulated output voltage	$V_{PBAT} \geq 14V$ I_{max} = 20mA	24	V_{VG}	11		14	V	A
3.2	Regulated output voltage	V_{PBAT} = 9V I_{max} = 20mA	24	V_{VG}	7.0		9.0	V	A
4	Reset and Watchdog								
4.1	V_{CC} threshold voltage level for /RESET	VMODE = “H” (VMODE = “L”)	29	V_{tHRESH}		4.8 (3.15)		V	A
4.1a	Tracking of reset thres-hold with regulated output voltage	VMODE = “H” (VMODE = “L”)	29	$V_{VCC1-VtHRESH}$	75 (50)			mV	A
4.2	V_{CC} threshold voltage level for /RESET	VMODE = “H” (VMODE = “L”)	29	V_{tHRESL}	4.3 (2.86)			V	A
4.3	Hysteresis of /RESET level	VMODE = “H” (VMODE = “L”)(4)	29	HYS_{RESth}	70	200	350 (240)	mV	A
4.4	Length of pulse at /RESET pin	(5)	5	t_{res}		7000		T_{100}	A
4.5	Length of short pulse at /RESET pin	(5)	5	$t_{resshort}$		200		T_{100}	A
4.6	Wait for the first WD trigger	(5)	5	t_d		7000		T_{100}	A
4.7	Time for VCC < V_{tHRESL} before activating /RESET	(4)	29	$t_{delayRESL}$	0.5		2	µs	C

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9. Electrical Characteristics (Continued)

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No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
4.8	Resistor defining internal bias currents for watchdog oscillator		3	R_{RWD}	10		91	kΩ	D
4.9	Watchdog oscillator period	R_{RWD} = 33kΩ	3	T_{OSC}	11.09		13.55	µs	A
4.11	Watchdog input low-voltage threshold		6	V_{ILWD}			$0.3 \times V_{VCC}$	V	A
4.12	Watchdog input high-voltage threshold		6	V_{IHWD}	$0.7 \times V_{VCC}$			V	A
4.13	Hysteresis of watchdog input voltage threshold		6	V_{hysWD}	0.3		0.8	V	A
4.14	Close window	(5)	6	t1		$980 \times T_{OSC}$			A
4.15	Open window	(5)	6	t2		$780 \times T_{OSC}$			A
4.16	Output low-voltage of /RESET	At I_{OLRES} = 1mA	5	V_{OLRES}			0.4	V	A
4.17	Internal pull-up resistor at pin /RESET		5	R_{PURES}	5	10	15	kΩ	A
5	High Voltage Serial Interface								
5.1	Low-level output current	Normal mode; V_{SIO} = 0V, V_{RX} = 0.4V	13	IL_{RX}	2			mA	A
5.2	High-level output current	Normal mode; $V_{SIO} = V_{VBAT}$ $V_{RX} = V_{CC} - 0.4V$	13	IH_{RX}	0.8			mA	A
5.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 500Ω	8	$V_{\_LoSUP}$			1.2	V	A
5.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VBAT} = 18V R_{load} = 500Ω	8	$V_{\_HiSUP}$			2	V	A
5.6	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 1000Ω	8	$V_{\_LoSUP\_1k}$	0.6			V	A
5.7	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VBAT} = 18V R_{load} = 1000Ω	8	$V_{\_HiSUP\_1k\_}$	0.8			V	A
5.8	Pull up resistor to VBAT	The serial diode is mandatory	8	R_{SIO}	20	30	60	kΩ	A

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11. See Figure 4-5 on page 9 “Definition of Bus Timing Parameters”

9. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \leq V_{VBAT} \leq V_{THOV}$ and for $-40°C \leq \vartheta_{ambient} \leq 150°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
5.9	Current limitation	$V_{SIO} = V_{BAT\_max}$	8	I_{SIO_LIM}	40		250	mA	A
5.9a	Current limitation in case of RESET and SIO overheat	$V_{SIO} = V_{BAT\_max}$ RESET = high	8	$I_{SIO\_LIM\_RESET}$	30		100	mA	A
5.10	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off $V_{SIO} = 0V$ $V_{VBAT} = 12V$	8	$I_{SIO\_PAS\_dom}$	–1			mA	A
5.11	Leakage current SIO recessive	Driver off $8V < V_{VBAT} < 18V$ $8V < V_{SIO} < 18V$ $V_{SIO} \geq V_{VBAT}$	8	$I_{SIO\_PAS\_rec}$			30	µA	A
5.12	Leakage current at ground loss Control unit disconnected from ground Loss of local ground must not affect communication in the residual network	$GND_{Device} = V_{VBAT}$ $V_{VBAT} = 12V$ $0V < V_{SIO} < 18V$	8	$I_{SIO\_NO\_gnd}$	–1		1	mA	A
5.13	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	V_{VBAT} disconnected V_{SUP_Device} = GND $0V < V_{SIO} < 18V$	8	I_{SIO}			100	µA	A
5.14	Center of receiver threshold	$V_{SIO\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$	8	V_{SIO_CNT}	$0.475 \times V_{VBAT}$	$0.5 \times V_{VBAT}$	$0.525 \times V_{VBAT}$	V	A
5.15	Receiver dominant state	$V_{EN} = 5V$	8	V_{SIOdom}			$0.4 \times V_{VBAT}$	V	A
5.16	Receiver recessive state	$V_{EN} = 5V$	8	V_{SIOrec}	$0.6 \times V_{VBAT}$			V	A
5.17	Receiver input hysteresis	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$	8	V_{SIOhys}		$0.1 \times V_{VBAT}$	$0.175 \times V_{VBAT}$	V	A
5.18	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_{VBAT}$ $TH_{Dom(max)} = 0.581 \times V_{VBAT}$ $V_{VBAT} = 7V$ to 18V $t_{Bit} = 50µs$ $D1 = t_{sio\_rec(min)} / 2 \times t_{Bit}$ (11)	8	D1	0.380				A

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9. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \leq V_{VBAT} \leq V_{THOV}$ and for $-40°C \leq \vartheta_{ambient} \leq 150°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
5.19	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_{VBAT}$ $TH_{Dom(min)} = 0.284 \times V_{VBAT}$ V_{VBAT} = 7V to 18V t_{Bit} = 50µs D2 = $t_{sio\_rec(max)} / 2 \times t_{Bit}$ (11)	8	D2			0.600		A
5.20	Propagation delay of receiver	$t_{rec\_pd} = max(t_{rx\_pdr}, t_{rx\_pdf})$ (11) 7V < V_{VBAT} < 18V	8	t_{rx_pd}			6	µs	A
5.21	Symmetry of receiver propagation delay	$t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$ (11) 7V < V_{VBAT} < 18V	8	t_{rx_sym}	–2		+2	µs	A
6	Control Inputs DIR, PWM, WD, TX								
6.1	Input low-voltage threshold		10, 11, 6, 9	V_{IL}			$0.3 \times V_{VCC}$	V	A
6.2	Input high-voltage threshold		10, 11, 6, 9	V_{IH}	$0.7 \times V_{VCC}$			V	A
6.3	Hysteresis		10, 11, 6, 9	HYS	0.3	0.5	0.8	V	A
6.4	Pull-down resistor	DIR, PWM, WD, TX	10, 11, 6, 9	R_{PD}	25	50	140	kΩ	A
6.5	Rise/fall time		10, 11, 6, 9	t_{rf}			100	ns	A
7	Charge Pump								
7.1	Charge pump voltage	Load = 0A	21	VCP			$V_{VBAT} + V_{VG}$	V	A
7.2	Charge pump voltage	Load = 3mA, C_{CP} = 100nF	21	VCP	$V_{VBAT} + V_{VG} - 1$			V	A
7.3	Period charge pump oscillator		21	T_{100}	9		11	µs	A
7.4	CP load current in VG without CP load	Load = 0A	21	I_{VGCPz}			600	µA	A
7.5	CP load current in VG with CP load	Load = 3mA, C_{CP} = 100nF	21	I_{VGCP}			4	mA	A
7.6	Charge pump OK threshold UP	Reference: PBAT	21	V_{CPOK_UP}	5.3		6.3	V	A

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9. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \leq V_{VBAT} \leq V_{THOV}$ and for $-40°C \leq \vartheta_{ambient} \leq 150°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
7.7	Charge pump OK threshold DOWN	Reference: PBAT	21	V_{CPOK_DOWN}	4.5		5.5	V	A
7.8	Charge pump OK hysteresis		21	V_{CPOK_HYS}	0.3		1.3	V	A
8	H-bridge Driver								
8.1	Low-side driver HIGH output voltage		26, 27	V_{LxH}	V_{VG} – 0.5V		V_{VG}	V	A
8.2	ON-resistance of sink stage of pins L1, L2		26, 27	R_{DSON_LxL}, x = 1, 2			25	Ω	A
8.3	ON-resistance of source stage of pins L1, L2		26, 27	R_{DSON_LxH}, x = 1, 2			25	Ω	A
8.4	Output peak current at pins L1, L2, switched to LOW	V_{Lx} = 3V	26, 27	I_{LxL}, x = 1, 2	100			mA	A
8.5	Output peak current at pins L1, L2, switched to HIGH	V_{Lx} = 3V	26, 27	I_{LxH}, x = 1, 2			–100	mA	A
8.6	Ohmic pull-down resistance at pins L1, L2	Designed for 0V < V_{VBAT} < 40V	26, 27	R_{PDLx} x = 1, 2	25		140	kΩ	A
8.7	ON-resistance of sink stage of pins H1, H2	V_{Sx} = 0	18, 20	R_{DSON_HxL}, x = 1, 2			25	Ω	A
8.8	ON-resistance of source stage of pins H1, H2	$V_{Sx} = V_{VBAT}$	18, 20	R_{DSON_HxH}, x = 1, 2			25	Ω	A
8.9	Output peak current at pins Hx, switched to LOW	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{Hx} = V_{VBAT}$ + 3V	18, 20	I_{HxL}, x = 1, 2	100			mA	A
8.10	Output peak current at pins Hx, switched to HIGH	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{Hx} = V_{VBAT}$ + 3V	18, 20	I_{HxH}, x = 1, 2			–100	mA	A
8.11	Static switch output low voltage at pins Hx and Lx	V_{Sx} = 0V I_{Hx} = 1mA, I_{Lx} = 1mA	18, 20, 26, 27	V_{HxL}, V_{LxL} x = 1, 2			0.3	V	A
8.12	Static high-side switch output high-voltage pins H1, H2	I_{Lx} = –10µA (PWM = static)	18, 20	$V_{HxHstat1}$ (7)	V_{VBAT} + V_{VG} – 1		V_{VBAT} + V_{VG}	V	A
8.13	Ohmic sink resistance between pins Hx and Sx	Designed for 0V < V_{VBAT} < 40V	17, 18, 19, 20	R_{PDHx}	25		140	kΩ	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
	Dynamic Parameters								
8.15	Propagation delay time, low-side driver from high to low	Figure 4-6 on page 12 V_{VBAT} = 13.5V	26, 27	t_{LxHL}			0.5	µs	A
8.16	Propagation delay time, low-side driver from low to high	V_{VBAT} = 13.5V	26, 27	t_{LxLH}			0.5 + t_{CC}	µs	A
8.17	Fall time low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5nF	26, 27	t_{Lxf}			0.5	µs	A
8.18	Rise time low-side driver	V_{VBAT} = 13.5V	26, 27	t_{Lxr}			0.5	µs	A
8.19	Propagation delay time, high-side driver from high to low	Figure 4-6 on page 12 V_{VBAT} = 13.5V	18, 20	t_{HxHL}			0.5	µs	A
8.20	Propagation delay time, high-side driver from low to high	V_{VBAT} = 13.5V	18, 20	t_{HxLH}			0.5 + t_{CC}	µs	A
8.21	Fall time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5nF	18, 20	t_{Hxf}			0.5	µs	A
8.22	Rise time high-side driver	V_{VBAT} = 13.5V	18, 20	t_{Hxr}			0.5	µs	A
8.24	External resistor		4	R_{CC}	5			kΩ	D
8.25	External capacitor		4	C_{CC}			5	nF	D
8.26	R_{ON} of t_{CC} switching transistor		4	R_{ONCC}			200	Ω	A
8.27	Cross conduction time(8)	R_{CC} = 10kΩ C_{CC} = 1nF	4	t_{CC}	3.75		4.45	µs	A
8.28	Short circuit detection voltage	(9)	17, 19	V_{SC}	3.5	4	4.7	V	A
8.29	Short circuit blanking time	(10)	17, 19	t_{SC}	5	10	15	µs	A
9	Diagnostic Outputs DG1, DG2, DG3								
9.1	Low level output current	V_{DG} = 0.4V(6)	14, 15, 16	IL	2			mA	A
9.2	High level output current	V_{DG} = VCC – 0.4V(6)	14, 15, 16	IH	0.8			mA	A

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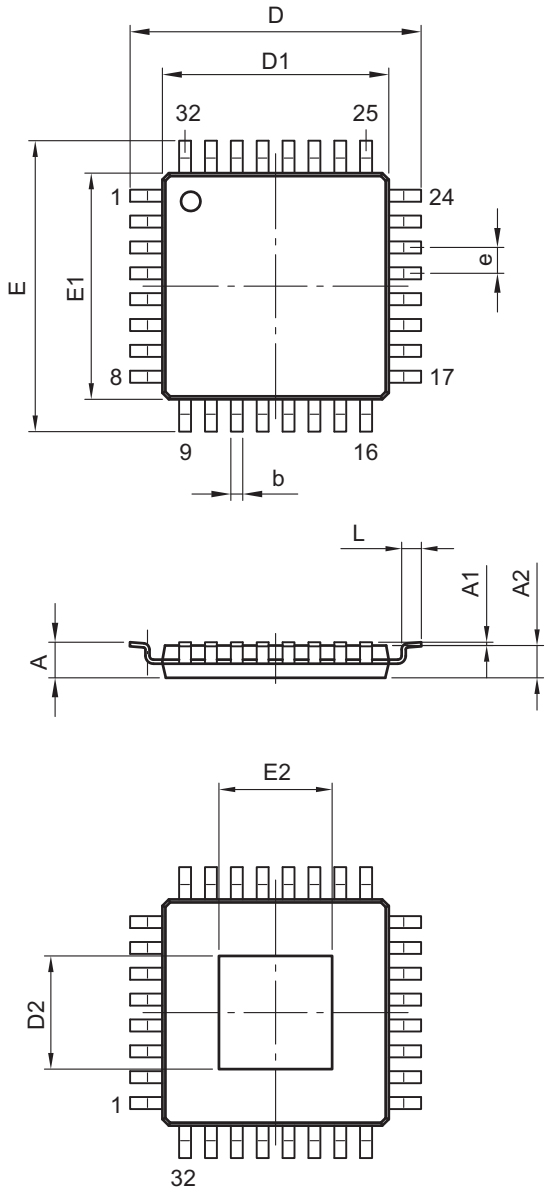
10. Ordering Information

Extended Type Number	Package	Remarks
ATA6824C-MFHW	TPQFP32, 7mm × 7mm	Pb-free

11. Package Information



technical drawings
according to DIN
specifications

Dimensions in mm

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A			1.2	
A1	0.05		0.15	
A2	0.95	1	1.05	
D		9 BSC		
D1		7 BSC		
D2		3.5 BSC		
E		9 BSC		
E1		7 BSC		
E2		3.5 BSC		
L	0.45	0.6	0.75	
N		32		
b	0.3	0.37	0.45	
e		0.8 BSC		

11/25/08

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: epad TPQFP32** (acc. JEDEC OUTLINE)		6.543-5157.01-4	1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9212G-AUTO-09/13	• Section 11 “Package Information” on page 22 updated
9212F-AUTO-04/12	• Section 5 “Absolute Maximum Ratings” on page 13 changed • Section 9 “Electrical Characteristics” number 4.1 on page 16 changed
9212E-AUTO-01/12	• QFN32 package variant on all pages removed
9212D-AUTO-11/11	• Figure 5-5 “Definition of Bus Timing Parameters” on page 9 changed • Section 6 “Absolute Maximum Ratings” on page 13 changed • Section 10 “Electrical Characteristics” numbers 5.12, 5.14, 5.15, 5.16 and 5.17 on page 18 changed
9212C-AUTO-09/11	• Section 5.1.2 “Voltage Supervisor” on page 6 changed • Section 5.5.2 “Pin PWM” on page 10 changed • Section 10 “Electrical Characteristics” numbers 1.4, 1.4.1 and 1.5 on page 15 changed
9212B-AUTO-04/11	• Section 10 “Electrical Characteristics” numbers 8.6 and 8.13 on page 20 changed

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