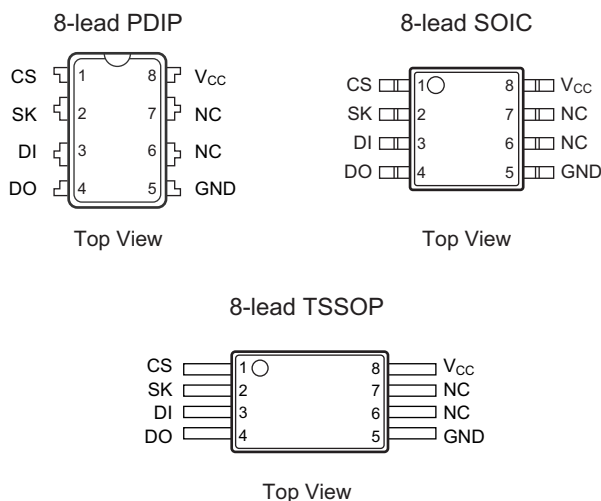


1. Pin Descriptions and Pinouts

Table 1-1. Pin Configurations

Pin	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V _{CC}	Power Supply
NC	No Connect



Note: Drawings are not to scale.

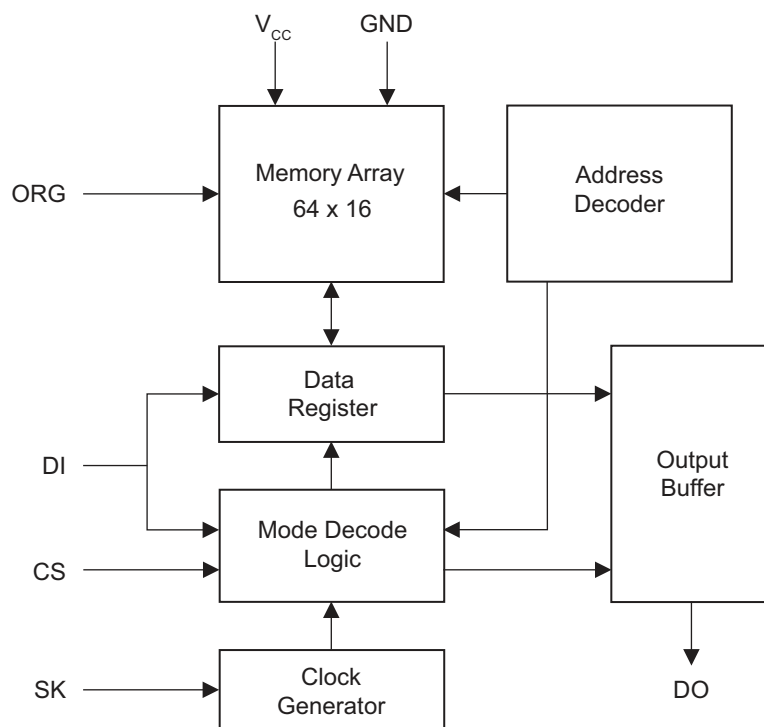
2. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Electrical Characteristics

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.8\text{V}$	CS = 0V		0.4	1.0	μA
I_{SB2}	Standby Current	$V_{CC} = 2.7\text{V}$	CS = 0V		6.0	10.0	μA
I_{SB3}	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V		10.0	15.0	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
$V_{IL1}^{(1)}$	Input Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6		0.8	V
$V_{IH1}^{(1)}$	Input High Voltage			2.0		$V_{CC} + 1$	
$V_{IL2}^{(1)}$	Input Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		-0.6		$V_{CC} \times 0.3$	V
$V_{IH2}^{(1)}$	Input High Voltage			$V_{CC} \times 0.7$		$V_{CC} + 1$	
V_{OL1}	Output Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{mA}$			0.4	V
V_{OH1}	Output High Voltage		$I_{OH} = -0.4\text{mA}$	2.4			V
V_{OL2}	Output Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OL} = 0.15\text{mA}$			0.2	V
V_{OH2}	Output High Voltage		$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$, $CL = 1$ TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		2	MHz
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		1	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		0.25	
t_{SKH}	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1,000			
t_{SKL}	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1,000			
t_{CS}	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1,000			
t_{CSS}	CS Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	200			
t_{DIS}	DI Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t_{CSH}	CS Hold Time	Relative to SK	0			ns
t_{DIH}	DI Hold Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t_{PD1}	Output Delay to "1"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			1,000	
t_{PD0}	Output Delay to "0"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			1,000	
t_{SV}	CS to Status Valid	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			250	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			1,000	
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL} $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			100	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$			150	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			400	
t_{WP}	Write Cycle Time		0.10	3	5	ms
Endurance ⁽¹⁾	5.0V, 25°C		1M			Write Cycle

Note: 1. This parameter is ensured by characterization.

5. Functional Description

The AT93C46E is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start condition (Logic 1) followed by the appropriate opcode and the desired memory address location.

Table 5-1. Instruction Set

Instruction	SB	Opcode	Address	Comments
			x16	
READ	1	10	$A_5 - A_0$	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	$A_5 - A_0$	Erase memory location $A_n - A_0$.
WRITE	1	01	$A_5 - A_0$	Writes memory location $A_n - A_0$.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
EWDS	1	00	00XXXX	Disables all programming instructions.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output (DO) pin. Output data changes are synchronized with the rising edges of Serial Clock (SK).

Note: It should be noted that a dummy bit (Logic 0) precedes the 16-bit data output string.

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the device.

ERASE: The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the device if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

WRITE: The WRITE instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP} .

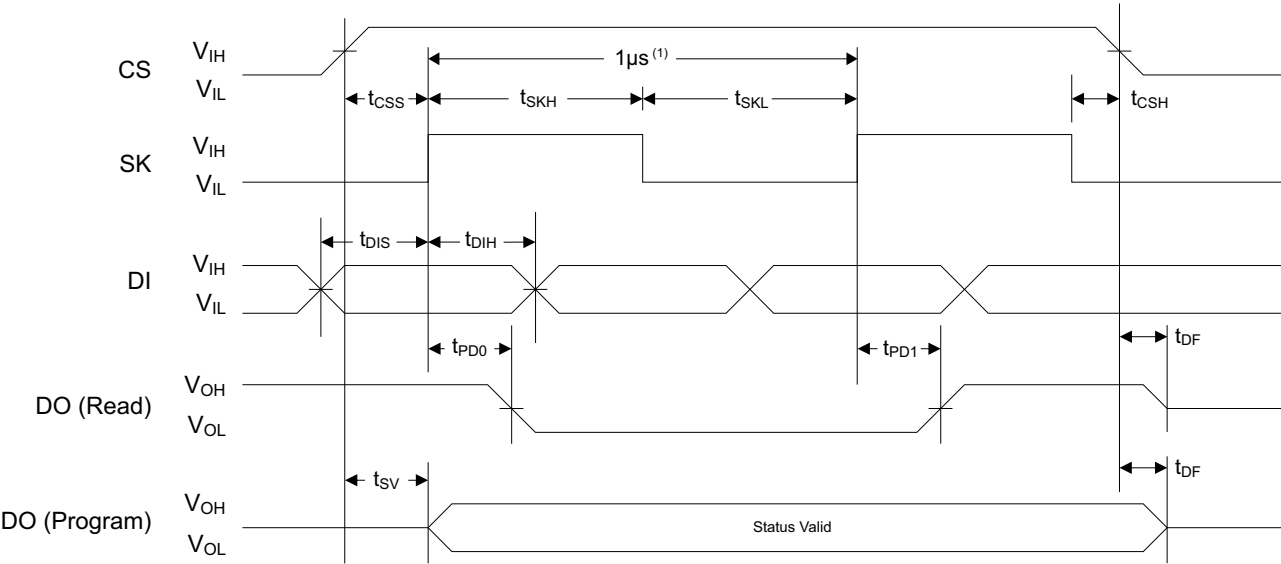
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

Erase/Write Disable (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 6-1. Organization Key for Timing Diagrams

I/O	x16
A _N	A ₅
D _N	D ₁₅

Figure 6-2. Read Timing

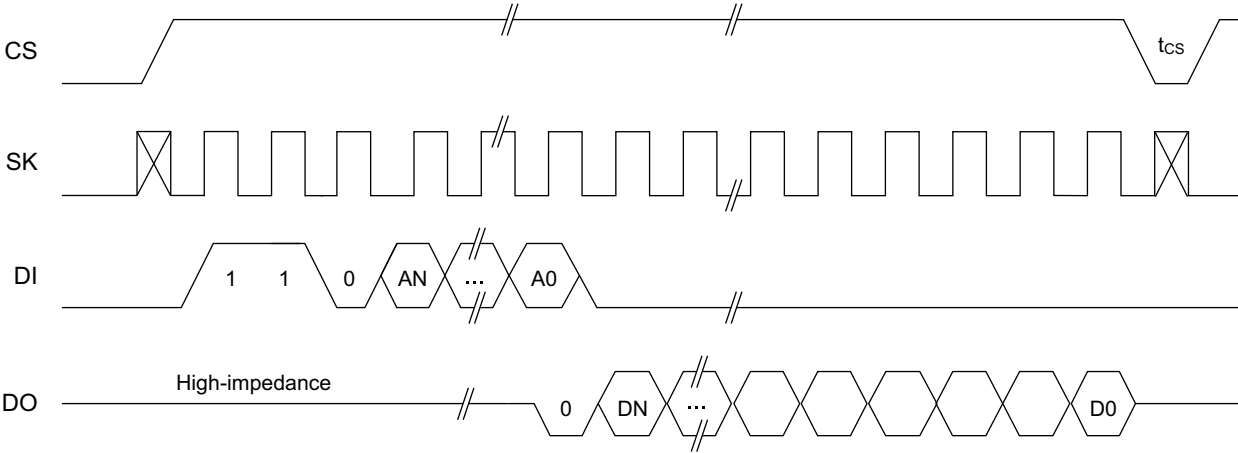
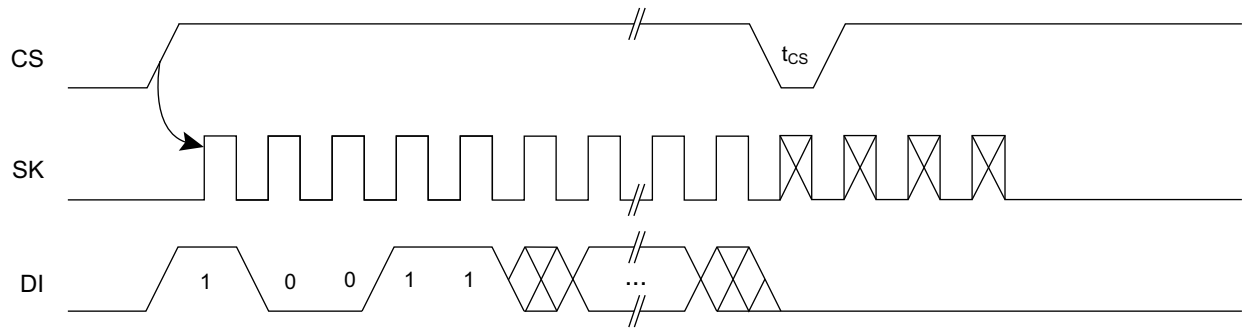


Figure 6-3. EWEN Timing⁽¹⁾



Note: 1. Requires a minimum of nine clock cycles.

Figure 6-4. ERASE Timing

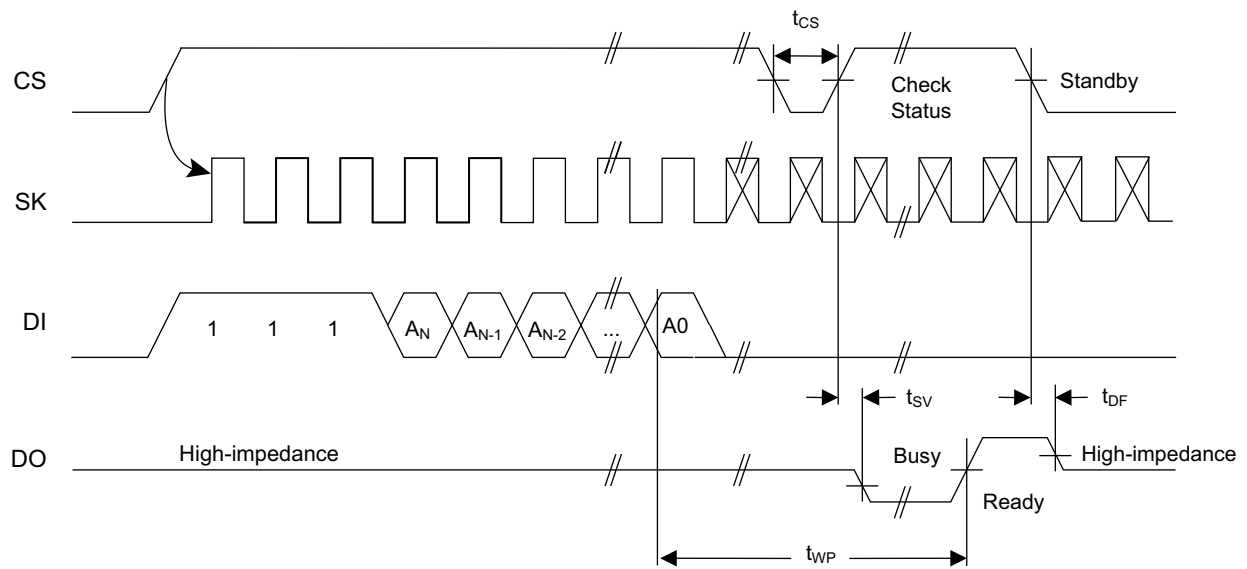


Figure 6-5. Write Timing

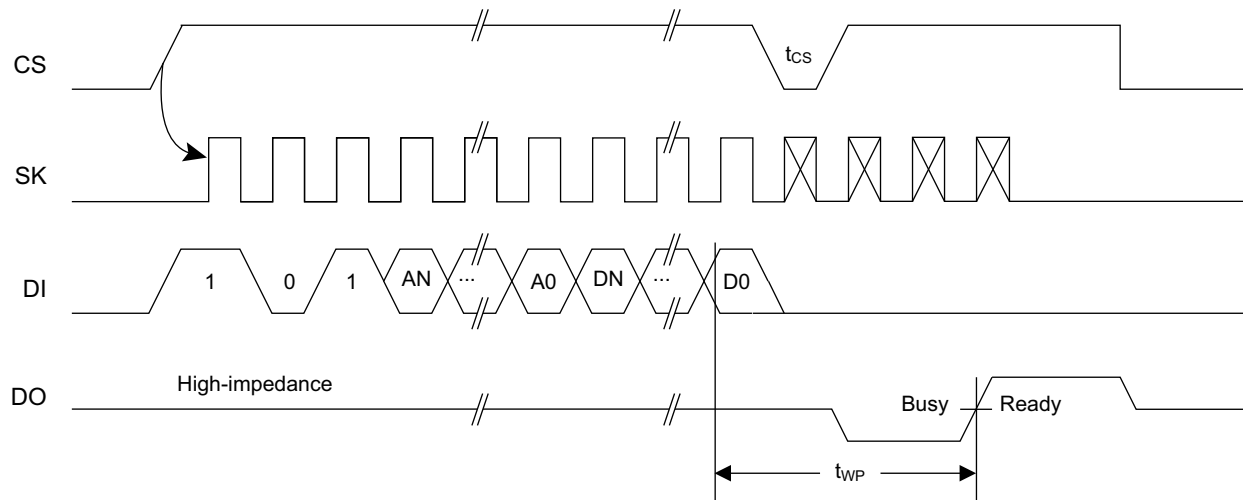
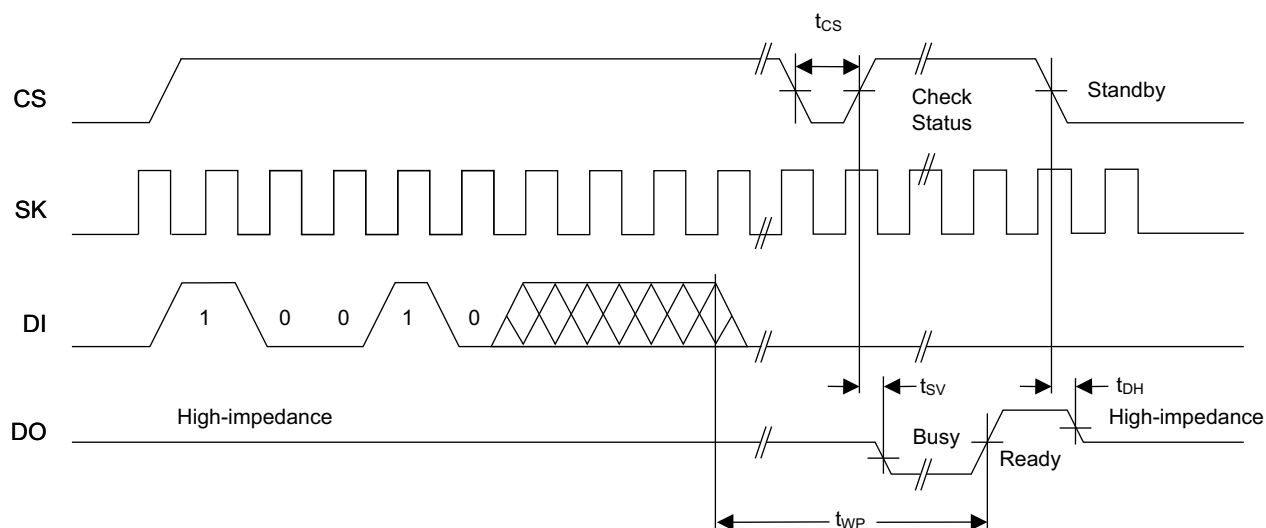
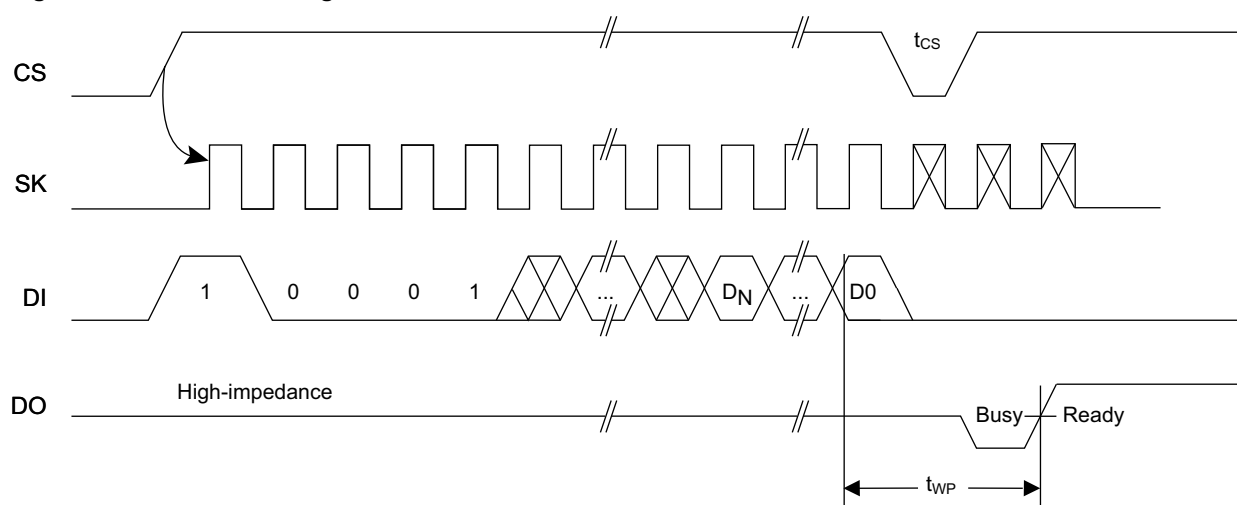


Figure 6-6. ERAL Timing⁽¹⁾



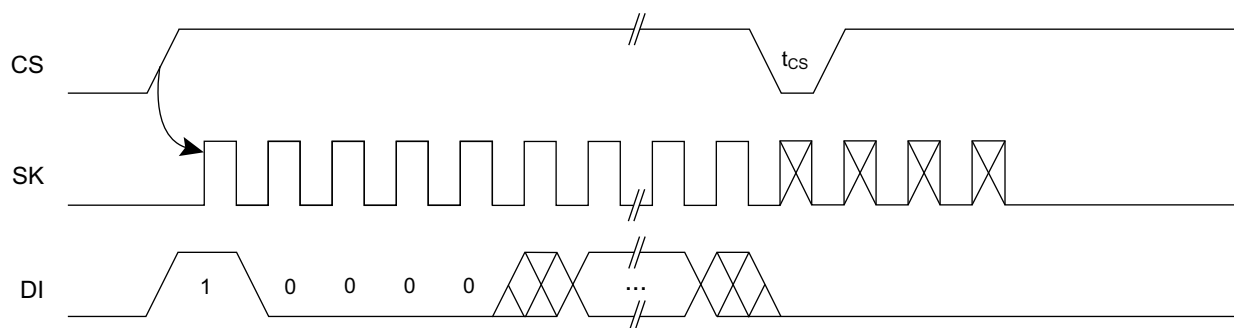
Note: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.

Figure 6-7. WRAL Timing^{(1) (2)}



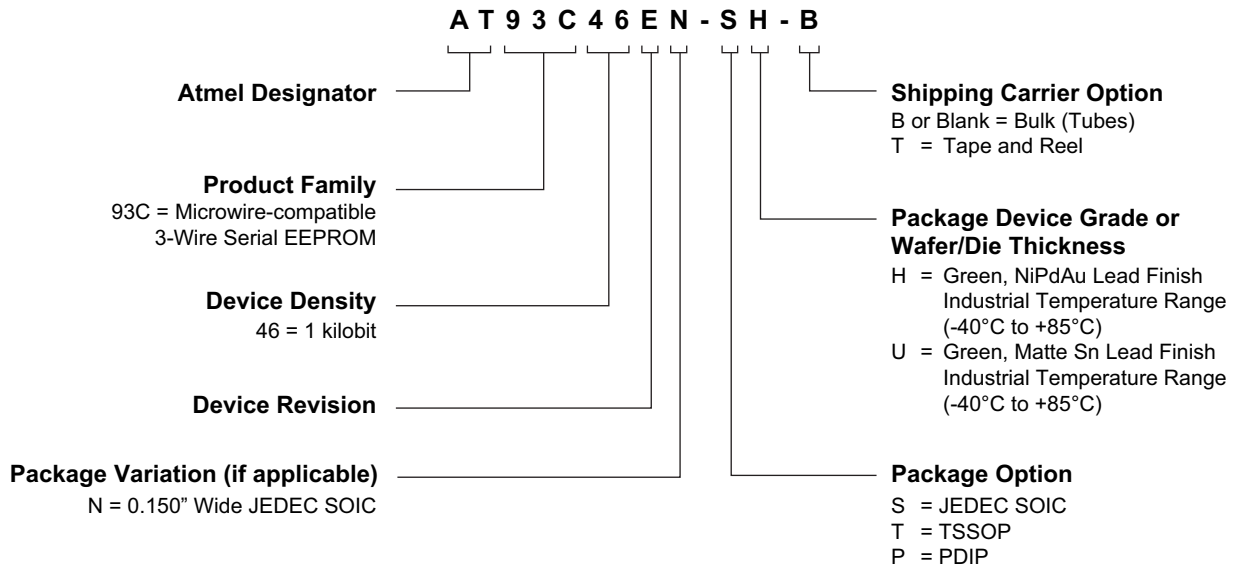
Notes: 1. Valid only at $V_{CC} = 4.5V$ to $5.5V$.
2. Requires a minimum of nine clock cycles.

Figure 6-8. EWDS Timing⁽¹⁾



Note: 1. Requires a minimum of nine clock cycles.

7. Ordering Code Detail



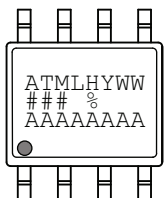

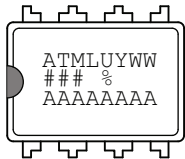
8. Ordering Information

Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT93C46EN-SH-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT93C46EN-SH-T			Tape and Reel	4,000 per Reel	
AT93C46E-TH-B		8X	Bulk (Tubes)	100 per Tube	
AT93C46E-TH-T			Tape and Reel	5,000 per Reel	
AT93C46E-PU	Matte Tin (Lead-free/Halogen-free)	8P3	Bulk (Tubes)	50 per Tube	

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline Package (TSSOP)
8P3	8-lead, 0.300" wide body, Plastic Dual In-line Package (PDIP)

9. Part Markings

AT93C46E: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-lead PDIP
	 <p>Note: Lot Number and location of assembly and on the bottom side of the package.</p>	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

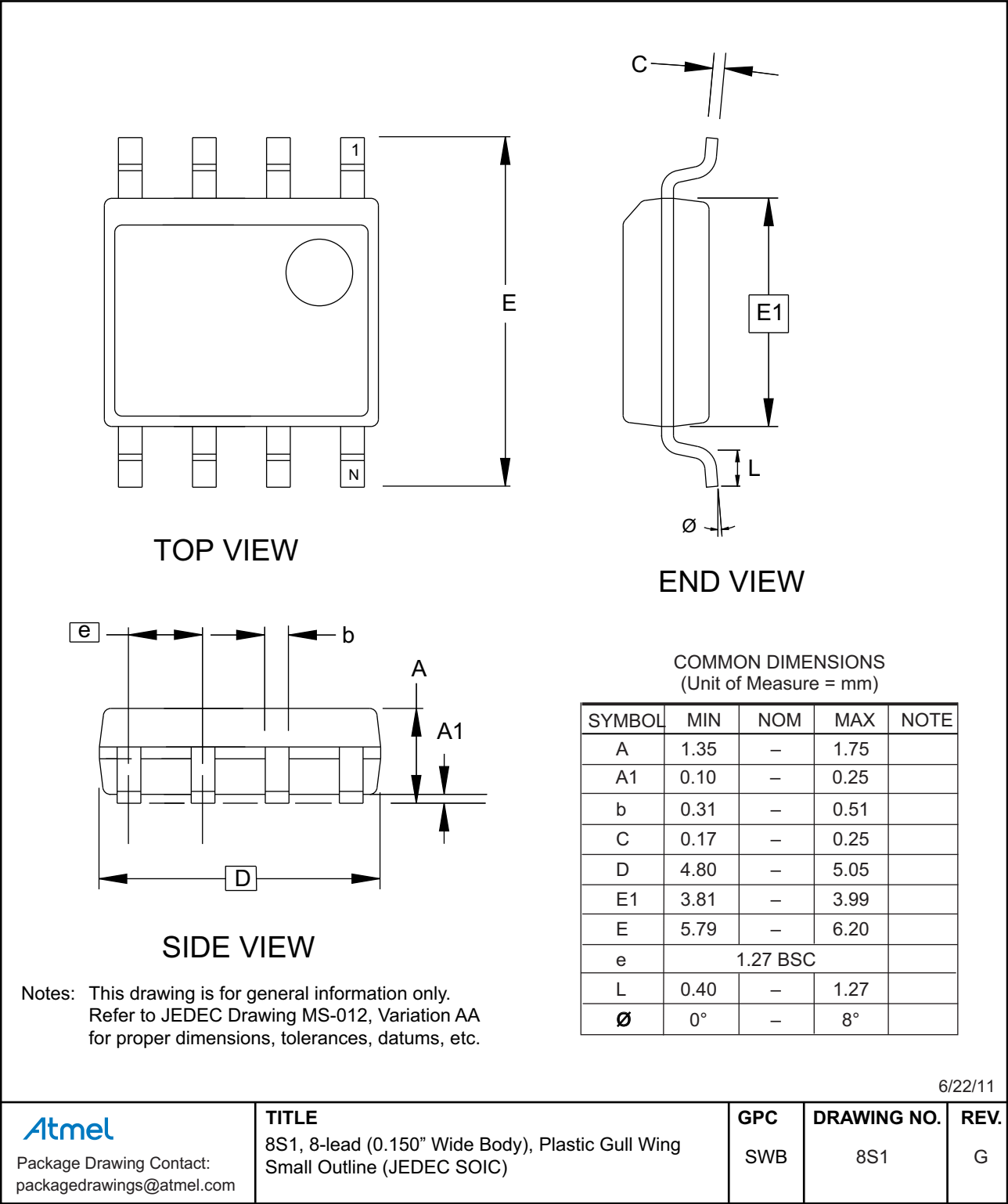
Catalog Number Truncation			
AT93C46E		Truncation Code ###: 46E	
Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014 8: 2018	A: January	02: Week 2	1: 1.8V min
5: 2015 9: 2019	B: February	04: Week 4	
6: 2016 0: 2020	
7: 2017 1: 2021	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	U: Industrial/Matte Tin/SnAgCu H: Industrial/NiPdAu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/13/14

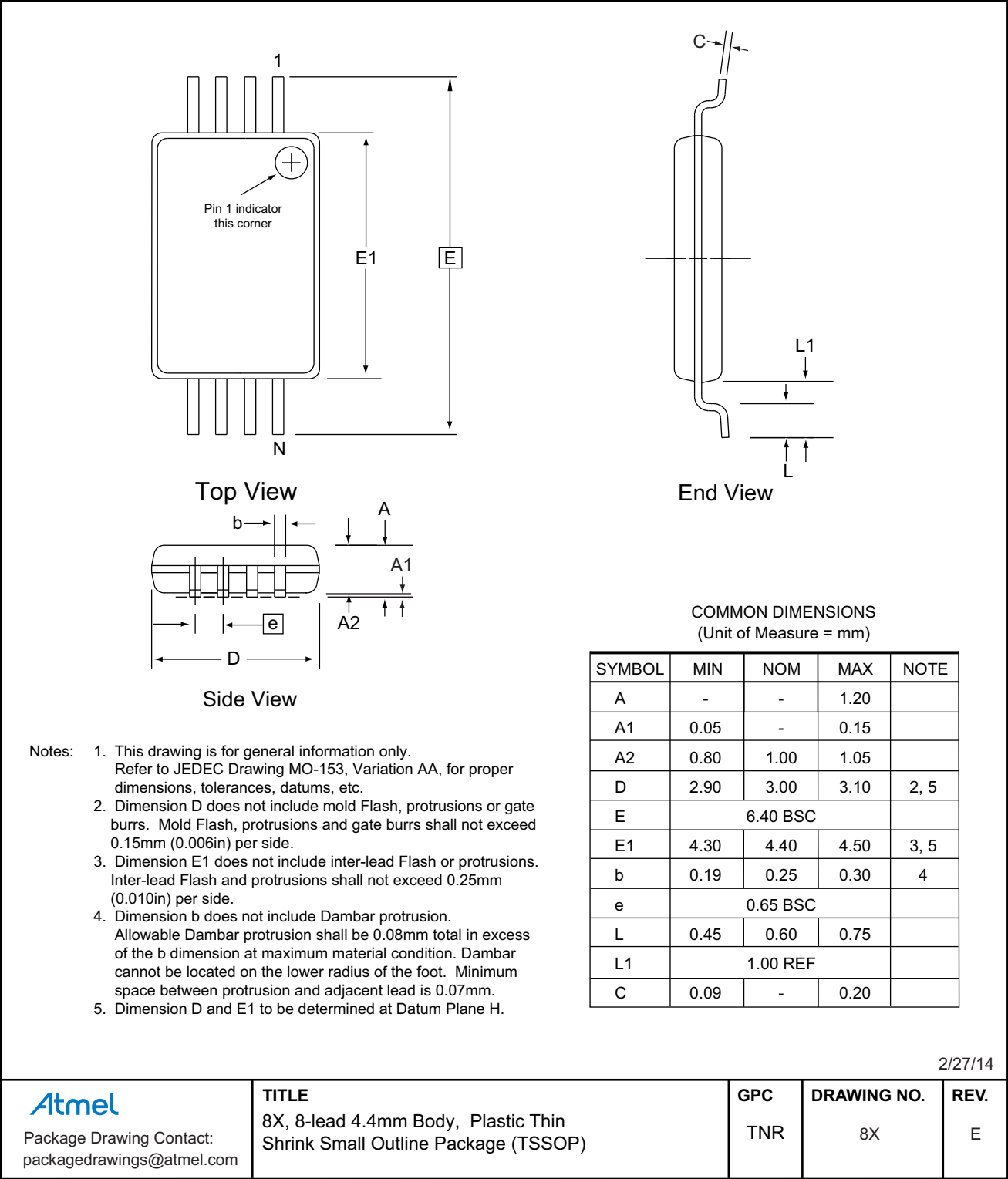
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE 93C46ESM, AT93C46E Package Marking Information	DRAWING NO. 93C46ESM	REV. A
--	---	--------------------------------	------------------

10. Packaging Information

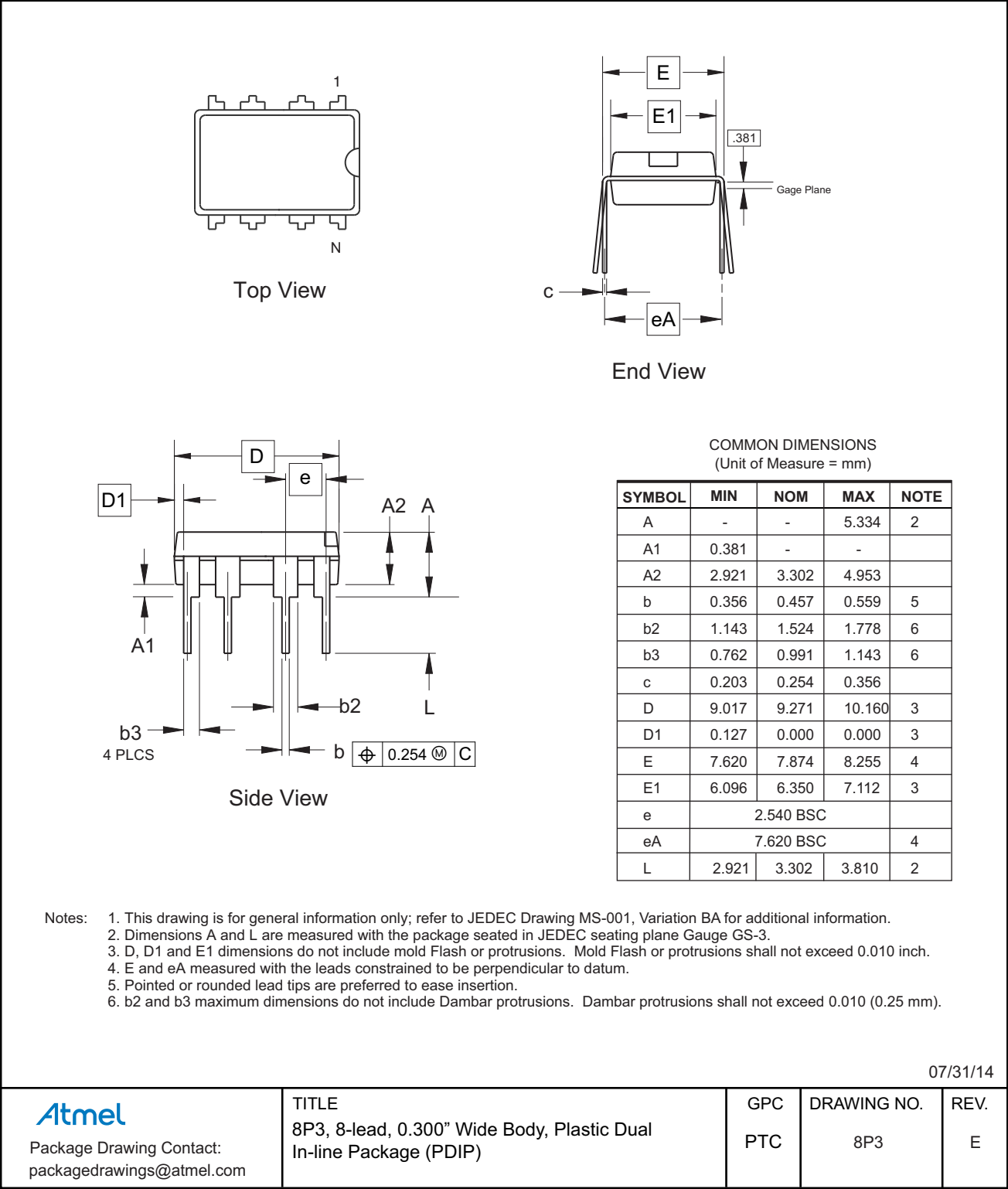
10.1 8S1 — 8-lead JEDEC SOIC



10.2 8X — 8-lead TSSOP



10.3 8P3 — 8-lead PDIP



07/31/14

 Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	GPC	DRAWING NO.	REV.
		PTC	8P3	E

11. Revision History

Doc. Rev.	Date	Comments
5207F	01/2015	Updated ordering information section.
5207E	10/2014	Added the part markings and ordering code detail. Updated the package outline drawings and the 8A2 to 8X. Updated the template, Atmel logos, and the disclaimer page.
5207D	01/2008	Removed 'preliminary' status
5207C	11/2007	Modified 'max' value on AC Characteristics table
5207B	08/2007	Modified Part Marking Scheme Tables
5207A	01/2007	Initial document release

