3. Absolute Maximum Ratings*

Operating Temperature	–55·C to +125·C
Storage Temperature	–65·C to +150·C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3-1. Block Diagram

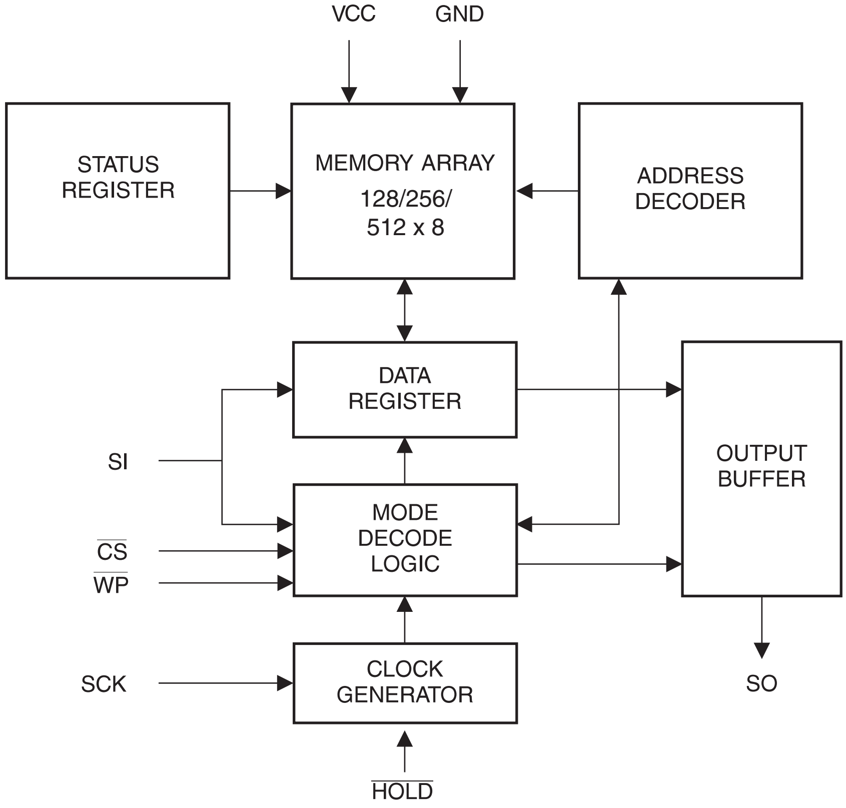


Table 3-1. Pin Capacitance[(1)]

Applicable over recommended operating range from T_A = 25·C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3-2. DC Characteristics

Applicable over recommended operating range from: T_A = –40·C to +125·C. V_{CC} = +2.7V to +5.5V

Symbol	Parameter	Test Condition		Min	Max	Units
V_{CC1}	Supply Voltage			2.7	5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open, Read			3.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open, Read, Write			6.0	mA
I_{CC3}	Supply Current	V_{CC} = 5.0V at 5 MHz, SO = Open, Read, Write			6.0	mA
I_{SB1}(1)	Standby Current	V_{CC} = 2.7V	$\overline{CS} = V_{CC}$		3.0	µA
I_{SB2}(1)	Standby Current	V_{CC} = 5.0V	$\overline{CS} = V_{CC}$		5.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–0.6	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}		–0.6	3.0	µA
V_{IL}(2)	Input Low Voltage			–0.6	V_{CC} x 0.3	V
V_{IH}(2)	Input High Voltage			V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.0 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = –1.0 mA	V_{CC} – 0.8		V
V_{OL2}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = –100 µA	V_{CC} – 0.2		V

Note:
1. Worst case measured at 125·C
2. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 3-3. AC Characteristics

Applicable over recommended operating range from T_A = –40·C to +125·C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	2.7–5.5	0	5.0	MHz
t_{RI}	Input Rise Time	2.7–5.5		2	µs
t_{FI}	Input Fall Time	2.7–5.5		2	µs
t_{WH}	SCK High Time	2.7–5.5	40		ns
t_{WL}	SCK Low Time	2.7–5.5	40		ns
t_{CS}	$\overline{\text{CS}}$ High Time	2.7–5.5	80		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time	2.7–5.5	80		ns
t_{CSH}	$\overline{\text{CS}}$ Hold Time	2.7–5.5	80		ns
t_{SU}	Data In Setup Time	2.7–5.5	5		ns
t_H	Data In Hold Time	2.7–5.5	20		ns
t_{HD}	$\overline{\text{Hold}}$ Setup Time	2.7–5.5	40		
t_{CD}	$\overline{\text{Hold}}$ Hold Time	2.7–5.5	40		ns
t_V	Output Valid	2.7–5.5	0	40	ns
t_{HO}	Output Hold Time	2.7–5.5	0		ns
t_{LZ}	$\overline{\text{Hold}}$ to Output Low Z	2.7–5.5	0	40	ns
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	2.7–5.5		80	ns
t_{DIS}	Output Disable Time	2.7–5.5		80	ns
t_{WC}	Write Cycle Time	2.7–5.5		5	ms
Endurance(1)	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

4. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25010A/020A/040A always operates as a slave.

TRANSMITTER/RECEIVER: The AT25010A/020A/040A has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the Read and Write instructions.

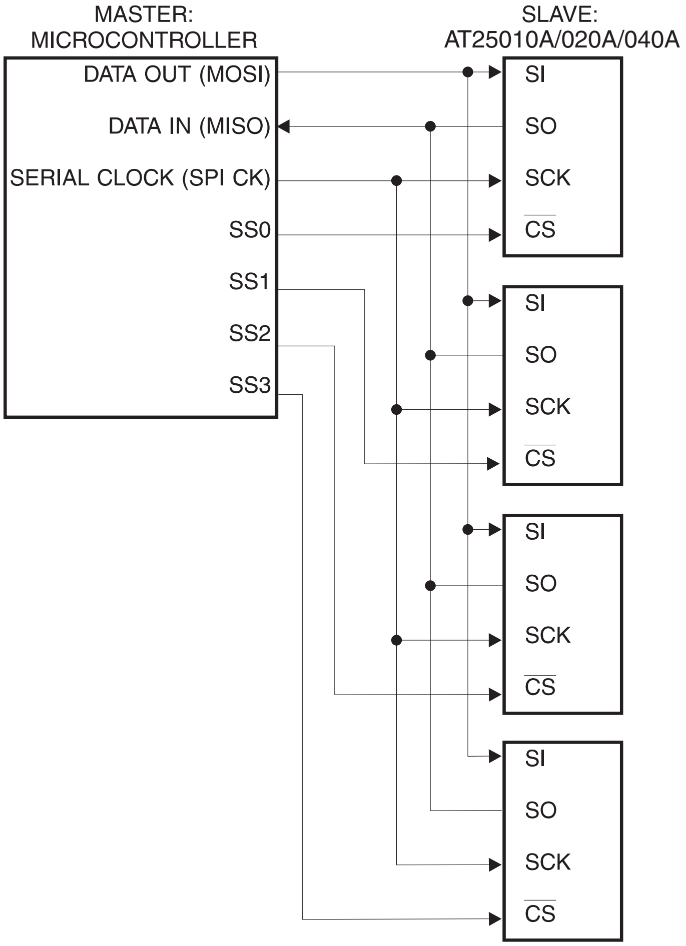
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25010A/020A/040A, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25010A/020A/040A is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25010A/020A/040A. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the WP pin is brought low, all write operations are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write to the AT25010A/020A/040A. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation.

Figure 4-1. SPI Serial Interface



5. Functional Description

The AT25010A/020A/040A is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25010A/020A/040A utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 5-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

Table 5-1. Instruction Set for the AT25010A/020A/040A

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{\text{WP}}$ pin must be held high during a WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{\text{WP}}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 5-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Table 5-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 (RDY)	Bit 0 = “0” (RDY) indicates the device is ready. Bit 0 = “1” indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= “0” indicates the device is not write-enabled. Bit 1 = “1” indicates the device is write-enabled.
Bit 2 (BP0)	See Table 5-4 on page 7.
Bit 3 (BP1)	See Table 5-4 on page 7.
Bits 4 – 6 are “0”s when device is not in an internal write cycle.	
Bits 0 – 7 are “1”s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25010A/020A/040A is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 5-4.

Bits BP0 and BP1 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 5-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected		
	BP1	BP0	AT25010A	AT25020A	AT25040A
0	0	0	None	None	None
1 (1/4)	0	1	60-7F	C0-FF	180-1FF
2 (1/2)	1	0	40-7F	80-FF	100-1FF
3 (All)	1	1	00-7F	00-FF	000-1FF

READ SEQUENCE (READ): Reading the AT25010A/020A/040A via the serial output (SO) pin requires the following sequence. After the CS line is pulled low to select a device, the read op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7–A0). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the CS line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address, allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25010A/020A/040A, the Write Protect (WP) pin must be held high and two separate instructions must be executed. First, the device ***must be write enabled*** via the WREN instruction. Then a write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A write instruction requires the following sequence. After the $\overline{\text{CS}}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7–A0) and the data (D7–D0) to be programmed. Programming will start after the $\overline{\text{CS}}$ pin is brought high. The low-to-high transition of the $\overline{\text{CS}}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a read status register (RDSR) instruction. If Bit 0 = “1”, the write cycle is still in progress. If Bit 0 = “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25010A/020A/040A is capable of an 8-byte page write operation. After each byte of data is received, the three low-order address bits are internally incremented by one; the six high-order bits of the address will remain constant. If more than eight bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25010A/020A/040A is automatically returned to the write disable state at the completion of a write cycle.

NOTE: If the $\overline{\text{WP}}$ pin is brought low or if the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state when $\overline{\text{CS}}$ is brought high. A new $\overline{\text{CS}}$ falling edge is required to reinitiate the serial communication.

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing (for Mode 0)

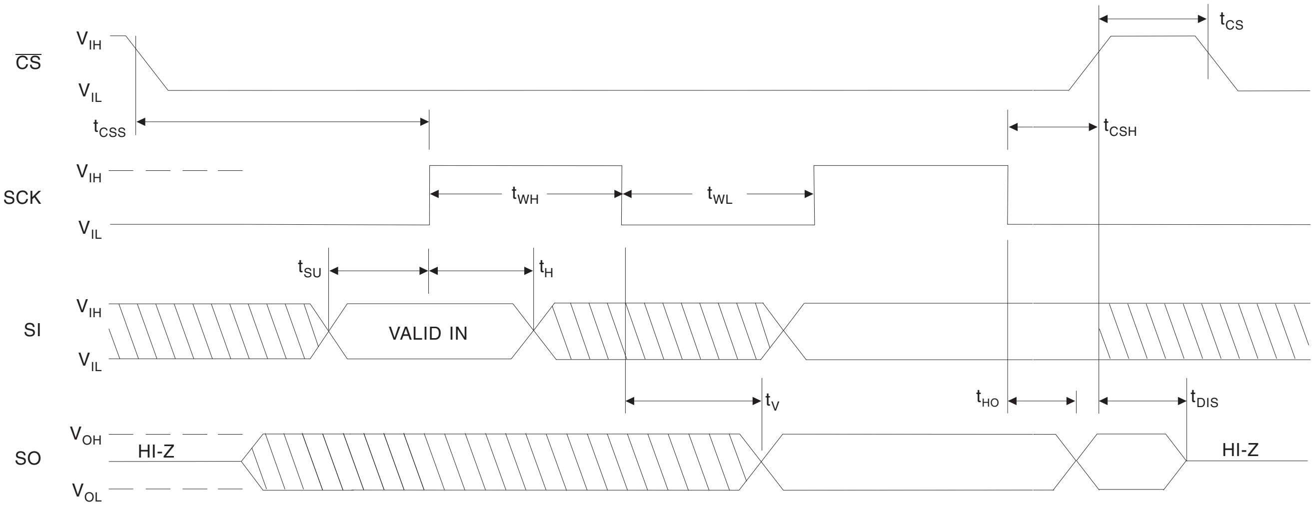


Figure 6-2. WREN Timing

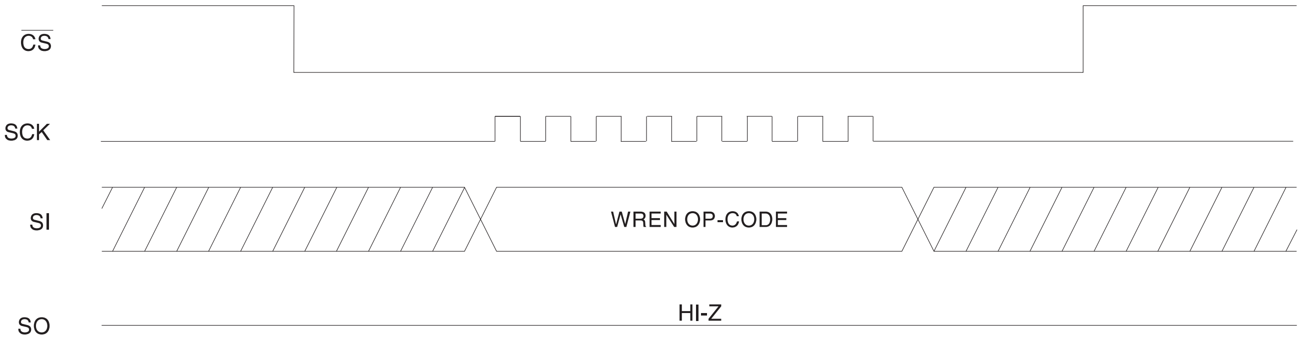


Figure 6-3. WRDI Timing

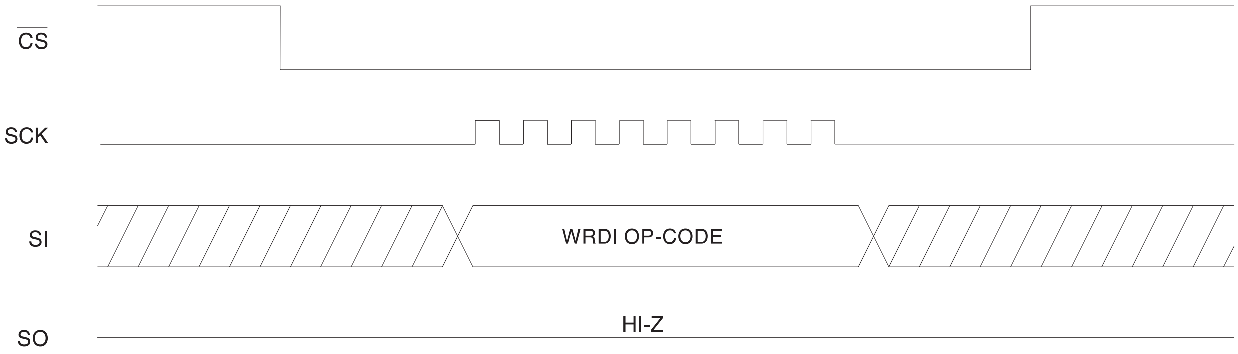


Figure 6-4. RDSR Timing

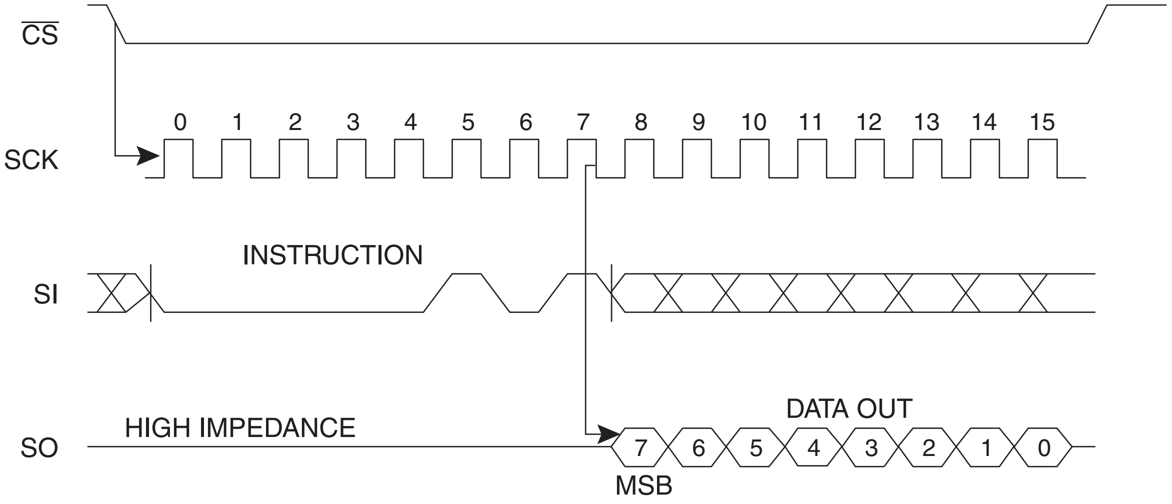


Figure 6-5. WRSR Timing

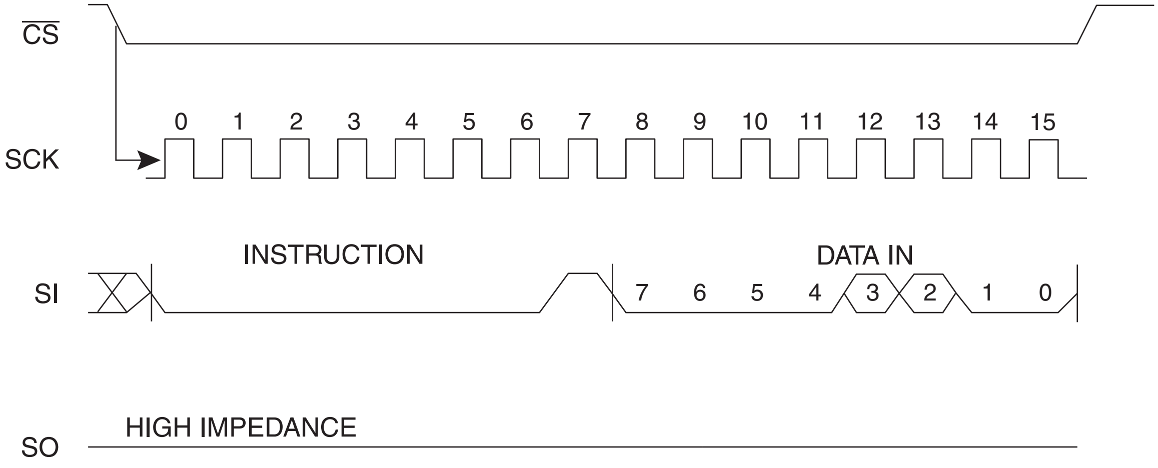


Figure 6-6. READ Timing

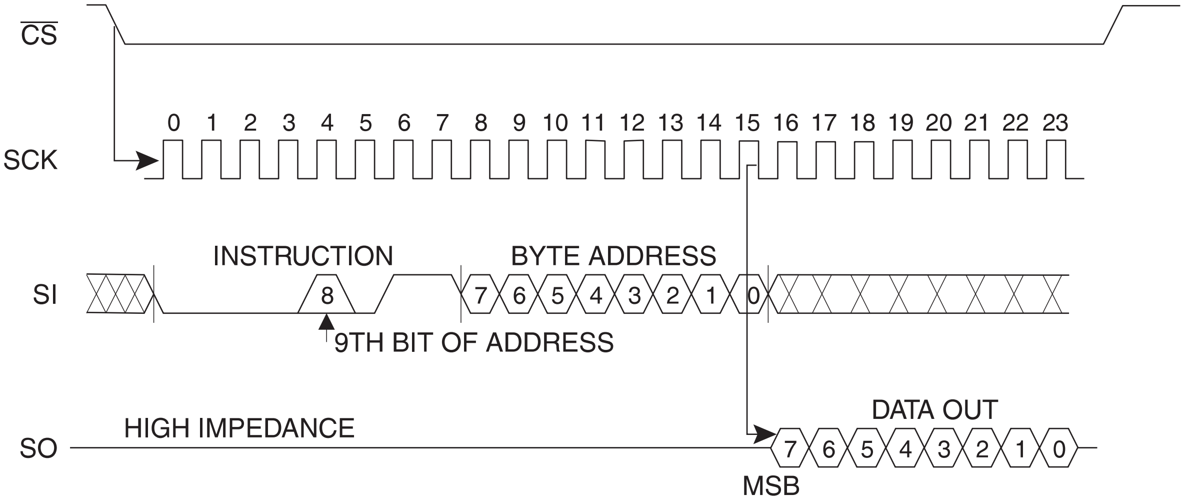
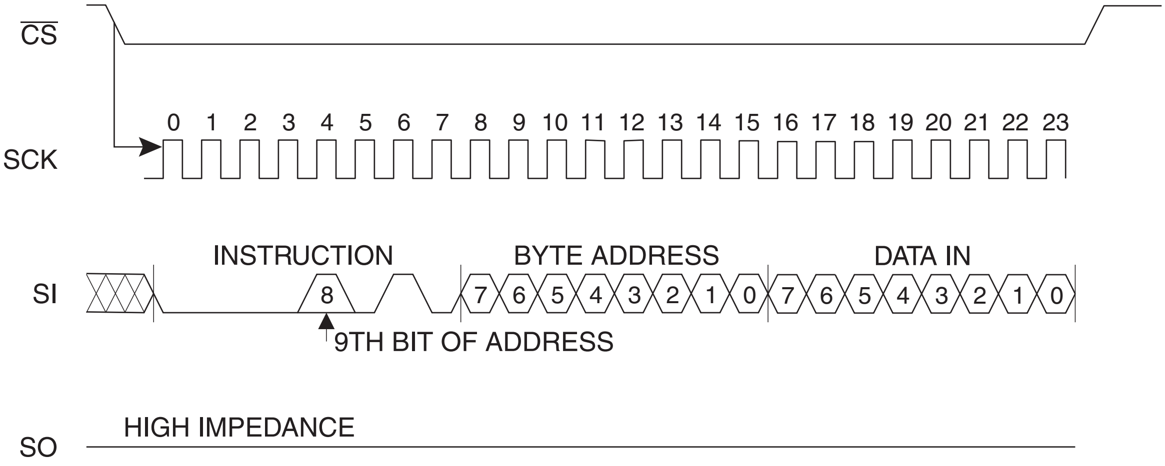


Figure 6-7. WRITE Timing



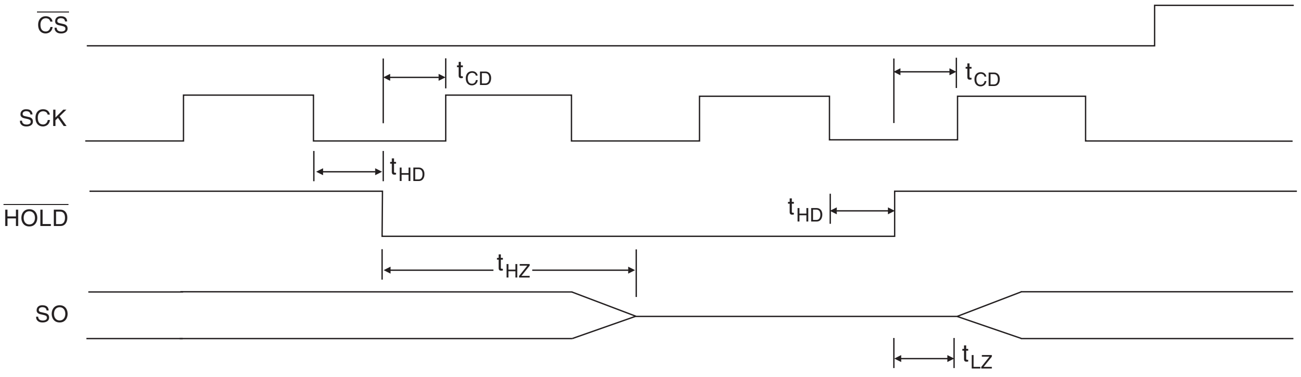


Figure 6-8. $\overline{\text{HOLD}}$ Timing

7. AT25010A Ordering Information

Ordering Code	Package	Operation Range
AT25010AN-10SQ-2.7 AT25010A-10TQ-2.7	8S1 8A2	Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170” Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
–2.7	Low Voltage (2.7V to 5.5V)

8. AT25020A Ordering Information

Ordering Code	Package	Operation Range
AT25020AN-10SQ-2.7 AT25020A-10TQ-2.7	8S1 8A2	Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
–**2.7**	Low Voltage (2.7V to 5.5V)

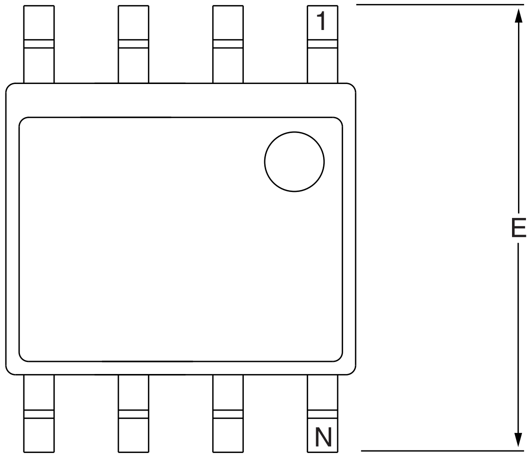
9. AT25040A Ordering Information

Ordering Code	Package	Operation Range
AT25040AN-10SQ-2.7 AT25040A-10TQ-2.7	8S1 8A2	Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)

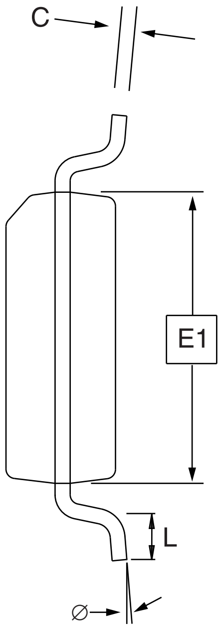
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
–2.7	Low Voltage (2.7V to 5.5V)

10. Packaging Information

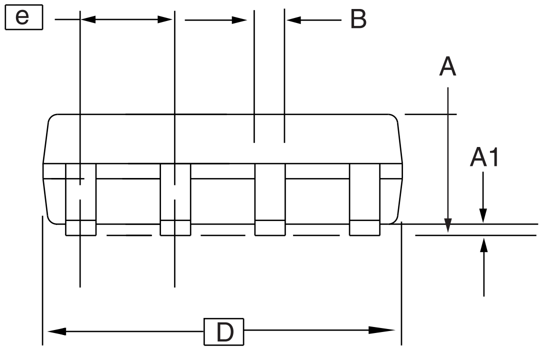
10.1 8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03

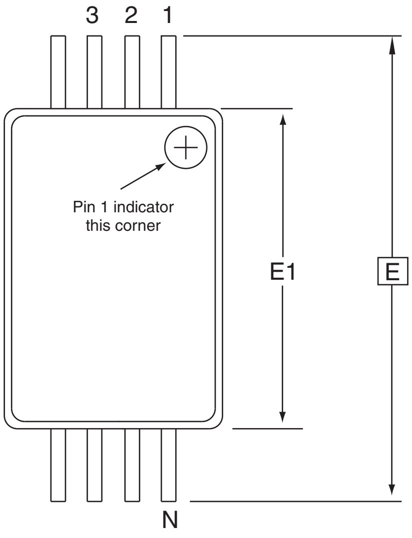
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

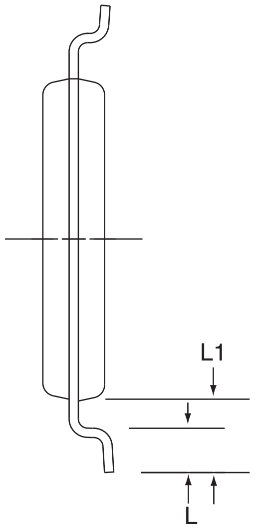
DRAWING NO.
8S1

REV.
B

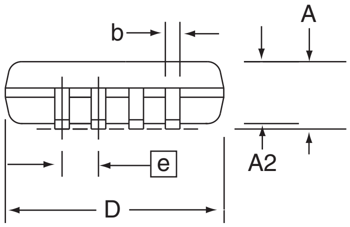
10.2 8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**DRAWING NO.** 8A2	**REV.** B

11. Revision History

Doc. Rev.	Date	Comments
5087E	08/2012	Not recommended for new design. Replaced by AT25010B/020B/040B Automotive.
5087E	06/2009	Correct type error in the Features listed on page 1. NO DEVICE CHARACTERISTICS HAVE CHANGED. The self-timed write cycle is 5 ms max (was 10 ms max only in the Features listed on pg 1). The tWC parameter entry (Write Cycle Time) in Table 4 AC Characteristics on page 4 has always been 5ms.
5087D	3/2007	Corrected package codes on pages 12 and 13
5087C	2/2007	Implemented revision history Removed PDIP package offering Removed PB'd parts

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
s_eeprom@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2009 Atmel Corporation. All rights reserved. Atmel®, Atmel logo and combinations thereof are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be the trademarks of others.

Downloaded from Arrow.com.