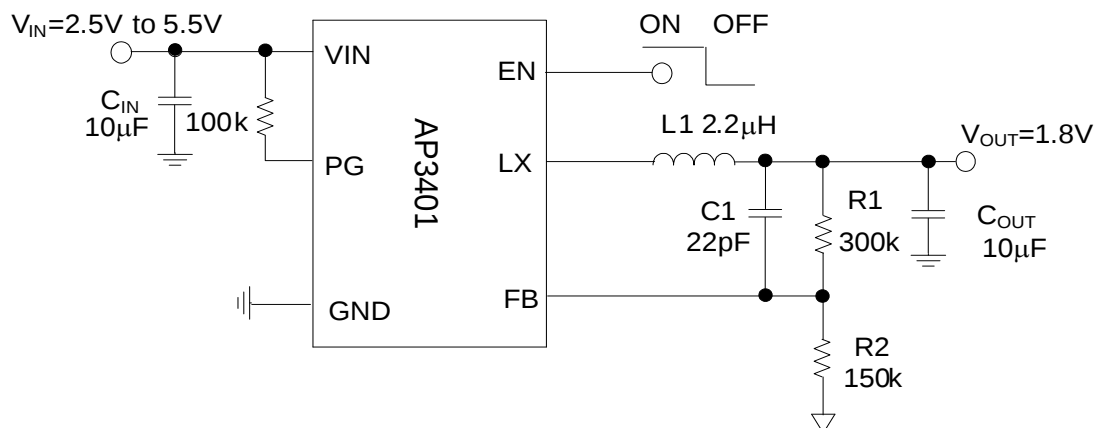


Typical Applications Circuit



Pin Descriptions

Pin Number		Pin Name	Function
TSOT26	U-DFN2020-6 (Type J)		
1	1	EN	Enable control input. Force this pin voltage above 1.5V enables the chip, and below 0.4V shuts down the device
2	5	GND	Ground pin
3	4	LX	The drains of the internal main and synchronous power MOSFET
4	3	VIN	Bias supply. Chip main power supply pin
5	2	PG	Power good indicator, open drain output. PG is pulled up to VIN when the output voltage is within 20% of the regulation level, otherwise it is low
6	6	FB	Feedback voltage to internal error amplifier, the threshold voltage is 0.6V

A(B)
A for TSOT26
B for U-DFN2020-6

Symbol	Parameter	Rating		Unit
V _{IN}	Input Voltage	-0.3 to 6		V
V _{EN}	EN Pin Voltage	-0.3 to V _{IN} +0.3		V
V _{LX}	LX Pin Voltage	-0.3 to V _{IN} +0.3		V
V _{FB}	Feedback Pin Voltage	-0.3 to V _{IN} +0.3		V
P _D	Power Dissipation (on PCB, T _A = +25°C)	TSOT26	0.4	W
		U-DFN2020-6 (Type J)	1.89	
θ _{JA}	Thermal Resistance (Junction to Ambient)	TSOT26	220	°C/W
		U-DFN2020-6 (Type J)	53	
θ _{JC}	Thermal Resistance (Junction to Case, Simulation)	TSOT26	130	°C/W
		U-DFN2020-6 (Type J)	25	
T _J	Operating Junction Temperature	+155		°C
T _{STG}	Storage Temperature	-55 to +150		°C
V _{MM}	ESD (Machine Model)	200		V
V _{HBM}	ESD (Human Body Model)	2000		V
V _{CDM}	ESD (Charge Device Mode)	1000		V

June 2016
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Recommended Operating Conditions

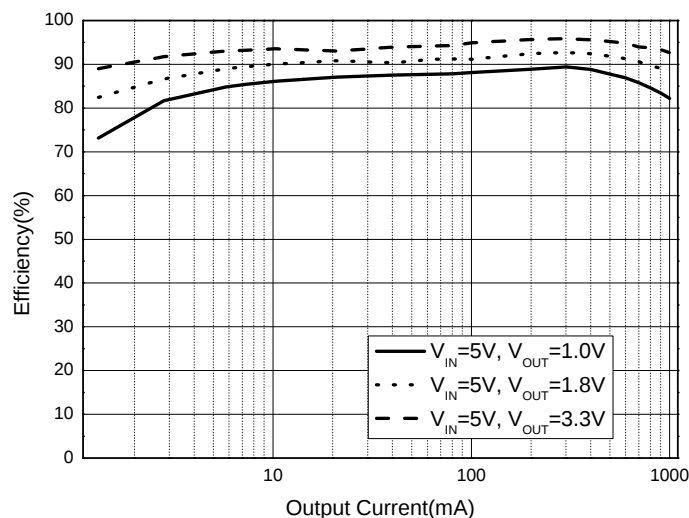
Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage Range	2.5	5.5	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Junction Temperature Range	-40	+125	°C

Electrical Characteristics (@ $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 2.2\mu H$, $C_{IN} = C_{OUT} = 10\mu F$, $T_A = +25^\circ C$, unless otherwise specified.)

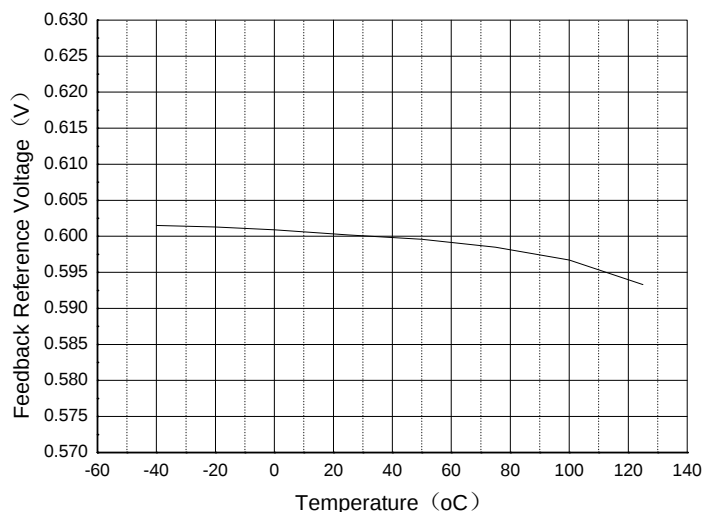
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	–	2.5	–	5.5	V
V_{FB}	Regulated Feedback Voltage	–	0.588	0.6	0.612	V
I_{FB}	FB Leakage Current	$V_{FB} = 1V$	–	–	0.2	μA
I_Q	Quiescent Current	$V_{FB} = 0.65V$	–	40	–	μA
I_{SD}	Shutdown Current	$V_{EN} = 0V$	–	0.1	1	μA
I_{LIM}	Peak Inductor Current	–	1.3	–	–	A
f_{OSC}	Oscillator Frequency	–	–	1.5	–	MHz
$R_{DS(ON)}$	Drain to Source On-state Resistance	$I_{LX} = 100mA$, high side	–	250	–	m Ω
		$I_{LX} = 100mA$, low side	–	170	–	
V_{ENH}	EN High Threshold	–	1.5	–	–	V
V_{ENL}	EN Low Threshold	–	–	–	0.4	V
I_{EN}	EN Leakage Current	$V_{IN} = V_{EN} = 5V$	-1.0	–	1.0	μA
V_{UVLO}	Input UVLO Threshold	–	–	2.4	2.7	V
V_{HYS}	UVLO Hysteresis	–	–	0.1	–	V
–	Maximum Duty Cycle	–	100	–	–	%
R_{DSCH}	Output Discharge Switch On Resistance	–	–	2.1	–	K Ω
T_{OTP}	Over Temperature Protection	–	–	+160	–	°C
T_{OTH}	OTP Hysteresis	–	–	+15	–	°C
t_{SS}	Soft-start Time	–	–	2	–	ms

Performance Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.8\text{V}$, unless otherwise specified.)

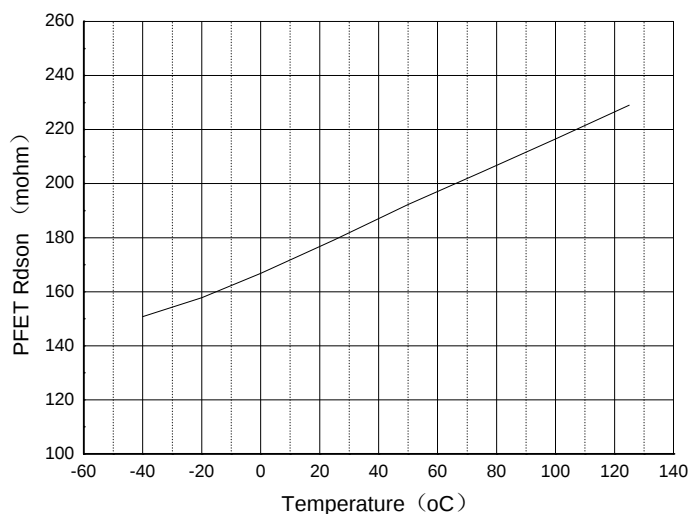
Efficiency vs. Load Current



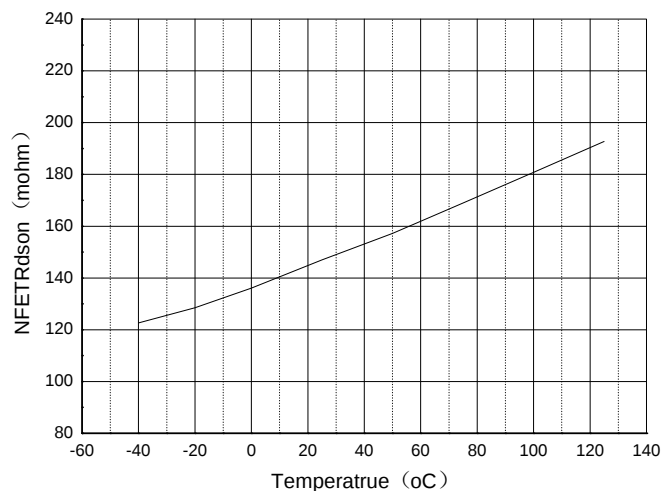
Feedback Reference Voltage vs. Temperature



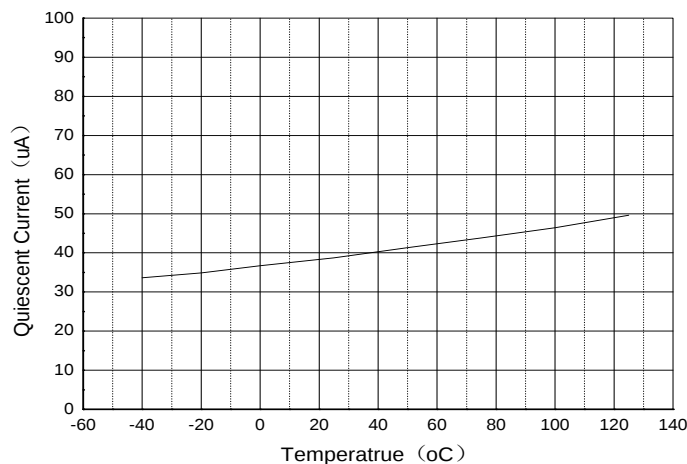
PFET Drain-Source On-State Resistance vs. Temperature



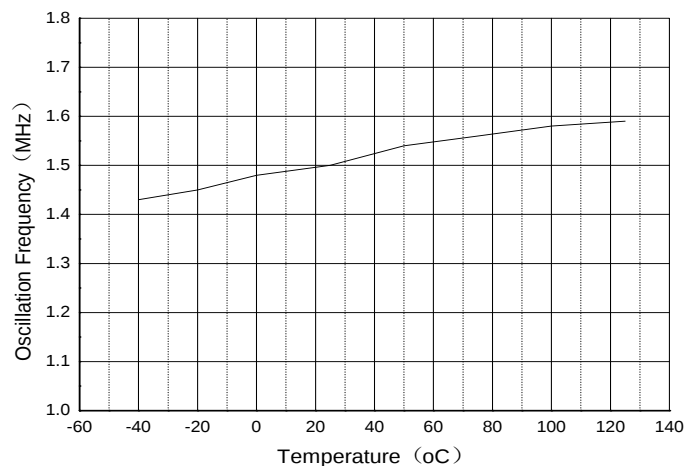
NFET Drain-Source On-State Resistance vs. Temperature



Quiescent Current vs. Temperature

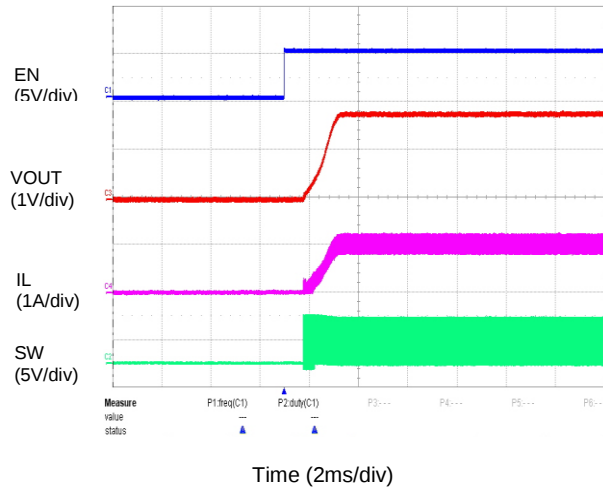


Oscillation Frequency vs. Temperature

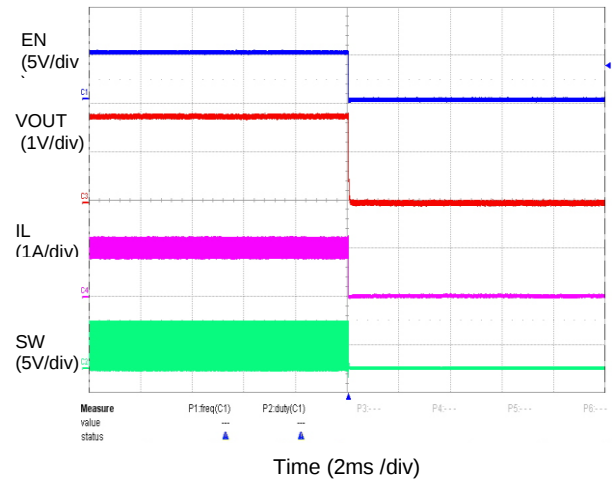


Performance Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $V_{OUT} = 1.8\text{V}$, unless otherwise specified.)

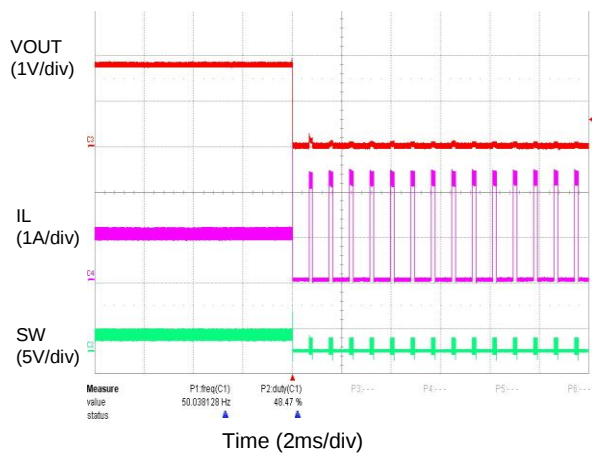
Enable Turn on Characteristic ($I_{OUT}=1\text{A}$)



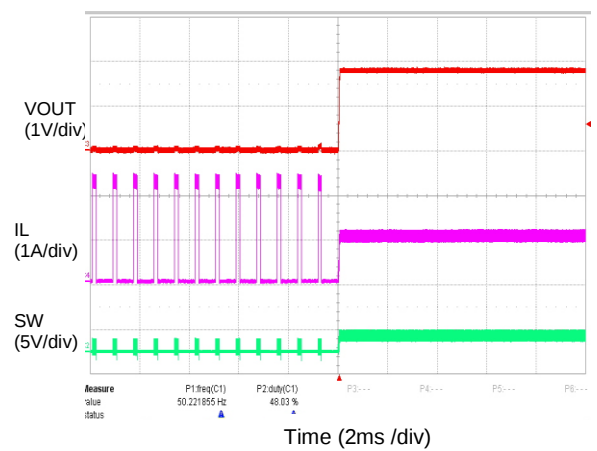
Enable Turn off Characteristic ($I_{OUT}=1\text{A}$)



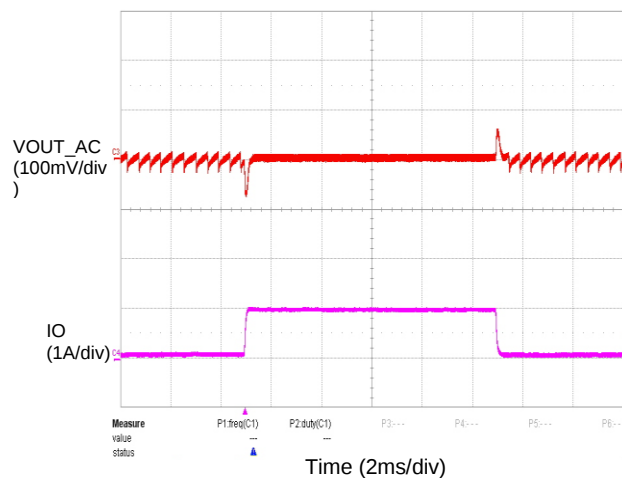
Short Current Protection ($I_{OUT}=1\text{A}$)



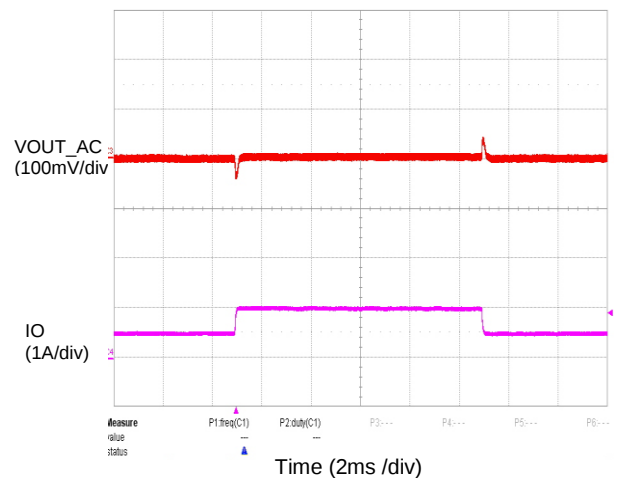
SCP Recovery ($I_{OUT}=1\text{A}$)



Load Transient ($I_{OUT}=0.1\text{A}$ to 1A)



Load Transient ($I_{OUT}=0.5\text{A}$ to 1A)



Application Information

Typical application circuit is shown in the application circuit and for the circuit parameters setting please refers to the following descriptions.

Under Voltage Lockout (UVLO) Circuit

When the V_{IN} drops lower than the UVLO detector threshold, the UVLO circuit starts to operate, V_{REF} stops, and high-side switch and low-side switch built-in switch transistors turn "OFF". As a result, V_{OUT} drops according to the C_{OUT} capacitance value and the load. When the V_{IN} is rising higher than UVLO released voltage, the IC will restart the operation.

Short Circuit Protection and Recovery

When the AP3401 output node is shorted to GND that V_{FB} drops under 0.42V, the AP3401 will enter hiccup mode to protect itself. If short circuit is removed, and V_{FB} rises over 0.42V, the AP3401 recovers to normal operation again. If the AP3401 reaches OCP threshold while short circuit, the AP3401 will enter cycle by cycle current limit mode until the current under OCP threshold.

Power Good

The PG pin output is an open drain MOSFET. The output is pulled low when the FB voltage enters the fault condition by falling below 80% or rising above 120% of the nominal internal reference voltage. When the FB voltage rises to the good condition above 90% or falls below 110% of the internal voltage reference PG output MOSFET is turned off. It is recommended using a pull-up to V_{IN} .

Over Temperature Protection

The internal thermal temperature protection circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When the junction temperature exceeds +160°C, it shuts down the internal control circuit and switching power MOSFET. The AP3401 will restart automatically under the control of soft start circuit when the junction temperature decreases to +145°C.

Input Over Voltage Protection

When input voltage of AP3401 is near 6.25V, the IC will enter Input-Over-Voltage-Protection. It would be shut down and there will be no output voltage in this state. As the input voltage goes down below 6V, it will leave input OVP and recover the output voltage.

Setting the Output Voltage

The output voltage can be adjusted from 1 to 5V using an external resistor divider. Table 1 shows a list of resistor selections for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However the tradeoff is output voltage accuracy due to the bias current in the error amplifier. R1 can be determined by the following equation. Meanwhile, the input capacitor should close to IC for preventing unexpected influences.

$$R1 = R2 \cdot \left(\frac{V_{out}}{0.6} - 1 \right)$$

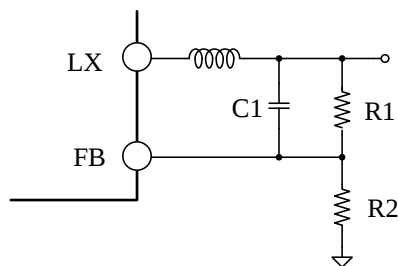
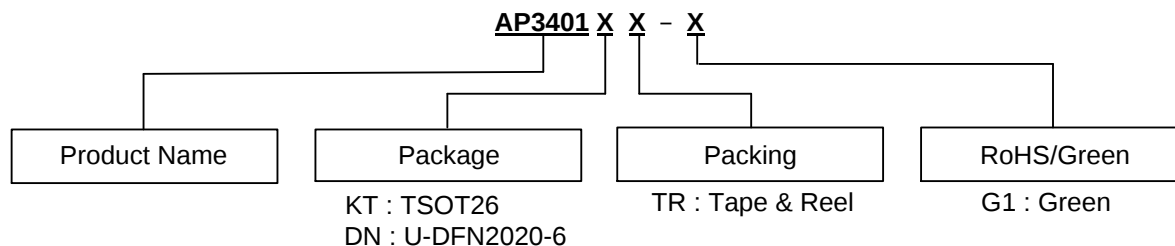


Figure 1. Feedback Divider Network

Out Voltage	R1	R2	C1
1.0V	91k	120k	22pf
1.2V	100k	100k	22pf
1.5V	150k	100k	22pf
1.8V	300k	150k	22pf
2.5V	380k	120k	22pf
2.8V	440k	120k	22pf
3.3V	430k	100k	22pf

Table 1. Resistor Selection for Common Output

Ordering Information

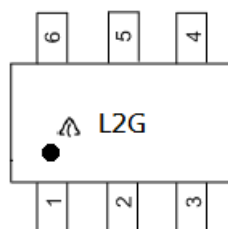


Package	Temperature Range	Part Number	Marking ID	Packing
TSOT26	-40 to +85°C	AP3401KTTR-G1	L2G	3000/Tape & Reel
U-DFN2020-6 (Type J)		AP3401DNTR-G1	CP	3000/Tape & Reel

Marking Information

(1) TSOT26

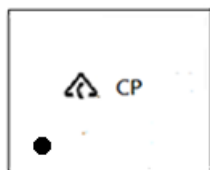
(Top View)



First Line: Logo and Marking ID

(2) U-DFN2020-6 (Type J)

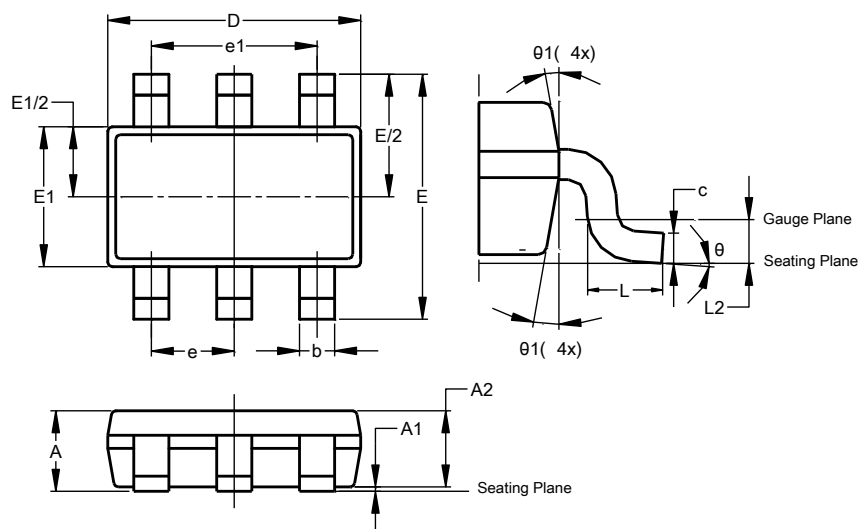
(Top View)



First Line: Logo and Marking ID

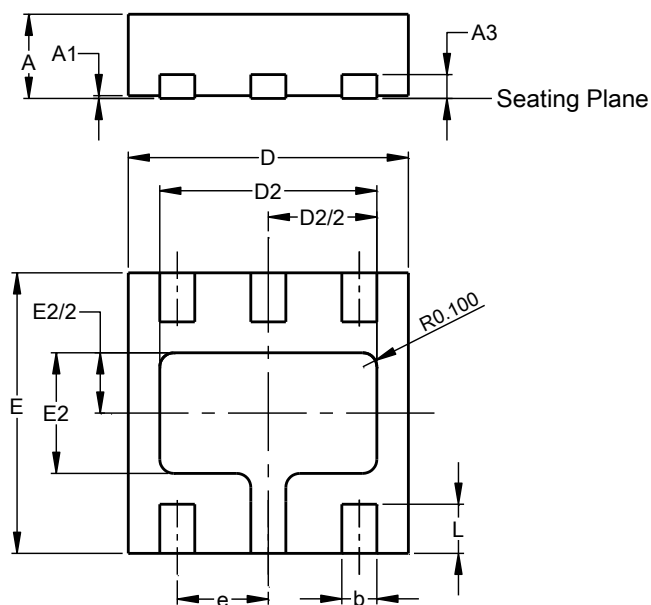
Package Outline Dimensions (All dimensions in mm.)

(1) Package Type: TSOT26



TSOT26			
Dim	Min	Max	Typ
A	—	1.00	—
A1	0.010	0.100	—
A2	0.840	0.900	—
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	—
c	0.120	0.200	—
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	—
L2	0.250 BSC		
θ	0°	8°	4°
$\theta1$	4°	12°	—
All Dimensions in mm			

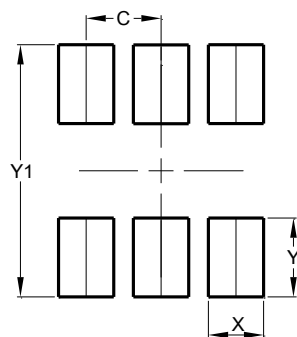
(2) Package Type: U-DFN2020-6 (Type J)



U-DFN2020-6 (Type J)			
Dim	Min	Max	Typ
A	0.50	0.60	—
A1	0.00	0.05	0.03
A3	—	—	0.203
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	1.45	1.65	1.55
E	1.95	2.075	2.00
E2	0.76	0.96	0.86
e	0.65 BSC		
L	0.30	0.40	0.35
All Dimensions in mm			

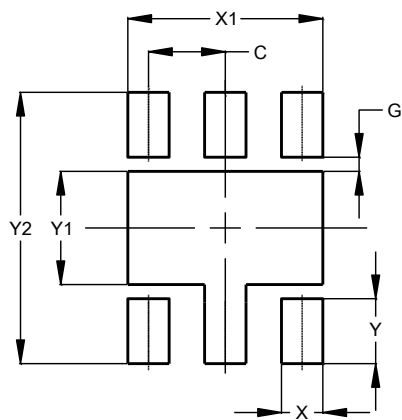
Suggested Pad Layout

(1) Package Type: TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

(2) Package Type: U-DFN2020-6 (Type J)



Dimensions	Value (in mm)
C	0.650
G	0.120
X	0.350
X1	1.650
Y	0.550
Y1	0.960
Y2	2.300

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