ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
+15V Supply (Pins 14)	0 to +16	Volts
–15V Supply (Pin 12)	0 to –16	Volts
+5V Supply (Pins 55, 69)	0 to +6	Volts
–5V Supply (Pin 57, 63)	0 to –6	Volts
Digital Input (Pin 32, 34)	–0.3 to +VDD +0.3	Volts
Analog Input (Pin 4)	–15 to +15	Volts
Lead Temperature (10 seconds)	+300	°C

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-945	0	—	+70	°C
ADS-945EX	–55	—	+125	°C
Thermal Impedance				
θjc	—	10	—	°C/Watt
θca	—	8	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	2" x 4" module			
Weight	2.1 oz. (60 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, V_{DD} = –5.2V, 10MHz sampling rate, and a minimum 10 minute warmup ① unless otherwise specified.)

	+25°C			0 TO +70°C			–55 TO +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±1.25	—	—	±1.25	—	—	±1.25	—	Volts
Input Resistance	300	500	—	300	500	—	300	500	—	kΩ
Input Capacitance	—	10	15	—	10	15	—	10	15	pF
Input Bias Current	—	±3	—	—	±3	—	—	±3	—	µA
DIGITAL INPUT										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	10	50	—	10	50	—	10	50	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (dc input)	—	±0.5	—	—	±0.75	—	—	±1	—	LSB
Differential Nonlinearity (fin = 10kHz)	–0.99	±0.5	+1.5	–0.99	±0.5	+1.5	–0.99	±0.75	+2.5	LSB
Full Scale Absolute Accuracy	—	±0.2	±0.4	—	±0.3	±0.5	—	±0.3	±0.7	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.15	±0.25	—	±0.25	±0.5	—	±0.3	±0.7	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.3	±0.7	%
No Missing Codes (fin = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 1mHz	—	–80	–75	—	—	—	—	—	—	dB
1MHz to 2.5MHz	—	–80	–75	—	—	—	—	—	—	dB
2.5MHz to 5MHz	—	–79	–73	—	–79	–73	—	–75	–69	dB
Total Harmonic Distortion (–0.5dB)										
dc to 1MHz	—	–80	–75	—	—	—	—	—	—	dB
1MHz to 2.5MHz	—	–80	–74	—	—	—	—	—	—	dB
2.5MHz to 5MHz	—	–78	–71	—	–78	–71	—	–75	–68	dB
Signal-to-Noise Ratio (w/o distortion, –0.5dB)										
dc to 1MHz	71	75	—	—	—	—	—	—	—	dB
100kHz to 2.5MHz	71	75	—	—	—	—	—	—	—	dB
2.5MHz to 5MHz	70	74	—	69	74	—	67	72	—	dB
Signal-to-Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	70	77	—	—	—	—	—	—	—	dB
1MHz to 2.5MHz	70	74	—	—	—	—	—	—	—	dB
2.5MHz to 5MHz	69	73	—	69	73	—	65	70	—	dB
Noise	—	110	—	—	110	—	—	110	—	µVrms
Two-Tone Intermodulation Distortion (fin = 2.45MHz, 1.975MHz, fs = 10MHz, –0.5dB)	—	–84	—	—	–84	—	—	–84	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	100	—	—	100	—	—	100	—	MHz
Large Signal (–0.5dB input)	—	50	—	—	50	—	—	50	—	MHz
Feedthrough Rejection (fin = 4.85MHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±650	—	—	±650	—	—	±650	—	V/µs
Aperture Delay Time	—	±8	—	—	±8	—	—	±8	—	ns
Aperture Uncertainty	—	2	—	—	2	—	—	2	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 2.5V step)	—	40	—	—	40	—	—	40	—	ns
Overvoltage Recovery Time ⑤	—	30	100	—	30	100	—	30	100	ns
A/D Conversion Rate	10	—	—	10	—	—	10	—	—	MHz

	+25°C			0 TO +70°C			–55 TO +125°C			
ANALOG OUTPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Reference Output	+9.95	+10	+10.05	+9.95	+10	+10.05	+9.95	+10	+10.05	Volts
Reference Temperature Drift	—	±40	—	—	±40	—	—	±40	—	ppm/°C
Reference Load Current	—	—	2.0	—	—	2.0	—	—	2.0	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.7	—	—	+2.7	—	—	+2.7	—	—	Volts
Logic "0"	—	—	+0.5	—	—	+0.5	—	—	+0.5	Volts
Logic Loading "1"	—	—	–0.4	—	—	–0.4	—	—	–0.4	mA
Logic Loading "0"	—	—	–8	—	—	–8	—	—	–8	mA
Delay, Rising Edge of Start Convert to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Delay, Edge of $\overline{\text{ENABLE}}$ to Output Data Valid/Invalid	—	—	18	—	—	18	—	—	18	ns
Output Coding	Complementary Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges										
+15V Supply	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	–14.25	–15.0	–15.75	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5.2V Supply	–4.95	–5.2	–5.45	–4.95	–5.2	–5.45	–5.1	–5.2	–5.45	Volts
Power Supply Currents ⑥										
+15V Supply	—	+35	+45	—	+35	+45	—	+35	+45	mA
–15V Supply	—	–10	–20	—	–10	–20	—	–10	–20	mA
+5V Supply	—	+290	+320	—	+290	+320	—	+290	+320	mA
–5.2V Supply	—	–350	–390	—	–350	–390	—	–350	–390	mA
Power Dissipation	—	4.0	4.3	—	4.0	4.3	—	4.0	4.3	Watts
Power Supply Rejection	—	—	±0.04	—	—	±0.04	—	—	±0.04	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② The input to the ADS-945 is internally clamped at ±2.3V.

③ An 50ns wide start convert pulse is used for all production testing. For applications requiring less than a 10MHz sampling rate, a wider start convert can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

⑥ Typical +5V and –5.2V current drain breakdowns are as follows:

+5V Analog	= +195mA	–5.2V Analog	= –170mA
+5V Digital	= + 95mA	–5.2V Digital	= –180mA
+5V Total	= +290mA	–5.2V Total	= –350mA

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-945 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. ***The bypass capacitors should be located as close to the unit as possible.***

2. The ADS-945 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. The typical adjustment range is ±0.2%FSR for this circuitry.

   When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. To enable the three-state outputs, apply a logic "0" (low) to $\overline{\text{OUTPUT ENABLE}}$ (pin 34). To disable, apply a logic "1" (high) to pin 34.

4. A passive bandpass filter is used at the input of the A/D for all production testing.

5. The ADS-945's digital outputs should not be directly connected to a noisy data bus. Drive the bus with 573 or 574 type latches and use "low-noise" logic, such as the 74ALS series.

CALIBRATION PROCEDURE (Refer to Figure 2 and Table 1)

Note: Connect pin 18 to ANALOG GROUND (pin 19) for operation without zero/offset adjustment. Connect pin 9 to ANALOG GROUND (pin 8) for operation without gain adjustment.

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-945's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-945, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +½ LSB (+76.3µV).

Gain adjusting is accomplished when all bits are 0's and the LSB just changes from a 0 to a 1. This transition ideally occurs when the analog input is at +full scale minus 1 ½ LSB's (+1.249771V).

Note: Due to inherent system noise, the averaging of several conversions may be needed to accurately adjust both offset and gain to 1LSB of accuracy.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 32) so the converter is continuously converting.
2. Apply +76.3µV to the ANALOG INPUT (pin 4).
3. Adjust the offset potentiometer until the output bits are 10 0000 0000 0000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +1.249771V to the ANALOG INPUT (pin 4).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between 0 and 1.
3. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 1.

   Note: A single +5V supply can be used for both the +5V ANALOG and the +5V DIGITAL. If separate supplies are used, the difference between the two can not exceed 100mV. This also applies to the –5.2V supply requirements.

Datel recommends using ferrite beads to separate the analog and digital supplies (FAIR-RITE # 2643000301).

Table 1. Output Coding

OUTPUT CODING MSB LSB	INPUT RANGE ±1.25V	BIPOLAR SCALE
00 0000 0000 0000	+1.249847	+FS –1 LSB
00 0111 1111 1111	+0.937500	+3/4 FS
00 1111 1111 1111	+0.625000	+1/2FS
01 1111 1111 1111	0.000000	0
10 1111 1111 1111	–0.625000	–1/2FS
11 0111 1111 1111	–0.937500	–3/4FS
11 1111 1111 1110	–1.249847	–FS +1 LSB
11 1111 1111 1111	–1.250000	–FS

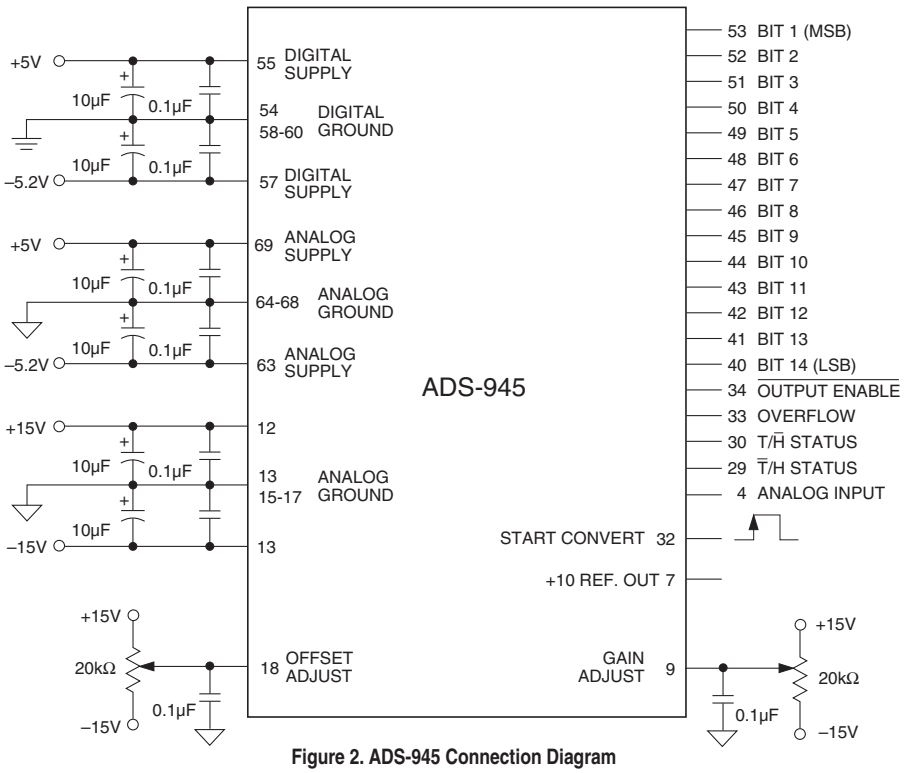


Figure 2. ADS-945 Connection Diagram

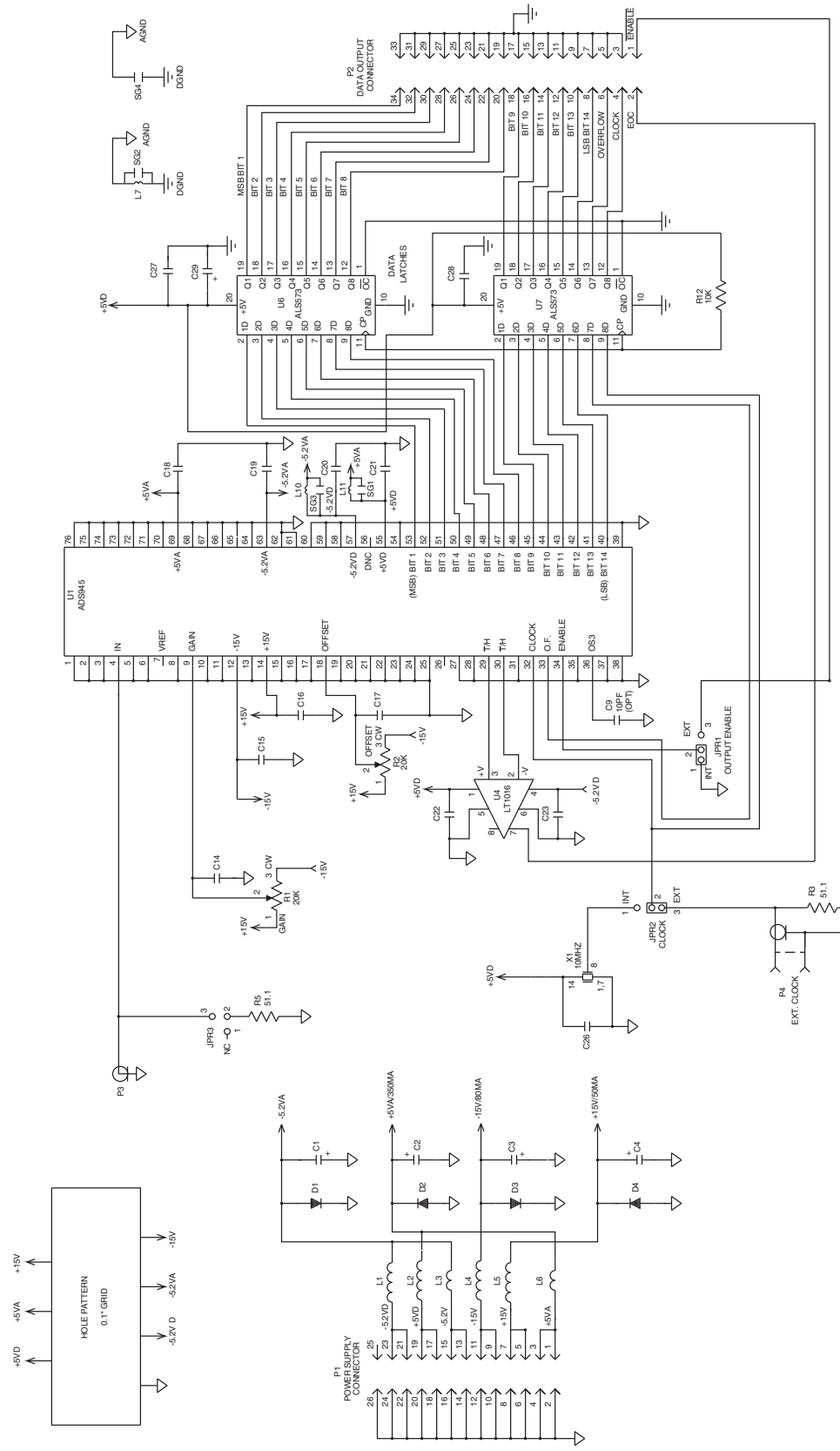


Figure 3. ADS-945 Evaluation Board Schematic (DATEL Dwg. #A-23442)

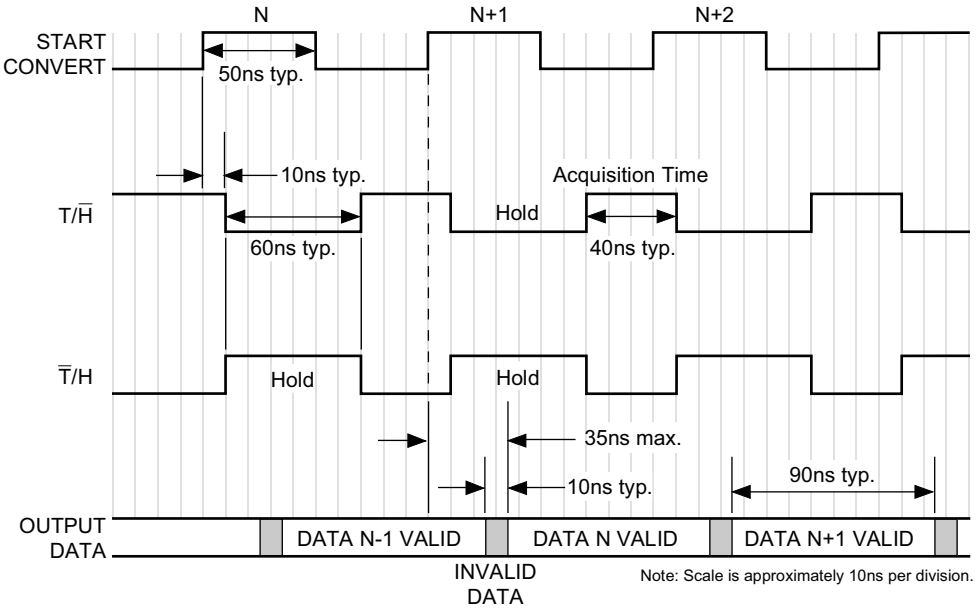


Figure 4. ADS-945 Timing Diagram

TIMING NOTES

1. The ADS-945 is an edge-triggered device requiring no additional external timing signals. The rising edge of the start convert pulse initiates a conversion.
2. A start convert pulse of 50ns is recommended when sampling at 10MHz.
3. The falling edge of the subsequent start convert pulse (N+1) or the rising edge of the N+2 pulse can be used to latch data from conversion N (1 pipeline delay).

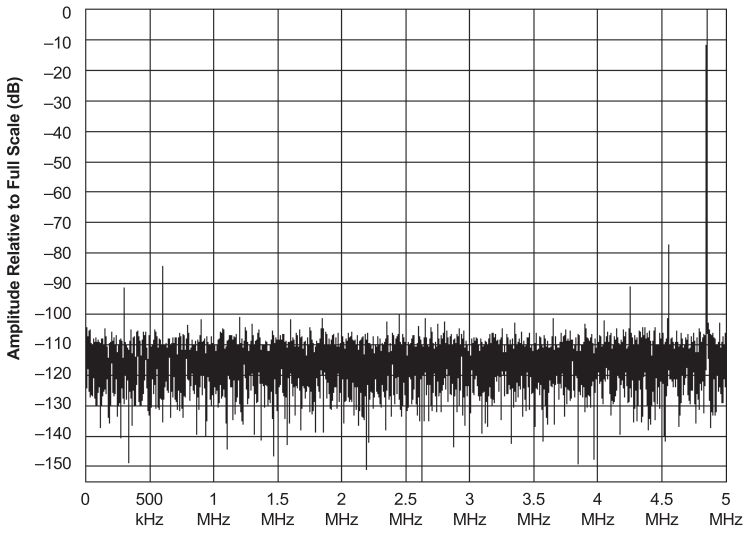
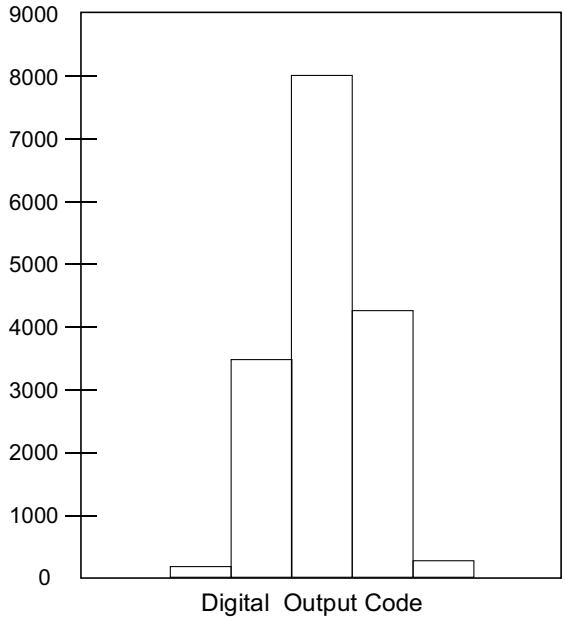


Figure 5. ADS-945 FFT Analysis



This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-945. 16,384 conversions were processed with the input to the ADS-945 tied to analog ground.

Figure 6. ADS-945 Grounded Input Histogram

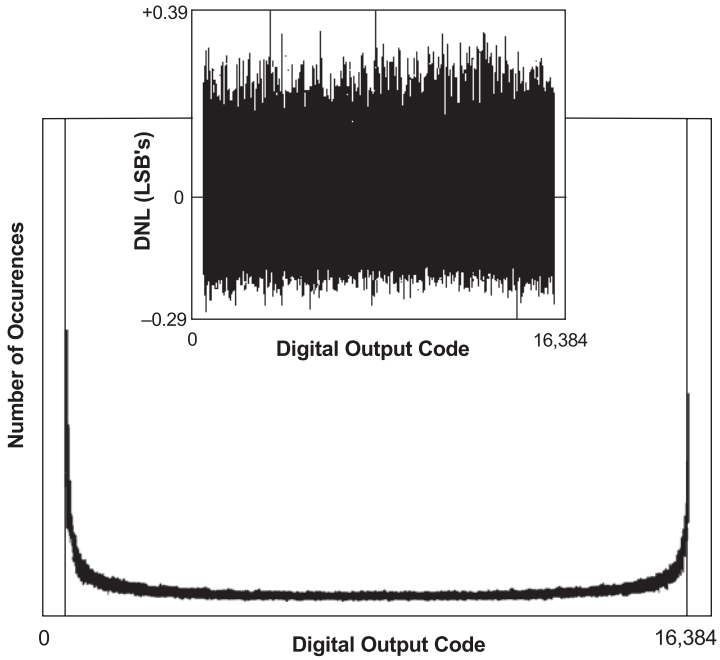


Figure 7. ADS-945 Histogram and Differential Nonlinearity

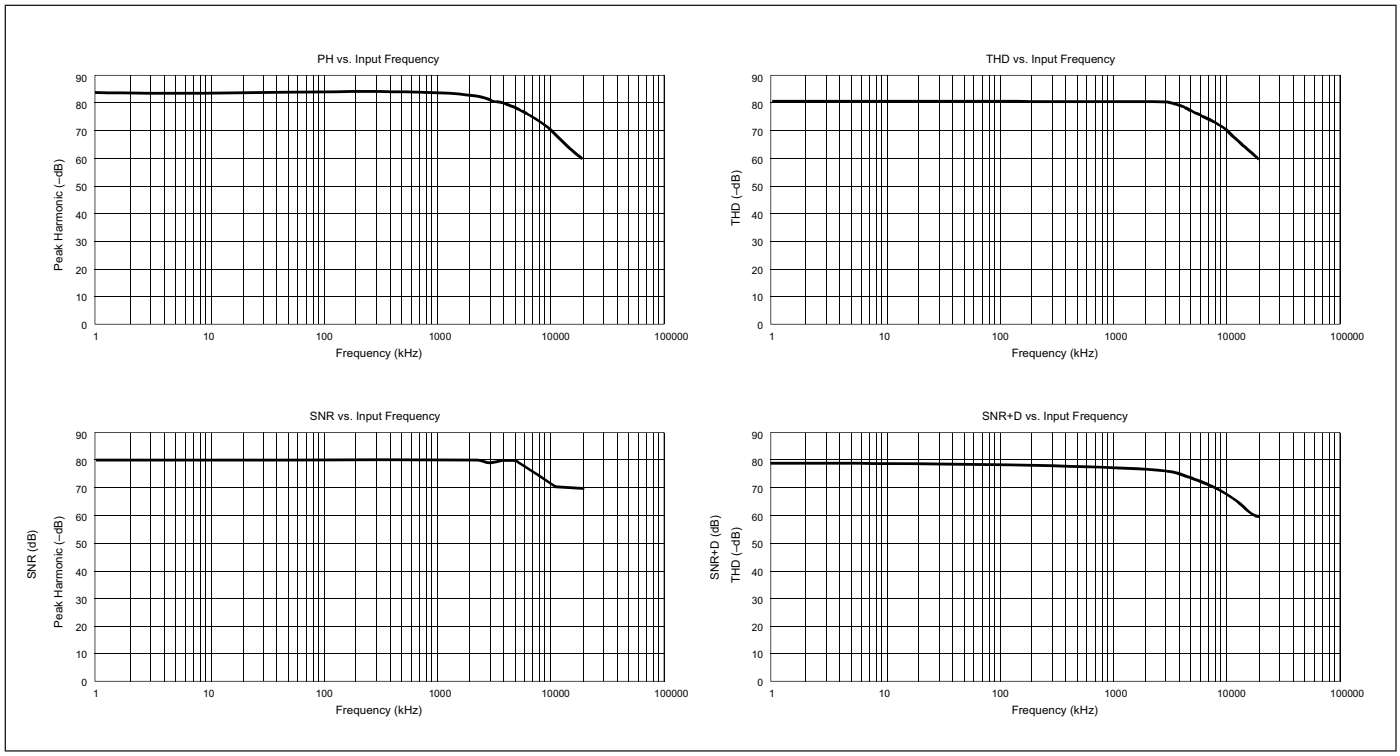
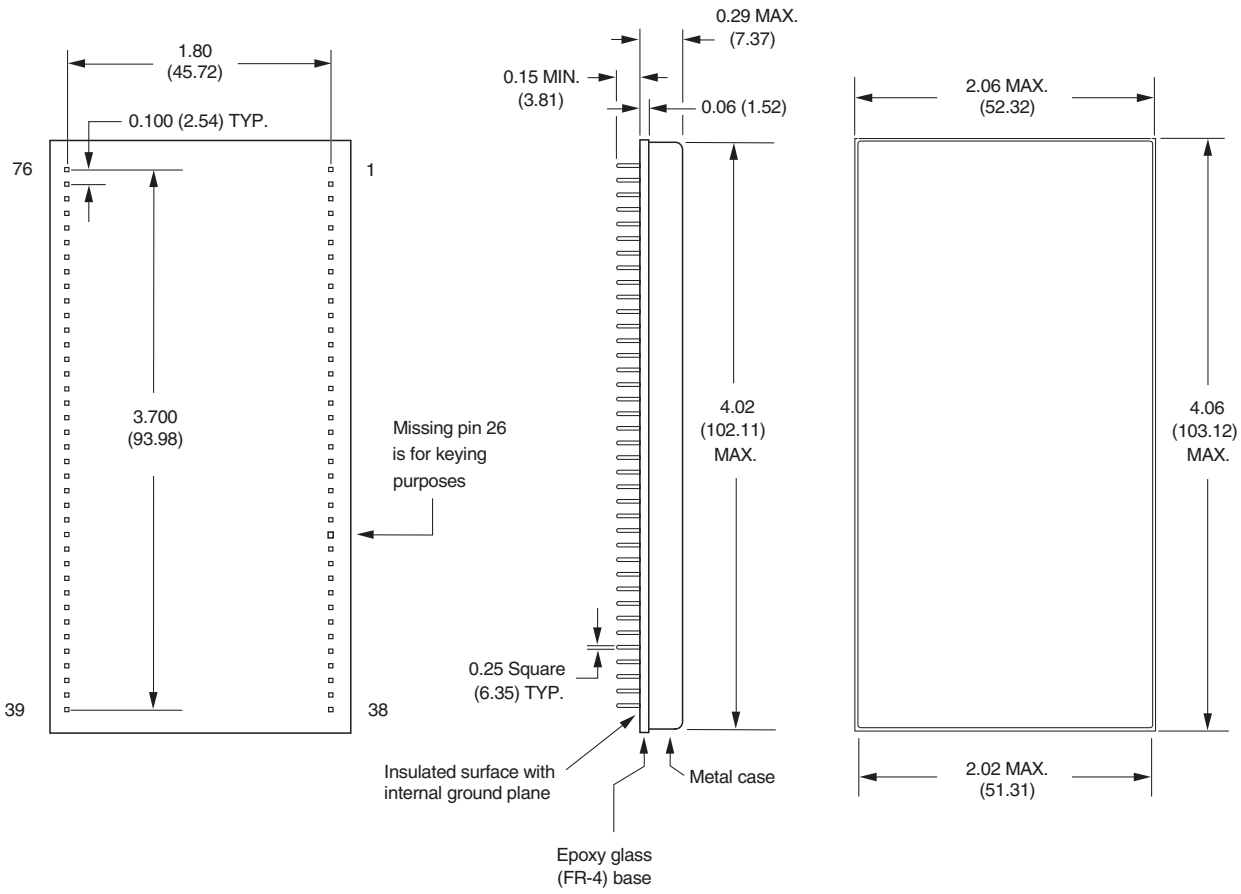


Figure 8. ADS-945 Dynamic Performance vs. Input Frequency at +25°C

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE	ACCESSORIES	
ADS-945	0 to +70°C	ADS-945	Evaluation Board (without ADS-945)
ADS-945EX	–55 to +125°C		

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