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REVISION HISTORY

5/2021—Rev. F to Rev. G
Added VCC Slew Rate Considerations Section ... 12

2/2018—Rev. E to Rev. F
Changes to General Description Section ... 1
Added Note 1, Table 1 ... 4
Changed Device Options Section to Model Options Section ... 15
Changes to Model Options Section ... 15
Added Table 15; Renumbered Sequentially ... 16
Changes to Ordering Guide ... 17

12/2017—Rev. D to Rev. E
Changes to Ordering Guide ... 17

2/2017—Rev. C to Rev. D
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5/2016—Rev. B to Rev. C
Changes to $\overline{MR}$ Pull-Up Resistance Parameter, Table 1 ... 4

12/2015—Rev. A to Rev. B
Changes to Watchdog Timeout Period Parameter, Table 1 ... 4
Changes to Ordering Guide ... 17

4/2015—Rev. 0 to Rev. A
Changes to Reset Threshold Hysteresis Parameter, Table 1 ... 3

1/2015—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2 V to 5.5 V, V_{IN} < V_{CC} + 0.3 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING VOLTAGE RANGE	V_{CC}					
ADM8611, ADM8613, ADM8614		0.9		5.5	V	Guarantees valid $\overline{\text{RESET}}$ output
ADM8612, ADM8615		2		5.5	V	Guarantees valid $\overline{\text{RESET}}$ output
		0.9			V	Guarantees $\overline{\text{RESET}}$ output low
UNDERVOLTAGE LOCKOUT (ADM8612, ADM8615)						
Input Voltage Rising	$UVLO_{RISE}$			1.95	V	
Input Voltage Falling	$UVLO_{FALL}$	1.6			V	
Hysteresis	$UVLO_{HYS}$		90		mV	
INPUT CURRENT						
VCC Quiescent Current	I_{CC}		92	190	nA	V_{CC} = 2 V to 5.5 V, $\overline{\text{RESET}}$ deasserts, V_{WDI} = V_{CC}
				110	nA	V_{CC} = 2 V to 5.5 V, $\overline{\text{RESET}}$ deasserts, V_{WDI} = V_{CC}, T_A = 25°C
VIN Average Input Current			4	8.5	nA	V_{IN} = 2 V, V_{CC} = 5.5 V
			4	32	nA	V_{IN} = 2 V, V_{CC} = 2 V
RESET THRESHOLD VOLTAGE[1]	V_{TH}					Input falling
ADM8611, ADM8613, ADM8614		V_{TH} − 1.3%	V_{TH}	V_{TH} + 1.3%	V	See Table 10 and Table 12
ADM8612, ADM8615		V_{TH} − 1.3%	V_{TH}	V_{TH} + 1.3%	V	V_{TH} ≥ 1.2 V, see Table 11
		V_{TH} − 1.4%	1.1	V_{TH} + 1.4%	V	1.1 V threshold option
		V_{TH} − 1.6%	1	V_{TH} + 1.6%	V	1 V threshold option
		V_{TH} − 1.6%	0.95	V_{TH} + 1.6%	V	0.95 V threshold option
		V_{TH} − 1.7%	0.9	V_{TH} + 1.7%	V	0.9 V threshold option
		V_{TH} − 1.8%	0.85	V_{TH} + 1.8%	V	0.85 V threshold option
		V_{TH} − 1.8%	0.8	V_{TH} + 1.8%	V	0.8 V threshold option
		V_{TH} − 1.9%	0.75	V_{TH} + 1.9%	V	0.75 V threshold option
		V_{TH} − 1.9%	0.7	V_{TH} + 1.9%	V	0.7 V threshold option
		V_{TH} − 2.0%	0.65	V_{TH} + 2.0%	V	0.65 V threshold option
		V_{TH} − 2.1%	0.6	V_{TH} + 2.1%	V	0.6 V threshold option
		V_{TH} − 2.1%	0.55	V_{TH} + 2.1%	V	0.55 V threshold option
		V_{TH} − 2.2%	0.5	V_{TH} + 2.2%	V	0.5 V threshold option
RESET THRESHOLD HYSTERESIS	V_{HYST}					
ADM8611, ADM8613, ADM8614			0.9% × V_{TH}		V	
ADM8612, ADM8615			0.9% × V_{TH}		V	V_{TH} > 1 V
			10.3		mV	V_{TH} ≤ 1 V
$\overline{\text{RESET}}$ TIMEOUT PERIOD	t_{RP}	170	200	240	ms	
PROPAGATION DELAY						
VCC to $\overline{\text{RESET}}$	t_{PD_VCC}					
ADM8611, ADM8613, ADM8614		18	26	37	µs	V_{CC} falling with V_{TH} × 10% overdrive
VIN to $\overline{\text{RESET}}$	t_{PD_VIN}					
ADM8612, ADM8615		13.5	23	35	µs	V_{IN} falling with V_{TH} × 10% overdrive
INPUT GLITCH REJECTION						
VCC Glitch Rejection	t_{GR_VCC}					
ADM8611, ADM8613, ADM8614		13.5	23	32	µs	V_{CC} falling, with V_{TH} × 10% overdrive
VIN Glitch Rejection	t_{GR_VIN}					
ADM8612, ADM8615		13.5	21	27	µs	V_{IN} falling with V_{TH} × 10% overdrive

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT, WDI (ADM8613, ADM8614, ADM8615)						
Watchdog Timeout Period[1]	t_{WD}					
ADM8613, ADM8615		t_{WD} − 13%	t_{WD}	t_{WD} + 19%	sec	
ADM8614		t_{WD} − 13%	t_{WD}	t_{WD} + 19%	sec	Base period, WD_SEL low
		t_{WD} − 13%	t_{WD}	t_{WD} + 19%	sec	Extended period, WD_SEL high
Leakage Current				5	nA	$V_{WDI} = V_{CC} = 5.5$ V
Input Threshold						
High		0.9			V	
Low				0.4	V	
WDI Pulse Width	t_{WPR}	85			ns	High pulse
	t_{WPF}	300			ns	Low pulse
WDI Glitch Rejection			60		ns	
$\overline{\text{RESET}}$ OUTPUT						
Output Voltage Low	V_{RST_OL}			0.4	V	$V_{CC} > 4.25$ V, $I_{SINK} = 6.5$ mA
				0.4	V	$V_{CC} > 2.5$ V, $I_{SINK} = 6$ mA
				0.4	V	$V_{CC} > 1.2$ V, $I_{SINK} = 4.6$ mA
				0.4	V	$V_{CC} > 0.9$ V, $I_{SINK} = 0.9$ mA
Leakage Current				5	nA	$V_{\overline{\text{RESET}}} = V_{CC} = 5.5$ V
MANUAL RESET INPUT, $\overline{\text{MR}}$ (ADM8611, ADM8612, ADM8613, ADM8615)						
V_{IL}				0.4	V	
V_{IH}		0.9			V	
$\overline{\text{MR}}$ Minimum Input Pulse Width		1			µs	
$\overline{\text{MR}}$ Glitch Rejection			0.4		µs	
$\overline{\text{MR}}$ To Reset Delay	t_{D_MR}		0.65		µs	
$\overline{\text{MR}}$ Pull-Up Resistance		300	600	900	kΩ	
WATCHDOG TIMEOUT DISABLE INPUT, WD_DIS (ADM8613, ADM8614)						
V_{IL}				0.4	V	
V_{IH}		0.9			V	
Leakage Current		−5		+5	nA	$V_{WD\_DIS} = 0$ V to V_{CC}
Glitch Rejection			0.1		µs	
WATCHDOG TIMEOUT SELECTION INPUT, WDT_SEL (ADM8614)						
V_{IL}				0.4	V	
V_{IH}		0.9			V	
Leakage Current		−5		+5	nA	$V_{WDT\_SEL} = 0$ V to V_{CC}

[1] Not all device options are available as standard models. See the Ordering Guide for details.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +6 V
WD_DIS	−0.3 V to +6 V
$\overline{\text{RESET}}$	−0.3 V to +6 V
VIN	−0.3 V to +6 V
$\overline{\text{MR}}$	−0.3 V to V_{CC} + 0.3 V
WDI	−0.3 V to V_{CC} + 0.3 V
WDT_SEL	−0.3 V to V_{CC} + 0.3 V
Input/Output Current	10 mA
Storage Temperature Range	−40°C to +150°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on an FR4 board with a minimum footprint.

Table 3.

Package Type	θ_{JA}	Unit
6-Ball WLCSP	105.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

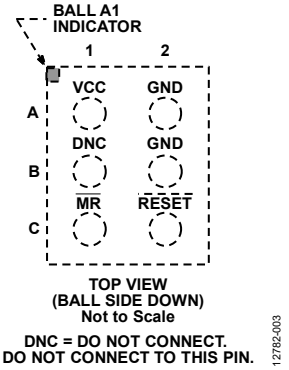

Figure 3. ADM8611 Pin Configuration

Table 4. ADM8611 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8611. It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground. Both GND pins on the ADM8611 must be grounded.
B1	DNC	Do Not Connect. Do not connect to this pin.
B2	GND	Ground. Both GND pins on the ADM8611 must be grounded.
C1	$\overline{MR}$	Manual Reset Input, Active Low.
C2	$\overline{RESET}$	Active Low, Open-Drain $\overline{RESET}$ Output.

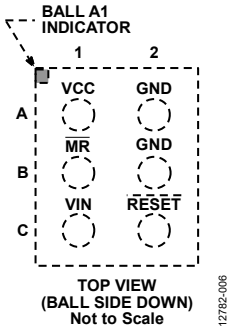

Figure 4. ADM8612 Pin Configuration

Table 5. ADM8612 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is not monitored on the ADM8612. It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground. Both GND pins on the ADM8612 must be grounded.
B1	$\overline{MR}$	Manual Reset Input, Active Low.
B2	GND	Ground. Both GND pins on the ADM8612 must be grounded.
C1	VIN	Low Voltage Monitoring Input. This separate supply input allows the ADM8612 to monitor low voltages on the VIN pin to 0.5 V.
C2	$\overline{RESET}$	Active Low, Open-Drain $\overline{RESET}$ Output.

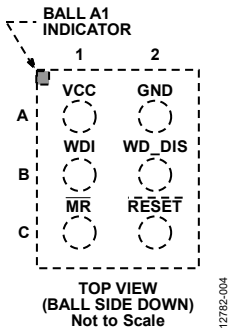

Figure 5. ADM8613 Pin Configuration

Table 6. ADM8613 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8613. It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	WDI	Watchdog Timer Input.
B2	WD_DIS	Watchdog Function Disable Input. Tie this pin high to disable the watchdog function of the device. Connect this pin to ground if it is not used.
C1	$\overline{MR}$	Manual Reset Input, Active Low.
C2	$\overline{RESET}$	Active Low, Open-Drain $\overline{RESET}$ Output.

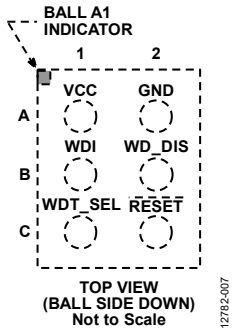

Figure 6. ADM8614 Pin Configuration

Table 7. ADM8614 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8614. It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	WDI	Watchdog Timer Input.
B2	WD_DIS	Watchdog Function Disable Input. Tie this pin high to disable the watchdog function of the device. Connect this pin to ground if it is not used.
C1	WDT_SEL	Watchdog Timeout Selection Input. Pull this pin high to extend the watchdog timeout period of the ADM8614 to 100 sec. Pull this pin low to return the watchdog timeout period to its base value. Toggling WDT_SEL resets the watchdog timer.
C2	$\overline{RESET}$	Active Low, Open-Drain $\overline{RESET}$ Output.

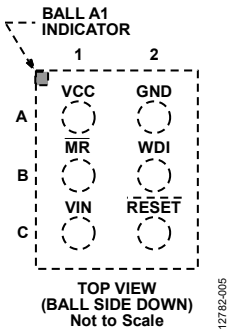

Figure 7. ADM8615 Pin Configuration

Table 8. ADM8615 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is not monitored on the ADM8615. It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	$\overline{MR}$	Manual Reset Input, Active Low.
B2	WDI	Watchdog Timer Input.
C1	VIN	Low Voltage Monitoring Input. This separate supply input allows the ADM8615 to monitor low voltages on the VIN pin to 0.5 V.
C2	$\overline{RESET}$	Active Low, Open-Drain $\overline{RESET}$ Output.

TYPICAL PERFORMANCE CHARACTERISTICS

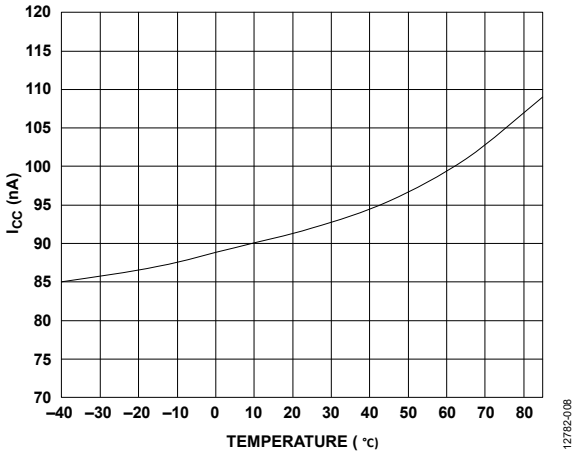

Figure 8. Supply Current (I_{CC}) vs. Temperature

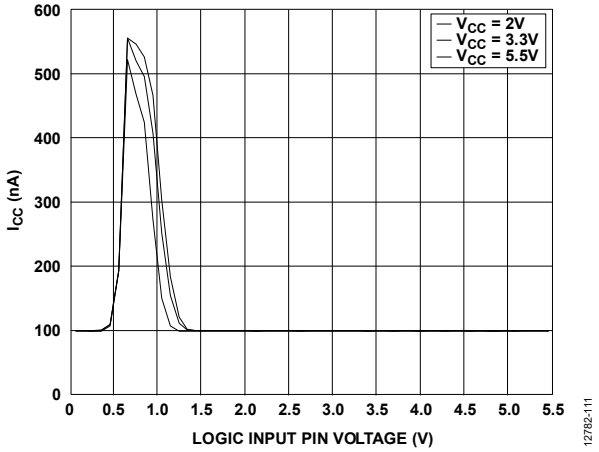

Figure 11. Supply Current (I_{CC}) vs. Logic Input Pin Voltage, with the Exception of the $\overline{MR}$ Pin

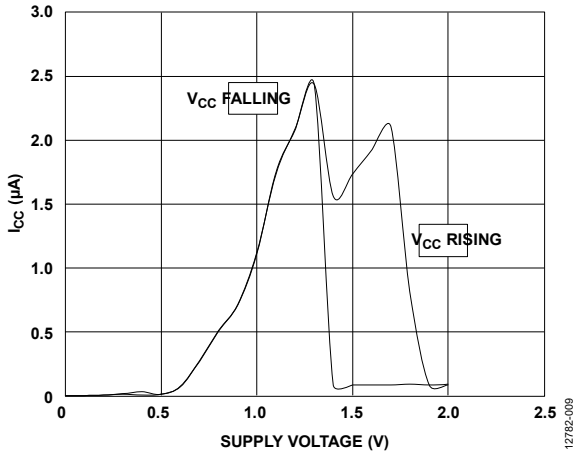

Figure 9. Supply Current (I_{CC}) vs. Supply Voltage, V_{CC} < 2V

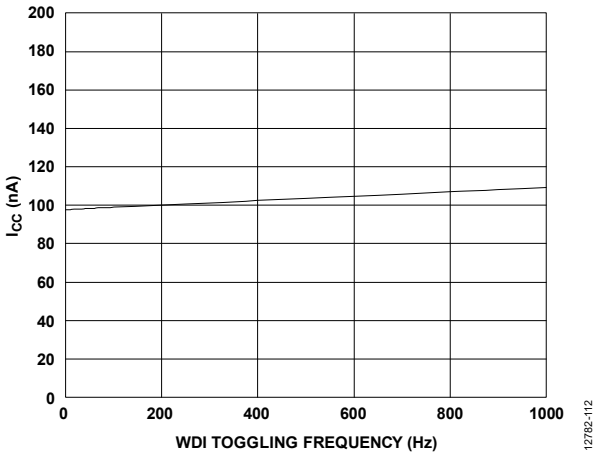

Figure 12. Average Supply Current (I_{CC}) vs. WDI Toggling Frequency, Using a Square Pulse Signal with a Duty Cycle of 50%

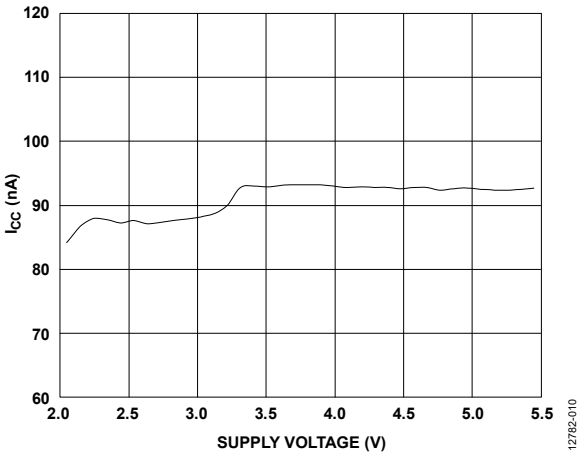

Figure 10. Supply Current (I_{CC}) vs. Supply Voltage

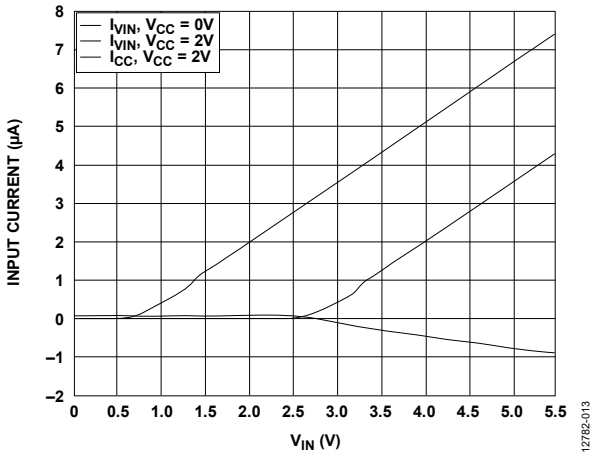

Figure 13. VIN Pin and VCC Pin Input Current vs. V_{IN}

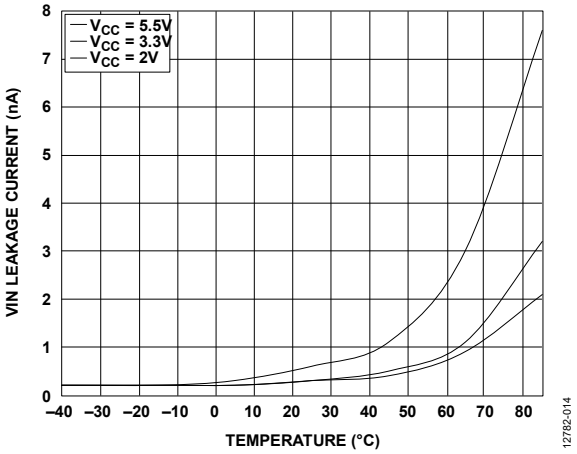

Figure 14. VIN Leakage Current vs. Temperature

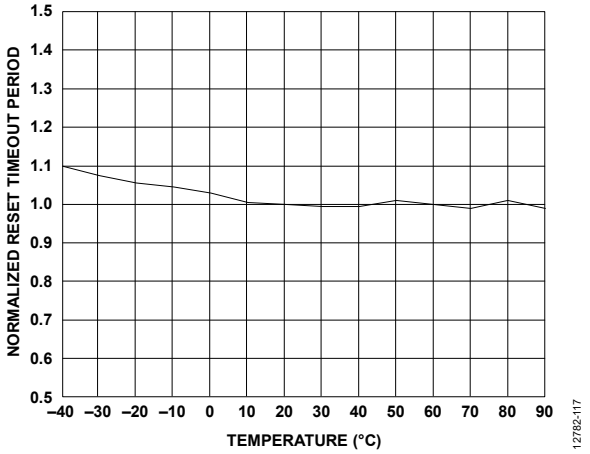

Figure 17. Normalized Reset Timeout Period vs. Temperature

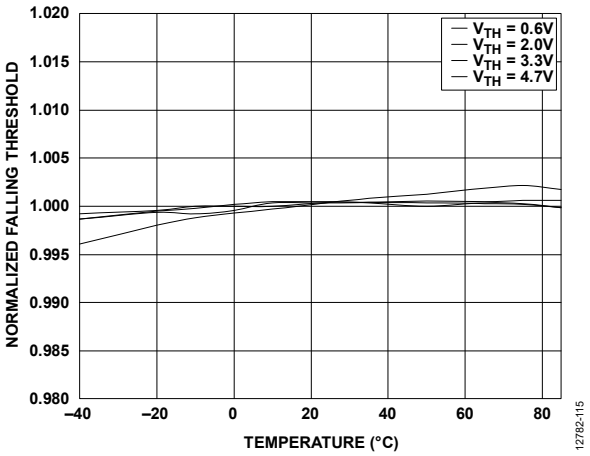

Figure 15. Normalized Falling Threshold vs. Temperature

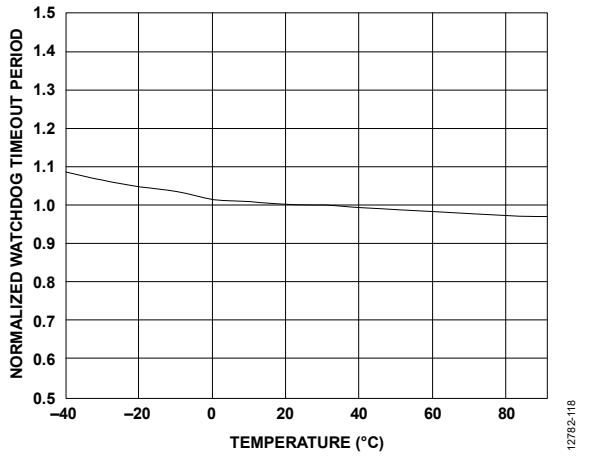

Figure 18. Normalized Watchdog Timeout Period vs. Temperature

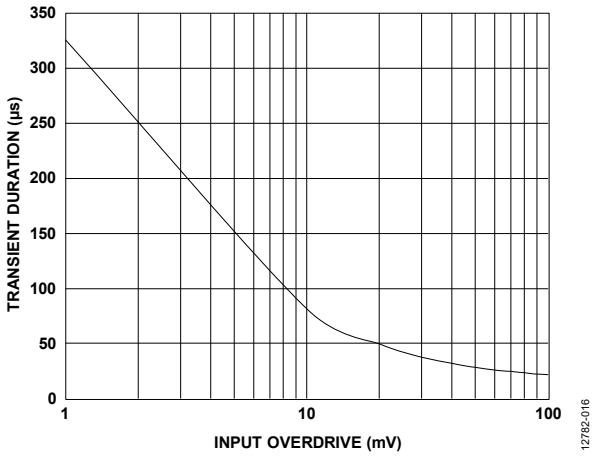

Figure 16. Maximum Transient Duration vs. Input Overdrive, V_{CC} and V_{IN} Falling

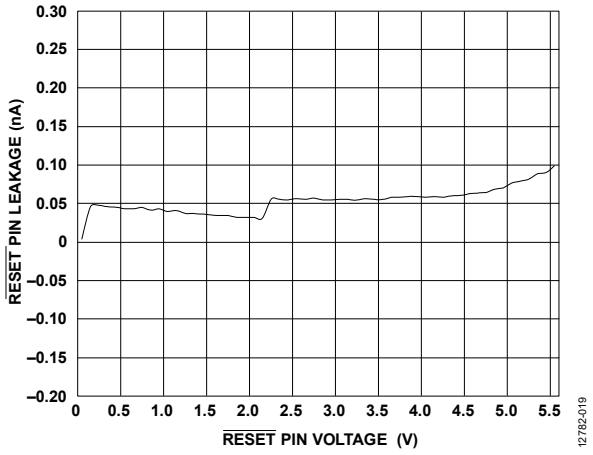

Figure 19. $\overline{RESET}$ Pin Leakage vs. $\overline{RESET}$ Pin Voltage

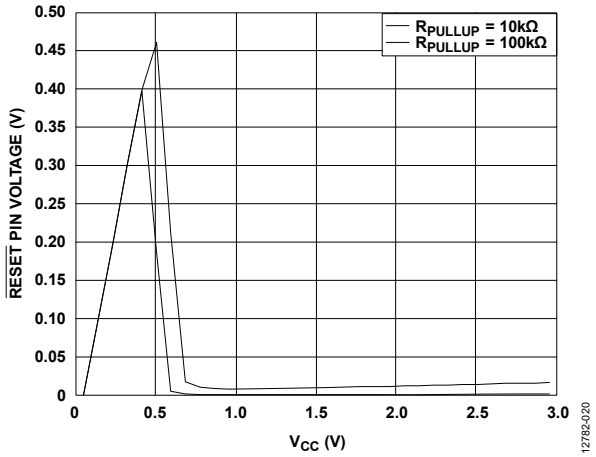

Figure 20. $\overline{RESET}$ Pin Voltage vs. Voltage on VCC
(with the $\overline{RESET}$ Pin Pulled Up to the VCC Pin Through R_{PULLUP})

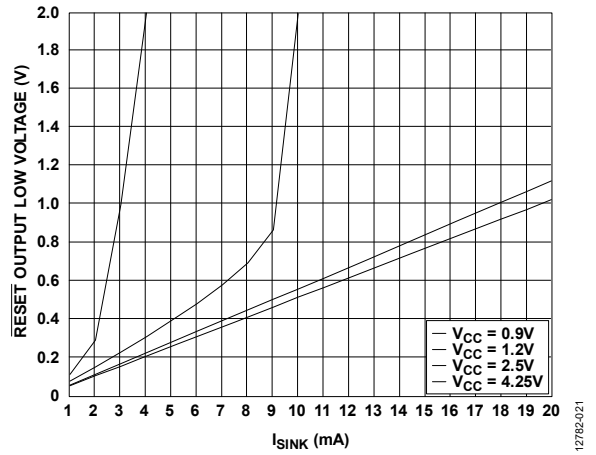

Figure 21. $\overline{RESET}$ Output Low Voltage (V_{RST_OL}) vs. Sink Current (I_{SINK})

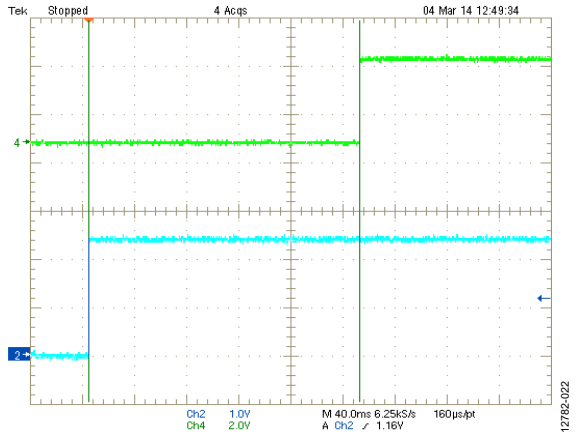

Figure 22. $\overline{RESET}$ Timeout Delay With V_{CC} and V_{IN} Rising

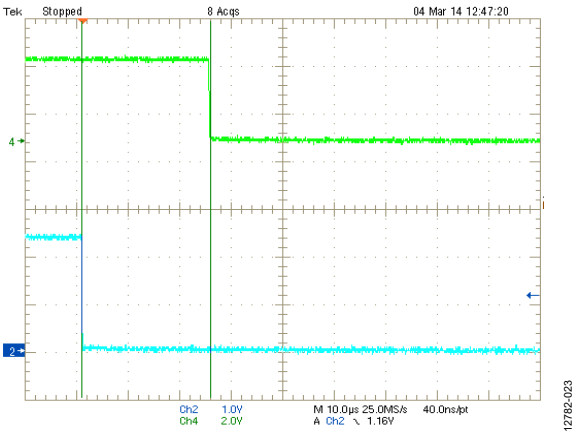

Figure 23. $\overline{RESET}$ Timeout Delay With V_{CC} and V_{IN} Falling

THEORY OF OPERATION

The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 low power voltage supervisors protect the integrity of system operation by ensuring the proper operation during power-up, power-down, and brownout conditions. These devices monitor the input voltage level and compare it against an internal reference. The $\overline{\text{RESET}}$ output asserts whenever the monitored voltage level is below the reference threshold, keeping the processor in a reset state. The $\overline{\text{RESET}}$ output deasserts if the monitored voltage rises above the threshold reference for a minimum period, the active reset timeout period. This ensures that the supply voltage for the processor is raised to an adequate level and stable before exiting reset.

The ultralow supply current makes the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 devices particularly suitable for use in low power, portable equipment.

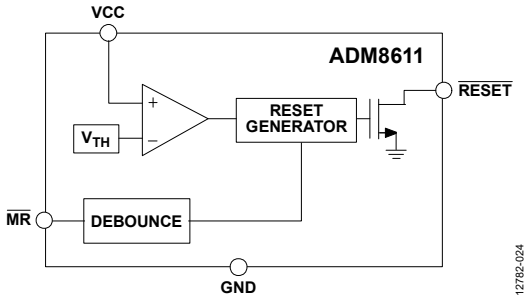

Figure 24. ADM8611 Functional Block Diagram

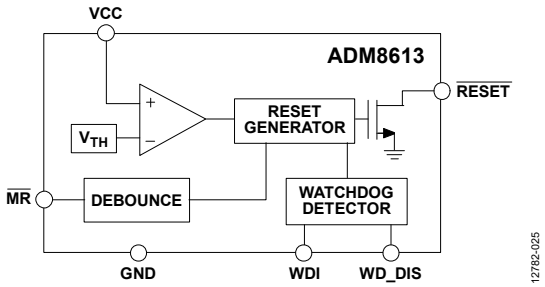

Figure 25. ADM8613 Functional Block Diagram

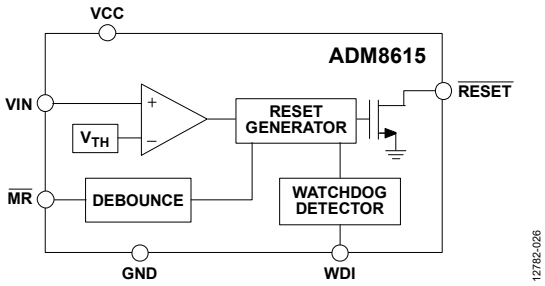

Figure 26. ADM8615 Functional Block Diagram

VOLTAGE MONITORING INPUT

The VCC pin of the ADM8611/ADM8613/ADM8614 acts as both a device power input node and a voltage monitoring input node. The ADM8612 uses separate pins for supply and voltage monitoring to achieve a low voltage monitoring threshold to 0.5 V.

It is recommended to place a 0.1 µF decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.

VCC Slew Rate Consideration

A fast VCC ramp (µs range) on power-up can cause the device to behave in an irregular manner. In applications where a high slew rate on VCC is possible, for example, powering up using a battery pack, it is recommended that an RC filter is used to reduce the slew rate. RC combinations of 3.3 kΩ + 2.2 µF and 1 kΩ + 10 µF have been tested and identified as safe options.

VIN AS AN ADJUSTABLE INPUT

Due to the low leakage nature of the VIN pin, the ADM8612 or ADM8615 can be used as devices with an adjustable threshold. Use an external resistor divider circuit to program the desired voltage monitoring threshold based on the VIN threshold, as shown in Figure 27.

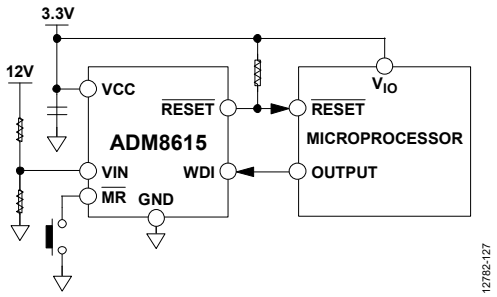

Figure 27. ADM8615 Typical Application Circuit

TRANSIENT IMMUNITY

To avoid unnecessary resets caused by fast power supply transients, an input glitch filter is added to the VCC pin of the ADM8611/ADM8613/ADM8614 and the VIN pin of the ADM8612 and ADM8615 to filter out the transient glitches on these pins.

Figure 16 shows the comparator overdrive (that is, the maximum magnitude of negative going pulses with respect to the typical threshold) vs. the pulse duration without a reset.

RESET OUTPUT

The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 devices all have an active low, open-drain reset output. For the ADM8611/ADM8613/ADM8614, the state of the output is guaranteed to be valid as soon as V_{CC} is greater than 0.9 V. For the ADM8612 and ADM8615, the output is guaranteed to be held low from when V_{CC} = 0.9 V to when the device exits ULVO.

When the monitored voltage falls below its associated threshold, $\overline{\text{RESET}}$ is asserted within 23 µs to 26 µs (typical). Asserting $\overline{\text{RESET}}$ this quickly ensures that the entire system can be reset at once before any part of the system voltage falls below its recommended operating voltage. This system reset can avoid dangerous and/or erroneous operation of a microprocessor-based system.

MANUAL RESET INPUT

The ADM8611, ADM8612, ADM8613, and ADM8615 feature a manual reset input ($\overline{MR}$). Drive $\overline{MR}$ low to assert the reset output. When $\overline{MR}$ transitions from low to high, the reset remains asserted for the duration of the reset timeout period before deasserting. The $\overline{MR}$ input has a 600 kΩ internal pull-up resistor so that the input is always high when unconnected. To drive the $\overline{MR}$ input, use an external signal or a push-button switch to ground; debounce circuitry is integrated on-chip for this purpose. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative going transients of up to 0.4 µs (typical) are ignored. If required, a 0.1 µF capacitor between the $\overline{MR}$ pin and ground provides additional noise immunity.

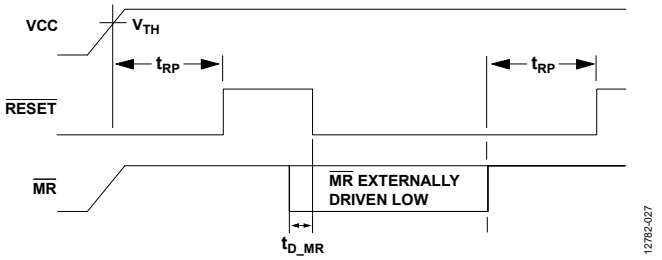

Figure 28. Manual Reset Timing

WATCHDOG TIMER

The ADM8613/ADM8614/ADM8615 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low to high or high to low logic transition on the watchdog input pin (WDI), which detects pulses as short as 85 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), a $\overline{RESET}$ output is asserted. The microprocessor must toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle the WDI pin within the timeout period indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion caused by an undervoltage condition on the VCC pin, WDT_SEL toggling, or $\overline{MR}$ being pulled low. When $\overline{RESET}$ is asserted, the watchdog timer is cleared and does not begin counting again until the $\overline{RESET}$ output is deasserted. The watchdog timer can be disabled by driving the watchdog disable input (WD_DIS) high.

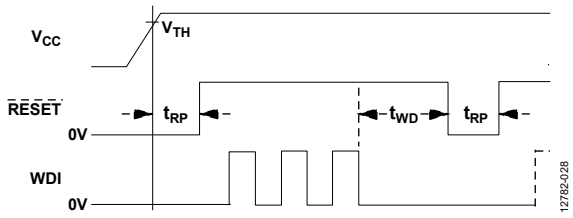

Figure 29. Watchdog Timer Timing

WATCHDOG TIMEOUT SELECT INPUT

Pulling the watchdog timeout select input (WDT_SEL) on the ADM8614 high allows the device to extend its watchdog timeout period from 1.6 sec (typical) to 100 sec (typical). This function allows processors to have a long initialization time during startup.

The long timeout period also enables the processor to stay in low power mode for a long period and work only intermittently, reducing overall system power consumption.

TYPICAL APPLICATION CIRCUITS

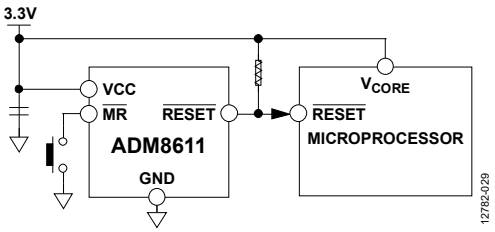

Figure 30. ADM8611 Typical Application Circuit

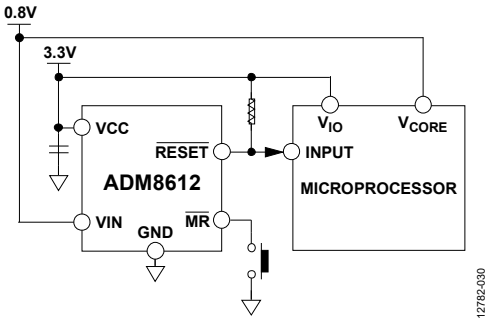

Figure 31. ADM8612 Typical Application Circuit

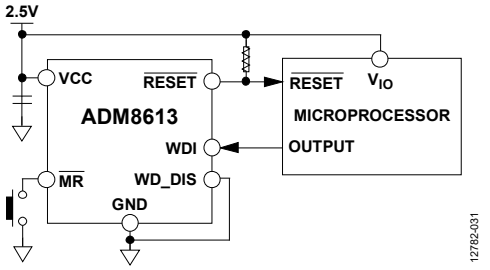

Figure 32. ADM8613 Typical Application Circuit

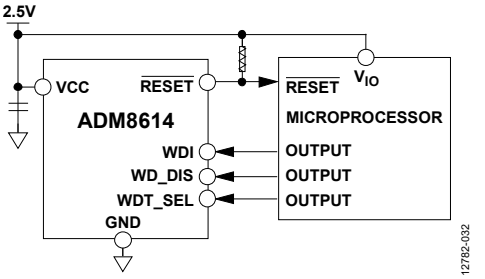

Figure 33. ADM8614 Typical Application Circuit

LOW POWER DESIGN TECHINQUES

With their ultralow power consumption level, the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 are ideal for battery-powered, low power applications where every bit of power matters. In addition to using low power ICs, good circuit design practices can help the user further reduce the overall system power loss.

Digital Inputs

The digital inputs of the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 voltage supervisors are designed with CMOS technology to minimize power consumption. The nature of the CMOS structure leads to an increase of the device I_{CC}, while the voltage level on the input approaches its undefined logic range, as shown in Figure 11. To minimize this effect, follow these recommendations:

- If the digital input does not need to be toggled in a particular design, tie it directly to the VCC or GND pin of the device.
- Push-pull outputs with logic high levels close to the V_{CC} of the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 are the ideal choice for driving the digital signal line.
- Using push-pull outputs with a logic high level near the minimum logic high specification of the digital input is usually not recommended. One exception is if the input is required to be driven high only infrequently for a relatively short period.
- Open-drain outputs with a pull-up resistor to VCC can be used to drive digital signal lines. Open-drain outputs are best suited for driving lines that are required to be driven low only infrequently for a relatively short period.
- The leakage current on both the digital input and the open-drain output determines the size of the pull-up resistor needed and, in turn, decides the power loss through the resistor while driving the input low.
- The $\overline{MR}$ pin on the ADM8611, ADM8612, ADM8613, and ADM8615 features an internal pull-up resistor. The infrequent usage of this pin makes its power loss while driven to logic low negligible.

WDI Input

When the watchdog input (WDI) is driven by a push-pull input/output with a logic high level near the V_{CC} level of the ADM8613/ADM8614/ADM8615, neither a high nor a low input logic causes the system to consume additional current. To reduce the total current consumption, increase the speed of the input transition to the number of transitions. One high to low or low to high transition within the watchdog timeout period is sufficient to prevent the watchdog timer from generating a reset output.

If the watchdog input is driven by a push-pull output with a logic high level near the minimum logic high specification of the digital input, then a logic high input may cause CMOS shoot through and increase the bias current (I_{CC}) of the ADM8613/ADM8614/ADM8615. To minimize the power loss in this setup, use short positive pulses to drive the WDI pin. The ideal pulse width is as small as possible but greater than the required minimum pulse width of the WDI input. One pulse within the watchdog timeout period is sufficient to prevent the watchdog timer from generating a reset output.

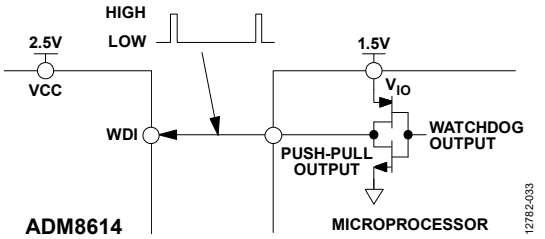

Figure 34. Using a Push-Pull Output with a Lower Logic High Level to VCC, Driving the WDI Pin with Short Positive Pulse to Reduce I_{CC}

Similarly, if an open-drain input/output with a pull-up resistor to VCC is used to drive WDI, a logic low input causes additional current flowing through the pull-up resistor. A short negative pulse technique can minimize the long-term current consumption.

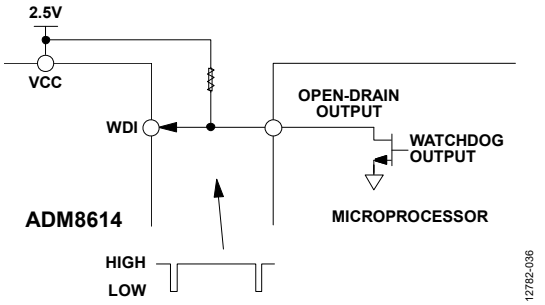

Figure 35. Short Negative Pulse on the WDI Pin to Reduce Leakage Current Through the Pull-Up Resistor

WD_DIS Input

For the ADM8613 and ADM8614, the watchdog disable input (WD_DIS) disables the watchdog function during system prototyping or during power-up to allow extra time for processor initialization.

To disable the watchdog timer function during power-up after a reset deassertion, the processor configures its input/output and drives WD_DIS high within the watchdog timeout period. If there is not enough time to configure the input/output or if an open-drain input/output is used to drive WD_DIS, an external pull-up resistor is required to keep the watchdog function disabled during power-up. Extra current is consumed through the pull-up resistor to enable the watchdog function. The leakage current on both WD_DIS and the input/output that drives it determines the size of the pull-up resistor needed and, in turn, determines the power loss through the resistor while driving the input low.

DEVICE MODEL OPTIONS

The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 include many device options; however, not all options are released for sale. Released options are called standard models and are listed in the Ordering Guide. For the most up to date list of standard models, refer to the Analog Devices website at www.analog.com/supervisory. Contact an Analog Devices sales representative for information on nonstandard models, and be aware that samples and production units have long lead times.

Table 9. Selection Table

Device Number	Low Voltage Monitoring	Manual Reset	Watchdog Timer	Watchdog Disable Input	Watchdog Timeout Selection Input
ADM8611	No	Yes	No	No	No
ADM8612	Yes	Yes	No	No	No
ADM8613	No	Yes	Yes	Yes	No
ADM8614	No	No	Yes	Yes	Yes
ADM8615	Yes	Yes	Yes	No	No

Table 10. ADM8611 V_{CC} Reset Threshold Voltage (V_{TH}) Options (T_A = −40°C to +85°C)

Reset Threshold Number	Min	Typ	Max	Unit
200	1.974	2	2.026	V
220	2.171	2.2	2.229	V
232	2.290	2.32	2.350	V
263	2.596	2.63	2.664	V
280	2.764	2.8	2.836	V
293	2.892	2.93	2.968	V
300	2.961	3	3.039	V
308	3.040	3.08	3.120	V
440	4.343	4.4	4.457	V
463	4.570	4.63	4.690	V

Table 11. ADM8612 and ADM8615 V_{IN} Reset Threshold Voltage (V_{TH}) Options (T_A = −40°C to +85°C)

Reset Threshold Number	Min	Typ	Max	Unit
050	0.489	0.5	0.511	V
055	0.538	0.55	0.562	V
060	0.588	0.6	0.612	V
065	0.637	0.65	0.663	V
070	0.686	0.7	0.714	V
075	0.736	0.75	0.764	V
080	0.785	0.8	0.815	V
085	0.835	0.85	0.865	V
090	0.885	0.9	0.915	V
095	0.935	0.95	0.965	V
100	0.984	1	1.016	V
110	1.084	1.1	1.116	V
120	1.184	1.2	1.216	V
130	1.283	1.3	1.317	V
140	1.382	1.4	1.418	V
150	1.481	1.5	1.520	V
160	1.579	1.6	1.621	V
170	1.678	1.7	1.722	V
180	1.777	1.8	1.823	V
190	1.875	1.9	1.925	V

Table 12. ADM8613 and ADM8614 V_{CC} Reset Threshold Voltage (V_{TH}) Options (T_A = −40°C to +85°C)

Reset Threshold Number	Min	Typ	Max	Unit
232	2.290	2.32	2.350	V
263	2.596	2.63	2.664	V
293	2.892	2.93	2.968	V
308	3.040	3.08	3.120	V
463	4.570	4.63	4.690	V

Table 13. ADM8613 and ADM8615 Watchdog Timeout Options (T_A = −40°C to +85°C)

Watchdog Timeout Period Code	Min	Typ	Max	Unit	Test Condition/Comments
Y	1.4	1.6	1.9	sec	WD_DIS low
Z	22.3	25.6	30.5	sec	WD_DIS low

Table 14. ADM8614 Watchdog Timeout Options (T_A = −40°C to +85°C)

Watchdog Timeout Period Code	Min	Typ	Max	Unit	Test Condition/Comments
Y	1.4	1.6	1.9	sec	WD_DIS low, WDT_SEL low
	87	100	119	sec	WD_DIS low, WDT_SEL high

Table 15. Standard Models

Model	Reset Threshold (V)	Watchdog Timeout (sec)
ADM8611N263ACBZ-R7	2.63	N/A
ADM8611N293ACBZ-R7	2.93	N/A
ADM8612N110ACBZ-R7	1.1	N/A
ADM8613Y232ACBZ-R7	2.32	1.6
ADM8613Z232ACBZ-R7	2.32	25.6
ADM8614Y263ACBZ-R7	2.63	1.6
ADM8615Y100ACBZ-R7	1	1.6
ADM8615Z050ACBZ-R7	0.5	25.6

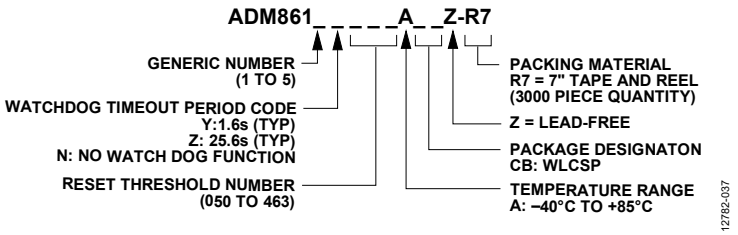

Figure 36. Ordering Code Structure

OUTLINE DIMENSIONS

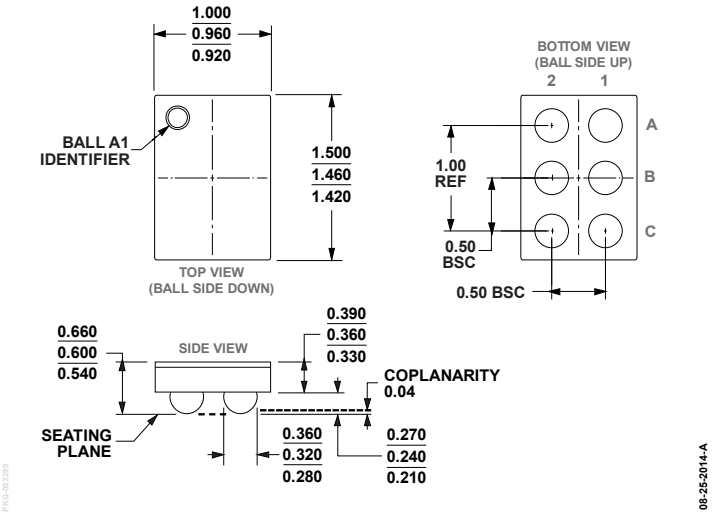

Figure 37. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option	Marking Code
ADM8611N263ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DJ
ADM8611N293ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	ES
ADM8612N110ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DV
ADM8613Y232ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DQ
ADM8613Z232ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	ED
ADM8614Y263ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DR
ADM8615Y100ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DS
ADM8615Z050ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	EG
ADM8611-EVALZ		Evaluation Board		
ADM8612-EVALZ		Evaluation Board		
ADM8613-EVALZ		Evaluation Board		
ADM8614-EVALZ		Evaluation Board		
ADM8615-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 include many device options; however, not all options are released for sale. Released options are called standard models and are listed in the Ordering Guide. For the most up to date list of standard models, refer to the Analog Devices website at www.analog.com/supervisory. Contact an Analog Devices sales representative for information on nonstandard models, and be aware that samples and production units have long lead times.
[3] If ordering nonstandard models, complete the ordering code shown in Figure 36 by inserting the model number, reset threshold, and watchdog timeout.