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REVISION HISTORY

4/05—Rev. B to Rev. C

Updated Format ..... Universal
Removed ADM223, ADM230L, and ADM235L ..... Universal
Changed Hysteresis Level ..... Universal
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Updated Outline Dimensions 14
Changes to Ordering Guide 17

5/01—Rev. A to Rev. B

Edits to Test Conditions/Comments of Specifications 2

1/01—Rev. 0 to Rev. A

Removed ESD information from Features section 1
Changes to Specifications Table 2
Removed ESD information from
Absolute Maximum Ratings section 2

Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 10% (ADM231L, ADM232L, ADM234L, ADM236L, ADM238L, ADM239L, ADM241L); V_{CC} = 5 V ± 5% (ADM233L and ADM237L); V+ = 7.5 V to 13.2 V (ADM231L and ADM239L); C1 to C4 = 1.0 µF ceramic. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Swing	±5	±9		V	All transmitter outputs loaded with 3 kΩ to ground
V_{CC} Power Supply Current		2.5	6.0	mA	No load, (ADM232L only)
		3.5	13	mA	No load
V+ Power Supply Current		1.5	4	mA	No load, V+ = 12 V (ADM231L and ADM239L only)
Shutdown Supply Current		1	10	µA	
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Logic Pull-Up Current		12	25	µA	
RS-232 Input Voltage Range[1]	−30		+30	V	T_{IN} = 0 V
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.6	2.4	V	
RS-232 Input Hysteresis		0.65		V	
RS-232 Input Resistance	3	5	7	kΩ	T_A = 0°C to 85°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
TTL/CMOS Output Leakage Current		+0.05	±10	µA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		250		ns	ADM236L, ADM239L, ADM241L (Figure 31, C_L = 150 pF)
Output Disable Time (T_{DIS})		50		ns	ADM236L, ADM239L, ADM241L (Figure 31, R_L = 1 kΩ)
Propagation Delay		0.3		µs	RS-232 to TTL
Transition Region Slew Rate		8		V/µs	R_L = 3 kΩ, C_L = 2500 pF, measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short-Circuit Current		±10		mA	

[1] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +14 V
V−	+0.3 V to −14 V
Input Voltages	
T_{IN}	−0.3 V to (V_{CC} + 0.3 V)
R_{IN}	±30 V
Output Voltages	
T_{OUT}	(V+, +0.3 V) to (V−, −0.3 V)
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short-Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
N-14 PDIP (Derate 10 mW/°C above 70°C)	800 mW
N-16 PDIP (Derate 10.5 mW/°C above 70°C)	840 mW
N-20 PDIP (Derate 11 mW/°C above 70°C)	890 mW
N-24-1 PDIP (Derate 13.5 mW/°C above 70°C)	1000 mW
R-16 SOIC (Derate 9 mW/°C above 70°C)	760 mW
R-24 SOIC (Derate 12 mW/°C above 70°C)	850 mW
R-28 SOIC (Derate 12.5 mW/°C above 70°C)	900 mW
RS-28 SSOP (Derate 10 mW/°C above 70°C)	900 mW
Q-14 CERDIP (Derate 10 mW/°C above 70°C)	720 mW
Q-16 CERDIP (Derate 10 mW/°C above 70•C)	800 mW
Q-24 CERDIP (Derate 12.5 mW/°C above 70°C)	1000 mW
Thermal Impedance, θ_{JA}	
N-14 PDIP	140°C/W
N-16 PDIP	135°C/W
N-20 PDIP	125°C/W
N-24-1 PDIP	120°C/W
R-16 SOIC	105°C/W
R-24 SOIC	85°C/W
R-28 SOIC	80°C/W
RS-28 SSOP	100°C/W
Q-14 CERDIP	105°C/W
Q-16 CERDIP	100°C/W
Q-24 CERDIP	55°C/W
Operating Temperature Range	
Commercial (J Version)	0°C to 70°C
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

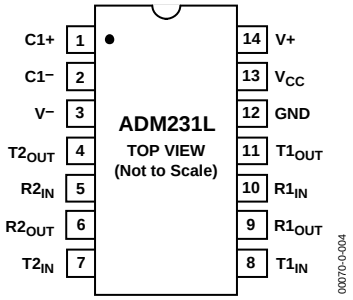


Figure 2. ADM231L PDIP Pin Configuration

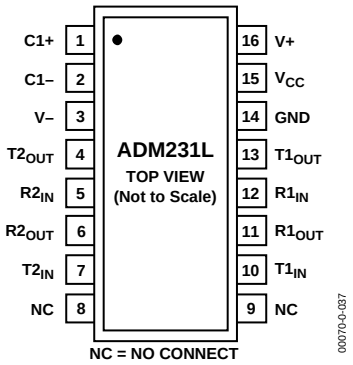


Figure 3. ADM231L SOIC Pin Configuration

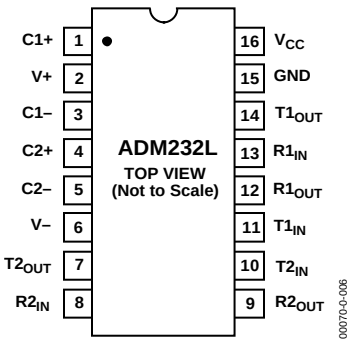


Figure 4. ADM232L PDIP/CERDIP/SOIC Pin Configuration

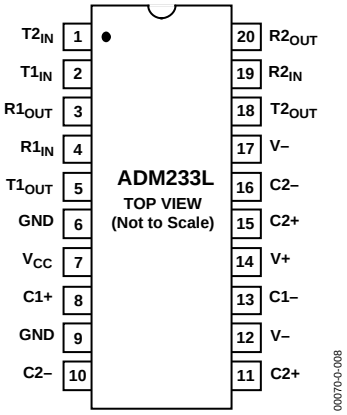


Figure 5. ADM233L PDIP Pin Configuration

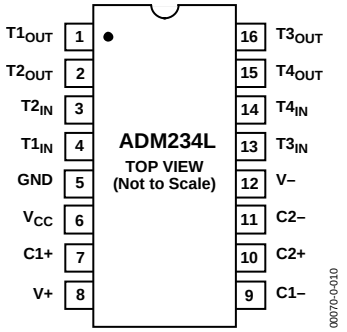


Figure 6. ADM234L PDIP/CERDIP/SOIC Pin Configuration

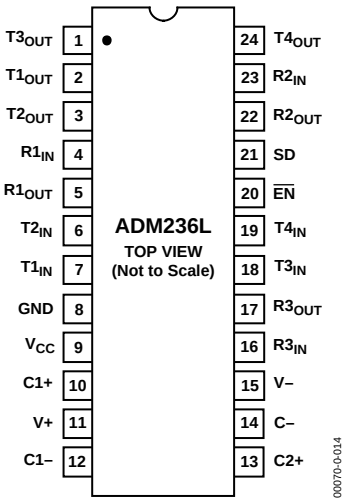


Figure 7. ADM236L PDIP/SOIC Pin Configuration

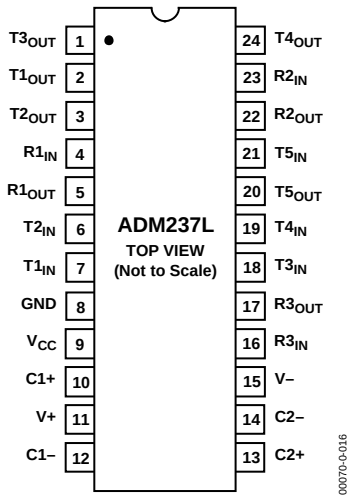


Figure 8. ADM237L PDIP/CERDIP/SOIC Pin Configuration

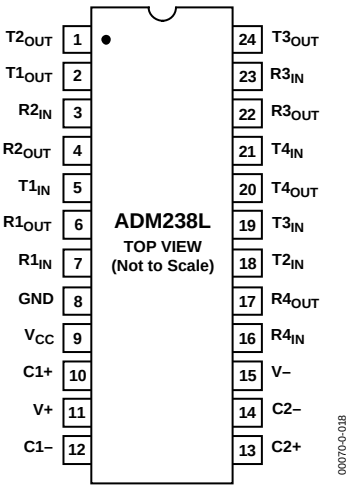


Figure 9. ADM238L PDIP/CERDIP/SOIC Pin Configuration

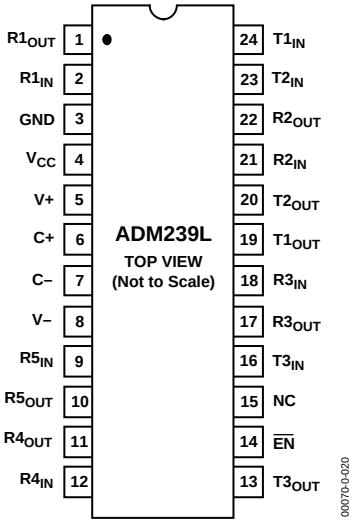


Figure 10. ADM239L PDIP/CERDIP/SOIC Pin Configuration

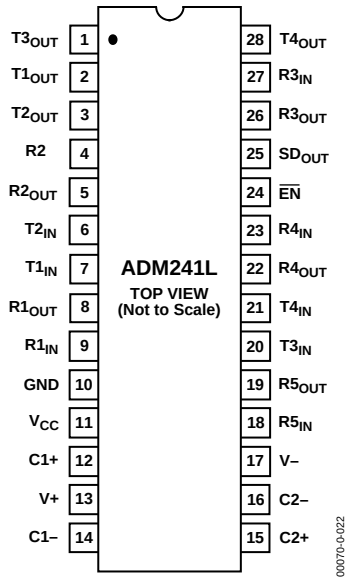


Figure 11. ADM241L SOIC/SSOP Pin Configuration

Table 4. Pin Function Descriptions

Mnemonic	Function
V_{CC}	Power Supply Input. 5 V ± 10% (5 V ± 5% for ADM233L).
V+	Internally Generated Positive Supply (+10 V nominal) on all parts, except ADM231L and ADM239L. ADM231L and ADM239L require an external 7.5 V to 13.2 V supply.
V−	Internally Generated Negative Supply (−10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C+	(ADM231L and ADM239L only) External capacitor (+ terminal) is connected to this pin.
C−	(ADM231L and ADM239L only) External capacitor (− terminal) is connected to this pin.
C1+	(ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, and ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C1−	(ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, and ADM241L) External capacitor (− terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C2+	(ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, and ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pin 11 and Pin 15, must be connected together.
C2−	(ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, and ADM241L) External capacitor (− terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pin 10 and Pin 16, must be connected together.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected to each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable Input. Active low on ADM236L, ADM239L, and ADM241L. This input is used to enable/disable the receiver outputs. With $\overline{EN}$ = low, the receiver outputs are enabled. With $\overline{EN}$ = high, the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD	Shutdown Input. Active high on ADM236L and ADM241L. With SD = high on the ADM236L and ADM241L, the charge pump is disabled, the receiver outputs are placed in a high impedance state, and the driver outputs are turned off.
NC	No Connect. No connections are required to this pin.

Table 5. ADM236L and ADM241L Truth Table

SD	$\overline{EN}$	Status	Transmitters T1 to T5	Receivers R1 to R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

TYPICAL PERFORMANCE CHARACTERISTICS

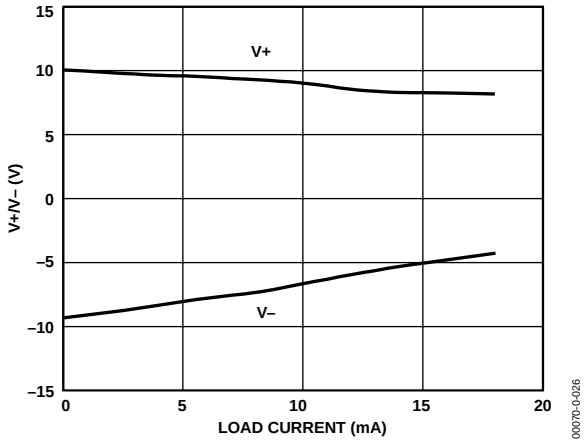


Figure 12. Charge Pump V+ and V– vs. Current

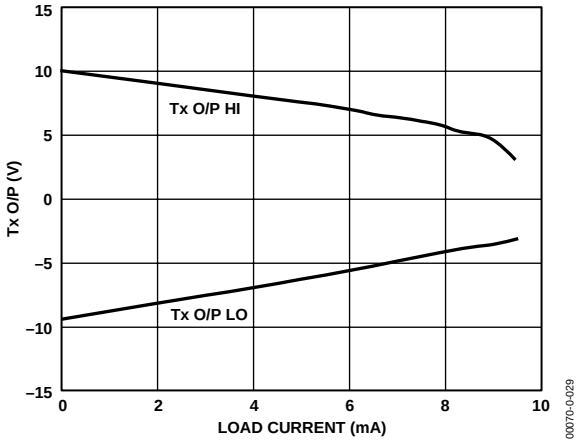


Figure 15. Transmitter Output Voltage vs. Current

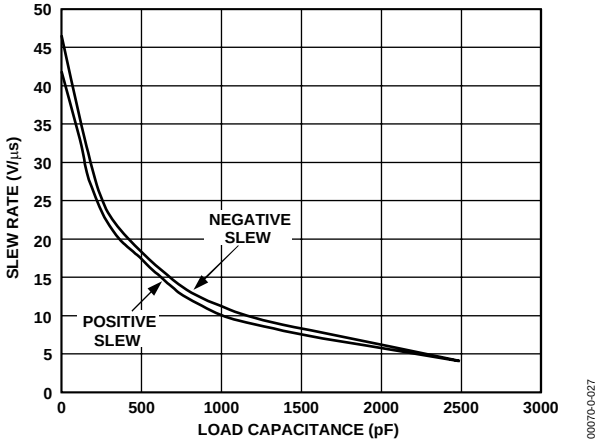


Figure 13. Transmitter Slew Rate vs. Load Capacitance

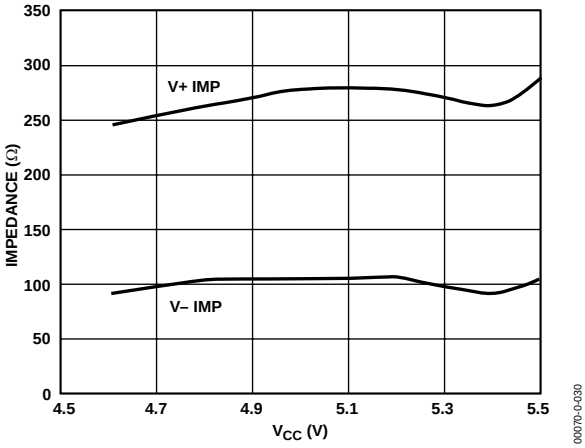


Figure 16. Charge Pump Impedance vs. V_{CC}

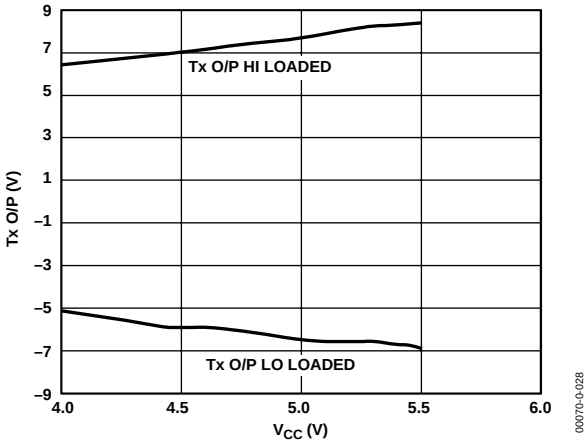


Figure 14. Transmitter Output Voltage vs. V_{CC}

TYPICAL OPERATING CIRCUITS

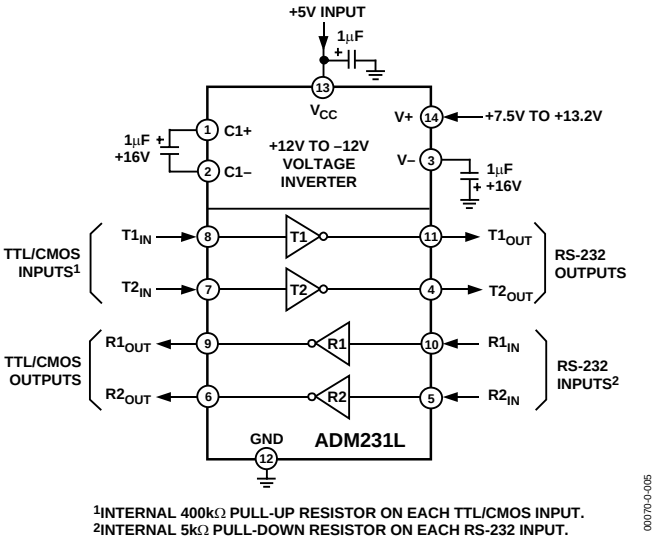


Figure 17. ADM231L Typical Operating Circuit (PDIP Pinout)

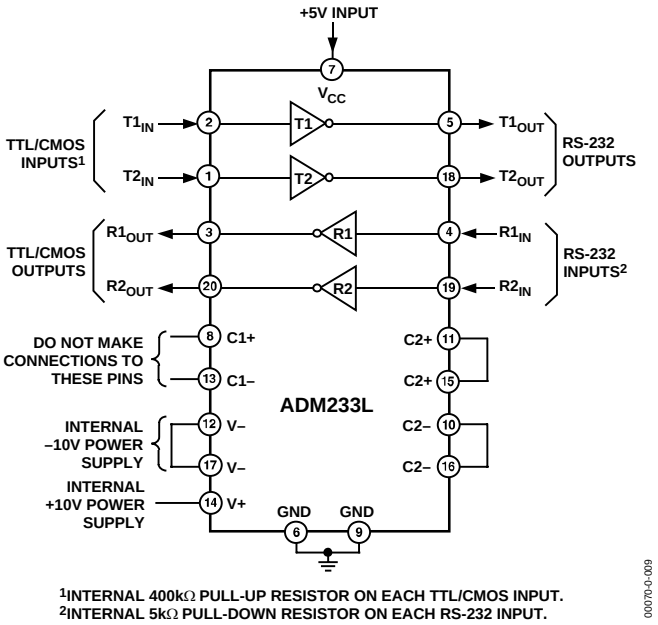


Figure 19. ADM233L Typical Operating Circuit

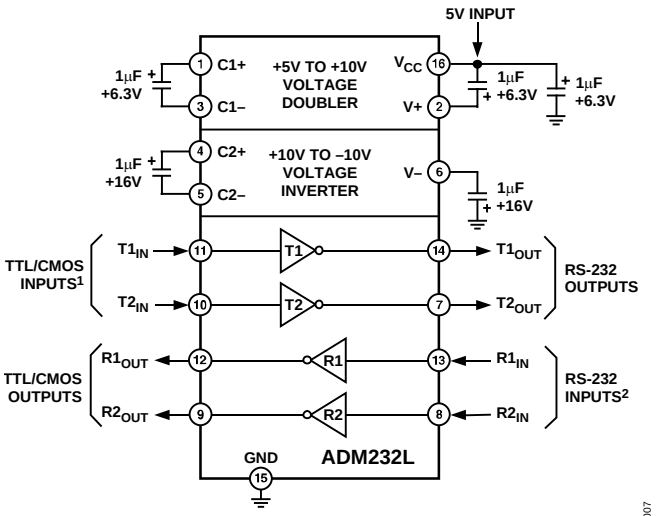


Figure 18. ADM232L Typical Operating Circuit

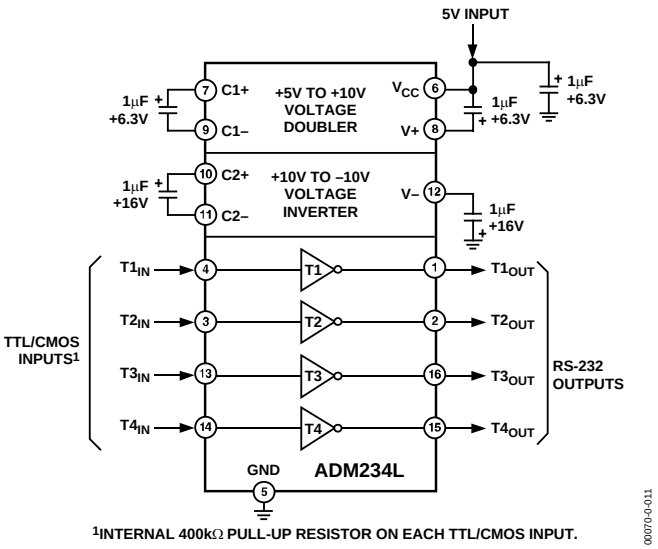


Figure 20. ADM234L Typical Operating Circuit

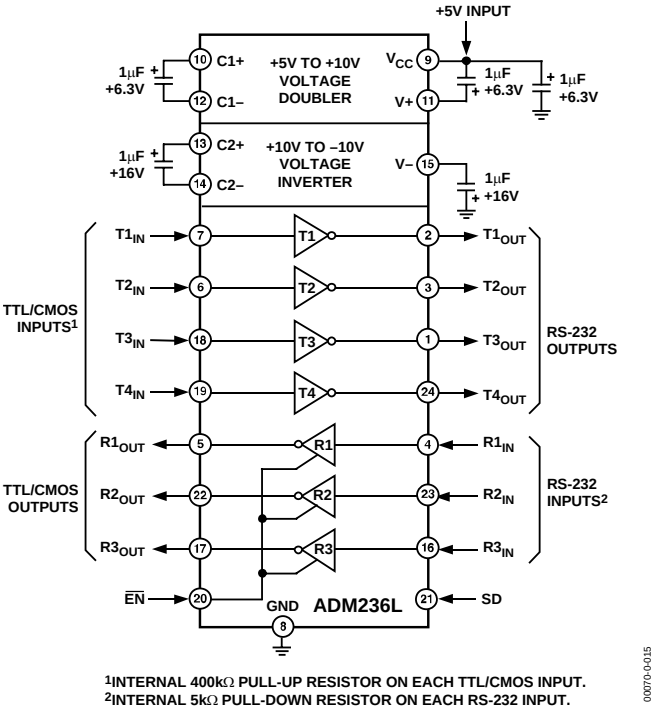


Figure 21. ADM236L Typical Operating Circuit

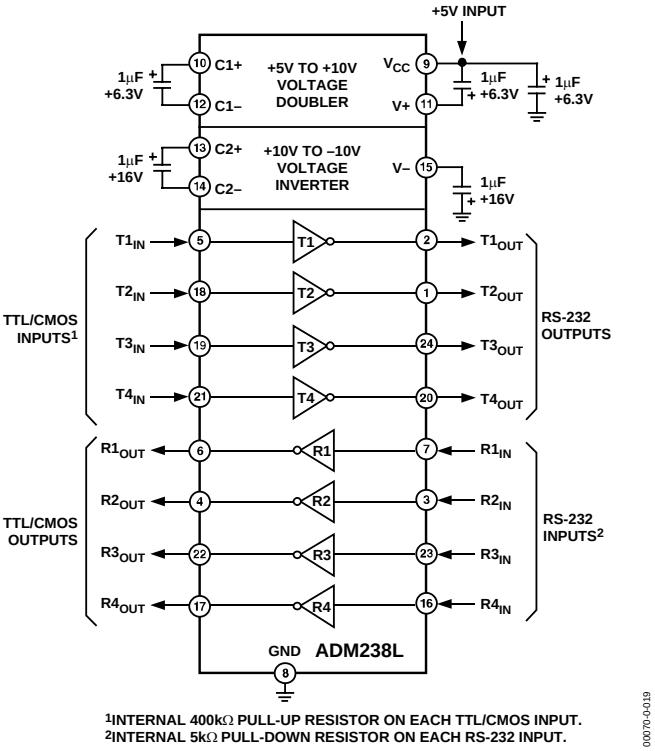


Figure 23. ADM238L Typical Operating Circuit

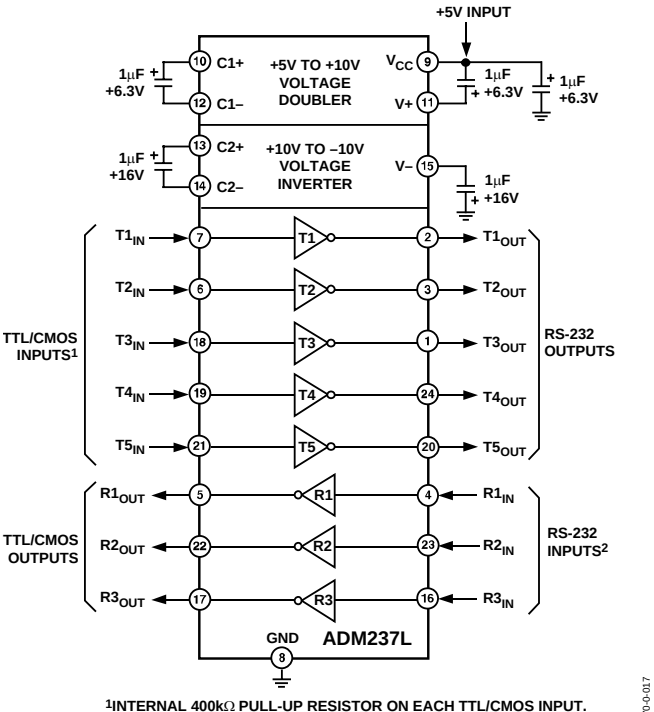
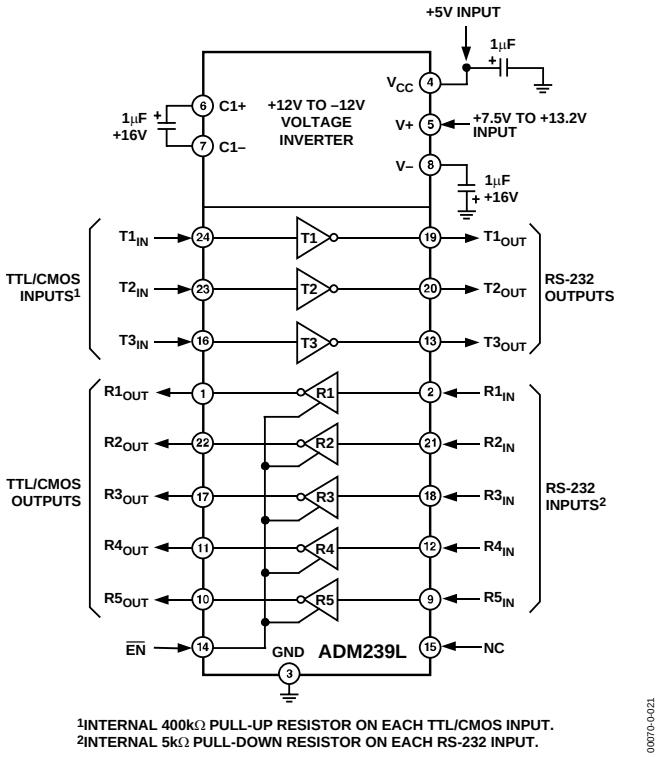


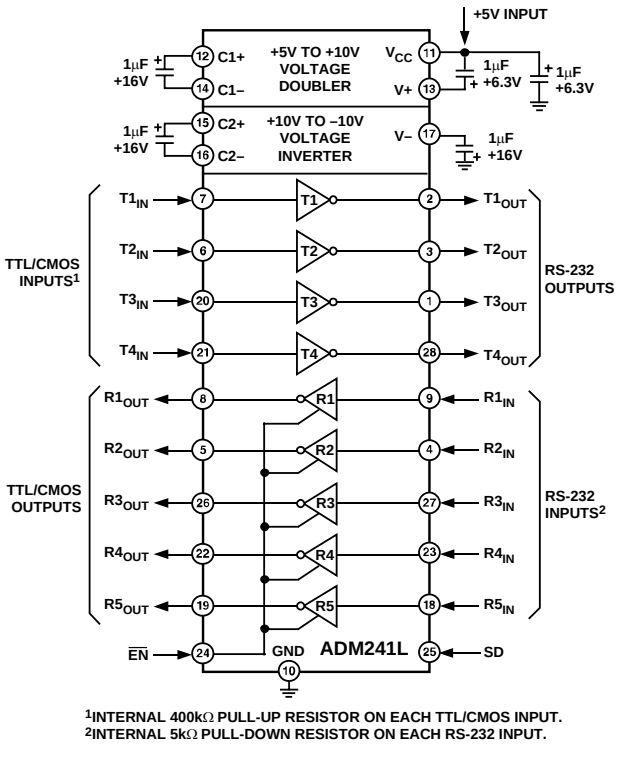
Figure 22. ADM237L Typical Operating Circuit



1INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
2INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

00070-0-021

Figure 24. ADM239L Typical Operating Circuit



1INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
2INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

00070-0-023

Figure 25. ADM241L Typical Operating Circuit

GENERAL INFORMATION

The ADM231L–ADM234L/ADM236L–ADM241L family of RS-232 drivers/receivers is designed to solve interface problems by meeting the EIA-232-E specifications while using a single digital 5 V supply. The EIA-232-E standard requires that transmitters deliver ±5 V minimum on the transmission channel and that receivers can accept signal levels down to ±3 V. The ADM231L–ADM234L/ADM236L–ADM241L meet these requirements by integrating step-up voltage converters and level-shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available for most communications needs.

The ADM236L and ADM241L are particularly useful in battery-powered systems because they feature a low power shutdown mode that reduces power dissipation to less than 5 µW.

The ADM233L is designed for applications in which space saving is important because the charge pump capacitors are molded into the package. The ADM231L and ADM239L include only a negative charge pump converter and are intended for applications in which +12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus, the ADM236L, ADM239L, and ADM241L feature an enable (EN, $\overline{EN}$) function. When the receivers are disabled, their outputs are placed in a high impedance state.

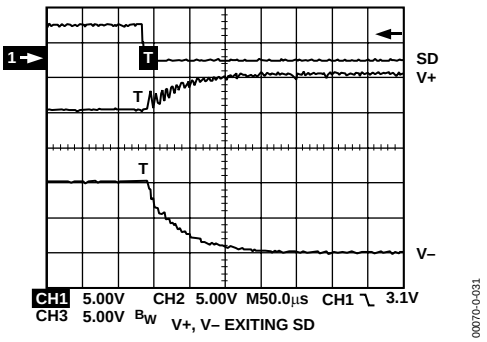


Figure 26. Charge Pump V+ and V– Exiting Shutdown

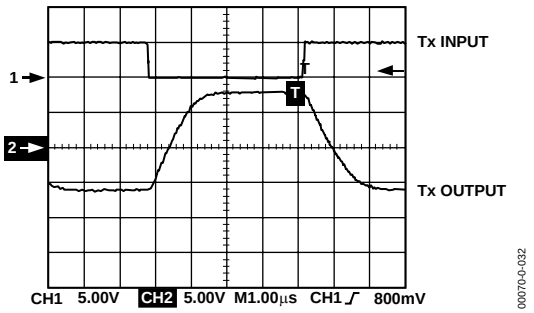


Figure 27. Transmitter Output Loaded Slew Rate

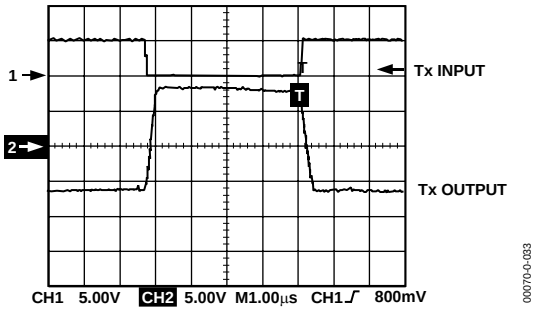


Figure 28. Transmitter Output Unloaded Slew Rate

CIRCUIT DESCRIPTION

The internal circuitry in the ADM236L to ADM241L consists of three main sections: a charge pump voltage converter, RS-232-to-TTL/CMOS receivers, and TTL/CMOS-to-RS-232 transmitters.

Charge Pump DC-to-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a 10 V supply from the 5 V input. This is done in two stages using a switched capacitor technique, as illustrated in Figure 29 and Figure 30. First, the 5 V input supply is doubled to 10 V, using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate –10 V, using C2 as the storage element.

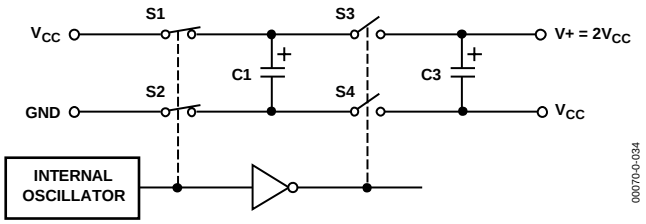


Figure 29. Charge Pump Voltage Doubler

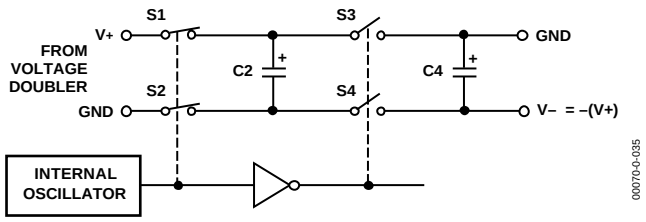


Figure 30. Charge Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors, C1 and C2, can be reduced at the expense of higher output impedance on the V+ and V– supplies, and the V+ and V– supplies can be used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With V_{CC} = +5 V and driving a typical EIA-232-E load, the output voltage swing is ±9 V. Even under worst-case conditions, the drivers are guaranteed to meet the ±5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL- and CMOS-compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V, the switching threshold is 1.25 V typical. Unused inputs can be left unconnected because an internal 400 kΩ pull-up resistor pulls them high, forcing the outputs into a low state.

As required by the EIA-232-E standard, the slew rate is limited to less than 30 V/µs without the need for an external slew-limiting capacitor, and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters that accept EIA-232-E input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum, which are well within the ±3 V EIA-232-E requirement. The low level threshold is deliberately positive because it ensures that an unconnected input is interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.65 V. This ensures error-free reception for both noisy inputs and inputs with slow transition times.

Shutdown (SD)

The ADM236L and ADM241L feature a control input that can be used to disable the part and reduce the power consumption to less than 5 µW. This is very useful in battery-operated systems. During shutdown, the charge pump is turned off, the transmitters are disabled, and all receivers are put into a high impedance, disabled state. The shutdown control input is active high on all parts (see Table 5).

Enable Input

ADM239L and ADM241L feature an enable input used to enable or disable the receiver outputs. The enable input is active low on the ADM239L and ADM241L (see Table 5). When the receivers are disabled, their outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 31.

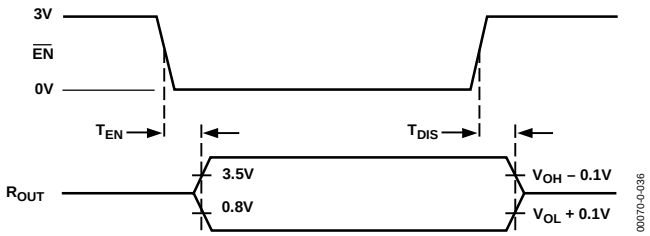


Figure 31. Enable Timing

APPLICATION HINTS

Driving Long Cables

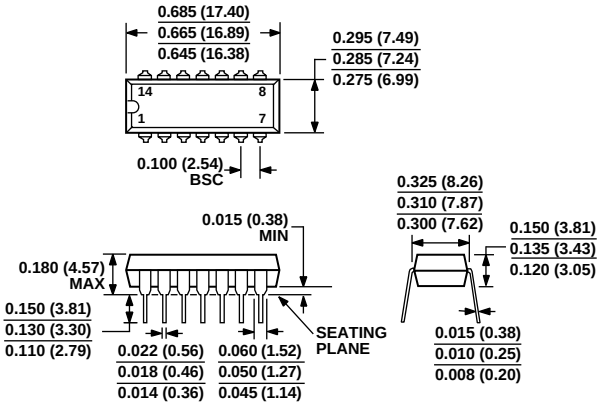
In accordance with the EIA-232-E standard, long cables are permissible, provided that the total load capacitance does not exceed 2500 pF. For longer cables that do exceed this, it is possible to trade off baud rate for cable length. Large load capacitances cause a reduction in slew rate; therefore, the maximum transmission baud rate is decreased. The ADM236L to ADM241L are designed to minimize the slew rate reduction that occurs as load capacitance increases.

For the receivers, it is important that a high level of noise immunity be built in so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The ADM236L to ADM241L have 0.65 V of hysteresis to guard against this. This ensures that even in noisy environments error-free reception can be achieved.

High Baud Rate Operation

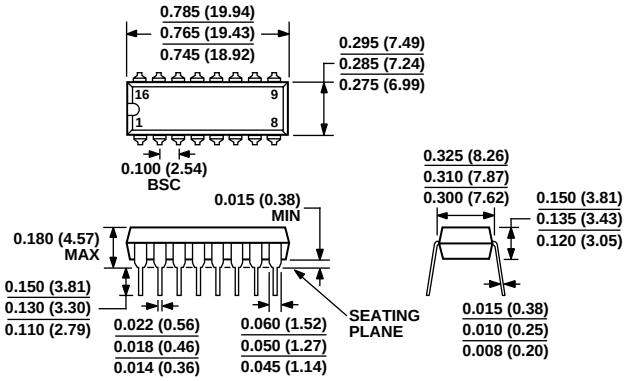
The ADM236L to ADM241L feature high slew rates, permitting data transmission at rates well in excess of the EIA-232-E specification. The drivers maintain ±5 V signal levels at data rates up to 100 kbps under worst-case loading conditions.

OUTLINE DIMENSIONS



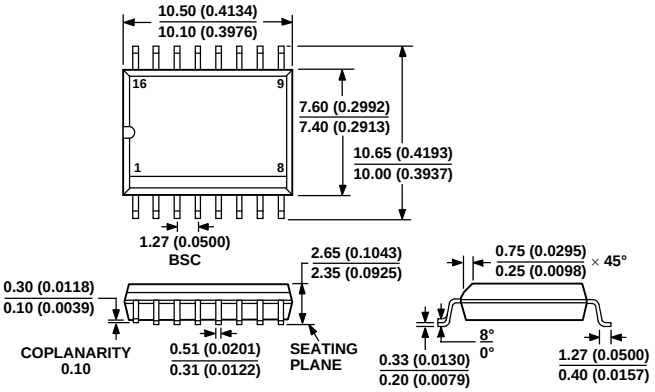
COMPLIANT TO JEDEC STANDARDS MO-095-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 32. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
Dimensions shown in inches and (millimeters)



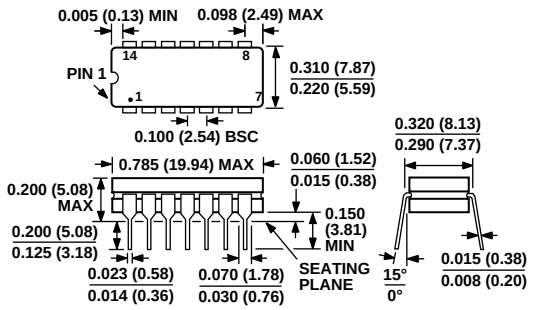
COMPLIANT TO JEDEC STANDARDS MO-095AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 33. 16-Lead Plastic Dual In-Line Package [PDIP]
(N-16)
Dimensions shown in inches and (millimeters)



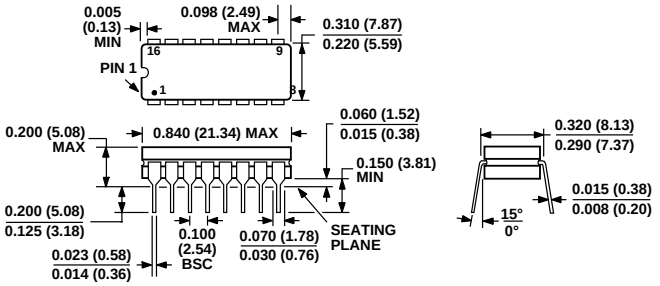
COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 34. 16-Lead Standard Small Outline Package [SOIC]
Wide Body (R-16)
Dimensions shown in millimeters and (inches)



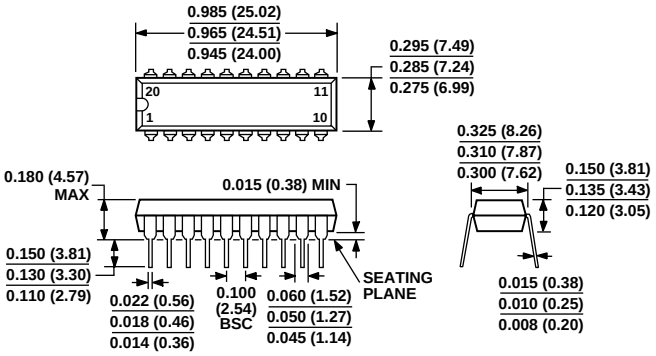
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 35. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Dimensions shown in inches and (millimeters)



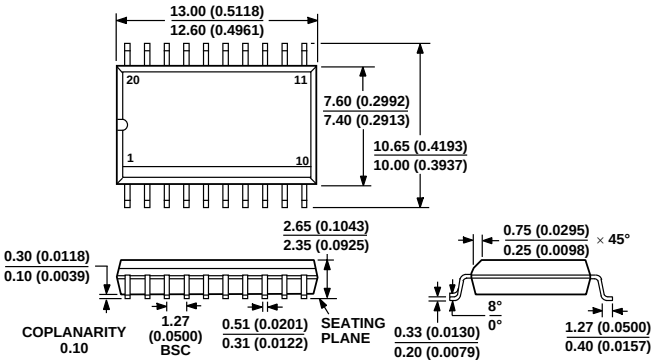
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 36. 16-Lead Ceramic Dual In-Line Package [CERDIP] (Q-16) Dimensions shown in inches and (millimeters)



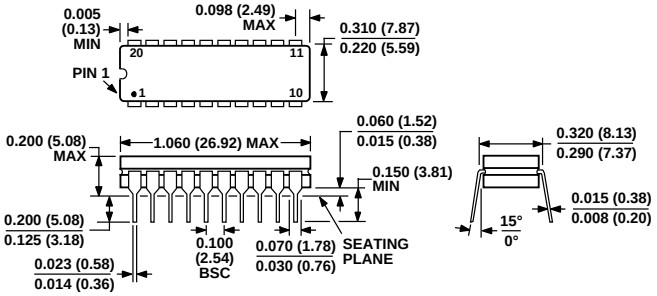
COMPLIANT TO JEDEC STANDARDS MO-095-AE
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 37. 20-Lead Plastic Dual In-Line Package [PDIP] (N-20) Dimensions shown in inches and (millimeters)



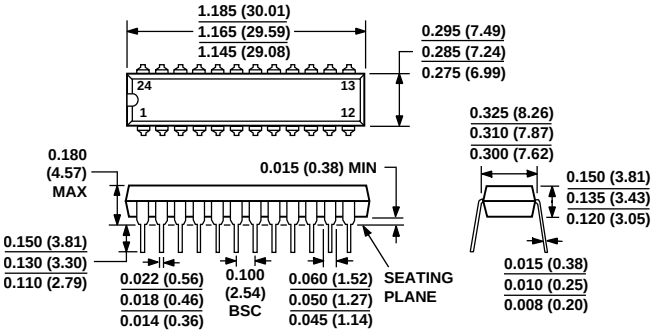
COMPLIANT TO JEDEC STANDARDS MS-013AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 38. 20-Lead Standard Small Outline Package [SOIC] Wide Body (R-20) Dimensions shown in millimeters and (inches)



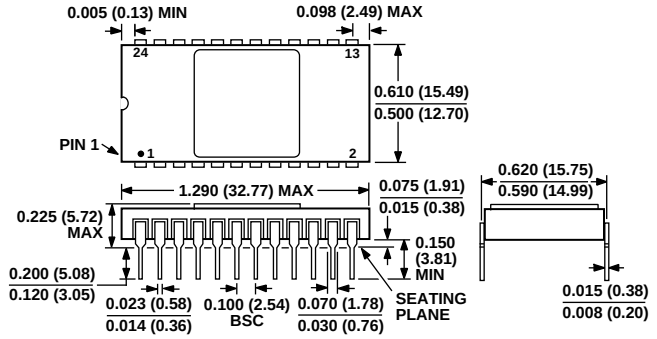
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 39. 20-Lead Ceramic Dual In-Line Package [CERDIP] (Q-20) Dimensions shown in inches and (millimeters)



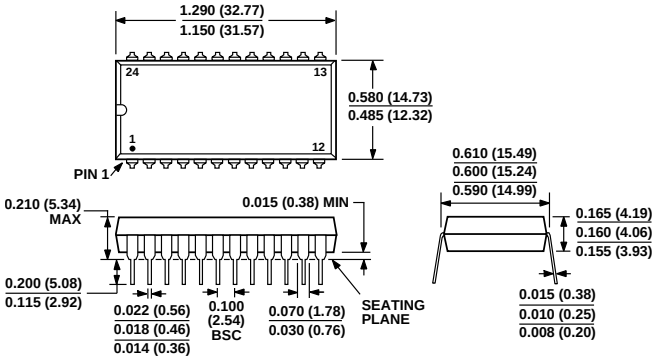
COMPLIANT TO JEDEC STANDARDS MO-095AG
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 40. 24-Lead Plastic Dual In-Line Package [PDIP] (N-24-1) Dimensions shown in inches and (millimeters)



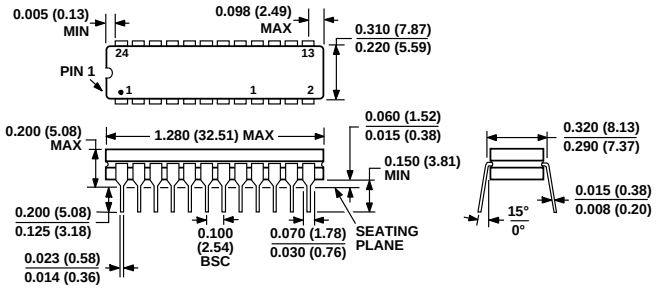
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 41. 24-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-24-2) Dimensions shown in inches and (millimeters)



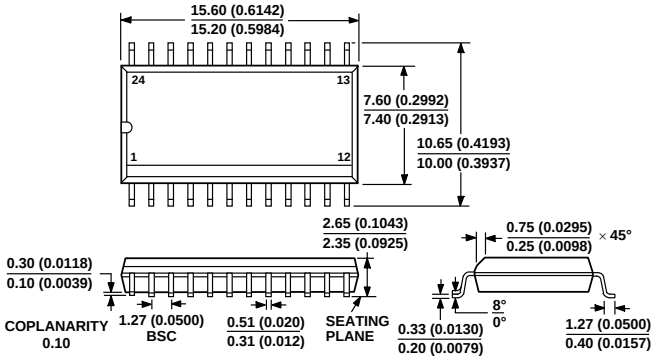
COMPLIANT TO JEDEC STANDARDS MS-011-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 42. 24-Lead Plastic Dual In-Line Package [PDIP]
Wide Body (N-24-2)
Dimensions shown in inches and (millimeters)



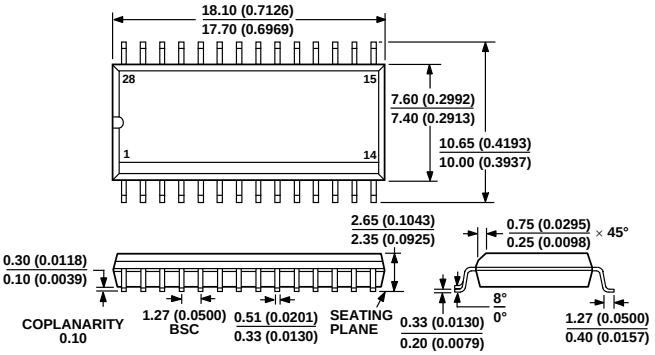
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 43. 24-Lead Ceramic Dual in-Line Package [CERDIP]
(Q-24)
Dimensions shown in inches and (millimeters)



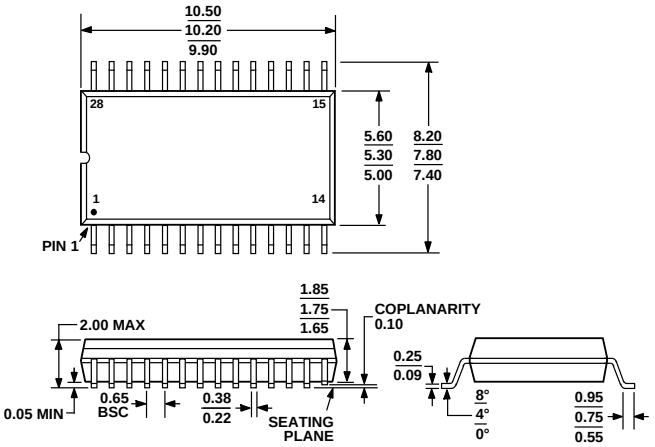
COMPLIANT TO JEDEC STANDARDS MS-013AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 44. 24-Lead Standard Small Outline Package [SOIC]
Wide Body (R-24)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 45. 28-Lead Standard Small Outline Package [SOIC]
Wide Body (R-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150AH

Figure 46. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM231LJN	0°C to 70°C	14-lead PDIP	N-14
ADM231LJR	0°C to 70°C	16-lead SOIC	R-16
ADM231LJR-REEL	0°C to 70°C	16-lead SOIC	R-16
ADM231LJRZ-REEL[1]	0°C to 70°C	16-lead SOIC	R-16
ADM231LAN	–40°C to +85°C	14-lead PDIP	N-14
ADM231LAQ	–40°C to +85°C	14-lead CERDIP	Q-14
ADM231LAR	–40°C to +85°C	16-lead SOIC	R-16
ADM231LAR-REEL	–40°C to +85°C	16-lead SOIC	R-16
ADM232LJR	0°C to 70°C	16-lead SOIC	R-16
ADM232LJR-REEL	0°C to 70°C	16-lead SOIC	R-16
ADM232LJRZ[1]	0°C to 70°C	16-lead SOIC	R-16
ADM232LJRZ-REEL7[1]	0°C to 70°C	16-lead SOIC	R-16
ADM232LAN	–40°C to +85°C	16-lead PDIP	N-16
ADM232LAR	–40°C to +85°C	16-lead SOIC	R-16
ADM232LAR-REEL	–40°C to +85°C	16-lead SOIC	R-16
ADM232LARZ[1]	–40°C to +85°C	16-lead SOIC	R-16
ADM232LARZ-REEL[1]	–40°C to +85°C	16-lead SOIC	R-16
ADM232LJN	0°C to 70°C	20-lead PDIP	N-16
ADM232LJNZ[1]	0°C to 70°C	20-lead PDIP	N-16
ADM233LJN	0°C to 70°C	20-lead PDIP	N-20
ADM233LAN	–40°C to +85°C	20-lead PDIP	N-20
ADM234LJN	0°C to 70°C	16-lead PDIP	N-16
ADM234LJR	0°C to 70°C	16-lead SOIC	R-16
ADM234LJR-REEL	0°C to 70°C	16-lead SOIC	R-16
ADM234LJRZ[1]	0°C to 70°C	16-lead SOIC	R-16
ADM234LJRZ-REEL[1]	0°C to 70°C	16-lead SOIC	R-16
ADM234LAN	–40°C to +85°C	16-lead PDIP	N-16
ADM234LAQ	–40°C to +85°C	16-lead CERDIP	Q-16
ADM234LAR	–40°C to +85°C	16-lead SOIC	R-16
ADM234LAR-REEL	–40°C to +85°C	16-lead SOIC	R-16
ADM236LJN	0°C to 70°C	24-lead PDIP	N-24-1
ADM236LJR	0°C to 70°C	24-lead SOIC	R-24
ADM236LJR-REEL	0°C to 70°C	24-lead SOIC	R-24
ADM236LAN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM236LAR	–40°C to +85°C	24-lead SOIC	R-24
ADM236LAR-REEL	–40°C to +85°C	24-lead SOIC	R-24
ADM237LJN	0°C to 70°C	24-lead PDIP	N-24-1
ADM237LJR	0°C to 70°C	24-lead SOIC	R-24
ADM237LJR-REEL	0°C to 70°C	24-lead SOIC	R-24
ADM237LJRZ[1]	0°C to 70°C	24-lead SOIC	R-24
ADM237LJRZ-REEL[1]	0°C to 70°C	24-lead SOIC	R-24
ADM237LAN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM237LAQ	–40°C to +85°C	24-lead CERDIP	Q-24
ADM237LAR	–40°C to +85°C	24-lead SOIC	R-24
ADM237LAR-REEL	–40°C to +85°C	24-lead SOIC	R-24
ADM238LJN	0°C to 70°C	24-lead PDIP	N-24-1
ADM238LJNZ[1]	0°C to 70°C	24-lead PDIP	N-24-1
ADM238LJR	0°C to 70°C	24-lead SOIC	R-24
ADM238LJR-REEL	0°C to 70°C	24-lead SOIC	R-24
ADM238LJRZ[1]	0°C to 70°C	24-lead SOIC	R-24
ADM238LJRZ-REEL[1]	0°C to 70°C	24-lead SOIC	R-24

Model	Temperature Range	Package Description	Package Option
ADM238LAN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM238LAQ	–40°C to +85°C	24-lead CERDIP	Q-24
ADM238LAR	–40°C to +85°C	24-lead SOIC	R-24
ADM238LAR-REEL	–40°C to +85°C	24-lead SOIC	R-24
ADM238LARZ[1]	–40°C to +85°C	24-lead SOIC	R-24
ADM238LARZ-REEL[1]	–40°C to +85°C	24-lead SOIC	R-24
ADM239LJN	0°C to 70°C	24-lead PDIP	N-24-1
ADM239LJR	0°C to 70°C	24-lead SOIC	R-24
ADM239LJR-REEL	0°C to 70°C	24-lead SOIC	R-24
ADM239LJRZ[1]	0°C to 70°C	24-lead SOIC	R-24
ADM239LJRZ-REEL[1]	0°C to 70°C	24-lead SOIC	R-24
ADM239LAN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM239LAQ	–40°C to +85°C	24-lead CERDIP	Q-24
ADM239LAR	–40°C to +85°C	24-lead SOIC	R-24
ADM239LAR-REEL	–40°C to +85°C	24-lead SOIC	R-24
ADM241LJR	0°C to 70°C	28-lead SOIC	R-28
ADM241LJR-REEL	0°C to 70°C	28-lead SOIC	R-28
ADM241LJRZ[1]	0°C to 70°C	28-lead SOIC	R-28
ADM241LJRZ-REEL[1]	0°C to 70°C	28-lead SOIC	R-28
ADM241LAR	–40°C to +85°C	28-lead SOIC	R-28
ADM241LAR-REEL	–40°C to +85°C	28-lead SOIC	R-28
ADM241LJRS	0°C to 70°C	28-lead SSOP	RS-28
ADM241LJRS-REEL	0°C to 70°C	28-lead SSOP	RS-28
ADM241LARS	–40°C to +85°C	28-lead SSOP	RS-28
ADM241LARS-REEL	–40°C to +85°C	28-lead SSOP	RS-28

[1] Z = Pb-free part.

NOTES

NOTES

C00070–0–4/05(C)