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2/12—Rev. 0 to Rev. A

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4/04—Revision 0: Initial Version

GENERAL DESCRIPTION

(continued from Page 1)

Further control of the inrush current is provided by modulating the width of the pulses, depending on the drain-source voltage across the FET. This allows maximum charge transfer to the load capacitance while maintaining the FET in its safe operating area (SOA).

The default duty cycle of the pulse train is 6%, decreasing to 2.5% with maximum FET drain-source voltage, with a maximum of seven successive autorestarts. After seven successive autorestarts, the fault is latched and the part goes into shutdown, with the result that the external FET is disabled until the power is reset. The $\overline{\text{LATCHED}}$ output signal indicates when the seven retries are complete.

Further programmability is offered by allowing alteration of the default 6% ratio. An extra resistor between the TIMER pin and V_{EE} allows the ratio of on-time to off-time to be decreased, while a resistor between TIMER and V_{IN} allows the ratio to be increased.

The ADM1073 has separate UV and OV pins for undervoltage and overvoltage detection. The FET is turned off, if a nontransient voltage less than the undervoltage threshold (typically −36 V) is detected on the UV pin, or if greater than the overvoltage threshold (typically −80 V) is detected on the OV pin. The operating voltage window of the ADM1073 is programmable via resistor networks on the UV and OV pins. The hysteresis levels on the undervoltage and overvoltage detectors can also be altered (see the Undervoltage/Overvoltage Detection section). The $\overline{\text{SPLYGD}}$ output signal indicates when the backplane supply is within the externally programmable operating voltage range.

Other functions include

- $\overline{\text{PWRGD}}$ output, which can be used to enable a power module (the DRAIN pin is monitored to determine when the load capacitance is fully charged)
- $\overline{\text{SHDN}}$ input to manually disable the GATE drive
- $\overline{\text{RESTART}}$ input to remotely initiate a 5 second shutdown

The ADM1073 is fabricated using BiCMOS technology for minimal power consumption and is available in a 14-lead TSSOP package.

SPECIFICATIONS

V_{DD} = 0 V, V_{EE} = −48 V; T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
BOARD SUPPLY (Not Connected Directly to Device)					Limited by external components
Maximum Voltage Range	−200	−48	−18	V	
Typical Operating Voltage Range	−80	−48	−35	V	
V_{IN} PIN—SHUNT REGULATOR					
Operating Supply Voltage Range	11.7	12.3	12.9	V	I_{IN} = 0.6 mA to 2 mA
Quiescent Supply Current		300	500	µA	V_{IN} = 11.7 V
Maximum Shunt Supply Voltage			14	V	I_{IN} = 10 mA
Undervoltage Lockout, V_{LKO}		8		V	
Power-On Reset Delay		150		ms	
UV, OV PINS—UNDERVOLTAGE AND OVERVOLTAGE DETECTION					
Undervoltage Falling Threshold, V_{UVF}	825	868	910	mV	
Undervoltage Hysteresis Current		5		µA	
Undervoltage Fault Filter		0.6		ms	
Overvoltage Rising Threshold, V_{OVR}	1.86	1.93	2.00	V	
Overvoltage Hysteresis Current		5		µA	
Overvoltage Fault Filter		5		µs	
Input Current			0.2	µA	
GATE PIN—FET DRIVER					
Maximum Gate Voltage	11.5		$V_{IN(MAX)}$	V	I_{GATE} = −1.0 µA
Minimum Gate Voltage		10	100	mV	I_{GATE} = 1.0 µA
Pull-Up Current		−50		µA	V_{GATE} = 0 V to 8 V; V_{SS} = 2 V
		−36		µA	V_{GATE} = 0 V to 8 V; V_{SS} = 0 V
Pull-Down Current	20			mA	V_{GATE} > 2 V
	50			mA	V_{GATE} > 5 V
SENSE PIN—CURRENT SENSE—SOFT START					
Current Limit Control Loop Threshold, V_{ACL}	97	100	103	mV	I_{GATE} = 0 mA
Circuit Breaker Limit Voltage, V_{CB}	86	90		mV	
Fast Current Limit Voltage, V_{FCL}		110		mV	
Control Loop Transconductance		4.5		µA/mV	
Soft Start Pin Current		5		µA	
TIMER PIN—PWM CONTROL					
Minimum TIMER Pull-Up Current	18	19	20	µA	$I_{\overline{PWRGD}}$ < 4 µA; T_A = 25°C to 85°C
	16	19	20	µA	$I_{\overline{PWRGD}}$ < 4 µA
Maximum TIMER Pull-Up Current	37	39	41	µA	$I_{\overline{PWRGD}}$ = 24 µA; T_A = 25°C to 85°C
	34	39	41	µA	$I_{\overline{PWRGD}}$ = 24 µA
TIMER Pull-Down Current		1		µA	
TIMER Low Voltage Trip Point	0.45	0.50	0.55	V	
TIMER High Voltage Trip Point	2.34	2.42	2.50	V	
Current Limit On-Time, t_{ON}		6		ms	I_{DRAIN} = 4 µA; C_{TIMER} = 47 nF
Current Limit On-Time, t_{ON}, with Foldback		3		ms	I_{DRAIN} = 20 µA; C_{TIMER} = 47 nF
Number of Consecutive PWM Retry Cycles		7			
Continuous Short-Circuit Time before Latched Shutdown		0.6		s	C_{TIMER} = 47 nF

Parameter	Min	Typ	Max	Unit	Test Conditions
DRAIN (FOLDBACK) AND $\overline{\text{PWRGD}}$					
DRAIN Voltage at Which $\overline{\text{PWRGD}}$ Asserts	1.9	2	2.1	V	R_{DRAIN} = 3.75 M to 20 M
Maximum DRAIN Pin Current Allowable, $I_{DRAIN(MAX)}$		36		µA	V_{DS} = 80 V; R_{DRAIN} = 3.25 M
$\overline{\text{PWRGD}}$ Output Voltage Low		1	2	V	$I_{\overline{PWRGD}}$ = 2.5 mA
		0.2	0.4	V	$I_{\overline{PWRGD}}$ = 0.5 mA
$\overline{\text{PWRGD}}$ Internal Pull-Up Current		6		µA	
$\overline{\text{PWRGD}}$ Output Voltage High		V_{IN}		V	
$\overline{\text{RESTART}}$					
Time before Restart		5		s	
Input Threshold	1.35	1.45	1.55	V	
Glitch Filter		5		µs	
Internal Pull-Up Current		6		µA	
$\overline{\text{SHDN}}$					
Glitch Filter		5		µs	
Input Threshold	1.35	1.45	1.55	V	
Internal Pull-Up Current		6		µA	
$\overline{\text{LATCHED}}$ AND $\overline{\text{SPLYGD}}$					
Output Voltage Low		1	2	V	$I_{\overline{LATCHED}}$, $I_{\overline{SPLYGD}}$ = 2.5 mA
		0.2	0.4	V	$I_{\overline{LATCHED}}$, $I_{\overline{SPLYGD}}$ = 0.5 mA
Internal Pull-Up Current		6		µA	
Output Voltage High		V_{IN}		V	

ABSOLUTE MAXIMUM RATINGS

All voltages referred to V_{EE}, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage (V_{DD} − V_{EE})	−0.3 V to −200.0 V
Maximum Shunt Supply Voltage, V_{SS}	16 V
SENSE Pin	−2 V to +2 V
GATE Pin	−0.3 V to +16 V
UV Pin	−0.3 V to +6 V
OV Pin	−0.3 V to +6 V
SS Pin	−0.3 V to +6 V
TIMER Pin	−0.3 V to +6 V
DRAIN Pin	−0.3 V to +6 V
$\overline{\text{SHDN}}$ Pin	−0.3 V to +16 V
$\overline{\text{SPLYGD}}$ Pin	−0.3 V to +16 V
$\overline{\text{LATCHED}}$ Pin	−0.3 V to +16 V
$\overline{\text{PWRGD}}$ Pin	−0.3 V to +16 V
$\overline{\text{RESTART}}$ Pin	−0.3 V to +16 V
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Continuous Power Dissipation	180 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

14-lead TSSOP Package:

θ_{JA} = 240°C/W
θ_{JC} = 43°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

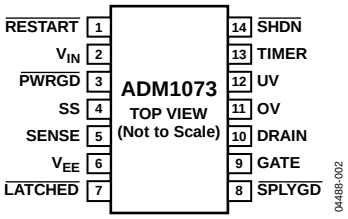

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin Number	Mnemonic	Function
1	$\overline{\text{RESTART}}$	Input Pin. Edge-triggered 5-second shutdown and automatic restart.
2	V_{IN}	Shunt Regulated Positive Supply to Chip. Connect to the positive supply rail via shunt resistor. A 1 µF capacitor to V_{EE} is recommended on the V_{IN} pin.
3	$\overline{\text{PWRGD}}$	Open Drain Output. Signals that the hot swap is complete.
4	SS	Analog Pin for Soft Start. An external capacitor on this pin sets the ramp rate of the inrush current profile. This pin can be overdriven to alter the current limit control loop threshold.
5	SENSE	Voltage Input from External Sense Resistor.
6	V_{EE}	Ground Supply to Chip (usually a −48 V system supply). Also low-side sense resistor connection.
7	$\overline{\text{LATCHED}}$	Open Drain Output. Signals the end of the PWM retry period after a current fault.
8	$\overline{\text{SPLYGD}}$	Open Drain Output. Signals that the device is not in reset and that the supply is in operating voltage window.
9	GATE	Output to External FET Gate Drive.
10	DRAIN	Analog Input for Monitoring of FET Drain Voltage.
11	OV	Input Pin for Overvoltage Detection Circuitry.
12	UV	Input Pin for Undervoltage Detection Circuitry.
13	TIMER	Analog Pin. An external capacitor on this pin sets the maximum allowable time in current limit, the PWM on-time, and the PWM duty cycle.
14	$\overline{\text{SHDN}}$	Input Pin. Level-triggered device shutdown and reset.

TYPICAL PERFORMANCE CHARACTERISTICS

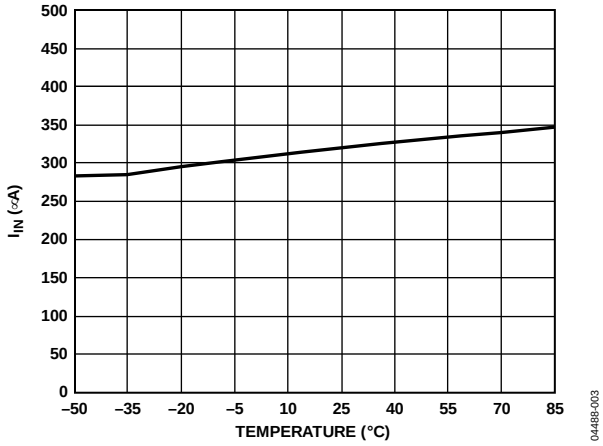

Figure 3. I_{IN} vs. Temperature

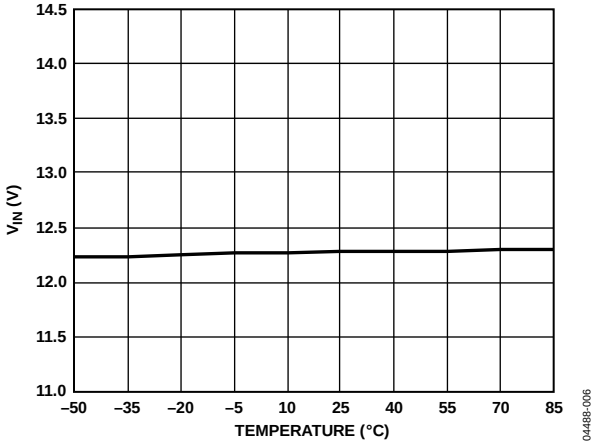

Figure 6. V_{IN} vs. Temperature

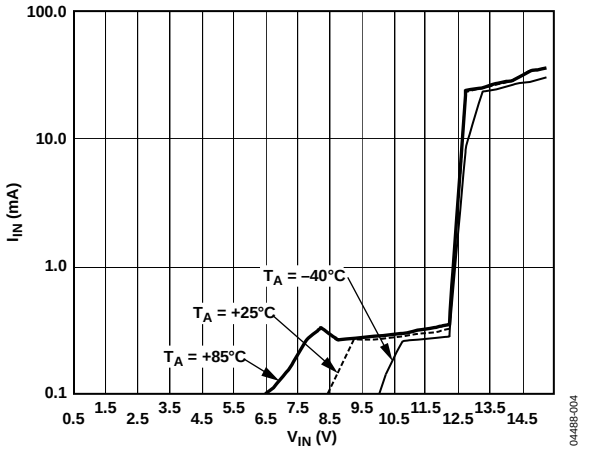

Figure 4. I_{IN} vs. V_{IN}

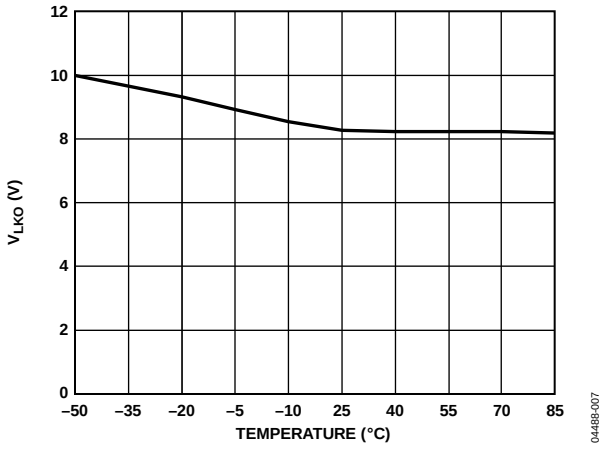

Figure 7. Undervoltage Lockout, V_{LKO}, vs. Temperature

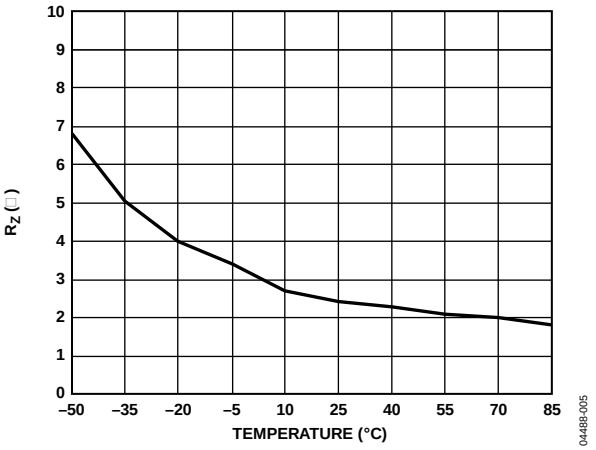

Figure 5. R_Z (V_{IN} Forward Voltage) vs. Temperature

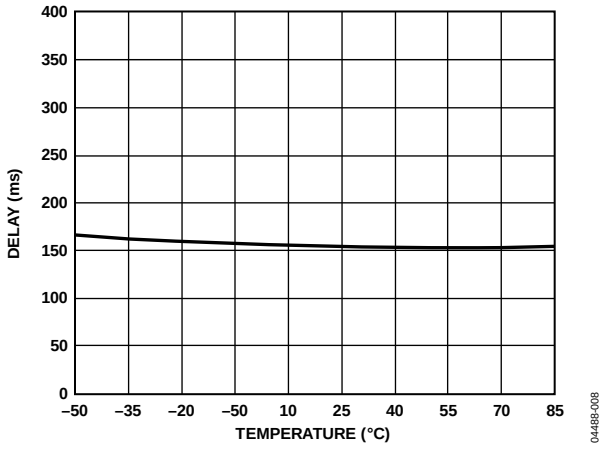

Figure 8. POR Delay vs. Temperature

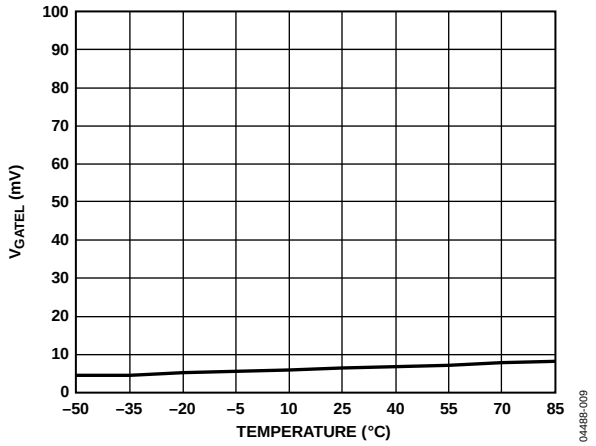

Figure 9. V_{GATEL} vs. Temperature

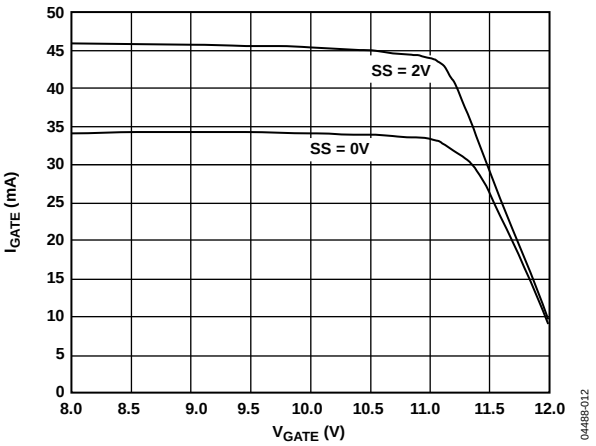

Figure 12. I_{GATE} (Source) vs. V_{GATE}

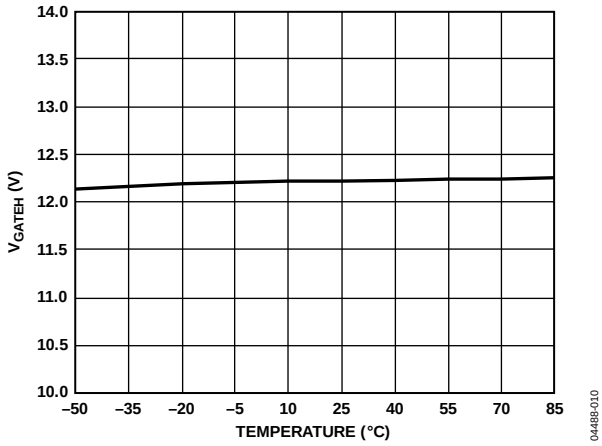

Figure 10. V_{GATEH} vs. Temperature

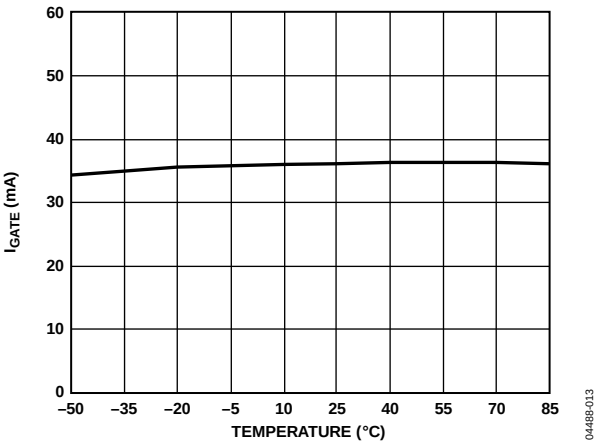

Figure 13. I_{GATE} (FCL, Sink) vs. Temperature (V_{GATE} = 2 V)

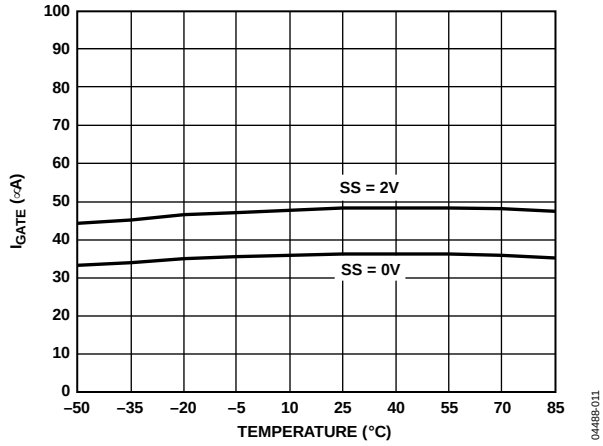

Figure 11. I_{GATE} (Source) vs. Temperature

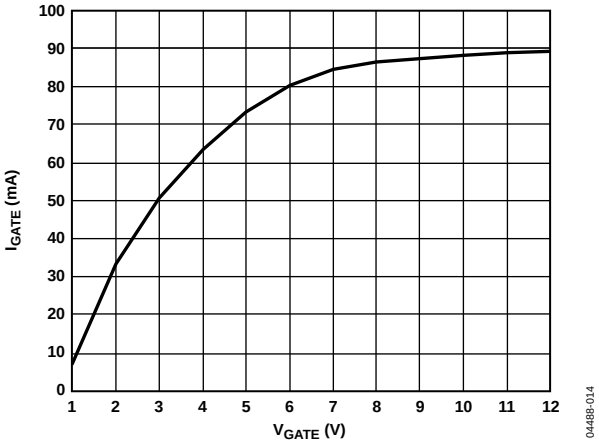

Figure 14. I_{GATE} (FCL, Sink) vs. V_{GATE}

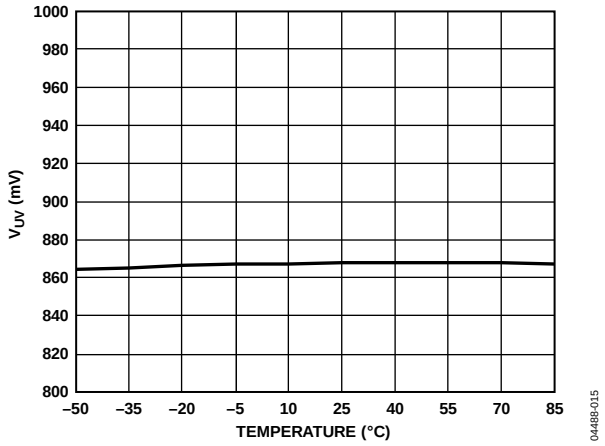

Figure 15. UV Threshold vs. Temperature

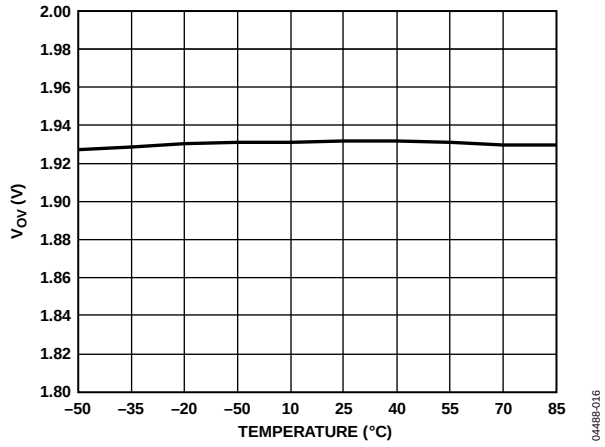

Figure 16. OV Threshold vs. Temperature

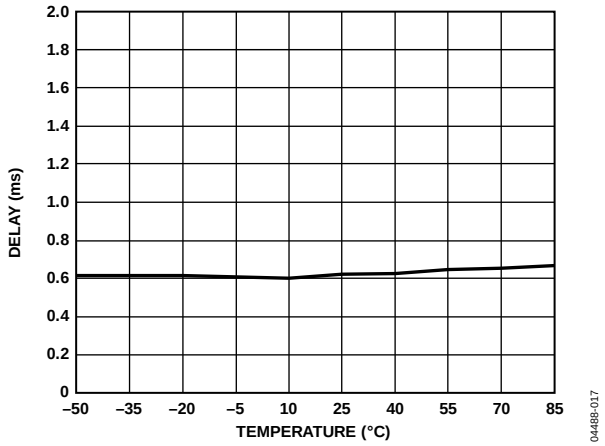

Figure 17. UV Voltage Fault Filter Time vs. Temperature

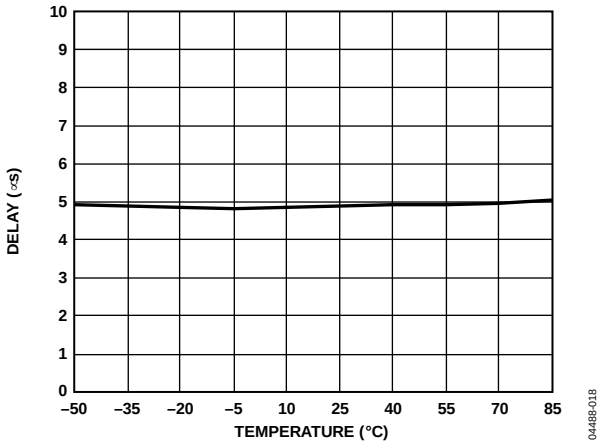

Figure 18. OV Voltage Fault Filter Time vs. Temperature

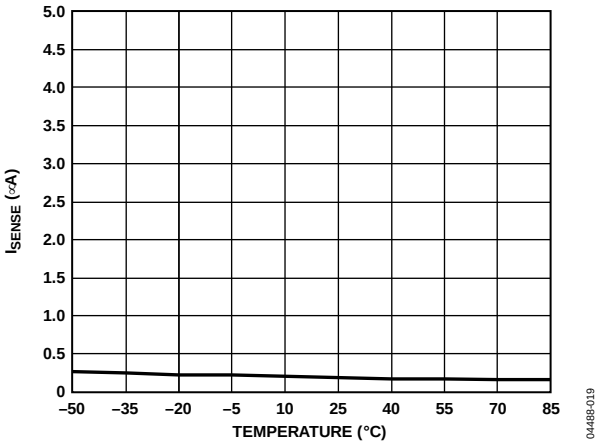

Figure 19. I_{SENSE} vs. Temperature (V_{SENSE} = 50 mV)

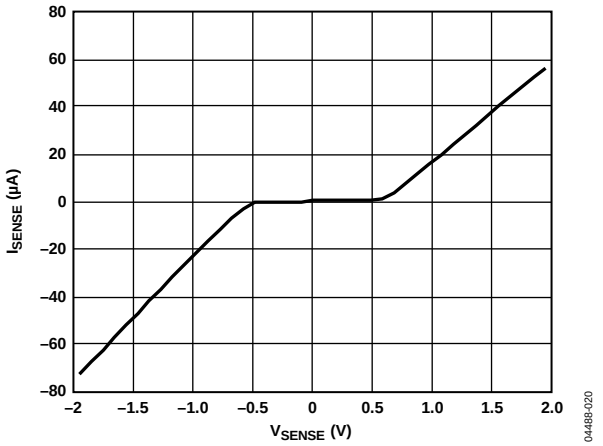

Figure 20. I_{SENSE} vs. (V_{SENSE} – V_{EE})

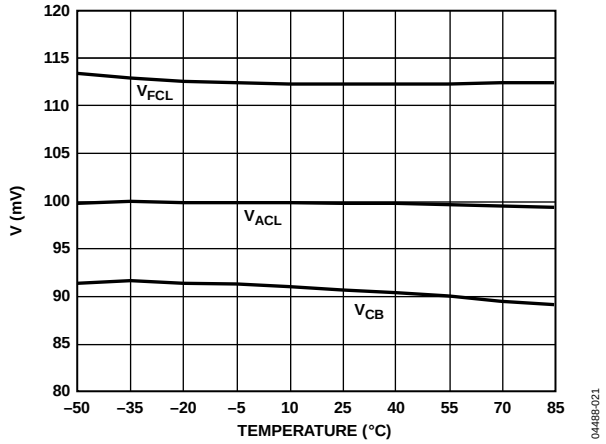

Figure 21. Voltage Limits for Load Current Control vs. Temperature

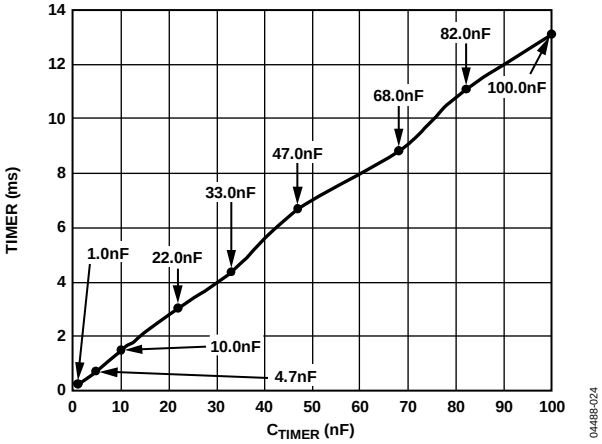

Figure 24. Current Limit On-Time vs. C_{TIMER} (1 nF – 100 nF)

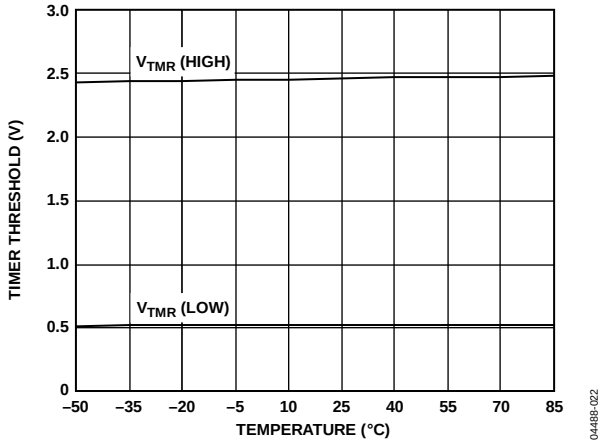

Figure 22. High and Low TIMER Thresholds vs. Temperature

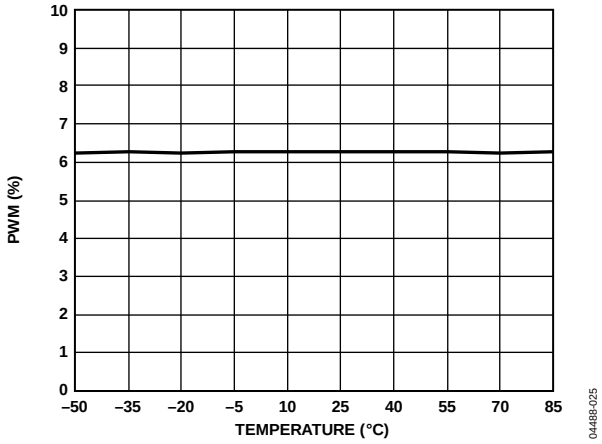

Figure 25. Current Limit PWM vs. Temperature

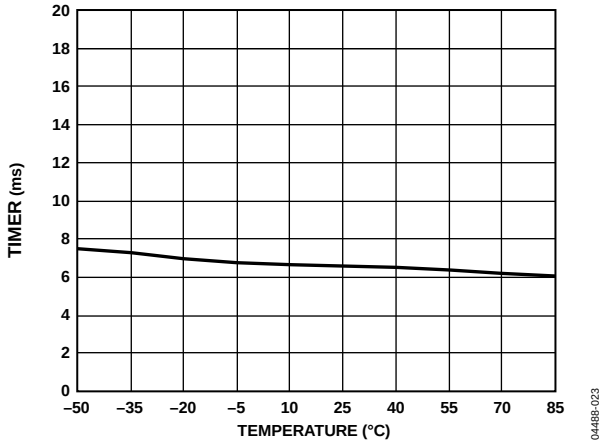

Figure 23. Maximum Current Limit On-Time vs. Temperature (I_{DRAIN} = 4 µA, C_{TIMER} = 47 nF)

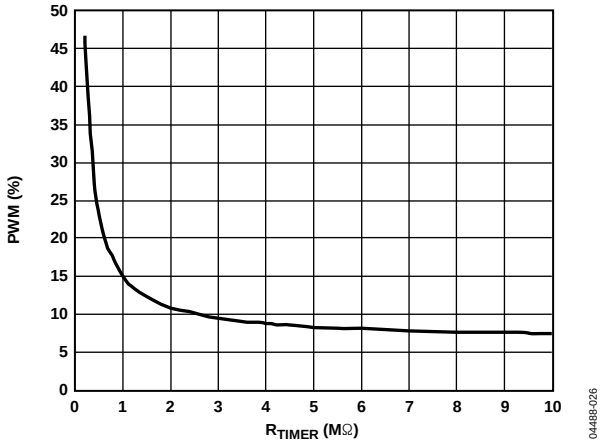

Figure 26. Current Limit PWM vs. R_{TIMER}

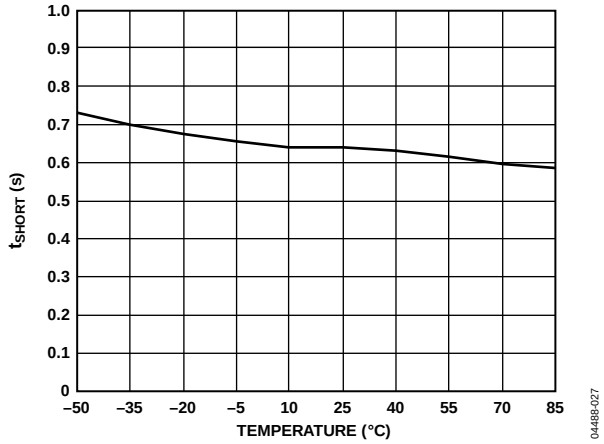

Figure 27. Continuous Short Circuit Time before Shutdown vs. Temperature

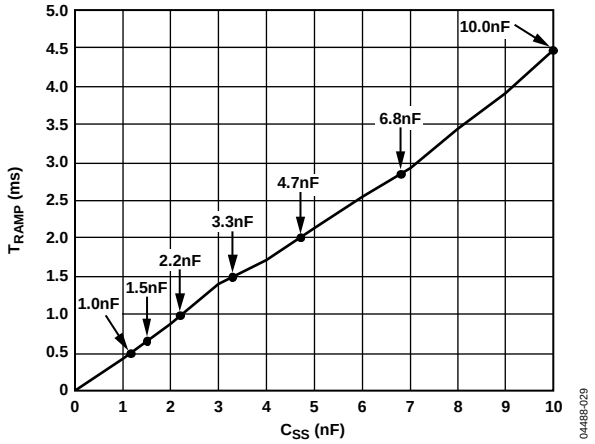

Figure 29. Soft Start Ramp Time vs. C_{SS}

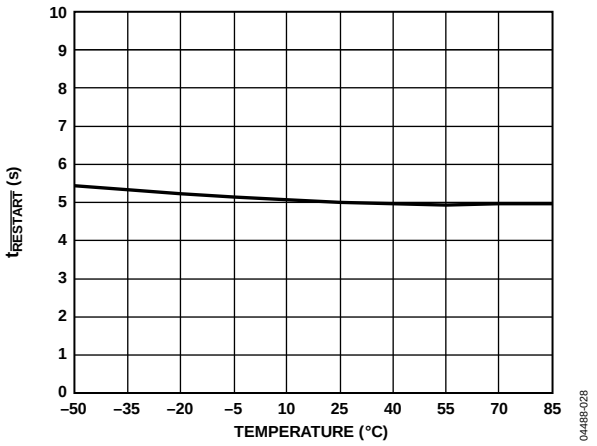

Figure 28. $\overline{RESTART}$ Time vs. Temperature

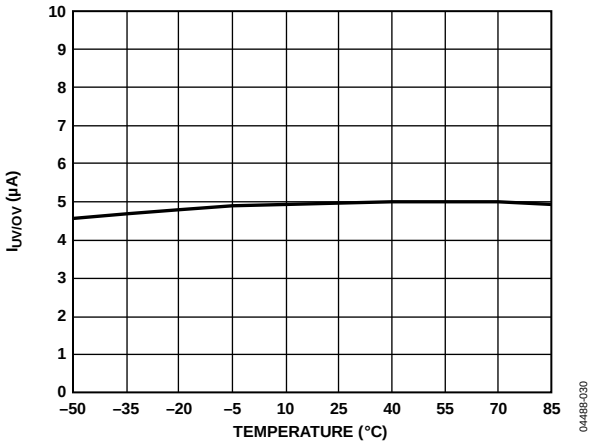

Figure 30. $I_{UV/OV}$ vs. Temperature

FUNCTIONAL DESCRIPTION

HOT CIRCUIT INSERTION

Inserting circuit boards into a live −48 V backplane can cause large transient currents to be drawn as the board capacitance charges up. These transient currents can cause glitches on the system power supply and can permanently damage the board connectors and components.

The ADM1073 is designed to control the manner in which a board's supply voltage is applied so that harmful transient currents do not occur and the board can be safely inserted or removed from a live backplane. Undervoltage, overvoltage, and overcurrent protection are other features of the part. The ADM1073 ensures that the input voltage is stable and within tolerance before being applied to the power module.

INITIAL STARTUP

The ADM1073 hot swap controller normally resides on a removable circuit board and controls the manner in which power is applied to the board upon connection. This is achieved using a FET, Q1, in the power path (see Figure 31). By controlling the gate voltage of the transistor, the surge of current to charge load capacitance can be limited to a safe value when the board makes connection. The ADM1073 can also reside on the backplane itself and perform the same function from there.

Figure 32 shows a typical ADM1073 application circuit. When the plug-in board is inserted into the live backplane, the −48 V and 0 V lines connect to the live supply. This powers up the device with the voltage on V_{IN} exceeding V_{LKO}. When the voltage on the UV pin exceeds the undervoltage rising threshold (0.868 V), it is now inside the programmed operating voltage window. It must stay inside this window for the duration of the power-on reset delay time, t_{POR} (150 ms).

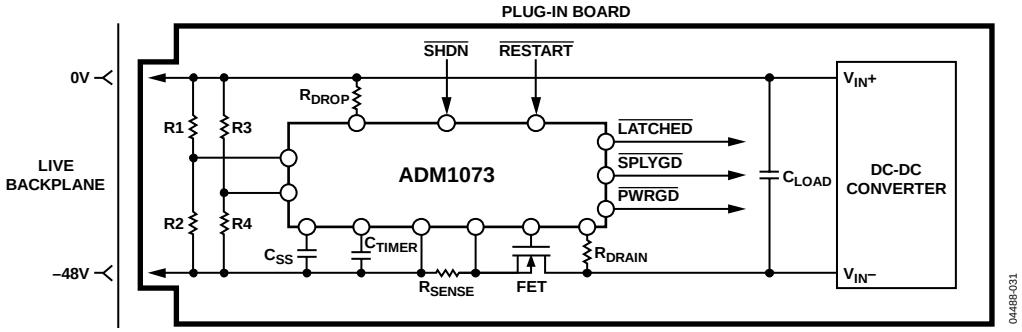

Figure 31. ADM1073 Topology

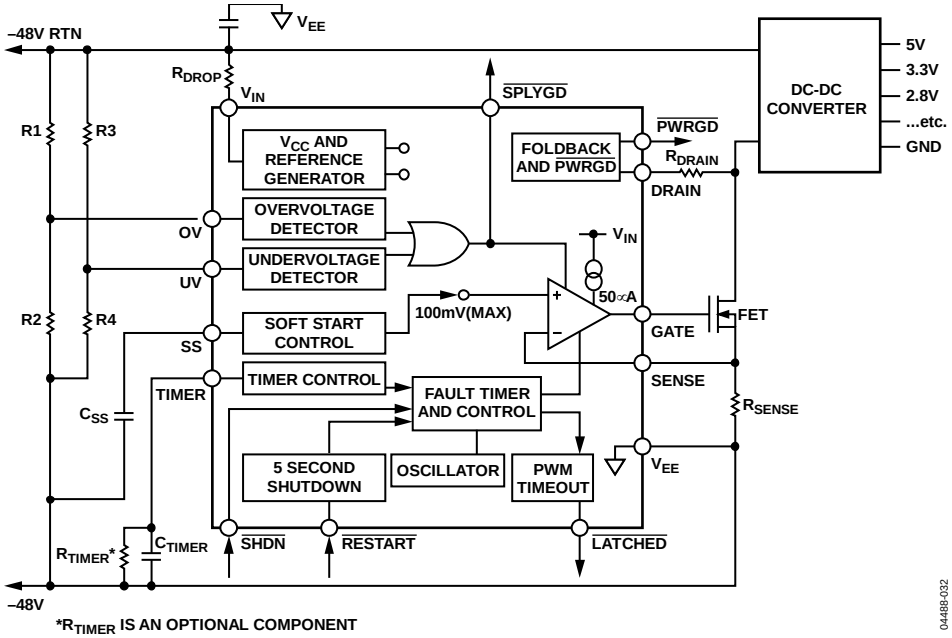

Figure 32. ADM1073 Application Diagram

When the device detects that the supply voltage is valid, it ramps up the GATE voltage until the FET turns on and the load current increases. The ADM1073 monitors the level of the current flowing through the FET by sensing the voltage across the external sense resistor, R_{SENSE}. When the SENSE voltage reaches 100 mV, the GATE pin is actively controlled, limiting the load current. In this way, the maximum current permitted to flow through the load is set by the choice of R_{SENSE}.

If a change in the level of the supply voltage causes the voltage on UV to fall below the undervoltage falling threshold (V_{UVF}), or the voltage on OV to rise above the overvoltage rising threshold (V_{OVR}), then the gate drive is disabled.

BOARD REMOVAL

If the board is removed from a card cage, the voltage on the UV pin falls to zero (that is, outside operating range) and the GATE drive is de-asserted, turning off the FET.

CONTROLLING THE CURRENT

The ADM1073 features the following current control functions:

- Precision maximum current limit
- Controlled time in current limit
- Limited number of consecutive maximum current events
- Current limit profiling—soft start
- Overcurrent fast limit

In the following sections, five distinct system operating conditions are described with reference to the current control features.

Startup into Nominal Load Capacitance

Once the supply voltage has exceeded the UV threshold, and following the 0.6 ms UV filter time, the current to the load ramps up linearly as the capacitor on the Soft Start (SS) pin is charged to 2.5 V. At the same time, current is sourced into the capacitor on the TIMER pin, both from an on-chip source and via the drain resistor. Once the soft start voltage has reached 2.5 V, the current to the load is limited to I_{MAX} (100 mV/R_{SENSE}). Assuming that the values of R_{SENSE} and the TIMER capacitance have been chosen to allow the load capacitance to charge within one ON period (t_{ON} period), the load capacitor is fully charged before the voltage on TIMER reaches 2.5 V. At this point, the current to the load decreases, and the FET gate voltage increases to V_{SS}, connecting the supply to the load.

Startup into Load with Large Capacitance

If the load capacitance is sufficiently large that to charge it fully in one attempt would compromise the FET's SOA, consecutive maximum current events may be used. The use of this technique assumes that the load is not yet enabled, so negligible load current is demanded. The initial current profiling is identical to that for startup into a nominal load capacitance. If the charge passed to the load in time t_{ON} with maximum current flowing is insufficient to fully charge the load capacitance, at the end of the t_{ON} period the load capacitance is still demanding maximum current. The ADM1073 now controls the FET gate to zero for a time t_{OFF}, determined by the time taken for the on-chip current sink to discharge the TIMER capacitance to 0.5 V. At the end of time t_{OFF}, the device retries, again following the soft start current profile. In this way, a large load capacitance can be charged using consecutive current limit periods. The external components should be chosen to ensure that the capacitance is fully charged within seven TIMER periods, if the default limited consecutive retry mode is used.

Startup into a Short Circuit or over Current Fault

The load might demand large currents at initial connection. The ADM1073 follows the Soft Start current profile as described for startup into a nominal load. The current is limited at I_{MAX} for time t_{ON} following which the FET gate is pulled low. The FET gate is held low for time t_{OFF}, before retrying, again with the soft start current profile. The ADM1073 cycles through 7 retries, after which it latches the FET off, assuming the default limited consecutive retry mode is used.

Voltage Step during Normal Operation

Once the load capacitance is charged at initial board insertion and a $\overline{\text{PWRGD}}$ signal is issued by the ADM1073, the load begins to demand current. Therefore, following a step increase in the magnitude of the supply voltage, not all the FET current is available for charging of the load capacitance. Because the FET is fully on following a step in the supply voltage, the current increases immediately from I_{LOAD} to supply charge to the load capacitance. If the current remains below the fast current limit, the FET gate drive amplifier controls it back to I_{MAX}. If the current exceeds the fast current limit, the FET gate is strongly pulled down and back into regulation with the current at I_{MAX}. The size of the voltage step and the headroom between the load current and I_{MAX} determine the time required at I_{MAX} to charge the load capacitance. External components should be chosen to ensure that any expected step size leads to a requirement of less than time t_{ON} to charge the load capacitance.

Short Circuit or Overcurrent Fault during Operation

If a short circuit or an overcurrent fault occurs during normal operation, the FET is fully on and initially allows increased current to flow. If the current remains below the fast current limit, the FET gate drive amplifier controls it back to I_{MAX}. If the current exceeds the fast current limit, the FET gate is strongly pulled down and back into regulation with the current at I_{MAX}. Following a period, t_{ON}, the ADM1073 pulls the FET gate low for a time t_{OFF}, then retries following the soft start current profile. If the fault persists, the ADM1073 cycles through 7 retries before latching off. If the fault clears within the 7-retry period, the ADM1073 controls the FET gate high to allow normal operation to continue.

SENSE

The SENSE pin is used for sensing the voltage across an external power sense resistor. This voltage is differentially measured with respect to V_{EE}, and used to control the GATE. If SENSE is lower than 100 mV (after the soft start time), the GATE pin is allowed to increase up to 12 V to provide maximum FET enhancement. If the current increases such that the SENSE pin tries to go above 100 mV, the GATE pin is controlled in a feedback loop to ensure that the voltage across the sense resistor is regulated at exactly 100 mV.

SENSE RESISTOR

The ADM1073's current limiting function can operate at different current levels. The current limit is determined by selection of the sense resistor, R_{SENSE}. Table 4 shows how the maximum allowable load current ($I_{LOAD(MAX)}$) and the minimum and maximum inrush currents ($I_{LIMIT(MIN)}$ and $I_{LIMIT(MAX)}$) are related to the value of R_{SENSE}.

Table 4. Minumum and Maximum Inrush Current and Load Current Levels for Different Values of R_{SENSE}

R_{SENSE} (mΩ)	$I_{LOAD(MAX)}$ (A)	$I_{LIMIT(MIN)}$ (A)	$I_{LIMIT(MAX)}$ (A)
5	17.20	19.40	20.60
10	8.60	9.70	10.30
15	5.73	6.47	6.87
18	4.78	5.39	5.72
22	3.91	4.41	4.68
33	2.61	2.94	3.12
47	1.83	2.06	2.19
51	1.69	1.90	2.02
68	1.26	1.43	1.51
75	1.15	1.29	1.37
90	0.96	1.08	1.14

SOFT START (SS PIN)

The SS pin is used to determine the inrush current profile. A capacitor should be attached to this pin. Whenever the FET is requested to turn on, the SS pin is held at ground until the SENSE pin reaches a few mV. A current source is then turned on, which linearly ramps the capacitor up to 2.5 V. The reference voltage for the GATE linear control amplifier is derived from the soft start voltage, such that the inrush linear current limit is defined as

$$I_{LIMIT} = V_{SOFT\_START} / 20 \times R_{SENSE}$$

Overdriving the SS Pin

The SS pin can be overdriven externally from 0.360 V to 1.95 V to offset the current limit control loop threshold from 18 mV to 100 mV. This allows different current limits to be selected at different points of operation without using multiple sense resistors. The current limit voltage is clamped at 100 mV maximum.

GATE

Analog output for driving the external FET gate. This pin is switched to V_{EE} when the FET is off, is linearly controlled when the FET is at the programmed inrush current limit, and is switched to V_{IN} when the FET is fully enhanced. The source current capability is small to provide slow controlled turn-on, and the sink current capability is large to provide fast turn-off.

V_{IN}

Positive supply pin. This current-driven supply is shunt-regulated at 12.3 V internally, and should be connected to the most positive input supply terminal (usually −48 V RTN or 0 V) through a dropper resistor. The resistor should be chosen such that it always supplies enough current to overcome the maximum quiescent supply current of the chip. Default R_{DROP} = 30 kΩ.

V_{EE}

Negative supply input. This pin should be connected directly to the most negative input supply terminal (−48 V). This pin is also used for differentially sensing across the external power resistor, and should, therefore, be connected as close to the sense resistor as possible. (See the Kelvin Sense Resistor Connection section.)

TIMING CONTROL—TIMER

The TIMER pin is an analog pin that determines the maximum on-time when the FET is in linear current limit, and controls the PWM duty cycle for pulsed load capacitor charging. A capacitor should be attached to this pin. When the FET is in current limit, a 19 µA current source charges the external capacitor. If the FET is still in current limit when the TIMER capacitor reaches 2.5 V, the GATE driver is turned off and a 1 µA discharge current sink is turned on. The GATE remains low until the TIMER capacitor is reduced to 0.5 V. At this point, the GATE pin is turned on again. If the FET goes back into current limit, the TIMER recharging starts again.

The PWM duty cycle is set at 6% default level by the size of these two current sources. Adding a resistor from TIMER to V_{EE} decreases the duty cycle. Adding a resistor from TIMER to V_{IN} increases the duty cycle.

In addition, a current proportional to the current into the DRAIN pin is added to the charging current. The additional current varies linearly with DRAIN voltage. This reduces the maximum on-time and the percentage PWM duty cycle when there is a large voltage across the FET.

DRAIN

Analog input fed by a resistor connected to the drain of the FET. This pin is clamped to go no higher than 4 V with respect to V_{EE}. Below this level, the voltage on the pin is monitored so that, if it falls below 2 V, the $\overline{PWRGD}$ output can be set. Above the 4 V level, the current into the pin is detected and used to modulate the maximum on-time for the linear FET driver. This is done by summing a proportion of the drain input current with the charging current for the TIMER timing capacitor, thereby reducing the allowable on-time.

$\overline{PWRGD}$

Output to indicate when the load capacitor is fully charged. This is an open collector output with internal pull-up to V_{IN}. When a normal startup is initiated, the $\overline{PWRGD}$ output is latched low when the DRAIN pin falls below 2 V. The latch is reset, if either the input supply goes out of range or a current limit time-out event occurs. The second of these cases ensures that, if a voltage step of greater than 2 V is presented at the input, the $\overline{PWRGD}$ flag does not go high while the load capacitor is being charged up to the additional voltage.

$\overline{LATCHED}$

Output to indicate when the device has completed the maximum number (7) of PWM cycles. This is an open collector output with an internal current source pull-up. If this PWM time-out event occurs, the GATE pin is latched low and the $\overline{LATCHED}$ output is set low. This condition can then be reset by either a power cycling event or a low signal to either the $\overline{SHDN}$ input or the $\overline{RESTART}$ input. By connecting the $\overline{LATCHED}$ signal directly to $\overline{SHDN}$, the device can effectively be put into a continuous PWM mode. By connecting the $\overline{LATCHED}$ signal directly to $\overline{RESTART}$, the device can effectively be put into autoretry mode, with a 5-second cooling period.

$\overline{SPLYGD}$

Output to indicate when the input supply is within the programmed voltage window. This is an open collector output with an internal pull-up current source. For very large capacitive loads where multiple FETs and controllers are required to meet the inrush requirements, this output can be used to drive directly into the UV pin of a second controller. This allows the second FET to start 1 ms after the first one, with the added advantage that the input supply UV detection is done on one controller only. The $\overline{SPLYGD}$ output is asserted only when the ADM1073 is not in reset mode.

$\overline{RESTART}$

Edge-triggered input. Allows the user to remotely command a 5-second shutdown and restart of the hot swap function, effectively simulating a board removal and replacement. The shutdown function is triggered by a low pulse of at least 5 µs at the pin. This pin has an internal pull-up of approximately 6 µA, allowing it to be driven by an open collector pull-down output or a push-pull output. The input threshold is 1.5 V.

$\overline{SHDN}$

Level-triggered input. Allows the user to command a shutdown of the hot swap function. When this input is set low, the GATE output is switched to V_{EE} to turn the FET off. This pin has an internal pull-up of approximately 6 µA, allowing it to be driven by an open collector pull-down output or a push-pull output. The input threshold is 1.5 V.

UNDERVOLTAGE/OVERVOLTAGE DETECTION

The ADM1073 incorporates dual pin undervoltage and overvoltage detection, with a programmable operating voltage window. When the voltage on the UV pin falls below the UV falling threshold or the voltage on the OV pin rises above the OV rising threshold, a fault signal is generated that disables the linear current regulator and results in the GATE pin being pulled low. The voltage fault signal is time filtered so that faults of a duration less than the UV glitch filter time (0.6 ms) and OV glitch filter time (5 µs) do not force the gate drive low. The filter operates only on the faulting edge, that is, on a high-to-low transition on the undervoltage monitor and on a low-to-high transition on the overvoltage monitor.

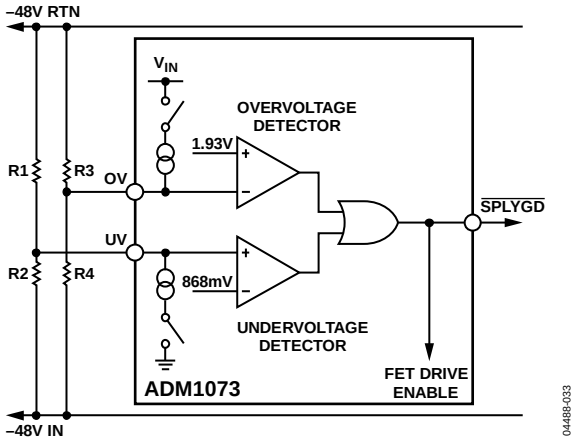

Figure 33. Undervoltage and Overvoltage Circuitry (Standard 4-Resistor Configuration)

The operating voltage window is determined by selecting the resistor ratios R1/R2 and R3/R4. These resistor networks form two resistor dividers that generate the voltages at the UV and OV pins, which are proportional to the supply voltage. By choosing these ratios carefully, the user can program the ADM1073 to apply the supply voltage to the load only when it is within specific thresholds. Note that 1% tolerance resistors should always be used to maintain the accuracy of the programmed thresholds.

UV (Undervoltage)

The voltage on the UV pin is compared to an internal 0.868 V reference. For the implementation in Figure 33, the undervoltage level is then set as

$$V_{UV} = 0.868 \times (R1 + R2)/R2$$

If the UV pin voltage is less than 0.868 V and the comparator trips, an internal 5 µA current sink is turned on. This pulls the UV voltage down by

$$V_{UVHYST(PIN)} = 5\ \mu A \times R1 \times R2/(R1 + R2)$$

at the UV pin, or by

$$V_{UVHYST(SUPPLY)} = 5\ \mu A \times R1$$

at the supply.

In this manner, the user can program the value of the voltage hysteresis by varying the parallel impedance of the resistor divider. The UV comparator has an internal 0.6 ms time delay to prevent nuisance shutdowns under noisy supply conditions.

OV (Overvoltage)

The voltage on the UV pin is compared to an internal 1.93 V reference. For the implementation in Figure 33, the overvoltage level is then set as

$$V_{OV} = 1.93 \times (R3 + R4)/R4$$

If the OV pin voltage exceeds 1.93 V and the comparator trips, an internal 5 µA current source is turned on. This pulls the OV voltage up by

$$V_{OVHYST(PIN)} = 5\ \mu A \times R3 \times R4/(R3 + R4)$$

at the OV pin, or by

$$V_{OVHYST(SUPPLY)} = 5\ \mu A \times R3$$

at the supply.

In this manner, the user can program the value of the voltage hysteresis by varying the parallel impedance of the resistor divider. The OV comparator has an internal 5 µs time delay.

If the voltage on UV or OV goes out of range (below 0.868 V on UV or above 1.93V on OV), GATE is pulled low. If the supply subsequently reenters the operating voltage window, the ADM1073 restores the GATE drive.

Hysteresis must be considered when reentering the operating window, that is, V_{UV} must increase above

$$0.868\ V + V_{UVHYST(SUPPLY)}$$

when recovering from an undervoltage fault, and V_{OV} must drop below

$$1.93\ V - V_{OVHYST(SUPPLY)}$$

when recovering from an overvoltage fault for GATE to be restored.

Alternative UV and OV Configurations

A 2-resistor or a 3-resistor implementation can also be used to set the UV and OV levels (see Figure 34 and Figure 35).

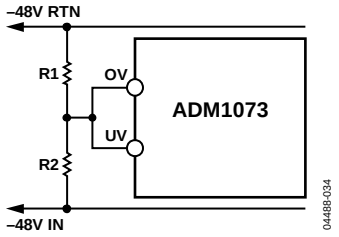

Figure 34. 2-Resistor UV/OV Implementation

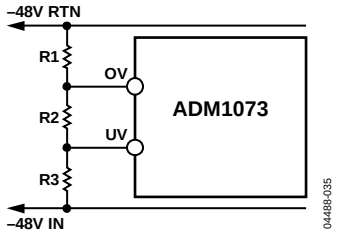

Figure 35. 3-Resistor UV/OV Implementation

FUNCTIONALITY AND TIMING

LIVE INSERTION

The timing waveforms associated with the live insertion of a plug-in board using the ADM1073 are shown in Figure 36. The long connector pins are the first to make connection, and the GND − V_{EE} potential climbs to 48 V. As this voltage is applied, the voltage at the V_{IN} pin ramps to a constant 12.3 V and is held at this level with the shunt resistor and external resistor combination at the V_{IN} pin. In this case, the connection pins are staggered so that the R1/R2 and R3/R4 resistor dividers are the last to connect to the backplane. This means that V_{UV} and V_{OV} begin to ramp after the other pins connect. Note that staggered connector pins are optional, because an internal time filter is included on the UV pin.

When V_{UV} crosses the undervoltage rising threshold, it is now inside the operating voltage window and the −48 V supply must be applied to the load. The $\overline{\text{SPLYGD}}$ output is asserted and after a time delay, t_{POR}, the ADM1073 begins to ramp up the gate drive. When the voltage on the SENSE pin reaches 100 mV (the analog current limit level), the gate drive is held constant. When the board capacitance is fully charged, the sense voltage begins to drop below the analog current limit voltage and the gate voltage is free to ramp up further. The gate voltage eventually climbs to its maximum value of 12.3 V and the $\overline{\text{PWRGD}}$ output is asserted. Figure 37 shows some typical startup waveforms.

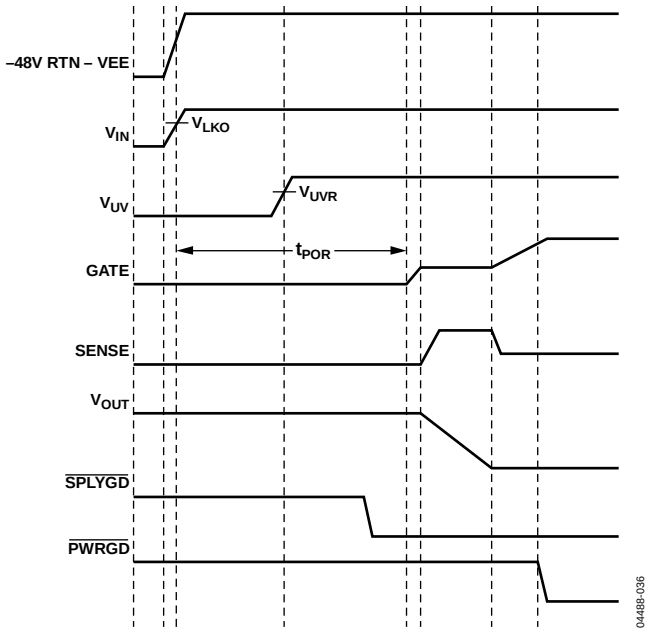

Figure 36. Timing Waveforms Associated with a Live Insertion Event

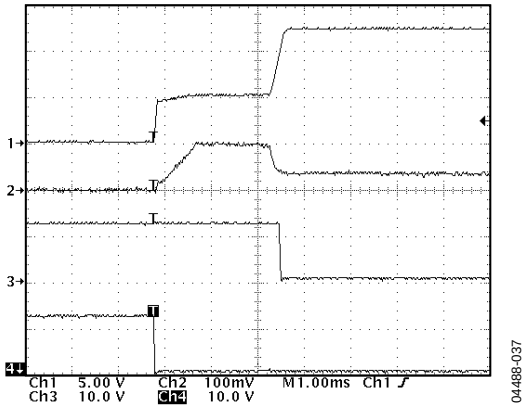

Figure 37. Typical Startup Sequence (Ch1 = GATE; Ch2 = SENSE; Ch3 = $\overline{\text{PWRGD}}$; Ch4 = $\overline{\text{SPLYGD}}$)

OVERVOLTAGE AND UNDERVOLTAGE FAULTS

The waveforms for an overvoltage glitch are shown in Figure 38. When V_{OV} glitches above the overvoltage threshold of 1.93 V, an overvoltage condition is detected and the GATE voltage is pulled low. V_{OV} begins to drop back toward the operating voltage window, and the GATE drive is restored when the overvoltage falling threshold (1.93 V minus preset OV hysteresis level) is reached. Figure 38 illustrates the ADM1073's reactions to an overvoltage condition.

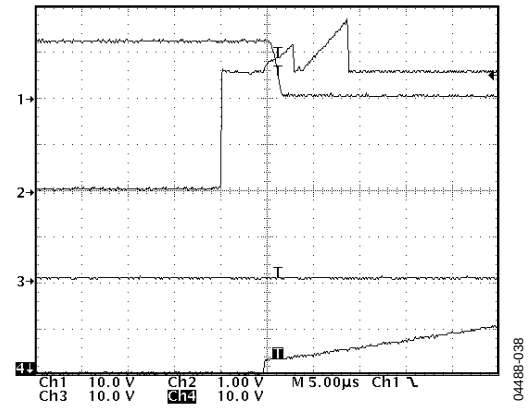

Figure 38. Timing Waveforms Associated with an Overvoltage Fault (Ch1 = GATE; Ch2 = OV; Ch3 = $\overline{\text{PWRGD}}$; Ch 4 = $\overline{\text{SPLYGD}}$)

An undervoltage glitch is dealt with in a similar way. When V_{UV} falls below the undervoltage threshold of 0.868 V, the GATE voltage is pulled low. V_{UV} begins to rise back toward the operating voltage window, and the GATE drive is restored when the undervoltage rising threshold (0.868 V plus preset UV hysteresis level) is reached. Figure 39 illustrates the ADM1073's operation in an undervoltage situation.

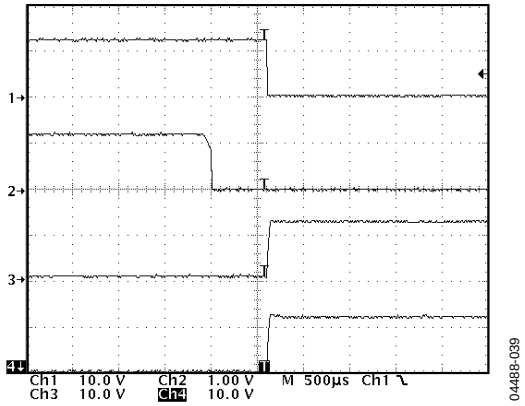

Figure 39. Timing Waveforms Associated with an Undervoltage Fault (Ch1 = GATE; Ch2 = UV; Ch3 = $\overline{PWRGD}$; Ch4 = $\overline{SPLYGD}$)

SOFT START

The ADM1073 offers a variable soft start feature. The value of the capacitor on the SS pin sets the ramp rate of the inrush current profile at startup. Figure 40 to Figure 42 show different inrush current ramp rates for three SS capacitors.

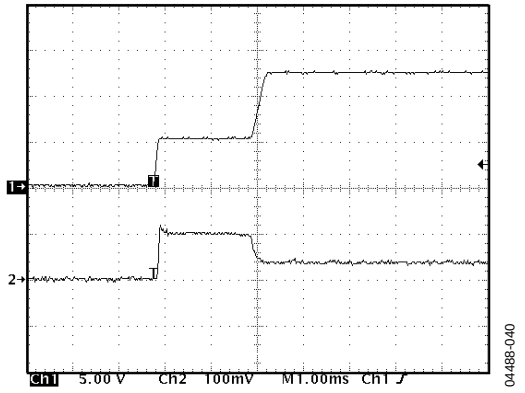

Figure 40. Soft Start Profile with a 0.1 nF Capacitor (Ch1 = GATE; Ch2 = SENSE)

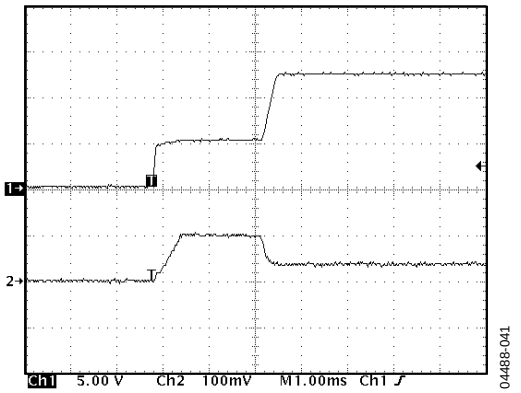

Figure 41. Soft Start Profile with a 1.5 nF Capacitor (Ch1 = GATE; Ch2 = SENSE)

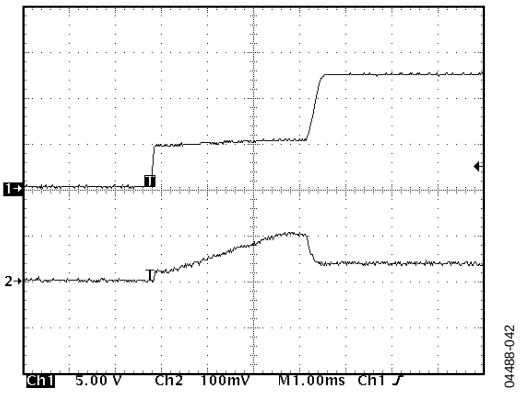

Figure 42. Soft Start Profile with an 8.2 nF Capacitor (Ch1 = GATE; Ch2 = SENSE)

CURRENT FAULTS

Some timing waveforms associated with overcurrent faults are shown in the following figures. Figure 43 shows how a permanent current fault is dealt with after startup. $\overline{\text{SPLYGD}}$ going low indicates when the supply voltage is good. Because the output is shorted, the sense voltage immediately rises through the 90 mV circuit breaker threshold, and the fault timer is started. The linear current control loop then goes into regulation at V_{SENSE} = 100 mV, accurately limiting the load current at the preset level. The limited consecutive retry scheme PWMs the GATE pin seven times. When the seventh retry occurs, the permanent fault is deemed permanent and the part latches off. The $\overline{\text{LATCHED}}$ output asserts at this time. Power must now be cycled to restart the device. This can be achieved via a manual card reseating event (which cycles the power) or with an external $\overline{\text{RESTART}}$ or $\overline{\text{SHDN}}$ signal.

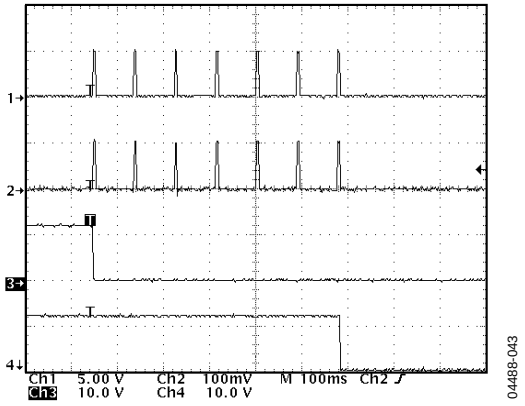

Figure 43. Timing Waveforms Associated with a Current Fault at Startup, Using Limited Consecutive Retry (Ch1 = GATE; Ch2 = SENSE; Ch3 = $\overline{\text{SPLYGD}}$; Ch4 = $\overline{\text{LATCHED}}$)

Note that the $\overline{\text{LATCHED}}$ output can also be tied back to the $\overline{\text{RESTART}}$ input, giving an infinite retry during current fault with a 5-second cool-down period after every seven retries. The waveforms for this event are similar to those in Figure 43, but repeats every five seconds.

Figure 44 shows the behavior of ADM1073 when a temporary current fault occurs followed by a permanent current fault. When the first overcurrent fault occurs, the first 97.5 mV spike on the SENSE line can be seen. The ADM1073 retries a number of times, and during the fifth t_{OFF} time this current fault corrects itself. After this time period, a no-fault condition is detected and the limited consecutive counter is reset. GATE is reasserted.

When the overcurrent fault returns permanently, the limited consecutive retry counter detects seven consecutive faults and the part latches off. In this way, the ADM1073 prevents nuisance shutdowns caused by transient shorts of a programmable duration (typically ~0.6 s, set via TIMER, as follows), but provides latched shutdown protection from permanently shorted loads.

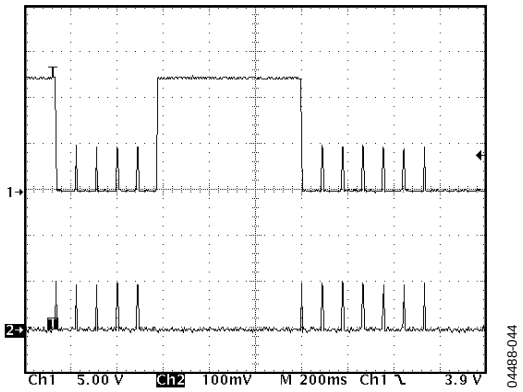

Figure 44. Timing Waveforms Associated with a Temporary Current Fault Followed by a Permanent Current Fault (Ch1 = GATE; Ch2 = SENSE)

Figure 45 shows the behavior of the TIMER pin during a retry cycle. Different current sources are switched in during the on-time (TIMER ramping up) and off-times (TIMER ramping down). This can be seen in the varying ramp-up and ramp-down rates of TIMER below. The default ratio of t_{ON} to t_{OFF} is 6%. This ratio can be reduced with a resistor from TIMER to V_{EE} or increased with a resistor from TIMER to V_{IN}. The total retry period can be extended or reduced by changing the value of the TIMER capacitor.

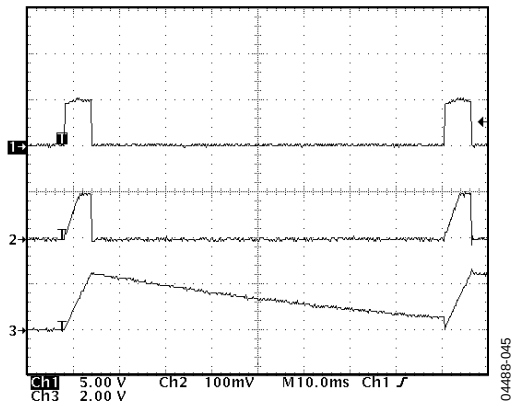

Figure 45. Timing Waveforms during a Retry Cycle for C_{TIMER} = 0.82 nF (Ch1 = GATE; Ch2 = SENSE; Ch3 = TIMER)

LOGIC INPUTS

Figure 46 shows assertion of the level-triggered $\overline{\text{SHDN}}$ signal for 150 ms, causing the ADM1073 to shut down for this duration.

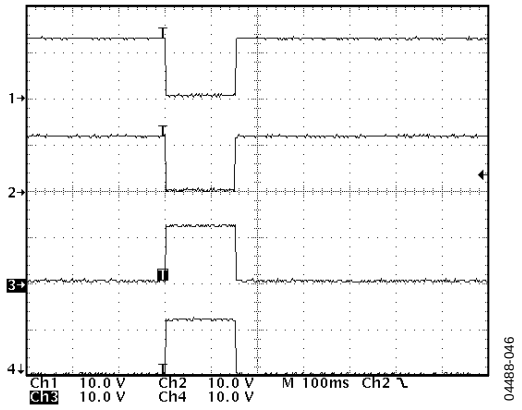

Figure 46. Timing Waveforms Associated with a RESET Event (Ch1 = GATE; Ch2 = $\overline{\text{SHDN}}$; Ch3 = $\overline{\text{PWRGD}}$; Ch4 = $\overline{\text{SPLYGD}}$)

Figure 47 shows the assertion of the edge-triggered $\overline{\text{RESTART}}$ signal, causing the ADM1073 to shut down for approximately five seconds before restarting automatically.

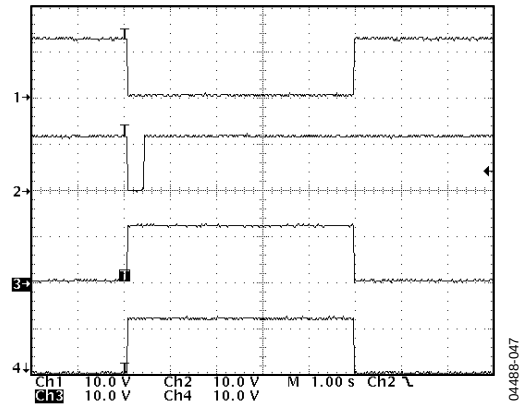

Figure 47. Timing Waveforms Associated with a $\overline{\text{RESTART}}$ Event (Ch1 = GATE; Ch2 = $\overline{\text{RESTART}}$; Ch3 = $\overline{\text{PWRGD}}$; Ch4 = $\overline{\text{SPLYGD}}$)

KELVIN SENSE RESISTOR CONNECTION

When using a low-value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 48 shows the correct way to connect the sense resistor between the SENSE and V_{EE} pins of the ADM1073.

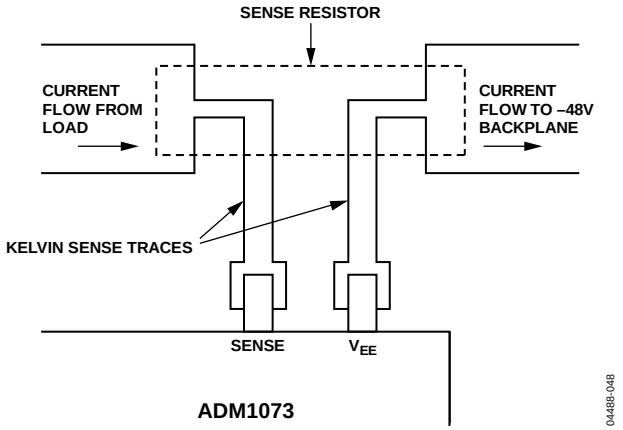

Figure 48. Kelvin Sensing with the ADM1073

OUTLINE DIMENSIONS

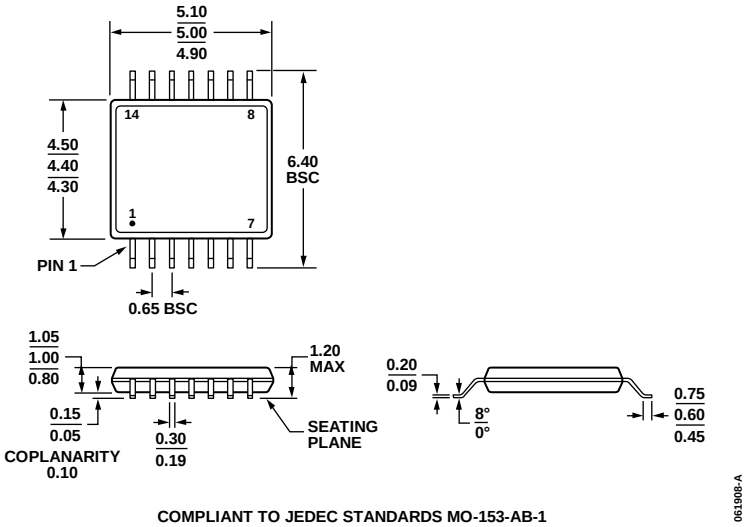

Figure 49. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM1073ARUZ	−40°C to +85°C	14-Lead TSSOP	RU-14
ADM1073ARUZ-REEL	−40°C to +85°C	14-Lead TSSOP	RU-14
ADM1073ARUZ-REEL7	−40°C to +85°C	14-Lead TSSOP	RU-14
EVAL-ADM1073MEBZ		Micro Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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