ADL5513* PRODUCT PAGE QUICK LINKS

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- ADL5513 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1040: RF Power Calibration Improves Performance of Wireless Transmitters

Data Sheet

- ADL5513: 1 MHz to 4 GHz, 80 dB Logarithmic Detector/ Controller Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF
- ADL5513 S-Parameters

REFERENCE DESIGNS

- CN0072

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Design a Logamp RF Pulse Detector
- Detecting Fast RF Bursts using Log Amps
- Log Amps and Directional Couplers Enable VSWR Detection
- Make Precise Base-Station Power Measurements
- Measurement and Control of RF Power, Part I
- Measurement and Control of RF Power, Part II
- Measurement and Control of RF Power, Part III
- Measuring the RF Power in CDMA2000 and W-CDMA High Power Amplifiers (HPAs)
- Measuring VSWR and Gain in Wireless Systems

DESIGN RESOURCES

- ADL5513 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

8/2017—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 25
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10/2008—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_0 = 50 Ω, Pin INHI and Pin INLO are ac-coupled, continuous wave (CW) input, single-ended input drive, VOUT tied to VSET, error referred to best-fit line (linear regression −20 to −40 dBm), unless otherwise noted. (Temperature adjust voltage optimized for 85°C.)

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency		1		4000	MHz
FREQUENCY = 100 MHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm	1.50	1.63	1.76	V
Output Voltage: Low Power Input	P_{IN} = −50 dBm	0.64	0.79	0.94	V
±3.0 dB Dynamic Range			75		dB
±1.0 dB Dynamic Range			64		dB
±0.5 dB Dynamic Range			58		dB
Maximum Input Level, ±1.0 dB			6		dBm
Minimum Input Level, ±1.0 dB			−58		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.27		dB
	P_{IN} = −30 dBm		0.003		dB
	P_{IN} = −50 dBm		−0.14		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		+0.15/−0.33		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.23/−0.43		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		0.8		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.12/−0.31		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		±0.31		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		+0.74		dB
	+25°C < T_A < +85°C; P_{IN} = −50 dBm		+0.35/−0.18		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		+0.25/−0.47		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		+0.52/−0.24		dB
Logarithmic Slope		19.5	21	22.5	mV/dB
Logarithmic Intercept			−87		dBm
Input Impedance			1.3/0.4		kΩ/pF
FREQUENCY = 900 MHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm		1.64		V
Output Voltage: Low Power Input	P_{IN} = −50 dBm		0.79		V
±3.0 dB Dynamic Range			76		dB
±1.0 dB Dynamic Range			70		dB
±0.5 dB Dynamic Range			68		dB
Maximum Input Level, ±1.0 dB			8		dBm
Minimum Input Level, ±1.0 dB			−62		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.2		dB
	P_{IN} = −30 dBm		0.002		dB
	P_{IN} = −50 dBm		0.34		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		+0.25/−0.3		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.2/−0.53		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		+0.72/−0.1		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.2/−0.3		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		+0.28/−0.37		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		0.7		dB
	25°C < T_A < 85°C; P_{IN} = −50 dBm		+0.4/−0.36		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		+0.37/−0.5		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		+0.67/−0.28		dB

Parameter	Conditions	Min	Typ	Max	Unit
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			−88		dBm
Input Impedance			1.3/0.4		kΩ/pF
FREQUENCY = 1900 MHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm		1.66		V
Output Voltage: Low Power Input	P_{IN} = −50 dBm		0.80		V
±3.0 dB Dynamic Range			75		dB
±1.0 dB Dynamic Range			70		dB
±0.5 dB Dynamic Range			68		dB
Maximum Input Level, ±1.0 dB			8		dBm
Minimum Input Level, ±1.0 dB			−62		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.25		dB
	P_{IN} = −30 dBm		0.0012		dB
	P_{IN} = −50 dBm		0.52		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		+0.14/−0.41		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.19/−0.51		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		0.9		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.1/−0.38		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		+0.37/−0.26		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		0.83		dB
	25°C < T_A < 85°C; P_{IN} = −50 dBm		+0.55/−0.3		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		+0.79/−0.16		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		+0.62/−0.41		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			−88		dBm
Input Impedance			0.6/0.5		kΩ/pF
FREQUENCY = 2140 MHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm		1.66		V
Output Voltage: Low Power Input	P_{IN} = −50 dBm		0.82		V
±3.0 dB Dynamic Range			77		dB
±1.0 dB Dynamic Range			70		dB
±0.5 dB Dynamic Range			66		dB
Maximum Input Level, ±1.0 dB			8		dBm
Minimum Input Level, ±1.0 dB			−62		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.33		dB
	P_{IN} = −30 dBm		0.02		dB
	P_{IN} = −50 dBm		0.23		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		±0.28		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.2/−0.52		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		+0.7/−0.1		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.15/−0.35		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		+0.24/−0.41		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		0.77		dB
	25°C < T_A < 85°C; P_{IN} = −50 dBm		+0.2/−0.6		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		+0.1/−0.94		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		+0.8/−0.2		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			−89		dBm
Input Impedance			0.5/0.5		kΩ/pF

Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY = 2600 MHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm		1.67		V
Output Voltage: Low Power Input	P_{IN} = −50 dBm		0.83		V
±3.0 dB Dynamic Range			80		dB
±1.0 dB Dynamic Range			74		dB
±0.5 dB Dynamic Range			69		dB
Maximum Input Level, ±1.0 dB			7		dBm
Minimum Input Level, ±1.0 dB			−67		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.33		dB
	P_{IN} = −30 dBm		0.02		dB
	P_{IN} = −50 dBm		0.01		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		+0.2/−0.4		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.05/−0.68		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		+0.75/−0.05		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.1/−0.37		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		+0.25/−0.4		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		0.8		dB
	25°C < T_A < 85°C; P_{IN} = −50 dBm		+0.2/−0.6		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		±0.5		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		1.13		dB
Logarithmic Slope			21		mV/dB
Logarithmic Intercept			−89		dBm
Input Impedance			0.4/0.6		kΩ/pF
FREQUENCY = 3.6 GHz					
Output Voltage: High Power Input	P_{IN} = −10 dBm		1.74		V
Output Voltage: Low Power Input	P_{IN} = −50 dBm		0.84		V
±3.0 dB Dynamic Range			76		dB
±1.0 dB Dynamic Range			62		dB
±0.5 dB Dynamic Range			58		dB
Maximum Input Level, ±1.0 dB			1		dBm
Minimum Input Level, ±1.0 dB			−61		dBm
Deviation at T_A = 25°C	P_{IN} = −10 dBm		0.43		dB
	P_{IN} = −30 dBm		−0.05		dB
	P_{IN} = −50 dBm		−0.14		dB
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	25°C < T_A < 85°C; P_{IN} = −10 dBm		+0.32/−0.28		dB
	−40°C < T_A < +25°C; P_{IN} = −10 dBm		+0.27/−0.54		dB
	25°C < T_A < 125°C; P_{IN} = −10 dBm		+0.58/−0.21		dB
	25°C < T_A < 85°C; P_{IN} = −30 dBm		+0.3/−0.22		dB
	−40°C < T_A < +25°C; P_{IN} = −30 dBm		+0.38/−0.33		dB
	25°C < T_A < 125°C; P_{IN} = −30 dBm		+0.67/−0.05		dB
	25°C < T_A < 85°C; P_{IN} = −50 dBm		+0.41/−0.37		dB
	−40°C < T_A < +25°C; P_{IN} = −50 dBm		+0.41/−0.62		dB
	25°C < T_A < 125°C; P_{IN} = −50 dBm		+0.8/−0.18		dB
Logarithmic Slope			22.5		mV/dB
Logarithmic Intercept			−87		dBm
Input Impedance			0.5/0.4		kΩ/pF
SETPOINT INPUT	Pin VSET				
Nominal Range	Log conformance error ≤ ±1 dB, RF input = 8 dBm		2		V
	Log conformance error ≤ ±1 dB, RF input = −62 dBm		0.58		V
Logarithmic Scale Factor			47.1		dB/ V
Input Impedance			40		kΩ

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT INTERFACE	Pin VOUT				
Voltage Swing	V_{SET} = 0 V, RF input = open		0.47		V
	V_{SET} = 0.47 V, RF input = open		4.7		V
Capacitance Drive	CLPF = open		47		pF
Capacitance Drive	CLPF = 20 pF		1		nF
Current Source/Sink	Output held at 1 V to 1% change		0.64/55		mA
Output Noise	RF input = 100 MHz, 0 dBm				
	f_{NOISE} = 100 kHz, CLPF = open		145		nV/√Hz
	f_{NOISE} = 100 kHz, CLPF = 1 nF		82		nV/√Hz
PULSE RESPONSE TIME	Input level = no signal to 0 dBm, 90% to 10%				
Fall Time	CLPF = open, 1 µs pulse width		21		ns
	CLPF = open, 500 µs pulse width		5.5		µs
Rise Time	CLPF = open, 1 µs pulse width		20		ns
	CLPF = open, 500 µs pulse width		20		ns
Fall Time	CLPF = 1000 pF, 10 µs pulse width		4.2		µs
	CLPF = 1000 pF, 500 µs pulse width		5.5		µs
Rise Time	CLPF = 1000 pF, 10 µs pulse width		3.2		µs
	CLPF = 1000 pF, 500 µs pulse width		4.3		µs
Small Signal Video Bandwidth (or Envelope Bandwidth)	CLPF = open, 3 dB video bandwidth		10		MHz
TEMPERATURE ADJUST/POWER-DOWN INTERFACE	Pin TADJ				
Temperature Adjust Useful Range			0 to 1.3		V
Minimum Logic Level to Disable	Logic high disables		V_{POS} − 0.3		V
Input Current	Logic high TADJ = 0 V		31		mA
	Logic low TADJ = 4.7 V		200		µA
Enable Time	PWDN low to VOUT at 100% final value, PWDN high to VOUT at 10% final value				
	CLPF = open, RF input = 0 dBm, 100 MHz, 1 µs pulse width		84		ns
	CLPF = 1000 pF, RF input = 0 dBm, 100 MHz, 1 µs pulse width		10.8		µs
Disable Time	CLPF = open, RF input = 0 dBm, 100 MHz, 1 µs pulse width		165		ns
	CLPF = 1000 pF, RF input = 0 dBm, 100 MHz, 1 µs pulse width		1.2		µs
Input Impedance[1]	TADJ = 0.9 V, sourcing 70 µA		13		kΩ
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		2.7		5.5	V
Quiescent Current	25°C, RF input = −55 dBm		31		mA
Supply Current	When disabled		<0.2		mA

[1] See the Temperature Compensation of Output Voltage section.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
V_{SET} Voltage	0 V to V_{POS}
Input Power (Single-Ended, Re: 50 Ω)	20 dBm
Internal Power Dissipation	220 mW
θ_{JA}	79.3°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

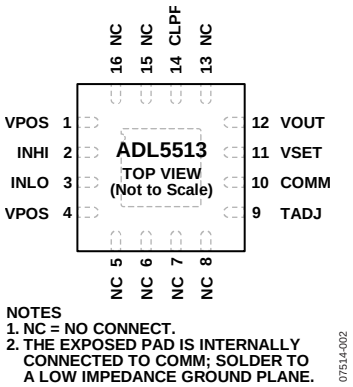


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	VPOS	Positive Supply Voltage, 2.7 V to 5.5 V.
2	INHI	RF Input. AC-coupled RF input.
3	INLO	RF Common for INHI. AC-coupled RF common.
5, 6, 7, 8, 13, 15, 16	NC	No Connect. These pins can be left open or be soldered to a low impedance ground plane.
9	TADJ	Temperature Compensation Adjustment. Frequency-dependent temperature compensation is set by applying a specified voltage to the pin. The TADJ pin has dual functionality as a power-down pin, PWDN. Applying a voltage of V_{POS} − 0.3 V disables the device.
10	COMM	Device Common.
11	VSET	Setpoint Input for Operation in Controller Mode. To operate in RSSI mode short VSET to VOUT.
12	VOUT	Logarithmic/Error Output.
14	CLPF	Loop Filter Capacitor Pin. In measurement mode, this capacitor pin sets the pulse response time and video bandwidth. In controller mode, the capacitance on this node sets the response time of the error amplifier/integrator.
15 (EPAD)	Exposed Pad (EPAD)	Internally connected to COMM; solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V; T_A = +25°C, −40°C, +85°C, +125°C; C_{LPF} = 0.1 µF, error is calculated by using the best-fit line between P_{IN} = −20 dBm and P_{IN} = −40 dBm at the specified input frequency, unless otherwise noted.

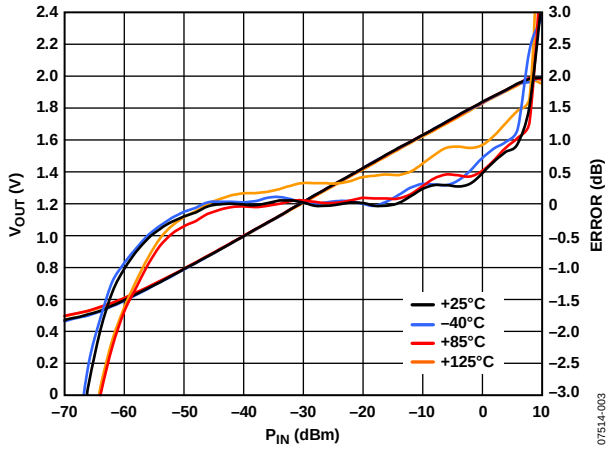


Figure 3. V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz, Typical Device, V_{TADJ} = 0.89 V

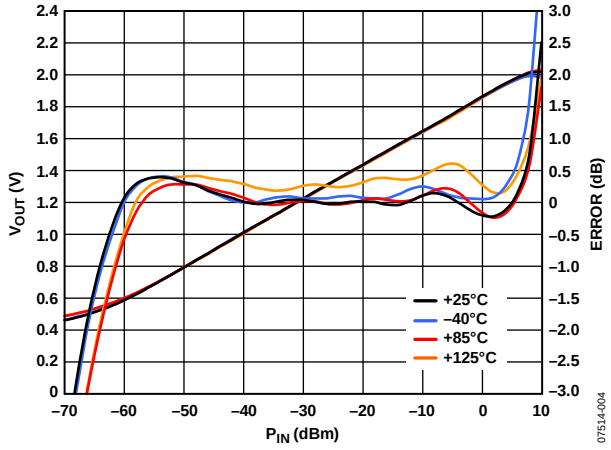


Figure 4. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device, V_{TADJ} = 0.86 V

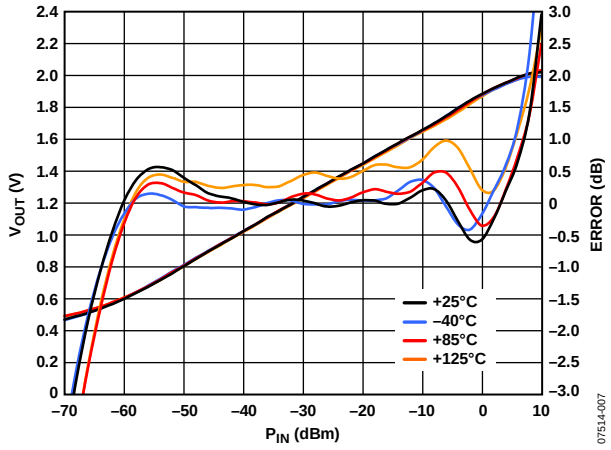


Figure 5. V_{OUT} and Log Conformance vs. Input Amplitude at 1900 MHz, Typical Device, V_{TADJ} = 0.80 V

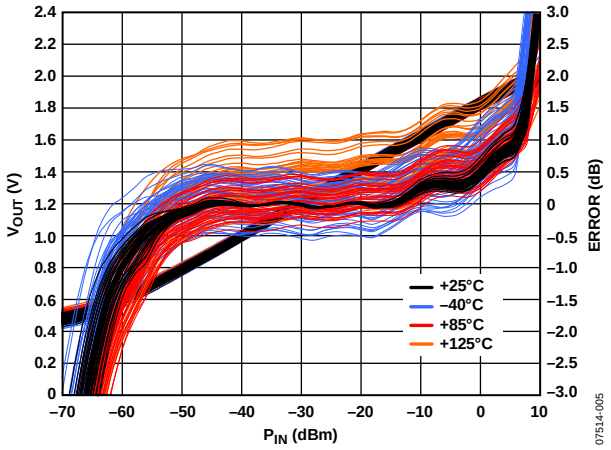


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz, Multiple Devices, V_{TADJ} = 0.89 V

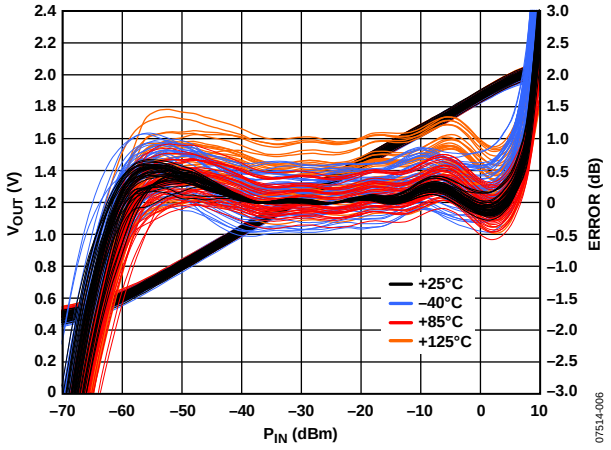


Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, Multiple Devices, V_{TADJ} = 0.86 V

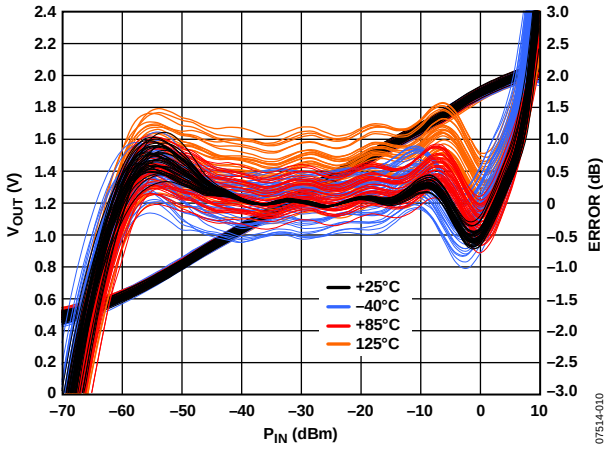


Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 1900 MHz, Multiple Devices, V_{TADJ} = 0.80 V

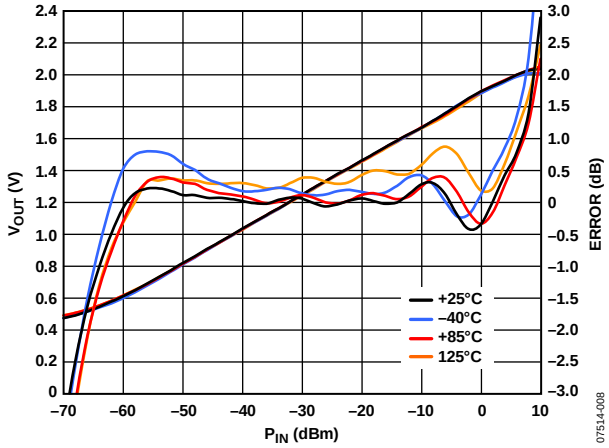


Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 2140 MHz, Typical Device, V_{TADJ} = 0.84 V

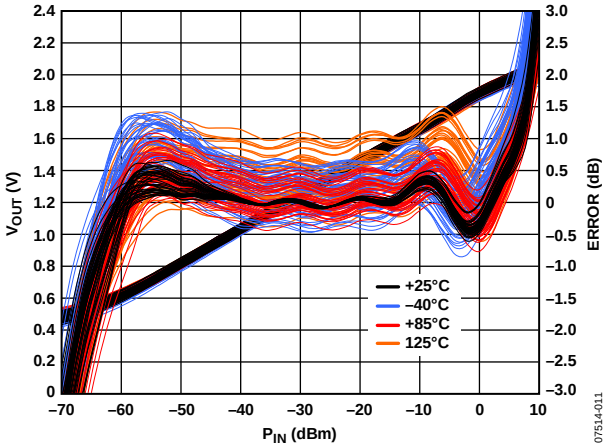


Figure 12. V_{OUT} and Log Conformance vs. Input Amplitude at 2140 MHz, Multiple Devices, V_{TADJ} = 0.84 V

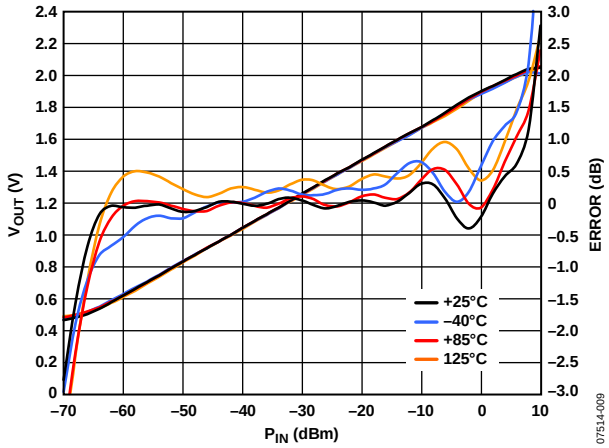


Figure 10. V_{OUT} and Log Conformance vs. Input Amplitude at 2600 MHz, Typical Device, V_{TADJ} = 0.83 V

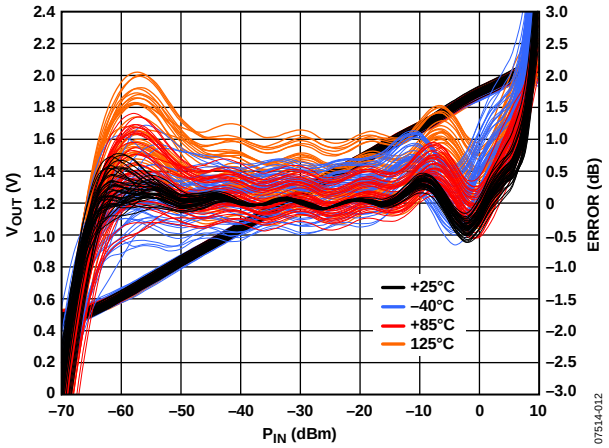


Figure 13. V_{OUT} and Log Conformance vs. Input Amplitude at 2600 MHz, Multiple Devices, V_{TADJ} = 0.83 V

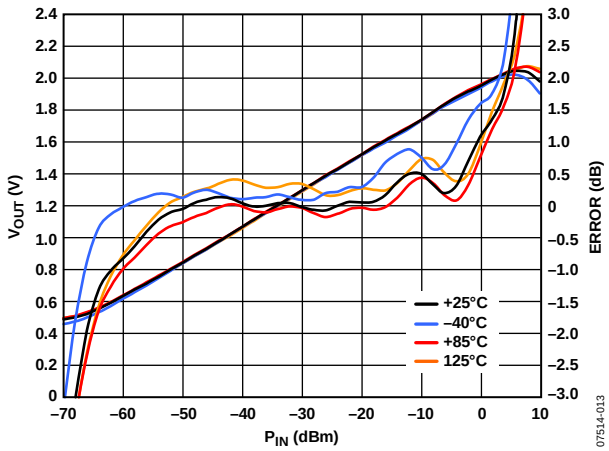


Figure 11. V_{OUT} and Log Conformance vs. Input Amplitude at 3600 MHz, Typical Device, V_{TADJ} = 0.90 V

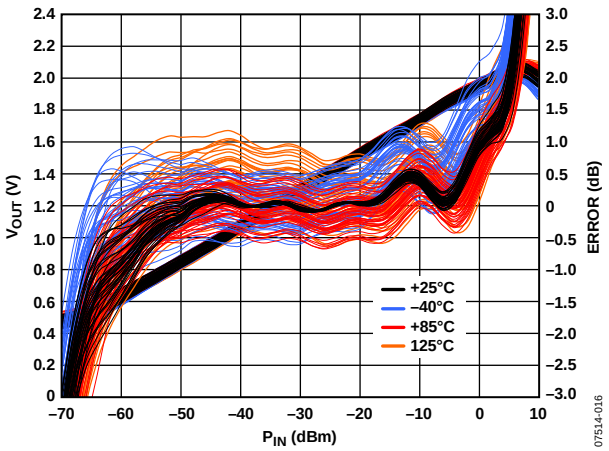


Figure 14. V_{OUT} and Log Conformance vs. Input Amplitude at 3600 MHz, Multiple Devices, V_{TADJ} = 0.90 V

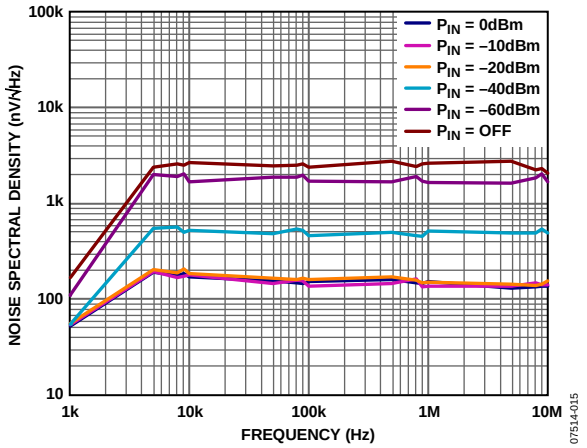


Figure 15. Output Noise Spectral Density, CLPF = Open

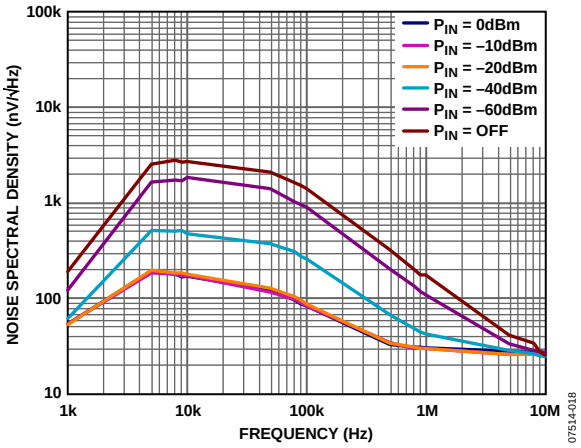


Figure 18. Output Noise Spectral Density, CLPF = 1 nF

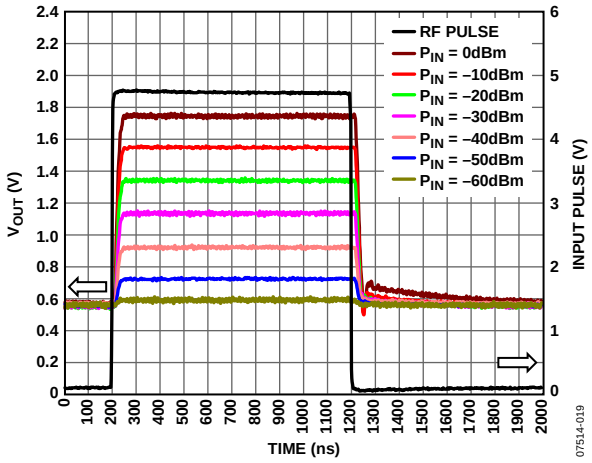


Figure 16. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency = 100 MHz, CLPF = Open

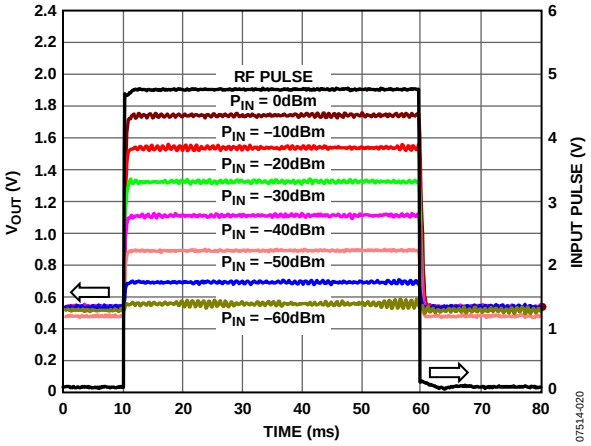


Figure 19. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency = 100 MHz, CLPF = 0.1 µF

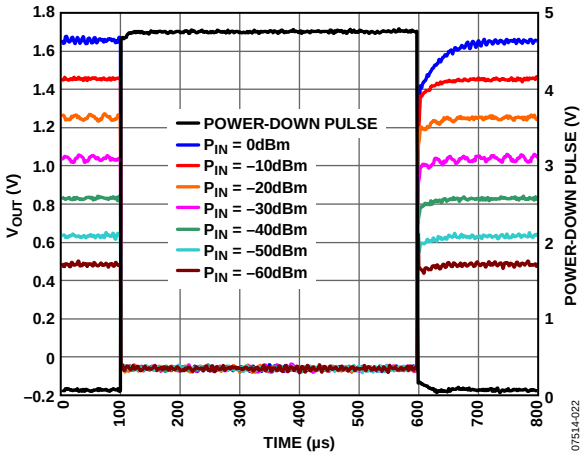


Figure 17. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 100 MHz, CLPF = Open

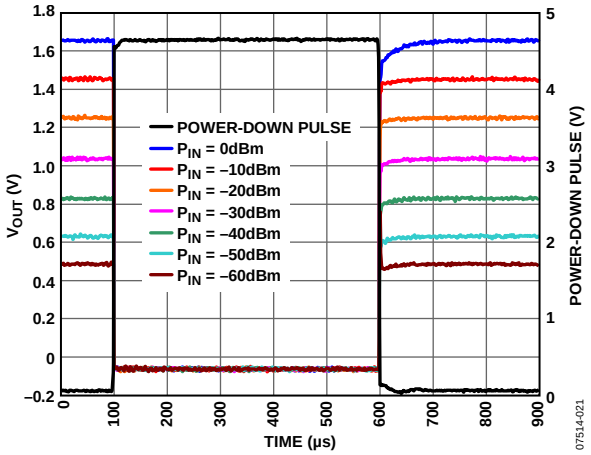


Figure 20. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 100 MHz, CLPF = 10 pF

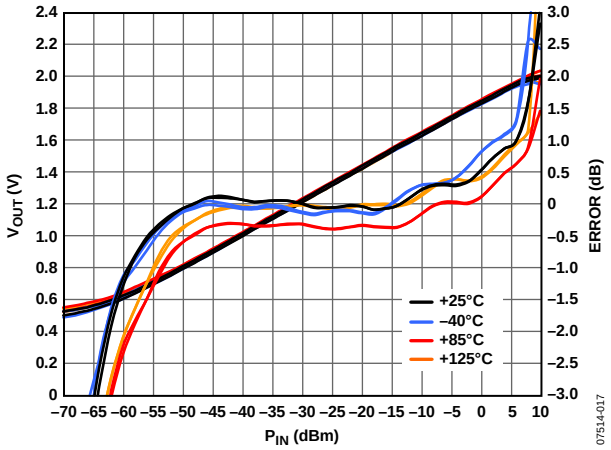


Figure 21. Output Voltage Stability vs. Input Amplitude at 1900 MHz When V_{POS} Varies from 2.7 V to 5.5 V

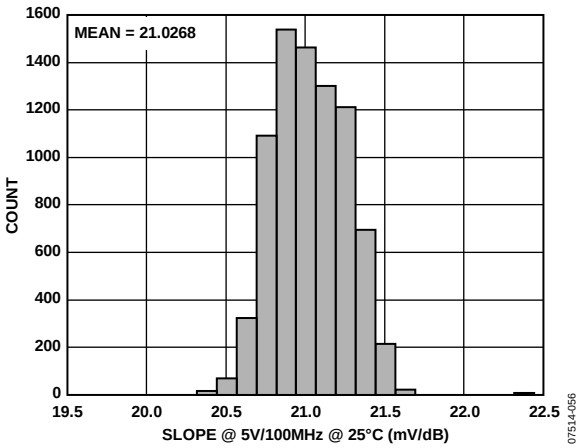


Figure 23. Slope Distribution, 100 MHz

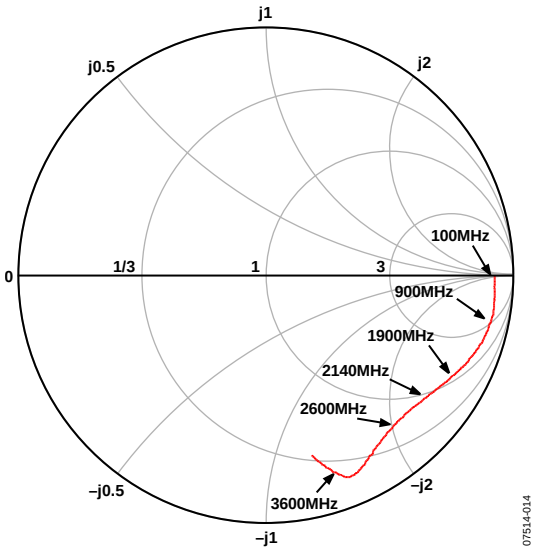


Figure 22. Input Impedance vs. Frequency, No Termination Resistor on INHI, $Z_0 = 50\ \Omega$

THEORY OF OPERATION

The ADL5513 is a demodulating logarithmic amplifier, specifically designed for use in RF measurement and power control applications at frequencies up to 4 GHz. A block diagram is shown in Figure 24. Sharing much of its design with the AD8313 logarithmic detector/controller, the ADL5513 maintains tight intercept variability vs. temperature over a 80 dB range. Additional enhancements over the AD8313, such as a reduced RF burst response time of 20 ns and board space requirements of only 3 mm × 3 mm, add to the low cost and high performance benefits found in the ADL5513.

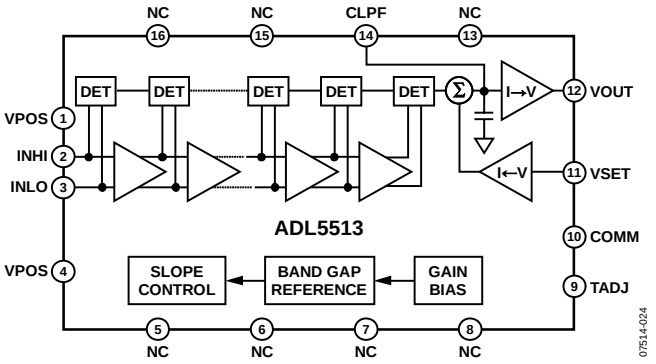


Figure 24. Block Diagram

A fully differential design, using a proprietary, high speed SiGe process, extends high frequency performance. The maximum input with ±1 dB log conformance error is typically 10 dBm (referred to 50 Ω). The noise spectral density of −70 dBm sets the lower limit of the dynamic range. The common pin, COMM, provides a quality low impedance connection to the printed circuit board (PCB) ground. The package paddle, which is internally connected to the COMM pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, see the AD8307 data sheet.) Using precision biasing, the gain is stabilized over temperature and supply variations. The overall dc gain is high, due to the cascaded nature of the gain stages.

The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. After the detector currents are summed and filtered, the following function is formed at the summing node:

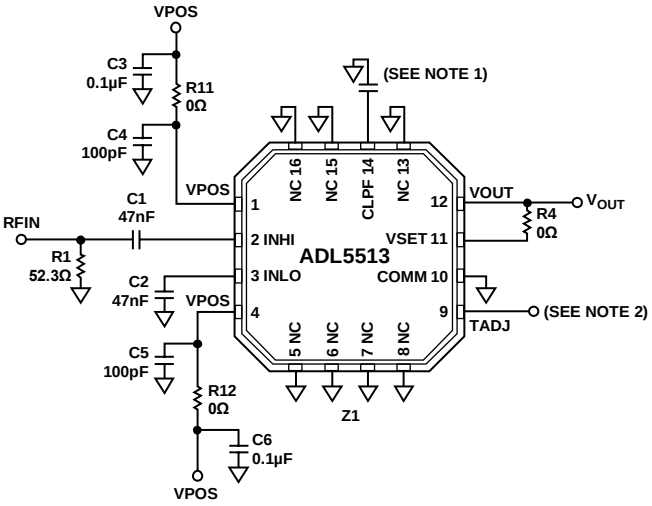
$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (1)$$

where:
I_D is the internally set detector current.
V_{IN} is the input signal voltage.
$V_{INTERCEPT}$ is the intercept voltage (that is, when $V_{IN} = V_{INTERCEPT}$, the output voltage is 0 V, if it were capable of going to 0).

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5513 is specified for operation up to 4 GHz; as a result, low impedance supply pins with adequate isolation between functions are essential. A power supply voltage of between 2.7 V and 5.5 V should be applied to VPOS. Connect 100 pF and 0.1 µF power supply decoupling capacitors close to this power supply pin.



NOTES
1. SEE THE OUTPUT FILTERING SECTION.
2. SEE THE TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE AND POWER-DOWN FUNCTIONALITY SECTIONS.

Figure 25. Basic Connections

The exposed paddle of the LFCSP package is internally connected to COMM. For optimum thermal and electrical performance, solder the paddle to a low impedance ground plane.

INPUT SIGNAL COUPLING

The RF input (INHI) is single-ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground. Suggested coupling capacitors are 47 nF, ceramic, 0402-style capacitors for input frequencies of 1 MHz to 4 GHz. The coupling capacitors should be mounted close to the INHI and INLO pins. The coupling capacitor values can be increased to lower the high-pass cutoff frequency of the input stage. The high-pass corner is set by the input coupling capacitors and the internal 20 pF high-pass capacitor. The dc voltage on INHI and INLO is about one diode voltage drop below V_{POS}.

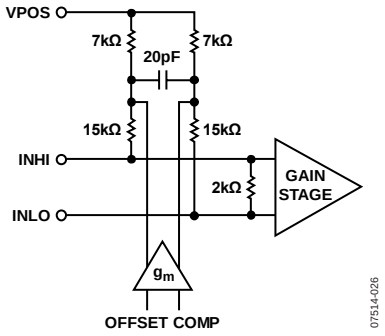


Figure 26. Input Interface

While the input can be reactively matched, in general, this is not necessary. An external 52.3 Ω shunt resistor (connected to the signal side of the input coupling capacitors, as shown in Figure 25) combines with relatively high input impedance to give an adequate broadband 50 Ω match.

The coupling time constant, $50 \times C_C/2$, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(2\pi \times 50 \times C_C)$, where $C1 = C2 = C_C$. Using the typical value of 47 nF, this high-pass corner is ~68 kHz. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This low-pass filter network should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

OUTPUT FILTERING

For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the CLPF pin be left unconnected and free of any stray capacitance.

The output video bandwidth, which is 10 MHz, can be reduced by connecting a ground-referenced capacitor (C_{FLT}) to the CLPF pin, as shown in Figure 27. This is generally done to reduce output ripple (at twice the input frequency for a symmetric input waveform such as sinusoidal signals).

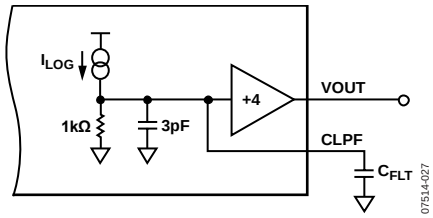


Figure 27. Lowering the Postdemodulation Bandwidth

C_{FLT} is selected by

$$C_{FLT} = \frac{1}{(2\pi \times 1.5\ \text{k}\Omega \times \textit{Video Bandwidth})} - 3.0\ \text{pF}$$

The video bandwidth should typically be set to a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered.

In many log amp applications, it may be necessary to lower the corner frequency of the postdemodulation filter to achieve low output ripple while maintaining a rapid response time to changes in signal level. An example of a four-pole active filter is shown in the AD8307 data sheet. Averaging the output measurement can also be done when filtering is not possible.

OUTPUT INTERFACE

The VOUT pin is driven by a PNP output stage. An internal 10 Ω resistor is placed in series with the output and the VOUT pin. The rise time of the output is limited mainly by the slew on CLPF. The fall time is an RC-limited slew given by the load capacitance and the pull-down resistance at VOUT. There is an internal pull-down resistor of 1.6 kΩ. A resistive load at VOUT is placed in parallel with the internal pull-down resistor to provide additional discharge current.

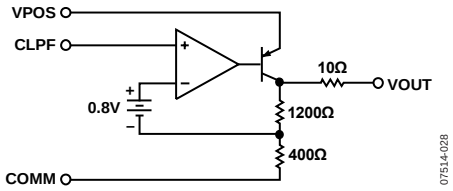


Figure 28. Output Interface

The ADL5513 output can drive over 1 nF of capacitance. When driving such high output capacitive loads, it is required to capacitively load the CLPF pin. The capacitance on the CLPF pin should be at least 1/50th that of the capacitance on the VOUT pin.

SETPOINT INTERFACE

The V_{SET} input drives the high impedance (40 kΩ) input of an internal op amp. The V_{SET} voltage appears across the internal 3.5 kΩ resistor to generate I_{SET}. When a portion of V_{OUT} is applied to VSET, the feedback loop forces

$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET} \quad (2)$$

If $V_{SET} = V_{OUT}/2x$, $I_{SET} = V_{OUT}/(2x \times 3.5\ k\Omega)$.

The result is $V_{OUT} = (I_D \times 3.5\ k\Omega \times 2x) \times \log_{10}(V_{IN}/V_{INTERCEPT})$.

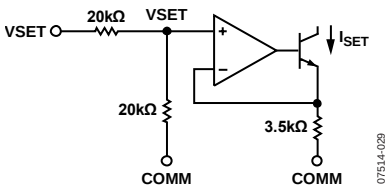


Figure 29. VSET Interface

The slope is given by $I_D \times 2x \times 3.5\ k\Omega = 20\ mV/dB \times x$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then x = 2. The slope is set to 800 V/decade or 40 mV/dB. See the Measurement Mode section for more information on setting the slope in measurement mode.

DESCRIPTION OF CHARACTERIZATION

The general hardware configuration used for most of the ADL5513 characterization is shown in Figure 30. The signal source and power supply used in this example are the Agilent E8251A PSG signal generator and E3631A triple output power supply. Output voltage was measured using the Agilent 34980A switch box.

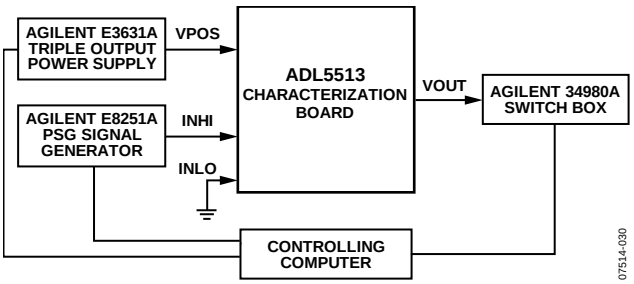


Figure 30. General Characterization Configuration

ERROR CALCULATIONS

The measured transfer function of the ADL5513 at 100 MHz is shown in Figure 31. The figure shows plots of measured output voltage, calculated error, and an ideal line. The input power and output voltage are used to calculate the slope and intercept values. The slope and intercept are calculated using linear regression over the input range from −40 dBm to −20 dBm. The slope and intercept terms are used to generate an ideal line. The error is the difference in measured output voltage compared to the ideal output line.

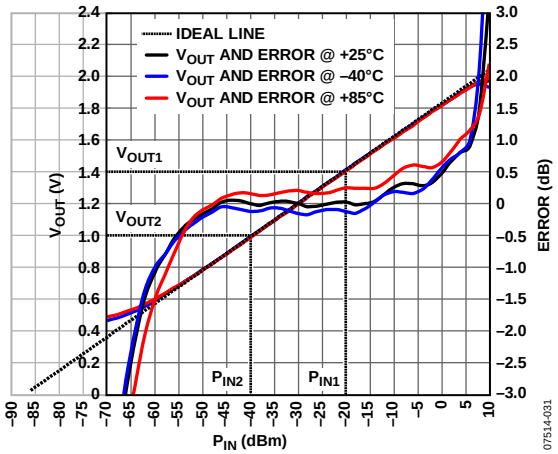


Figure 31. Typical Output Voltage vs. Input Signal

The equation for output voltage can be written as

$$V_{OUT} = Slope \times (P_{IN} - Intercept)$$

where:
Slope is the change in output voltage divided by the change in input power, P_{IN}. Slope is expressed in volts per decibel (V/dB).
Intercept is the calculated power in decibels (dB) at which the output voltage is 0 V. Note that $V_{OUT} = 0$ V can never be achieved.

Calibration is performed by applying two known signal levels to the ADL 5513 and measuring the corresponding voltage outputs. The calibration points are in general chosen to be within the linear-in-dB range of the device.

Calculation of the slope and intercept are accomplished by using the following equations:

$$Slope = \frac{V_{OUT(MEASURED)1} - V_{OUT(MEASURED)2}}{P_{IN1} - P_{IN2}}$$

$$Intercept = P_{IN1} - \frac{V_{OUT(MEASURED)}}{Slope}$$

Once the slope and intercept are calculated, $V_{OUT(IDEAL)}$ can be calculated, and the error is determined using the following equation:

$$Error = \frac{(V_{OUT(MEASURED)} - V_{OUT(IDEAL)})}{Slope}$$

Figure 31 shows a plot of the error at 25°C, the temperature at which the device is calibrated. Error is not 0 dB over the full dynamic range. This is because the log amp does not perfectly follow the ideal V_{OUT} vs. P_{IN} equation, even within its operating range. The error at the calibrating points of −20 dBm and −40 dBm is equal to 0 dB by definition.

Figure 31 also shows error plots for output voltages measured at −40°C and 85°C. These error plots are calculated using slope and intercept at 25°C, which is consistent in a mass-production environment, where calibration over temperature is not practical. This is a measure of the linearity of the device. Error from the linear response to the CW waveform is not a measure of absolute accuracy because it is calculated using the slope and intercept of each device. However, error verifies the linearity of the devices. Similarly, at temperature extremes, error represents the output voltage variations from the 25°C ideal line performance. Data presented in the graphs are the typical error distributions observed during characterization of the ADL5513. Device performance was optimized for operation at 85°C; this can be changed by changing the voltage at TADJ.

ADJUSTING ACCURACY THROUGH CHOICE OF CALIBRATION POINTS

Choose calibration points to suit the specific application, but usually they should be in the linear range of the log amp.

In some applications, very high accuracy is required at a reduced input range; in other applications, good linearity is necessary over the full power input range. The linearity of the transfer function can be adjusted by choice of calibration points. Figure 32 and Figure 33 show plots for a typical device at 3600 MHz as an example of adjusting accuracy through choice of calibration points.

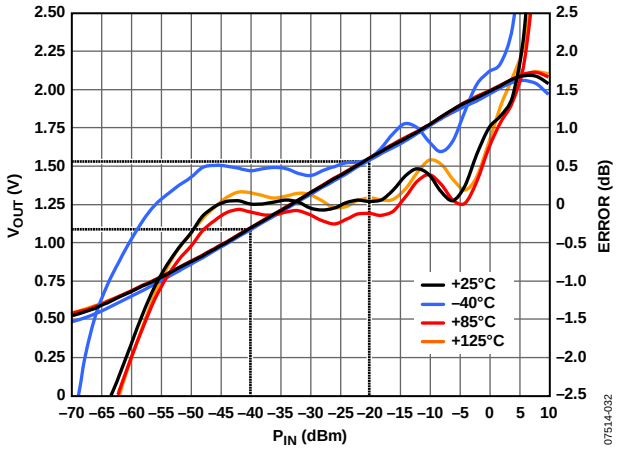


Figure 32. Typical Device at 3600 MHz, Calibration Points at P_{IN} = −20 dBm and −40 dBm

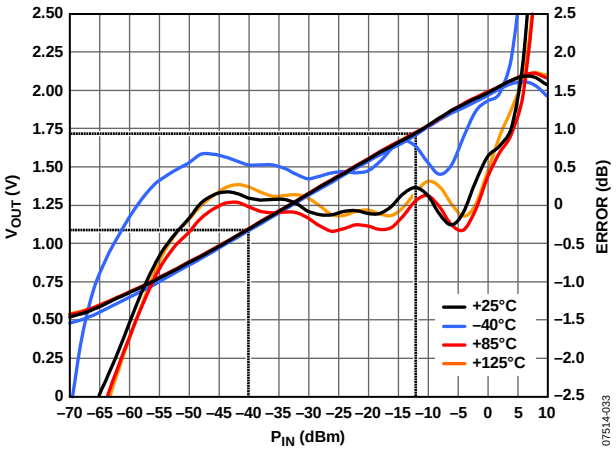


Figure 33. Typical Device at 3600 MHz, Calibration Points at P_{IN} = −12 dBm and −40 dBm

In Figure 32, calibration points are chosen so that linearity is improved over the full dynamic range, but error at the higher power level at P_{IN} = −10 dBm is 0.5 dB at 25°C. In Figure 33, calibration points are chosen so that error is smaller at higher power input ,but with loss of linearity over the full dynamic range.

Figure 34 shows another way of presenting the error of a log amp detector. The same typical device from Figure 32 and Figure 33 is presented where the error at −40°C, +85°C, and +125°C are calculated with respect to the output voltage at +25°C. This is the key difference in presenting the error of a log amp compared with the plots in Figure 32 and Figure 33 where the error is calculated with respect to the ideal line at 25°C.

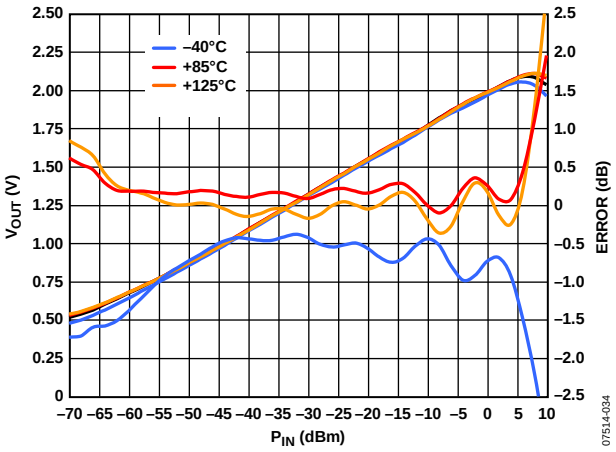


Figure 34. Error vs. Temperature with Respect to Output Voltage at 25°C, 3600 MHz

With this alternative technique, the error at ambient becomes 0 dB by definition. This would be valid if the device transfer function perfectly followed the ideal equation or if there were many calibration points used.

$$V_{OUT} = Slope \times (P_{IN} - Intercept)$$

Because the log amp never perfectly follows this equation, especially outside of its linear range, Figure 34 can be misleading as a representation of log amp error. This plot tends to artificially improve linearity and extend the dynamic range, unless enough calibration points are used to remove error.

Figure 34 is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) output voltage at ambient.

TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE

The primary component of the variation in V_{OUT} vs. temperature as the input signal amplitude is held constant is the drift of the intercept. This drift is also a weak function of the input signal frequency; therefore, a provision is made for the optimization of the internal temperature compensation at a given frequency by providing Pin TADJ with dual functionality. The first function for this pin is temperature compensation and the second function is to power down the device when $V_{TADJ} = V_{POS} - 0.3$ V (see the Power-Down Functionality section).

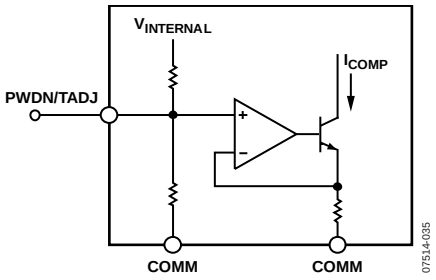


Figure 35. TADJ Interface

V_{TADJ} is a voltage forced between TADJ and ground. The value of this voltage determines the magnitude of an analog correction coefficient, which is used to reduce intercept drift.

The relationship between output temperature drift and frequency is not linear and cannot be easily modeled. As a result, experimentation is required to select the optimum V_{TADJ} voltage.

The V_{TADJ} voltage applied to Pin TADJ can be supplied by a DAC with sufficient resolution, or Resistor R8 and Resistor R9 on the evaluation board (see Figure 47) can be configured as a voltage divider using VPOS as the voltage source.

Table 4 shows the recommended voltage values for some commonly used frequencies in characterization to optimize operation at 85°C. The TADJ pin has high input impedance.

Table 4. Recommended V_{TADJ} Values

Frequency	Recommended V_{TADJ} (V)
100 MHz	0.89
900 MHz	0.86
1.9 GHz	0.80
2.14 GHz	0.84
2.6 GHz	0.83
3.6 GHz	0.90

Compensating the device for temperature drift using TADJ allows for great flexibility. If the user requires minimum temperature drift at a given input power or subset of the dynamic range, the TADJ voltage can be swept while monitoring VOUT over temperature. Figure 36 shows how error changes on a typical part over the full dynamic range when V_{TADJ} is swept from 0.5 V to 1.2 V in steps of 0.1 V.

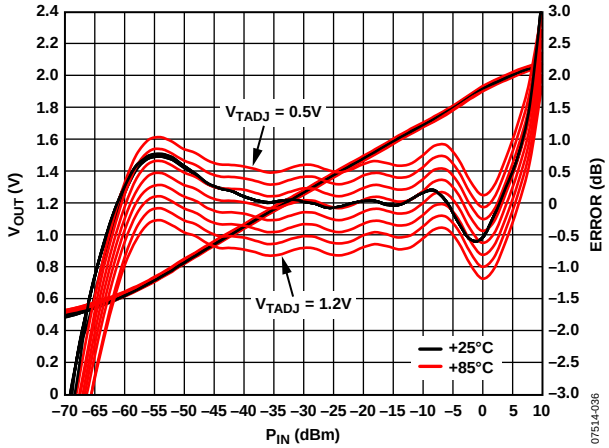


Figure 36. V_{OUT} vs. TADJ at 85°C, 1900 MHz

Figure 37 shows the results of sweeping V_{TADJ} over multiple temperatures while holding P_{IN} constant. The same V_{TADJ} should be used for the full dynamic range for a specified supply operation.

DEVICE CALIBRATION

V_{TADJ} voltages in Table 4 are chosen so that the error is at its minimum at 85°C. Criteria for the choice of V_{TADJ} is unique for a given application. Figure 37 shows how error on a typical device changes at INHI = −30 dBm when V_{TADJ} is swept at different temperatures. If the ADL5513 must have minimum error at a certain temperature, then V_{TADJ} should be chosen such that the line for that temperature intersects the 25°C line. At this V_{TADJ} setting, the error at all other temperatures is not the minimum. If the deviation of error over temperature is more important than the error at a single temperature, V_{TADJ} should be determined by the intersection of the lines for the temperatures of interest. For the characterization data presented, V_{TADJ} values were chosen so that ADL5513 has a minimum error at 85°C, which is at the intersection of the lines for 85°C and 25°C. For example, at 1900 MHz, V_{TADJ} = 0.8 V. If a given application requires error deviation to be at a minimum when the temperature changes from −40°C to 85°C, V_{TADJ} is determined by the intersection of the error line for those temperatures.

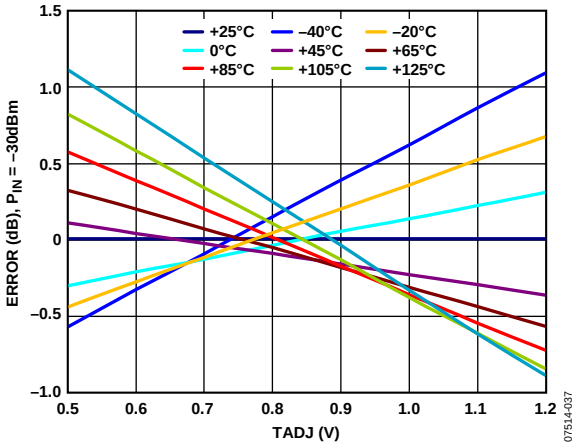


Figure 37. Error vs. V_{TADJ}, P_{IN} = −30 dBm at 1900 MHz

It is important that temperature adjustment be performed on multiple devices.

POWER-DOWN FUNCTIONALITY

Power-down functionality of ADL5513 is achieved through externally applied voltage on the TADJ pin. If $V_{TADJ} = V_{POS} - 0.3$ V, the output voltage and supply current are close to 0.

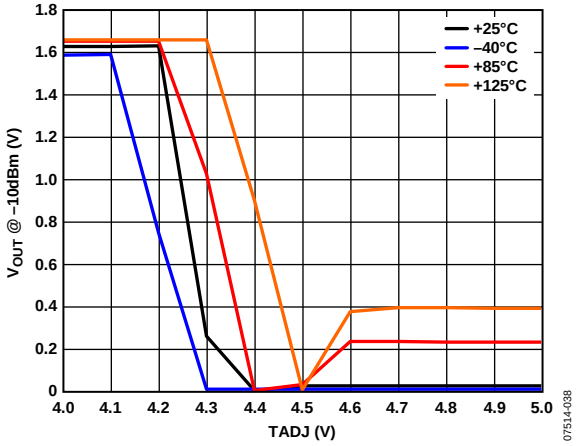


Figure 38. V_{OUT} vs. V_{TADJ} at 100 MHz, V_{POS} = 5 V

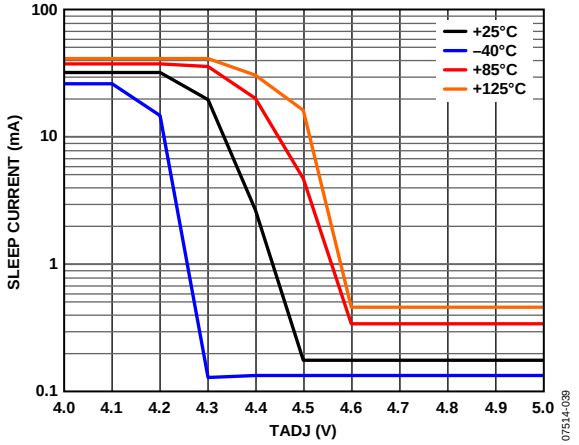


Figure 39. Sleep Current vs. V_{TADJ}, V_{POS} = 5 V

MEASUREMENT MODE

When the V_{OUT} voltage or a portion of the V_{OUT} voltage is fed back to the VSET pin, the device operates in measurement mode. As shown in Figure 40, the ADL5513 has an offset voltage, a positive slope, and a V_{OUT} measurement intercept at the low end of its input signal range.

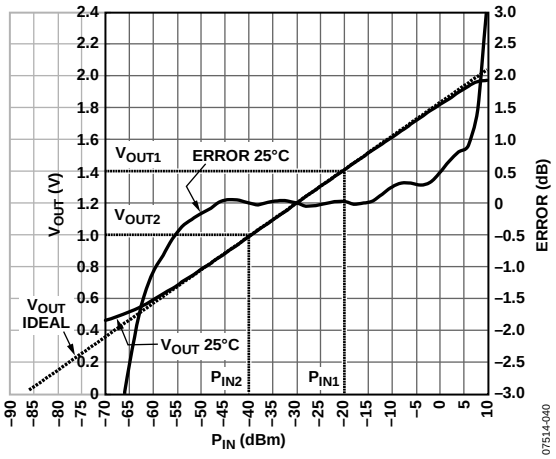


Figure 40. Typical Output Voltage vs. Input Signal

The output voltage vs. input signal voltage of the ADL5513 is linear-in-dB over a multidecade range. The equation for this function is

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log_{10}(V_{IN}/V_{INTERCEPT}) =$$
$$X \times V_{SLOPE/dB} \times 20 \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (3)$$

where:
X is the feedback factor in $V_{SET} = V_{OUT}/X$.
$V_{SLOPE/DEC}$ is nominally 400 mV/decade or 20 mV/dB.
$V_{INTERCEPT}$ is the x-axis intercept of the linear-in-dB portion of the V_{OUT} vs. P_{IN} curve (see Figure 40).
$V_{INTERCEPT}$ is −100 dBV for a sinusoidal input signal.

An offset voltage, V_{OFFSET}, of 0.47 V is internally added to the detector signal, so that the minimum value for V_{OUT} is $X \times V_{OFFSET}$; therefore, for X = 1, the minimum V_{OUT} is 0.47 V.

The slope is very stable vs. process and temperature variation. When Base 10 logarithms are used, $V_{SLOPE/DEC}$ represents the volts per decade. A decade corresponds to 20 dB; $V_{SLOPE/DEC}/20 = V_{SLOPE/dB}$ represents the slope in volts per decibel (V/dB).

As shown in Figure 40, V_{OUT} voltage has a positive slope.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_0, must be known to convert voltages to their corresponding power levels. The following equations are used to perform this conversion:

$$P(\text{dBm}) = 10 \times \log_{10}(V_{rms}^2/(Z_0 \times 1\ \text{mW})) \quad (4)$$

$$P(\text{dBV}) = 20 \times \log_{10}(V_{rms}/1\ V_{rms}) \quad (5)$$

$$P(\text{dBm}) = P(\text{dBV}) - 10 \times \log_{10}(Z_0 \times 1\ \text{mW}/1\ V_{rms}^2) \quad (6)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal expressed in terms of decibels referred to 1 mW (dBm) in a 50 Ω system is

$$P_{INTERCEPT}(\text{dBm}) =$$
$$P_{INTERCEPT}(\text{dBV}) - 10 \times \log_{10}(Z_0 \times 1\ \text{mW}/1\ V_{rms}^2) =$$
$$-100\ \text{dBV} - 10 \times \log_{10}(50 \times 10^{-3}) = -87\ \text{dBm} \quad (7)$$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

SETTING THE OUTPUT SLOPE IN MEASUREMENT MODE

To operate in measurement mode, VOUT is connected to VSET. Connecting VOUT directly to VSET yields the nominal logarithmic slope of approximately 20 mV/dB. The output swing corresponding to the specified input range is then approximately 0.47 V to 2.0 V. The slope and output swing can be increased by placing a resistor divider between VOUT and VSET (that is, one resistor from VOUT to VSET and one resistor from VSET to ground). The input impedance of VSET is approximately 40 kΩ. Slope-setting resistors should be kept below 20 kΩ to prevent this input impedance from affecting the resulting slope. If two equal resistors are used (for example, 10 kΩ/10 kΩ), the slope doubles to approximately 40 mV/dB.

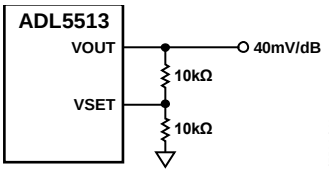


Figure 41. Increasing the Slope

The required resistor values needed to increase the slope are calculated from the following equation.

$$\frac{R1}{R2} + 1 = \frac{Slope2}{Slope1} \quad (8)$$

where:
R1 is the resistor from VOUT to VSET.
R2 is the resistor from VSET to ground.
Slope1 is the nominal slope of the ADL5513.
Slope2 is the new slope.

It is important to remember when increasing the slope of the ADL5513 that R1 and R2 must be properly sized so the output current drive capability is not exceeded. The dynamic range of the ADL5513 may be limited if the maximum output voltage is achieved before the maximum input power is reached. In cases where V_{POS} is 5 V, the maximum output voltage is 4.7 V.

The slope of the ADL5513 can be reduced by connecting VSET to VOUT and adding a voltage divider on the output.

CONTROLLER MODE

The ADL5513 provides a controller mode feature at Pin VOUT. Using V_{SET} for the setpoint voltage, it is possible for the ADL5513 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs), which have output power that increases monotonically with respect to their gain control signal.

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input, VOUT is connected to the gain control terminal of the VGA, and the RF input of the detector is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the ADL5513 adjusts the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. When the ADL5513 operates in controller mode, there is no defined relationship between the V_{SET} and the V_{OUT} voltage; V_{OUT} settles to a value that results in the correct input signal level appearing at INHI/INLO.

For this output power control loop to be stable, a ground-referenced capacitor must be connected to the CLPF pin. This capacitor, C_{FLT}, integrates the error signal (in the form of a current) to set the loop bandwidth and ensure loop stability. Further details on control loop dynamics can be found in the AD8315 data sheet.

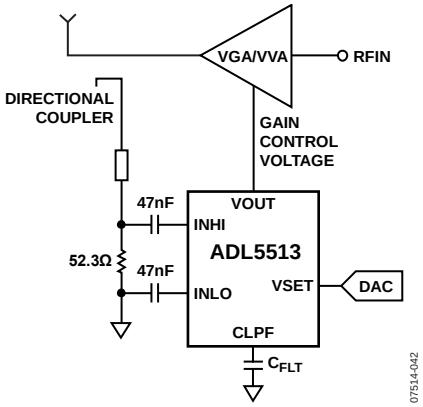


Figure 42. Controller Mode

CONSTANT POWER OPERATION

In controller mode, the ADL5513 can be used to hold the output power stable over a broad temperature/input power range. This can be useful in topologies where a transmit card is driving an HPA or when connecting power-sensitive modules together. Figure 44 shows a schematic of a circuit setup that holds the output power to approximately −39 dBm at 900 MHz when the input power is varied over a 62 dB dynamic range. Figure 43 shows the performance results. A portion of the output power is coupled to the input of ADL5513 using a 20 dB coupler. The VSET voltage is set to 0.65 V, which forces the ADL5513 output voltage to control the ADL5330 to deliver −59 dBm. (If the ADL5513 is in measurement mode and a −59 dBm input power is applied, the output voltage is 0.65 V). A generic op amp is used (AD8062) to invert the slope of the ADL5513 so that the gain of the ADL5330 decreases as the ADL5513 control voltage increases. The high end power is limited by the maximum gain of the ADL5330 and can increase if VSET is moved so that the ADL5513 has a higher power on its input and a VGA with higher linearity is used. The low power is limited by the sensitivity of the ADL5513 and can be increased with a reduction in the coupling value of the coupler.

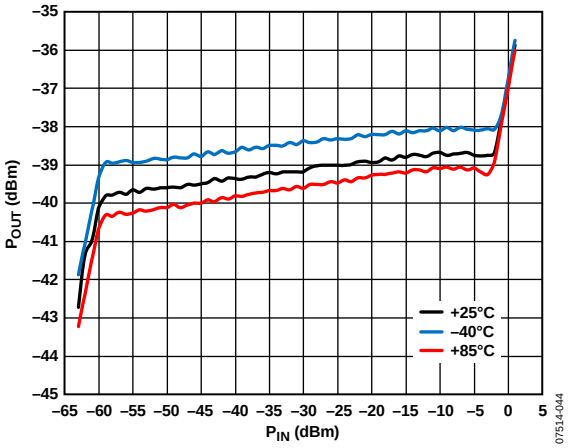


Figure 43. Performance of ADL5330/ADL5513 Constant Power Circuit

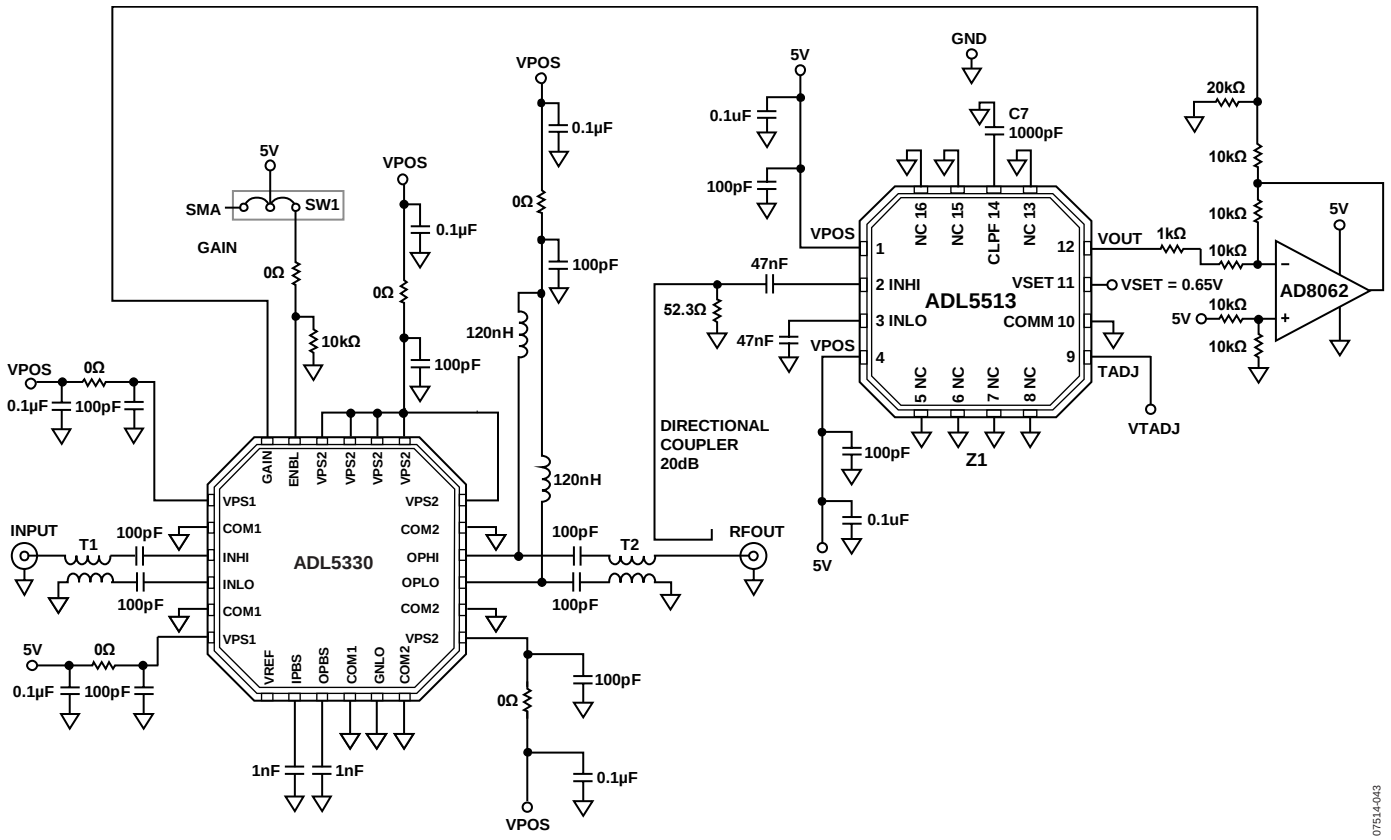


Figure 44. Schematic of the ADL5513 Operating in Controller Mode to Provide Automatic Gain Control Functionality in Combination with the ADL5330

INCREASING THE DYNAMIC RANGE OF THE ADL5513

The ADL5513 dynamic range can be extended by adding a standalone VGA, whose gain control input is derived directly from VOUT. This extends the dynamic range by the gain control range of the VGA. In order for the overall measurement to remain linear in dB, the VGA must provide a linear-in-dB (exponential) gain control function. The VGA gain must decrease with an increase in its gain bias in the same way as the ADL5513. Alternatively, an inverting op amp with suitable level shifting can be used. It is convenient to select a VGA that needs only a single 5.0 V supply and is capable of generating a single-ended output. All of these conditions are met by the AD8368. Figure 46 shows the schematic. Using the inverse gain mode (MODE pin low) of the AD8368, its gain decreases on a slope of 37.5 mV/dB to a minimum value of −12 dB for a gain voltage (V_{GAIN}) of 1.0 V. The voltage, V_{GAIN}, that is required by the AD8368 is 50% of the output of the ADL5513. To scale this voltage, it is necessary to install a voltage divider at the output of the ADL5513. Over the 1.5 V range from the output of the ADL5513, the gain of the AD8368 varies by (0.5 × 1.5 V)/(37.5 mV/dB), or 20 dB. Combined with the 75 dB gain span (at 120 MHz) of the ADL5513, this results in a 95 dB variation for a 1.5 V change in V_{OUT}.

Due to the amplification of out-of-band noise by the AD8368, a band-pass filter was inserted between the AD8368 and ADL5513 to increase the low end sensitivity. The VGA amplifies low power signals and attenuates high power signals to fit them in the detectable range of the ADL5513. If an amplifier with higher gain and lower noise figure is used, better than 90 dB sensitivity can be achieved for use in an RSSI application.

Figure 45 shows data results of the extended dynamic range at 120 MHz with error in VOUT.

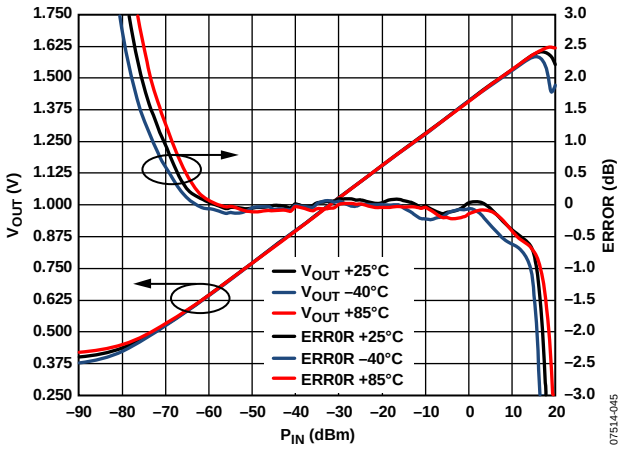


Figure 45. Output and Conformance for the AD8368/ADL5513 Extended Dynamic Range Circuit

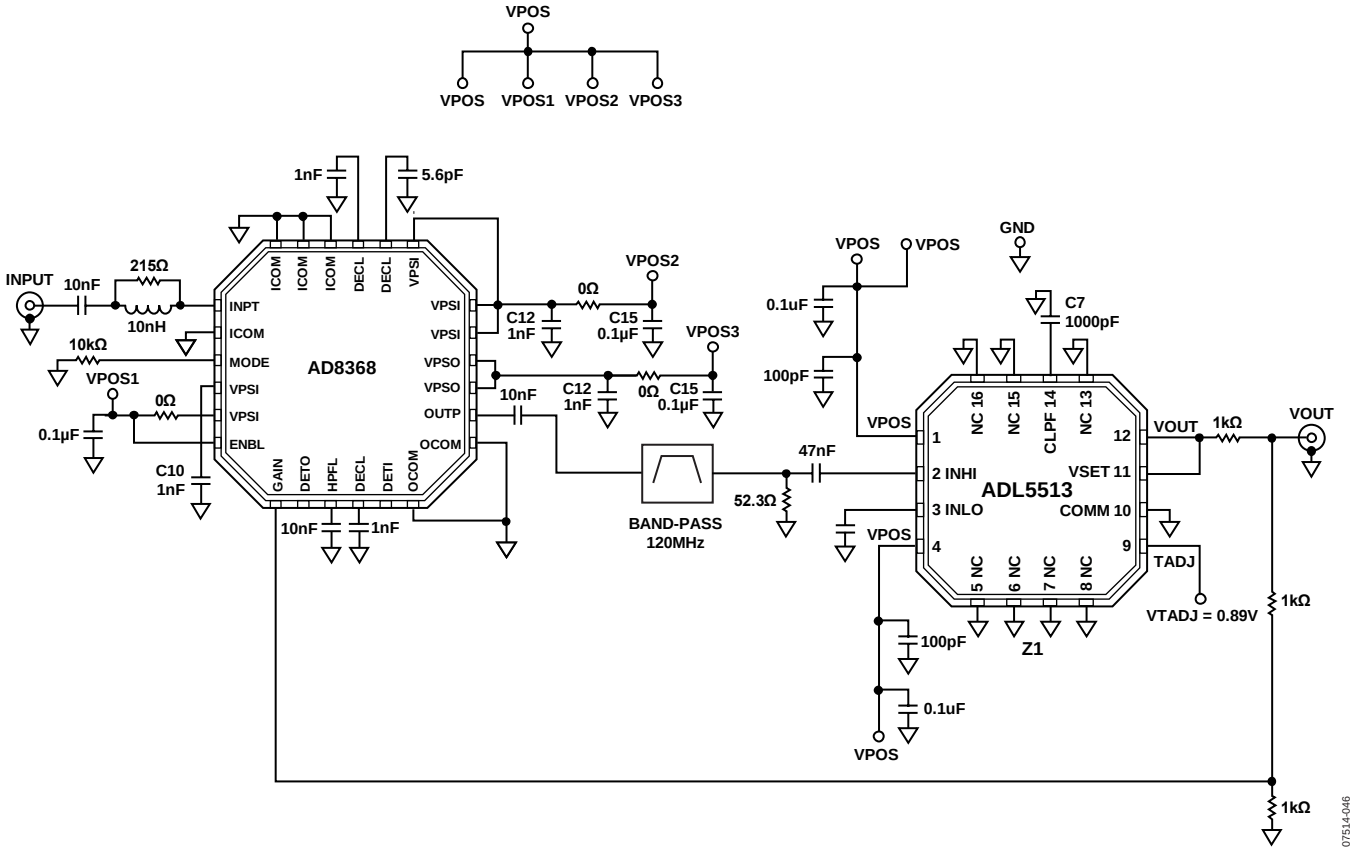


Figure 46. ADL5513 with 95 dB Dynamic Range

EVALUATION BOARD

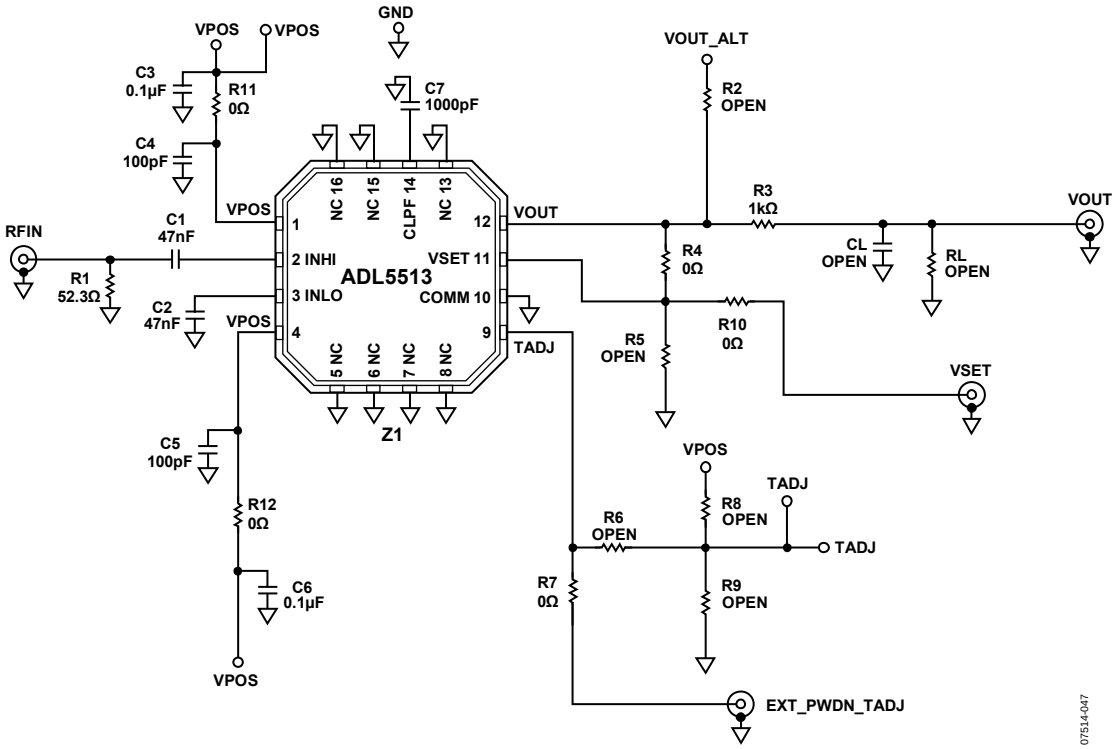


Figure 47. Evaluation Board Schematic

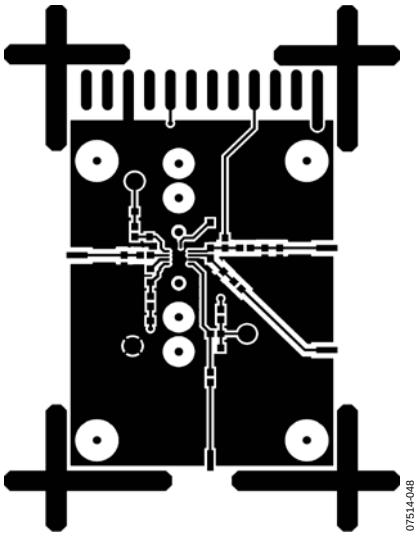


Figure 48. Component Side Layout

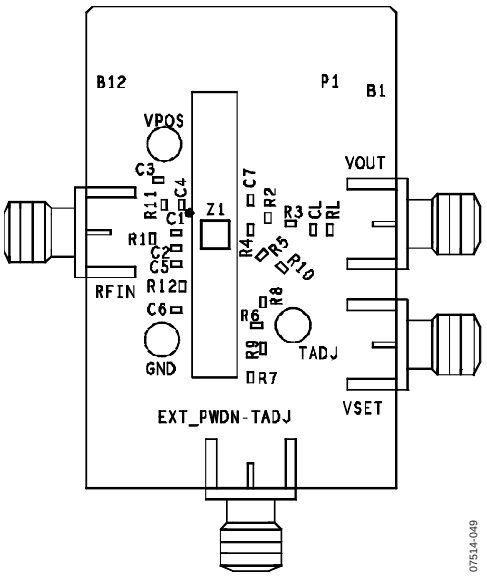


Figure 49. Component Side Silkscreen

Table 5. Evaluation Board Configuration Options

Component	Function	Default Value
C1, C2, R1	Input interface. The 52.3 Ω resistor in Position R1 combines with the internal input impedance of the ADL5513 to give a broadband input impedance of about 50 Ω. C1 and C2 are dc-blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately valued capacitors.	R1 = 52.3 Ω (Size 0402) C1 = 47 nF (Size 0402) C2 = 47 nF (Size 0402)
C3, C4, C5, C6, R11, R12	Power supply decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the ADL5513 and a 0.1 µF capacitor placed nearer to the power supply input pin. If additional isolation from the power supply is required, a small resistance (R11 or R12) can be installed between the power supply and the ADL5513.	C3 = 0.1 µF (Size 0402) C4 = 100 pF (Size 0402) C5 = 100 pF (Size 0402) C6 = 0.1 µF (Size 0402) R11 = 0 Ω (Size 0402) R12 = 0 Ω (Size 0402)
C7	Filter capacitor. The low-pass corner frequency of the circuit that drives the VOUT pin can be lowered by placing a capacitor between CLPF and ground. Increasing this capacitor increases the overall rise/fall time of the ADL5513 for pulsed input signals.	C7 = 1000 pF (Size 0402)
R2, R3 R4, R5, R10, RL, CL	Output interface—measurement mode. In measurement mode, a portion of the output voltage is fed back to the VSET pin via R4. The magnitude of the slope of the V_{OUT} output voltage response can be increased by reducing the portion of V_{OUT} that is fed back to VSET. R3 can be used as a back-terminating resistor or as part of a single-pole, low-pass filter. If a reduction in slope is desired, a voltage divider can be installed at the output using R3 and RL.	R2 = open (Size 0402) R3 = 1 kΩ (Size 0402) R4 = 0 Ω (Size 0402) R5 = open (Size 0402) R10 = open (Size 0402) RL = CL = open (Size 0402)
	Output interface—controller mode. In controller mode, the ADL5513 can control the gain of an external component. To allow for this, remove the R4 resistor. A setpoint voltage is applied to Pin VSET. The value of this setpoint voltage corresponds to the desired RF input signal level applied to the ADL5513 RF input. A sample of the RF output signal from this variable gain component is applied to the ADL5513 input by a directional coupler. The voltage at the VOUT pin is applied to the gain control of the variable gain element. The magnitude of the control voltage can optionally be reduced via a voltage divider comprising R3 and RL, or a low-pass filter can be installed using R3 and CL.	R2 = open (Size 0402) R3 = 1 kΩ (Size 0402) R4 = open (Size 0402) R5 = open (Size 0402) R10 = 0 Ω (Size 0402) RL = CL = open (Size 0402)
R6, R7, R8, R9	Temperature compensation interface. A voltage source can be used to optimize the temperature performance for various input frequencies. The pads for R8 and R9 can be used for a voltage divider from the VPOS node to set the T_{ADJ} voltage at different frequencies. The ADL5513 can be disabled by applying a voltage of V_{POS} − 0.3 V to this node.	R6 = open (Size 0402) R7 = 0 Ω (Size 0402) R8 = open (Size 0402) R9 = open Ω (Size 0402)

OUTLINE DIMENSIONS

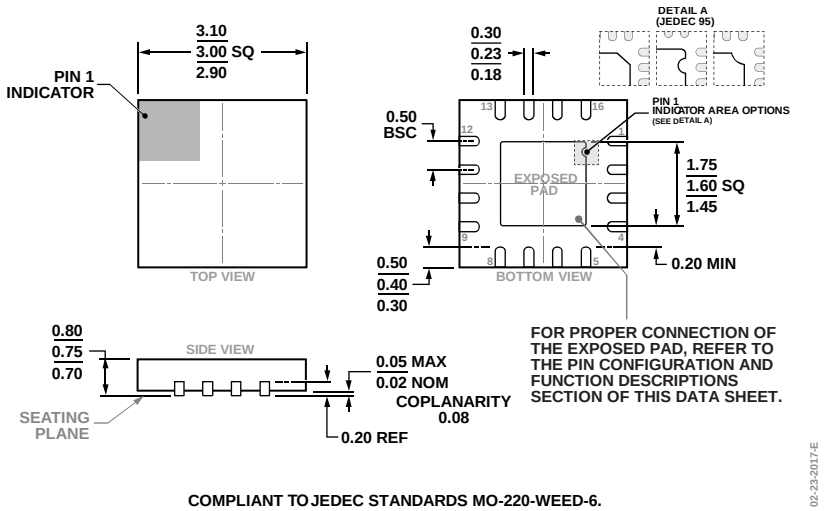


Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADL5513ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	Q1L
ADL5513ACPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	Q1L
ADL5513ACPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	Q1L
ADL5513-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

D07514-0-8/17(A)