ADG774A* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- ADSP-SC584 Evaluation Hardware for the ADSP-SC58x/ ADSP-2158x SHARC Family (349-ball CSPBGA)
- ADSP-SC589 Evaluation Hardware for the ADSP-SC58x/ ADSP-2158x SHARC Family (529-ball CSPBGA)

Documentation

Application Notes

- AN-1024: How to Calculate the Settling Time and Sampling Rate of a Multiplexer
- AN-944: Signal Bandwidth vs. Resolution for Analog Video
- AN-945: System Bandwidth vs. Resolution for Analog Video

Data Sheet

- ADG774A: Low Voltage, 400 MHz, Quad 2:1 Mux with 3 ns Switching Time Data Sheet

Reference Materials

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

Design Resources

- ADG774A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADG774A EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

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8/06—Rev. A to Rev. B

Updated Format ... Universal
Added LFCSP Model ... Universal
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7/01—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

Parameter	B Version 25°C	T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to 2.5	V	
On Resistance, R_{ON}	2.2		Ω typ	V_D = 0 V to 1 V, I_S = −10 mA
	3.5	4	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.15		Ω typ	V_D = 0 V to 1 V, I_S = −10 mA
		0.5	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.3		Ω typ	V_D = 0 V to 1 V, I_S = −10 mA
		0.6	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (OFF)	±0.001		nA typ	V_D = 3 V/1 V, V_S = 1 V/3 V, see Figure 17
	±0.1	±0.25	nA max	
Drain Off Leakage, I_D (OFF)	±0.001		nA typ	V_D = 3 V/1 V, V_S = 1 V/3 V, see Figure 17
	±0.1	±0.25	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.001		nA typ	V_D = V_S = 3 V/1 V, see Figure 18
	±0.1	±0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.001		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
Digital Input Capacitance, C_{IN}	3		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}, t_{ON} ($\overline{EN}$)		6	ns typ	C_L = 35 pF, R_L = 50 Ω, V_S = 2 V, see Figure 22
		12	ns max	
t_{OFF}, t_{OFF} ($\overline{EN}$)		3	ns typ	C_L = 35 pF, R_L = 50 Ω, V_S = 2 V, see Figure 22
		6	ns max	
Break-Before-Make Time Delay, t_D		3	ns typ	C_L = 35 pF, R_L = 50 Ω, V_{S1} = V_{S2} = 2 V, see Figure 23
		1	ns min	
Off Isolation		−65	dB typ	f = 10 MHz, R_L = 50 Ω, see Figure 20
Channel-to-Channel Crosstalk		−70	dB typ	f = 10 MHz, R_L = 50 Ω, see Figure 21
Bandwidth −3 dB		400	MHz typ	R_L = 50 Ω, see Figure 19
Distortion		0.3	% typ	R_L = 100 Ω
Charge Injection		6	pC typ	C_L = 1 nF, see Figure 24, V_S = 0 V
C_S (OFF)		5	pF typ	
C_D (OFF)		7.5	pF typ	
C_D, C_S (ON)		12	pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
				Digital inputs = 0 V or V_{DD}
I_{DD}		1	µA max	
	0.001		µA typ	

[1] Temperature range for B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	B Version 25°C	B Version T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to 1.5	V	
On Resistance, R_{ON}	4		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA
	6	7	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.15		Ω typ	V_D = 0 V to 1 V, I_S = −10 mA
		0.5	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	1.5		Ω typ	V_D = 0 V to 1 V, I_S = −10 mA
		3	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (OFF)	±0.001		nA typ	V_D = 2 V/1 V, V_S = 1 V/2 V, see Figure 17
	±0.1	±0.25	nA max	
Drain Off Leakage, I_D (OFF)	±0.001		nA typ	V_D = 2 V/1 V, V_S = 1 V/2 V, see Figure 17
	±0.1	±0.25	nA max	
Channel On Leakage, I_D, I_S(ON)	±0.001		nA typ	V_D = V_S = 2 V/1 V, see Figure 18
	±0.1	±0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.001		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
Digital Input Capacitance, C_{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}, t_{ON} ($\overline{EN}$)		7	ns typ	C_L = 35 pF, R_L = 50 Ω, V_S = 1.5 V, see Figure 22
		14	ns max	
t_{OFF}, t_{OFF} ($\overline{EN}$)		4	ns typ	C_L = 35 pF, R_L = 50 Ω, V_S = 1.5 V, see Figure 22
		8	ns max	
Break-Before-Make Time Delay, t_D		3	ns typ	C_L = 35 pF, R_L = 50 Ω, V_{S1} = V_{S2} = 1.5 V, see Figure 23
		1	ns min	
Off Isolation		−65	dB typ	f = 10 MHz, R_L = 50 Ω
Channel-to-Channel Crosstalk		−70	dB typ	f = 10 MHz, R_L = 50 Ω, see Figure 21
Bandwidth −3 dB		400	MHz typ	R_L = 50 Ω, see Figure 19
Distortion		1.5	% typ	R_L = 100 Ω
Charge Injection		4	pC typ	C_L = 1 nF, see Figure 24, V_S = 0 V
C_S (OFF)		5	pF typ	
C_D (OFF)		7.5	pF typ	
C_D, C_S (ON)		12	pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
				Digital inputs = 0 V or V_{DD}
I_{DD}		1	µA max	
	0.001		µA typ	

[1] Temperature range for B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

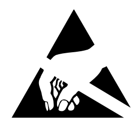
Table 3.

Parameters	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead QSSOP	105.44°C/W[2]
16-Lead LFCSP (3 mm × 3 mm)	48.7°C/W[2]
Lead Temperature Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Reflow Soldering (Pb-free)	
Peak Temperature	260°C (+0°C/−5°C)
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.
[2] Measured with the device soldered on a four-layer board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

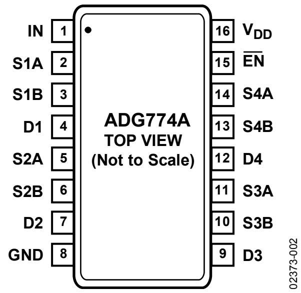


Figure 2. QSOP Pin Configuration

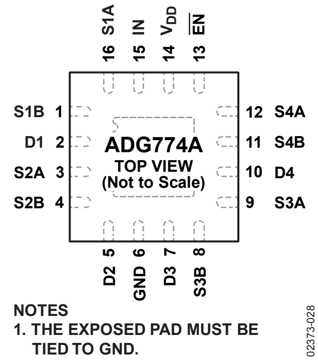


Figure 3. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
QSOP	**LFCSP**	**Mnemonic**	**Function**
1	15	IN	Logic Control Input.
2	16	S1A	Source Terminal 1A. May be an input or output.
3	1	S1B	Source Terminal 1B May be an input or output.
4	2	D1	Drain Terminal D1. May be an input or output.
5	3	S2A	Source Terminal 2A. May be an input or output.
6	4	S2B	Source Terminal 2B. May be an input or output.
7	5	D2	Drain Terminal D2. May be an input or output.
8	6	GND	Ground (0 V) Reference.
9	7	D3	Drain Terminal D3. May be an input or output.
10	8	S3B	Source Terminal 3B. May be an input or output.
11	9	S3A	Source Terminal 3A. May be an input or output.
12	10	D4	Drain Terminal D4. May be an input or output.
13	11	S4B	Source Terminal 4B. May be an input or output.
14	12	S4A	Source Terminal 4A. May be an input or output.
15	13	$\overline{EN}$	Logic Control Input. When high, all switches are disabled.
16	14	V_{DD}	Most Positive Power Supply Potential.
Not applicable	17	EPAD	Exposed Pad. The exposed pad must be tied to GND.

Table 5. Truth Table

$\overline{EN}$	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

TYPICAL PERFORMANCE CHARACTERISTICS

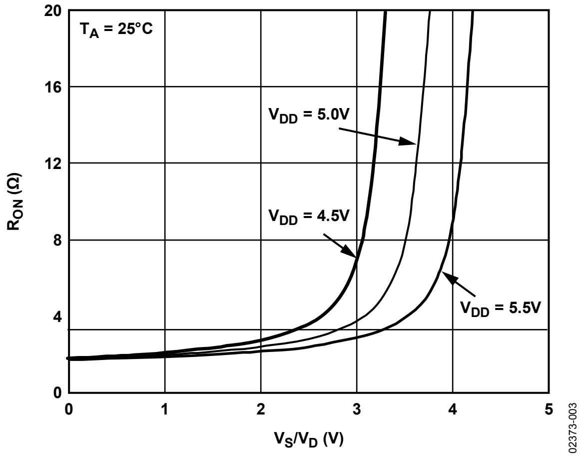


Figure 4. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for V_{DD} = 5 V ± 10%

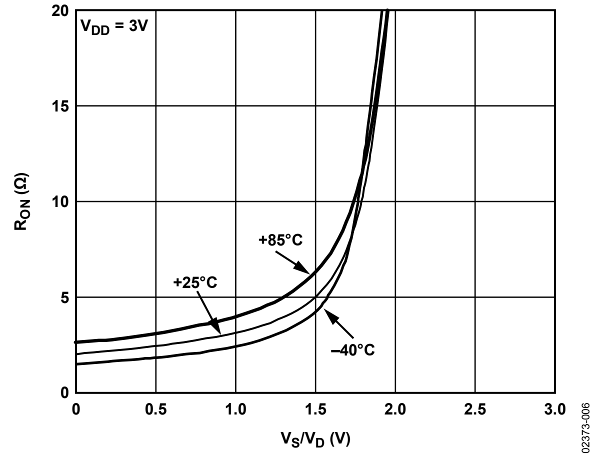


Figure 7. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for Different Temperatures with 3 V Single Supplies

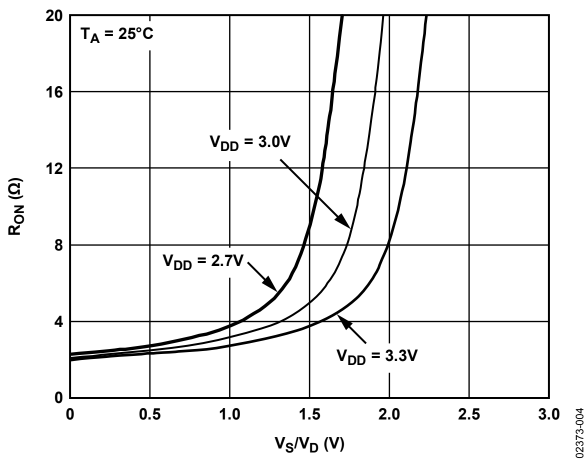


Figure 5. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for V_{DD} = 3 V ± 10%

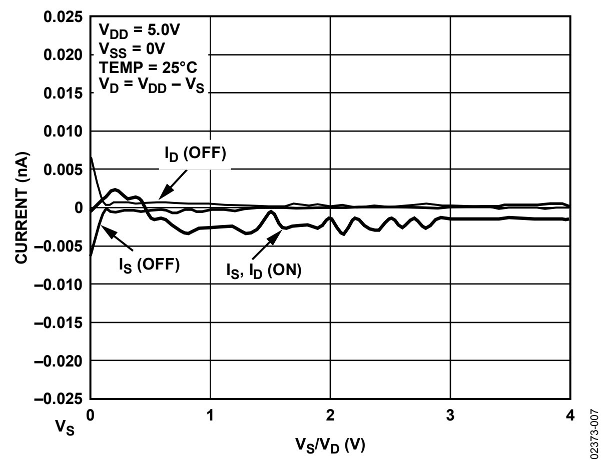


Figure 8. Leakage Current as a Function of Drain (V_D) or Source (V_S) Voltage for V_{DD} = 5 V

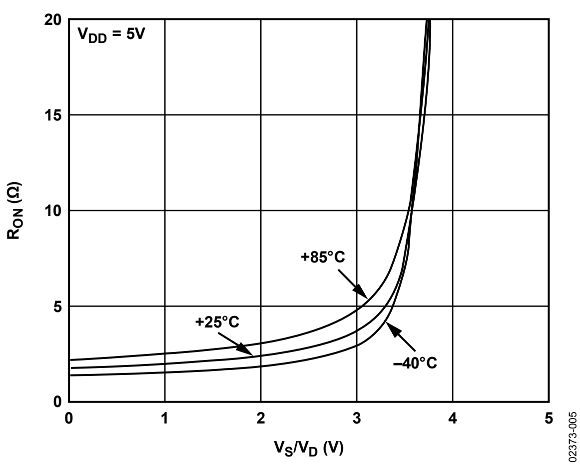


Figure 6. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for Different Temperatures with 5 V Single Supplies

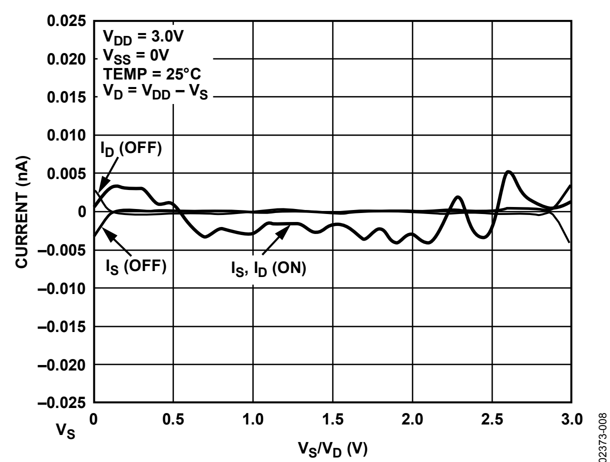


Figure 9. Leakage Current as a Function of Drain (V_D) or Source (V_S) Voltage for V_{DD} = 3 V

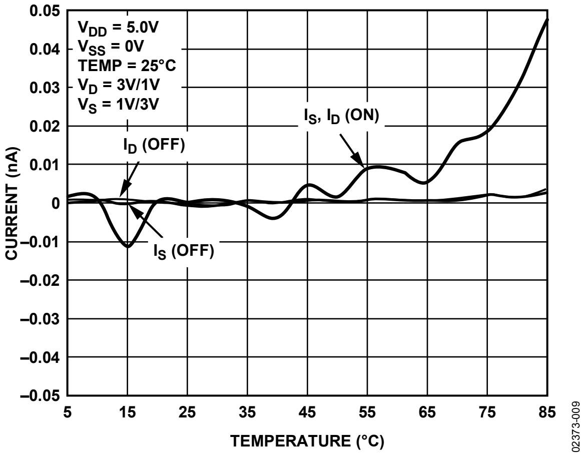


Figure 10. Leakage Current as a Function of Temperature, V_{DD} = 5 V

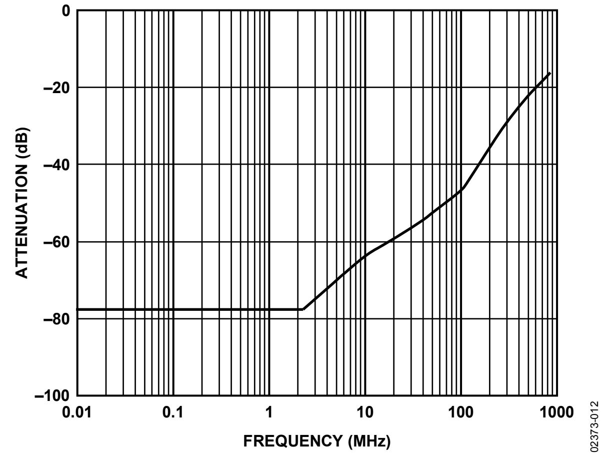


Figure 13. Crosstalk vs. Frequency

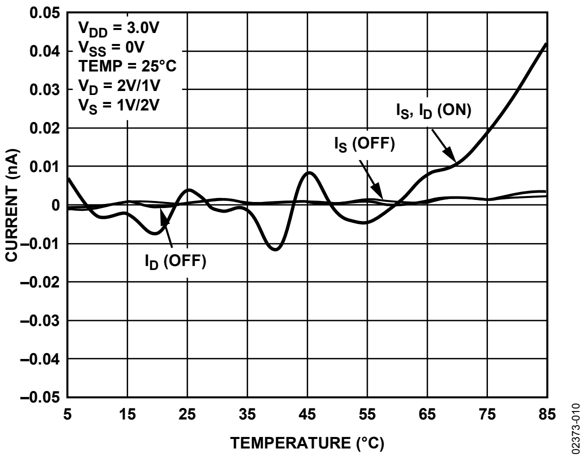


Figure 11. Leakage Current as a Function of Temperature, V_{DD} = 3 V

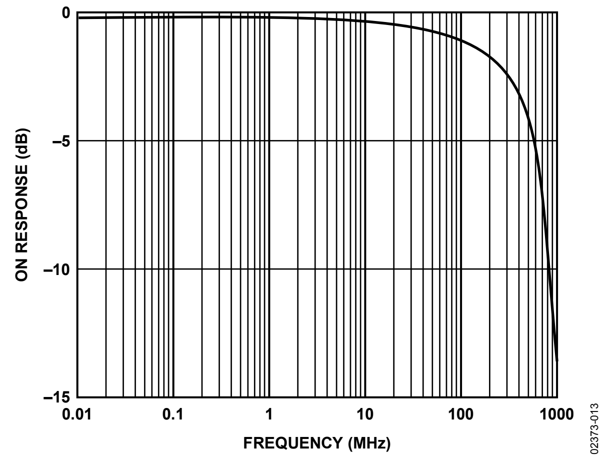


Figure 14. Bandwidth

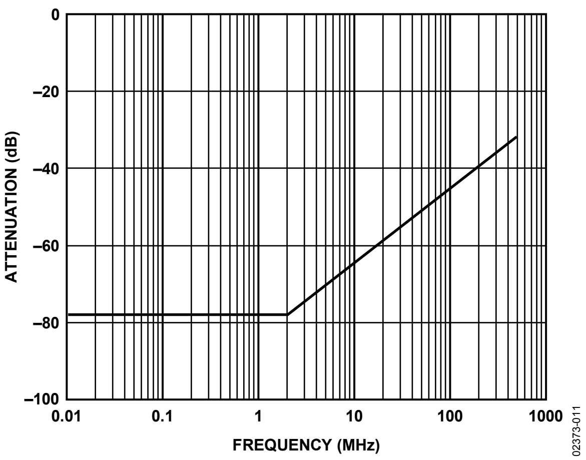


Figure 12. Off Isolation vs. Frequency

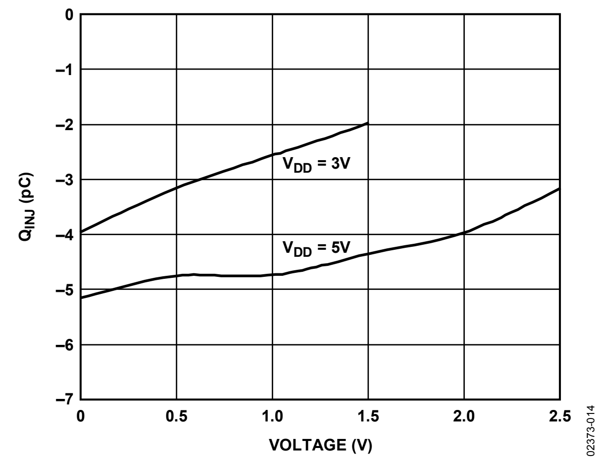


Figure 15. Charge Injection vs. Source Voltage

TEST CIRCUITS

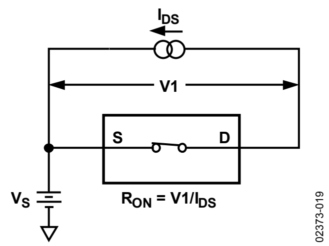


Figure 16. On Resistance

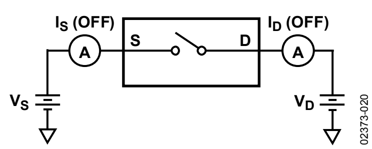


Figure 17. Off Leakage

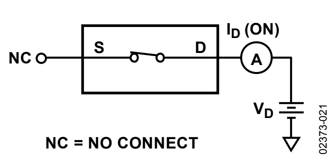


Figure 18. On Leakage

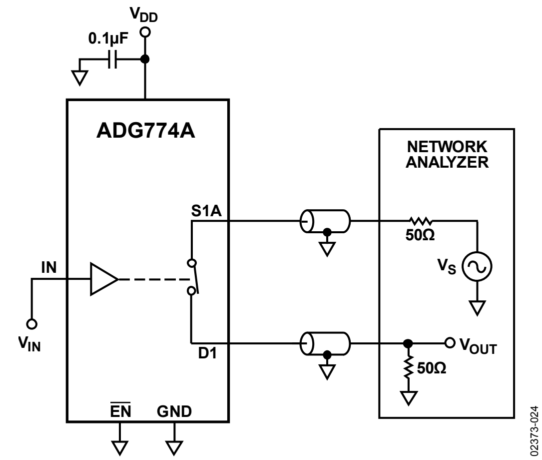


Figure 19. Bandwidth

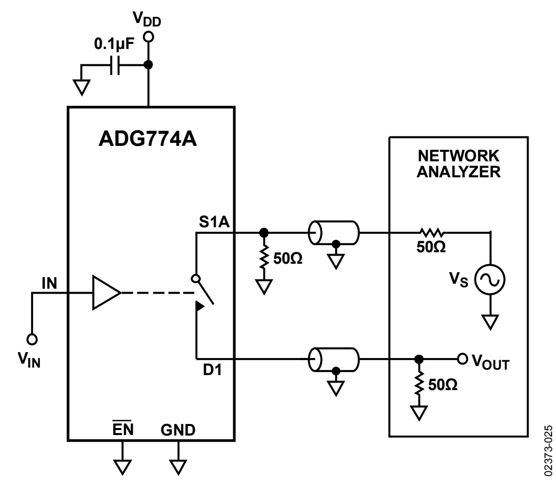


Figure 20. Off Isolation

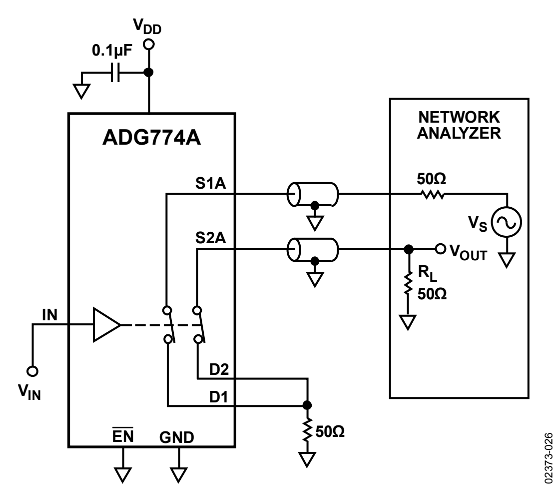


Figure 21. Channel-to-Channel Crosstalk

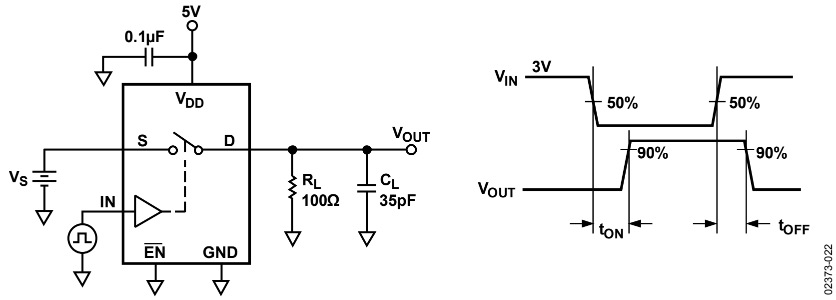


Figure 22. Switching Times

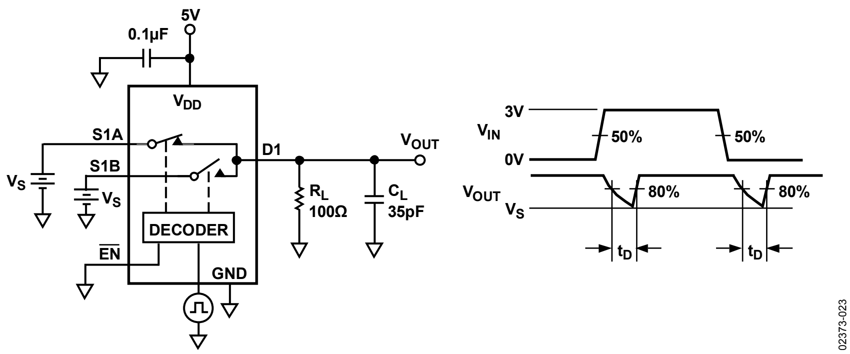


Figure 23. Break-Before-Make Time Delay

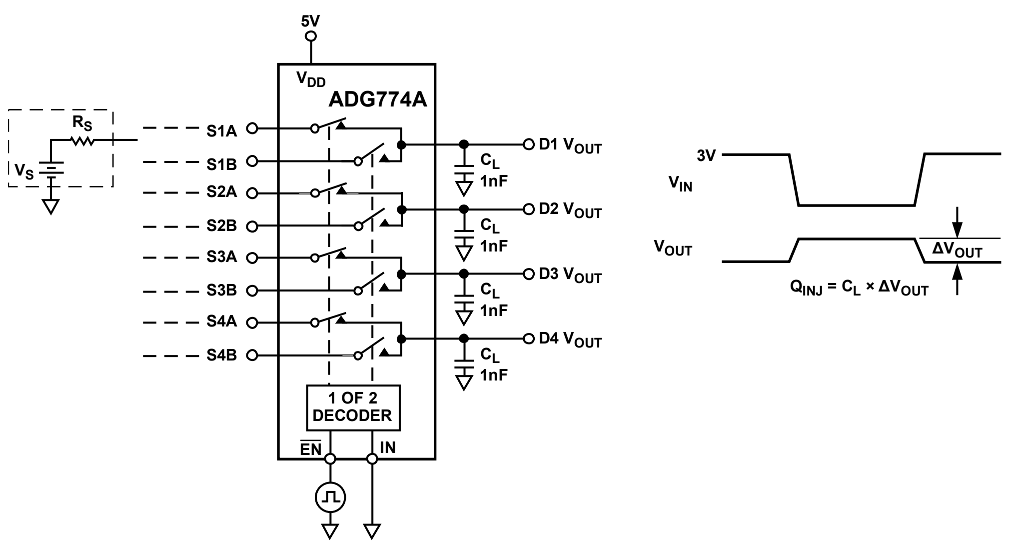


Figure 24. Charge Injection

TERMINOLOGY

V_{DD}
Most positive power supply potential.

GND
Ground (0 V) reference.

S
Source terminal. May be an input or output.

D
Drain terminal. May be an input or output.

IN
Logic control input.

$\overline{EN}$
Logic control input.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON} max − R_{ON} min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on the D and S terminals.

C_S (OFF)
Off switch source capacitance.

C_D (OFF)
Off switch drain capacitance.

C_D, C_S (ON)
On switch capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on. See Figure 22.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_D
Off time or on time measured between the 80% points of both switches when switching from one address state to another. See Figure 23.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
Frequency response of the switch in the on state measured at 3 dB down.

Distortion
$R_{FLAT(ON)}/R_L$

APPLICATION CIRCUITS

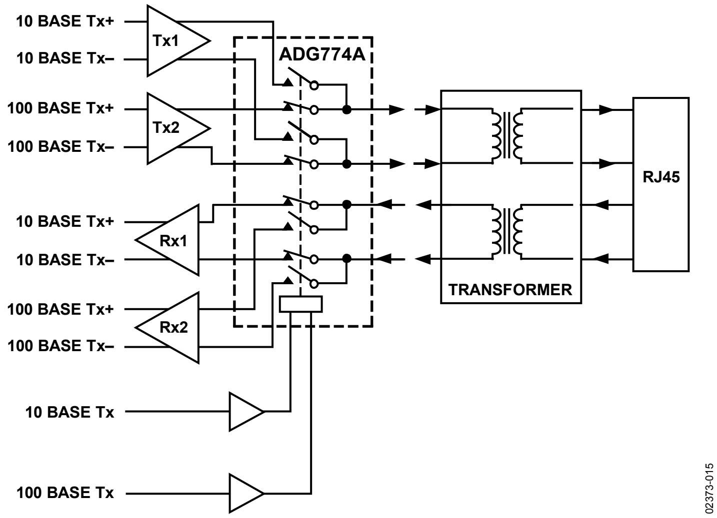


Figure 25. Full Duplex Transceiver

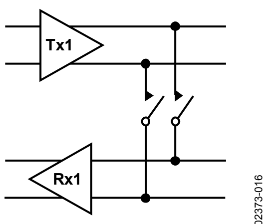


Figure 26. Loop Back

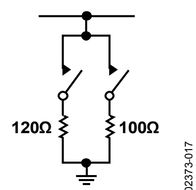


Figure 27. Line Termination

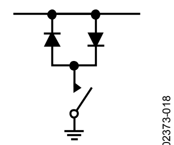


Figure 28. Line Clamp

OUTLINE DIMENSIONS

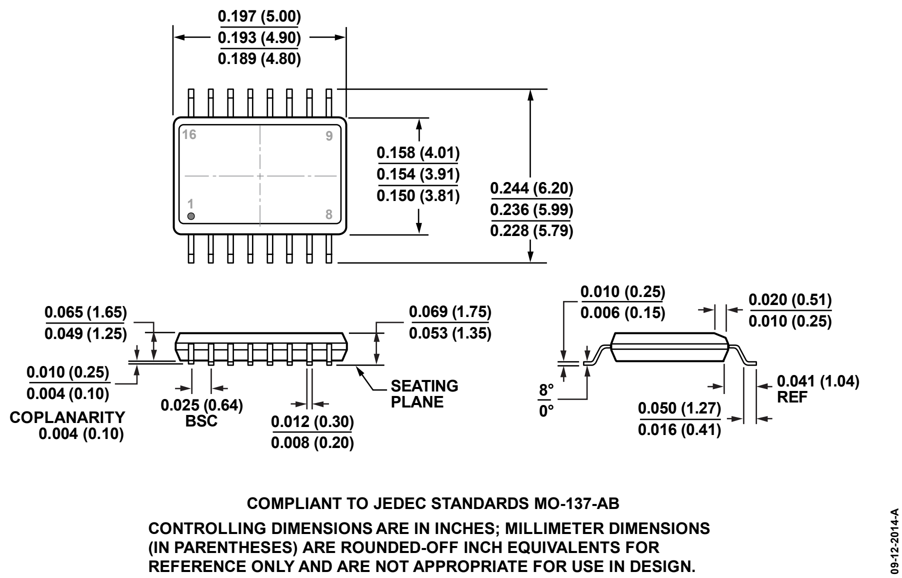


Figure 29. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

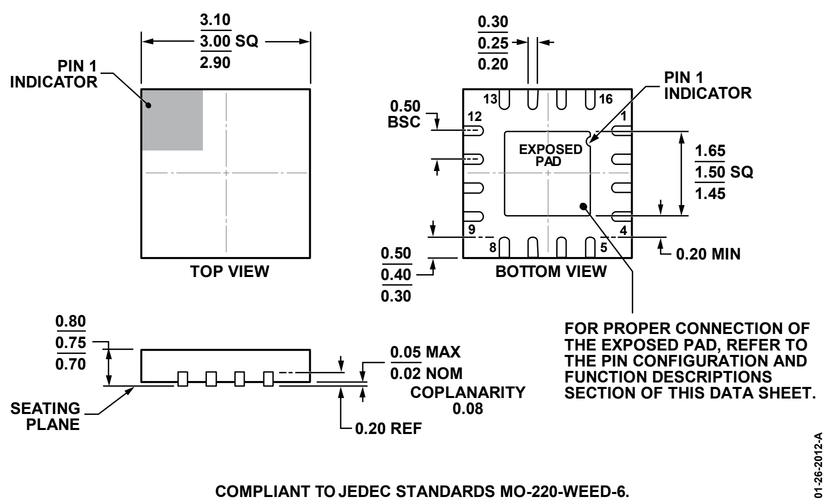


Figure 30. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-27)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG774ABRQ-REEL7	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ-REEL	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ-REEL7	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABCPZ-REEL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27
ADG774ABCPZ-R2	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27

[1] Z = RoHS Compliant Part.

NOTES

ANALOG DEVICES

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