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REVISION HISTORY

8/06—Rev. A to Rev. B

Updated Format.....	Universal
Added LFCSP Model.....	Universal
Added Lead-Free Models	Universal
Changes to Table 3.....	5
Updated Outline Dimensions	13
Changes to Ordering Guide	13

4/03—Rev. 0 to Rev. A

Changes to TPCs 9–11	5
Updated Outline Dimensions	8

7/01—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.¹

Table 1.

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T _{MIN} to T _{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 to 2.5	V	
On Resistance, R _{ON}	2.2		Ω typ	V _D = 0 V to 1 V, I _S = −10 mA
	3.5	4	Ω max	
On Resistance Match Between Channels, ΔR _{ON}	0.15		Ω typ	V _D = 0 V to 1 V, I _S = −10 mA
		0.5	Ω max	
On Resistance Flatness, R _{FLAT(ON)}	0.3		Ω typ	V _D = 0 V to 1 V, I _S = −10 mA
		0.6	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I _S (OFF)	±0.001		nA typ	V _D = 3 V/1 V, V _S = 1 V/3 V, see Figure 17
	±0.1	±0.25	nA max	
Drain Off Leakage, I _D (OFF)	±0.001		nA typ	V _D = 3 V/1 V, V _S = 1 V/3 V, see Figure 17
	±0.1	±0.25	nA max	
Channel On Leakage, I _D , I _S (ON)	±0.001		nA typ	V _D = V _S = 3 V/1 V, see Figure 18
	±0.1	±0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
I _{INL} or I _{INH}	0.001		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
Digital Input Capacitance, C _{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{ON} , t _{ON} (EN)		6	ns typ	C _L = 35 pF, R _L = 50 Ω, V _S = 2 V, see Figure 22
		12	ns max	
t _{OFF} , t _{OFF} (EN)		3	ns typ	C _L = 35 pF, R _L = 50 Ω, V _S = 2 V, see Figure 22
		6	ns max	
Break-Before-Make Time Delay, t _D		3	ns typ	C _L = 35 pF, R _L = 50 Ω, V _{S1} = V _{S2} = 2 V, see Figure 23
		1	ns min	
Off Isolation		−65	dB typ	f = 10 MHz, R _L = 50 Ω, see Figure 20
Channel-to-Channel Crosstalk		−70	dB typ	f = 10 MHz, R _L = 50 Ω, see Figure 21
Bandwidth −3 dB		400	MHz typ	R _L = 50 Ω, see Figure 19
Distortion		0.3	% typ	R _L = 100 Ω
Charge Injection		6	pC typ	C _L = 1 nF, see Figure 24, V _S = 0 V
C _S (OFF)		5	pF typ	
C _D (OFF)		7.5	pF typ	
C _D , C _S (ON)		12	pF typ	
POWER REQUIREMENTS				
I _{DD}		1	μA max	V _{DD} = 5.5 V
	0.001		μA typ	Digital inputs = 0 V or V _{DD}

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

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$V_{DD} = 3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.¹

Table 2.

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T _{MIN} to T _{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 to 1.5	V	
On Resistance, R _{ON}	4		Ω typ	V _D = 0 V to 1 V; I _S = −10 mA
	6	7	Ω max	
On Resistance Match Between Channels, ΔR _{ON}	0.15		Ω typ	V _D = 0 V to 1 V, I _S = −10 mA
		0.5	Ω max	
On Resistance Flatness, R _{FLAT(ON)}	1.5		Ω typ	V _D = 0 V to 1 V, I _S = −10 mA
		3	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I _S (OFF)	±0.001		nA typ	V _D = 2 V/1 V, V _S = 1 V/2 V, see Figure 17
	±0.1	±0.25	nA max	
Drain Off Leakage, I _D (OFF)	±0.001		nA typ	V _D = 2 V/1 V, V _S = 1 V/2 V, see Figure 17
	±0.1	±0.25	nA max	
Channel On Leakage, I _D , I _S (ON)	±0.001		nA typ	V _D = V _S = 2 V/1 V, see Figure 18
	±0.1	±0.25	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.4	V max	
Input Current				
I _{INL} or I _{INH}	0.001		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
Digital Input Capacitance, C _{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{ON} , t _{ON} (EN)		7	ns typ	C _L = 35 pF, R _L = 50 Ω, V _S = 1.5 V, see Figure 22
		14	ns max	
t _{OFF} , t _{OFF} (EN)		4	ns typ	C _L = 35 pF, R _L = 50 Ω, V _S = 1.5 V, see Figure 22
		8	ns max	
Break-Before-Make Time Delay, t _D		3	ns typ	C _L = 35 pF, R _L = 50 Ω, V _{S1} = V _{S2} = 1.5 V, see Figure 23
		1	ns min	
Off Isolation		−65	dB typ	f = 10 MHz, R _L = 50 Ω
Channel-to-Channel Crosstalk		−70	dB typ	f = 10 MHz, R _L = 50 Ω, see Figure 21
Bandwidth −3 dB		400	MHz typ	R _L = 50 Ω, see Figure 19
Distortion		1.5	% typ	R _L = 100 Ω
Charge Injection		4	pC typ	C _L = 1 nF, see Figure 24, V _S = 0 V
C _S (OFF)		5	pF typ	
C _D (OFF)		7.5	pF typ	
C _D , C _S (ON)		12	pF typ	
POWER REQUIREMENTS				
I _{DD}		1	μA max	V _{DD} = 3.3 V
	0.001		μA typ	Digital inputs = 0 V or V _{DD}

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameters	Rating
V_{DD} to GND	–0.3 V to +6 V
Analog, Digital Inputs ¹	–0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead QSSOP	105.44°C/W ²
16-Lead LFCSP(3 mm × 3 mm)	48.7°C/W ²
Lead Temperature Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Reflow Soldering (Pb-free)	
Peak Temperature	260°C (+0°C/–5°C)
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

² Measured with the device soldered on a four-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

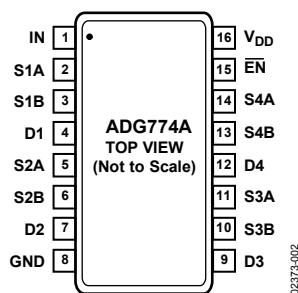
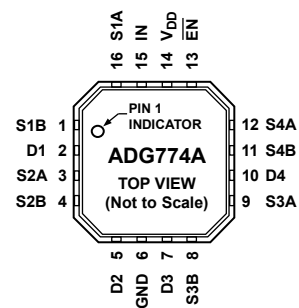


Figure 2. QSOP Pin Configuration



NOTES
1. THE EXPOSED PAD SHOULD BE TIED TO GND.

Figure 3. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.		Mnemonic	Function
QSOP	LFCSP		
1	15	IN	Logic Control Input.
2	16	S1A	Source Terminal 1A. May be an input or output.
3	1	S1B	Source Terminal 1B. May be an input or output.
4	2	D1	Drain Terminal D1. May be an input or output.
5	3	S2A	Source Terminal 2A. May be an input or output.
6	4	S2B	Source Terminal 2B. May be an input or output.
7	5	D2	Drain Terminal D2. May be an input or output.
8	6	GND	Ground (0 V) Reference.
9	7	D3	Drain Terminal D3. May be an input or output.
10	8	S3B	Source Terminal 3B. May be an input or output.
11	9	S3A	Source Terminal 3A. May be an input or output.
12	10	D4	Drain Terminal D4. May be an input or output.
13	11	S4B	Source Terminal 4B. May be an input or output.
14	12	S4A	Source Terminal 4A. May be an input or output.
15	13	EN	Logic Control Input. When high, all switches are disabled.
16	14	VDD	Most Positive Power Supply Potential.

Table 5. Truth Table

EN	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

TYPICAL PERFORMANCE CHARACTERISTICS

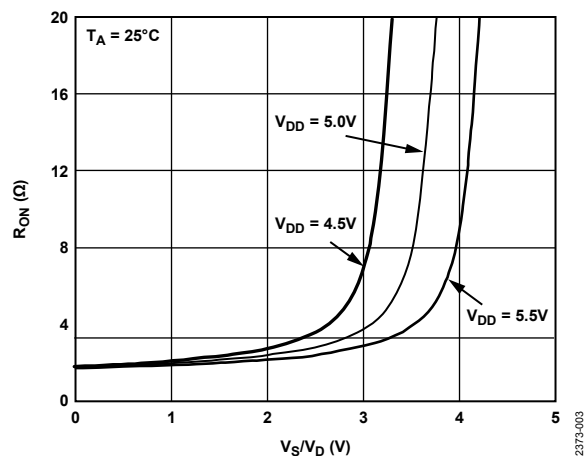


Figure 4. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for $V_{DD} = 5\text{ V} \pm 10\%$

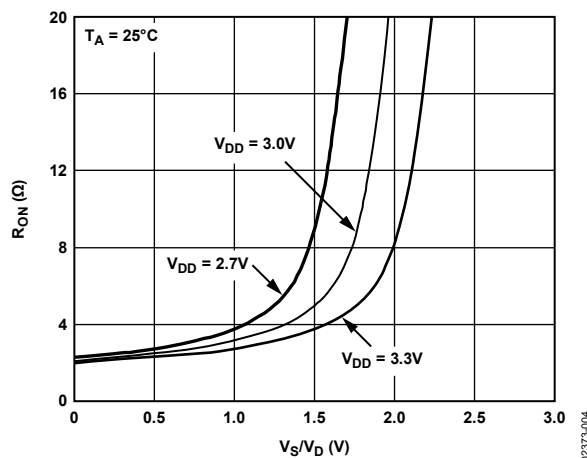


Figure 5. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for $V_{DD} = 3\text{ V} \pm 10\%$

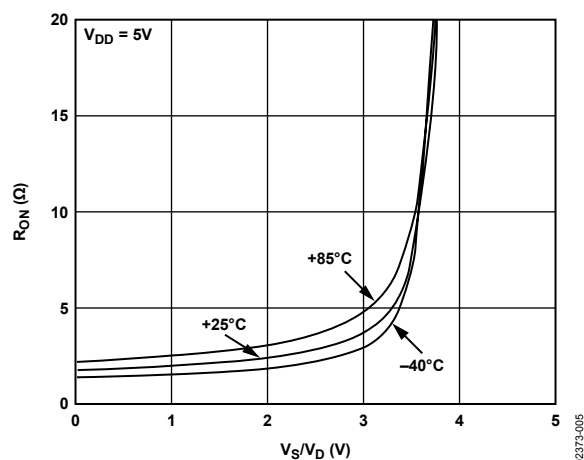


Figure 6. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for Different Temperatures with 5 V Single Supplies

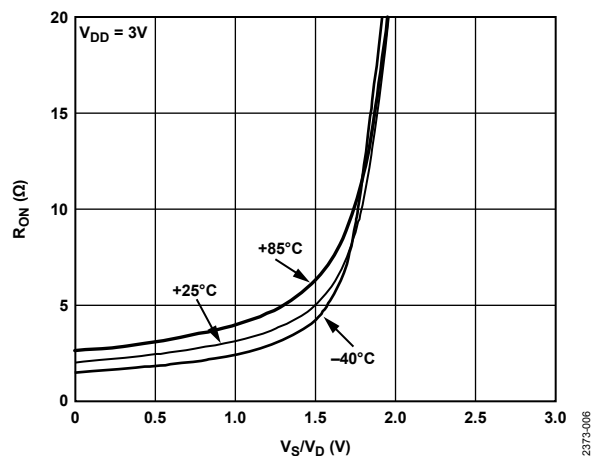


Figure 7. On Resistance as a Function of Drain (V_D) or Source (V_S) Voltage for Different Temperatures with 3 V Single Supplies

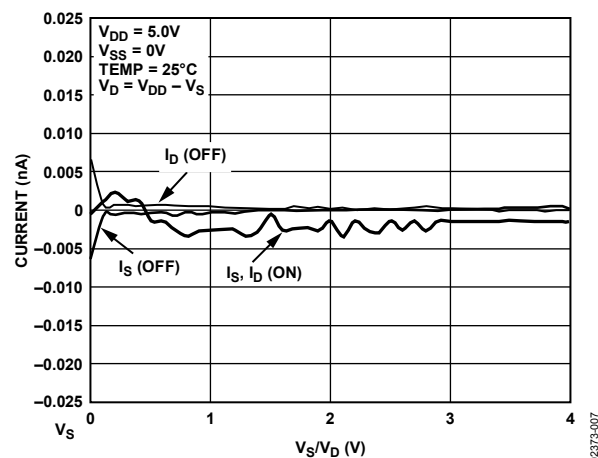


Figure 8. Leakage Current as a Function of Drain (V_D) or Source (V_S) Voltage for $V_{DD} = 5\text{ V}$

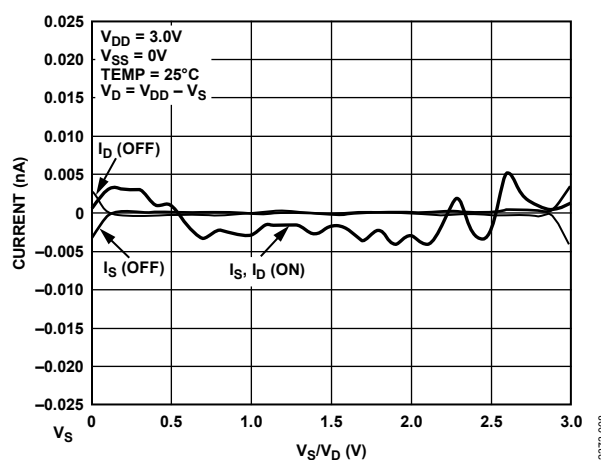


Figure 9. Leakage Current as a Function of Drain (V_D) or Source (V_S) Voltage for $V_{DD} = 3\text{ V}$

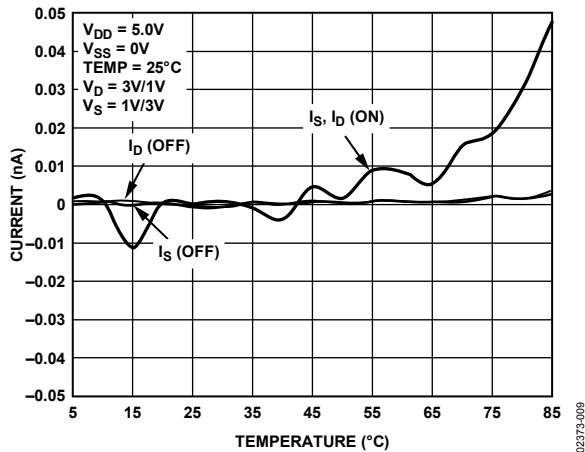


Figure 10. Leakage Current as a Function of Temperature, $V_{DD} = 5\text{ V}$

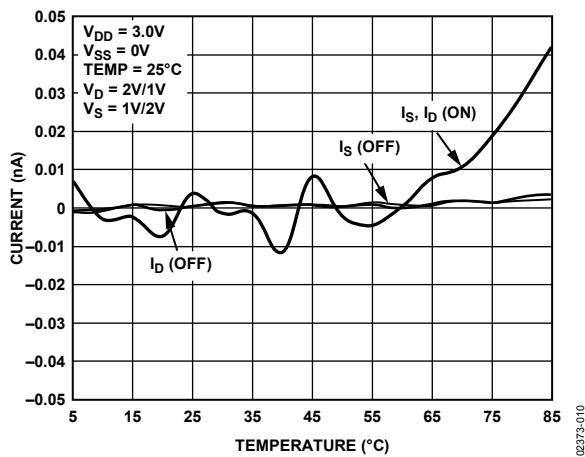


Figure 11. Leakage Current as a Function of Temperature, $V_{DD} = 3\text{ V}$

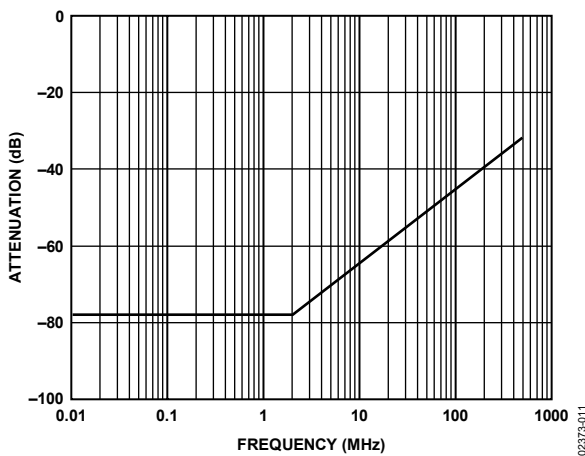


Figure 12. Off Isolation vs. Frequency

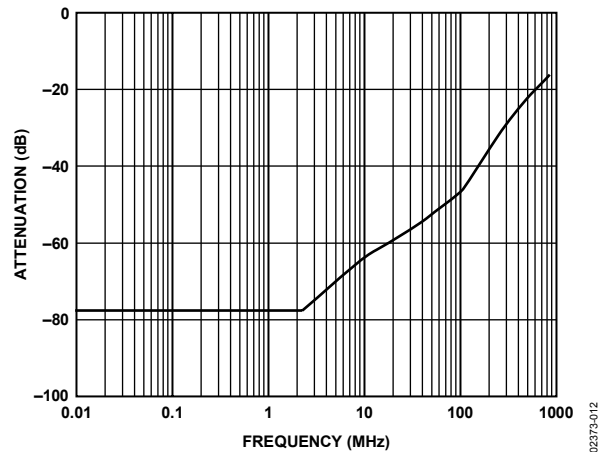


Figure 13. Crosstalk vs. Frequency

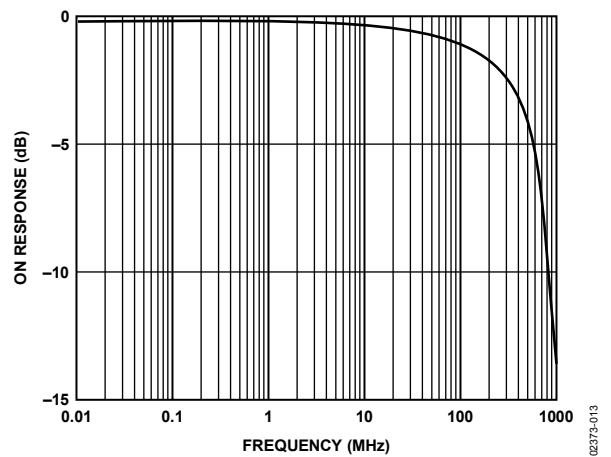


Figure 14. Bandwidth

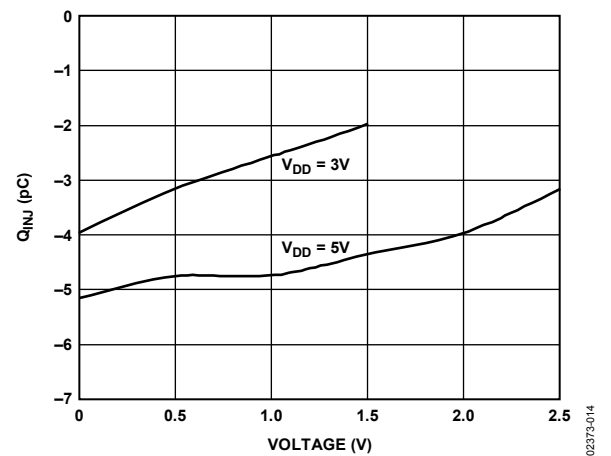


Figure 15. Charge Injection vs. Source Voltage

TEST CIRCUITS

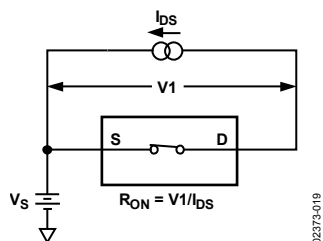


Figure 16. On Resistance

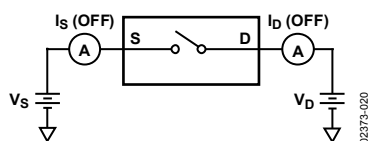


Figure 17. Off Leakage

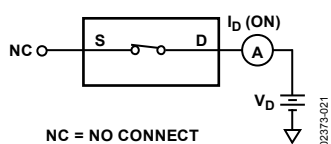


Figure 18. On Leakage

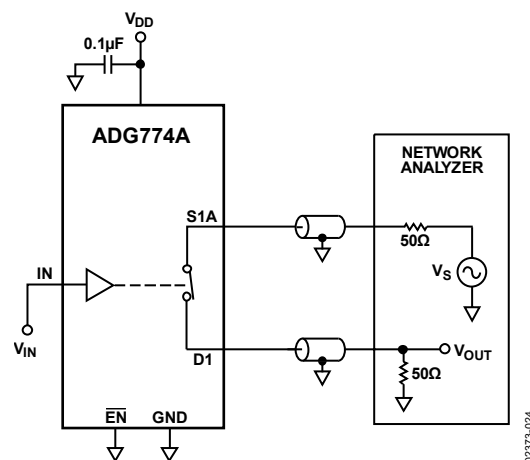


Figure 19. Bandwidth

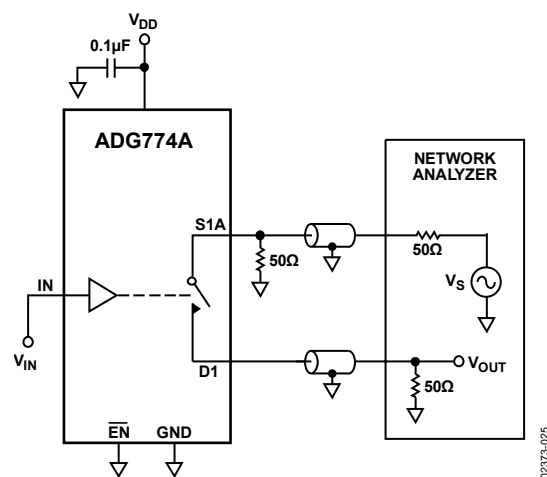


Figure 20. Off Isolation

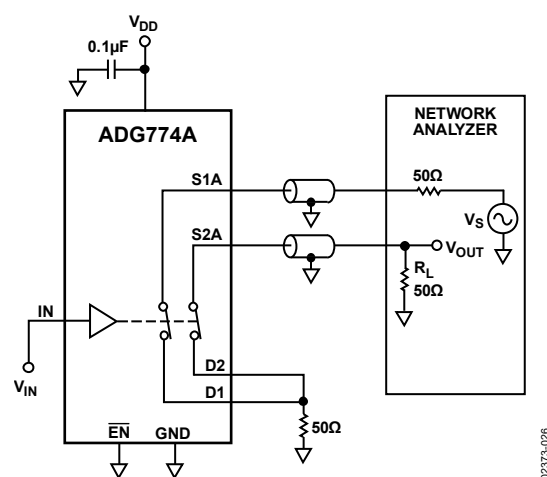


Figure 21. Channel-to-Channel Crosstalk

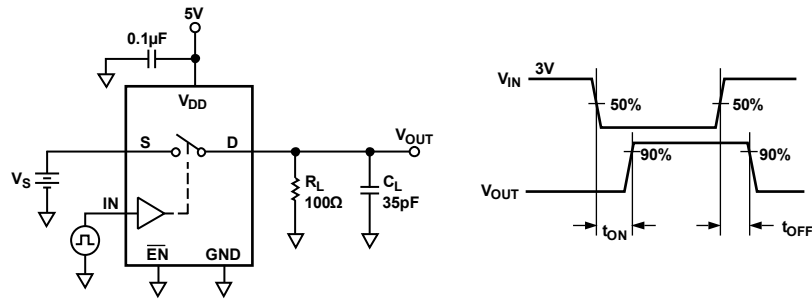


Figure 22. Switching Times

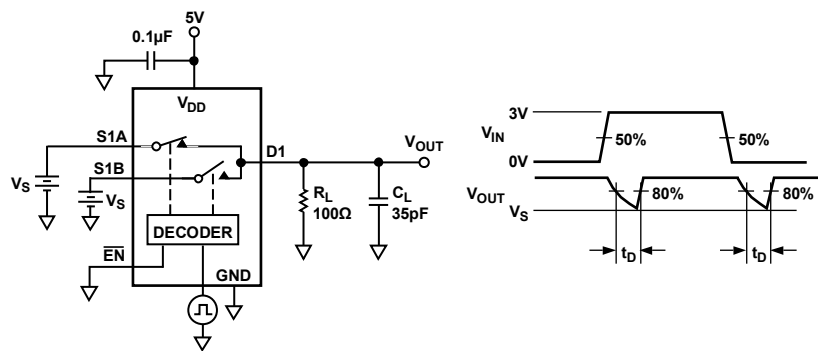


Figure 23. Break-Before-Make Time Delay

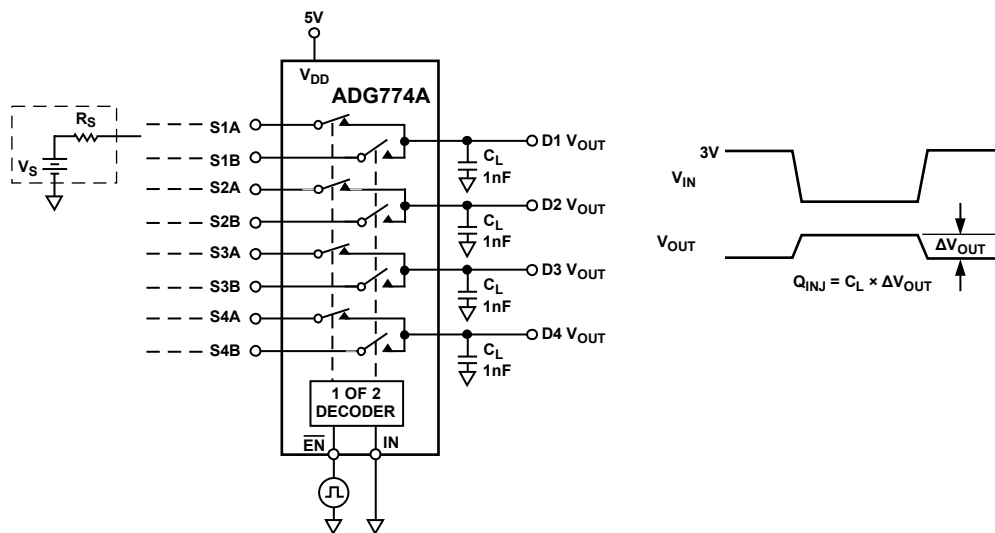


Figure 24. Charge Injection

TERMINOLOGY

V_{DD}

Most positive power supply potential.

GND

Ground (0 V) reference.

S

Source terminal. May be an input or output.

D

Drain terminal. May be an input or output.

IN

Logic control input.

$\overline{\text{EN}}$

Logic control input.

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

On resistance match between any two channels, that is, $R_{ON \text{ max}} - R_{ON \text{ min}}$.

$R_{\text{FLAT(ON)}}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (OFF)

Source leakage current with the switch off.

I_D (OFF)

Drain leakage current with the switch off.

I_D, I_S (ON)

Channel leakage current with the switch on.

V_D (V_S)

Analog voltage on the D and S terminals.

C_S (OFF)

Off switch source capacitance.

C_D (OFF)

Off switch drain capacitance.

C_D, C_S (ON)

On switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on. See Figure 22.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_D

Off time or on time measured between the 80% points of both switches when switching from one address state to another. See Figure 23.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Bandwidth

Frequency response of the switch in the on state measured at 3 dB down.

Distortion

$R_{\text{FLAT(ON)}}/R_L$

APPLICATION CIRCUITS

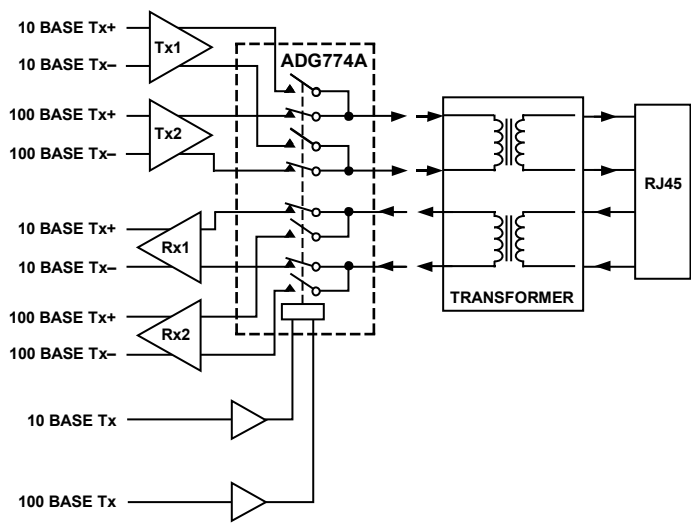


Figure 25. Full Duplex Transceiver

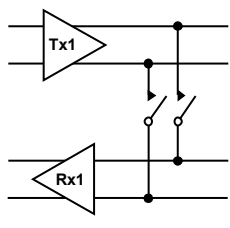


Figure 26. Loop Back

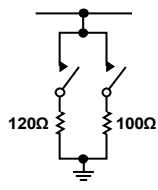


Figure 27. Line Termination

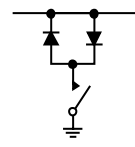
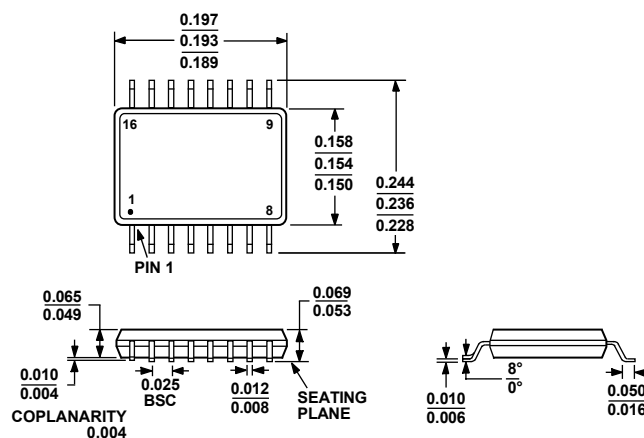


Figure 28. Line Clamp

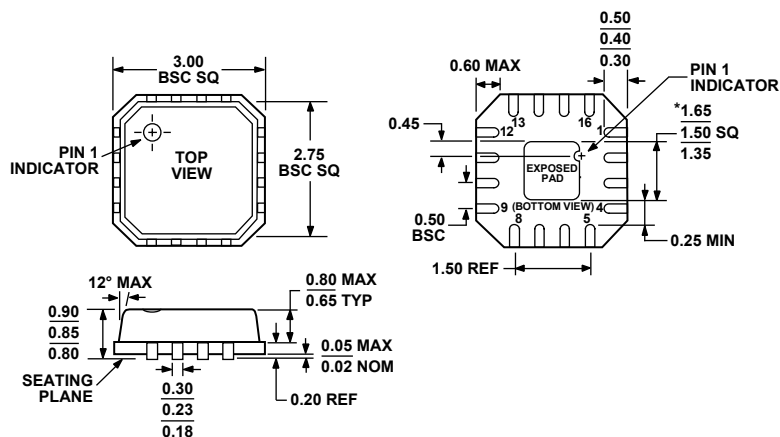
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 29. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)

Dimensions shown in inches



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 30. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
(CP-16-3)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG774ABRQ	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQ-REEL	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQ-REEL7	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ-REEL ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABRQZ-REEL7 ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG774ABCPZ-REEL	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3

¹ Z = Pb-free part.

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