AD8320—SPECIFICATIONS (@ V_{CC} = 12 V, T_A = +25°C, V_{IN} = 0.310 V p-p, R_L = 75 Ω, R_S = 75 Ω unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Full-Scale Input Voltage	Max Gain, P_{OUT} = 18 dBm, V_{CC} = 12 V		0.310		V p-p
	Max Gain, P_{OUT} = 12 dBm, V_{CC} = 5 V		0.155		V p-p
Input Resistance			220		Ω
Input Capacitance			2.0		pF
GAIN CONTROL INTERFACE					
Gain Range			36		dB
Full Scale (Max) Gain			26 (20)		dB (V/V)
Gain Offset (Min) Gain			–10.0 (0.316)		dB (V/V)
Gain Scaling Factor			0.077		V/V/LSB
OUTPUT CHARACTERISTICS					
Bandwidth (–3 dB)	All Gain Codes		150		MHz
Bandwidth Roll-Off	F = 65 MHz		0.7		dB
Bandwidth Peaking	F = 65 MHz		0		dB
Output Offset Voltage	All Gain Codes		±40		mV
Output Offset Drift	Full Temperature Range		±0.25		mV/°C
Output Noise Spectral Density	Max. Gain, Frequency = 10 MHz		73		nV/√Hz
	Min. Gain, Frequency = 10 MHz		53		nV/√Hz
	$\overline{PD}$ = 0, Frequency = 10 MHz		4.5		nV/√Hz
1 dB Compression Point	V_{CC} = 12 V		22.5		dBm
	V_{CC} = 5 V		16		dBm
Output Impedance	Power Up and Power Down	65	75	85	Ω
Overload Recovery	Max Gain, V_{IN} = 500 mV p-p		40		ns
OVERALL PERFORMANCE					
Worst Harmonic Distortion	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 12 V		–57.0	–52.0	dBc
	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		–43.0	–39.0	dBc
	F = 42 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		–46.0	–42.0	dBc
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 12 V		–57.0	–52.0	dBc
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		–42.5	–39.0	dBc
	F = 65 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		–43.0	–40.0	dBc
3rd Order Intercept	F = 42 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		34		dBm
	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		32		dBm
	F = 65 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		32.5		dBm
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		28.5		dBm
Full-Scale (Max Gain) Accuracy	F = 10 MHz		±0.1		dB
Gain Offset (Min Gain) Accuracy	F = 10 MHz		±0.2		dB
Gain Accuracy	F = 10 MHz, All Gain Codes	–0.75	±0.2	0.75	dB
Gain Drift	Full Temperature Range		±0.5		mdB/°C
Gain Variation w/Supply	V_{CC} = +5 V to 12 V		35		mdB/V
Output Settling to 1 mV					
Gain Change @ $T_{\overline{DATEN}}$ = 1	Min to Max Gain, V_{IN} = 0.31 V p-p		30		ns
Input Change	Max Gain, V_{IN} = 0 V to 0.31 V p-p		25		ns
POWER CONTROL					
Power-Down Settling Time to 1 mV	Max Gain, V_{IN} = 0		45		ns
Power-Up Settling Time to 1 mV	Max Gain, V_{IN} = 0		65		ns
Power-Down Pedestal Offset	Max Gain, V_{IN} = 0		±30		mV
Spectral Output Leakage	F ($\overline{PD}$) = 400 Hz @ 15% Duty Cycle		–70		dBm
	5 MHz ≤ F ≤ 65 MHz				
Maximum Reverse Power	$\overline{PD}$ = 0		5		dBm
POWER SUPPLY					
Specified Operating Range		+5		+12	V
Quiescent Current	$\overline{PD}$ = 1, V_{CC} = +5 V		80	85	mA
Power Down	$\overline{PD}$ = 0, V_{CC} = +5 V		25	30	mA
Power Up, V_{CC} = +12 V	$\overline{PD}$ = 1, V_{CC} = +12 V		97	105	mA
Power Down, V_{CC} =+12 V	$\overline{PD}$ = 0, V_{CC} = +12 V		32	37	mA

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LOGIC INPUTS (TTL/CMOS Logic) ($\overline{DATEN}$, CLK, SDATA, 5 V ≤ V_{CC} ≤ 12 V; Full Temperature Range)

Parameter	Min	Typ	Max	Units
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, $\overline{DATEN}$	0		20	nA
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, $\overline{DATEN}$	–450		–75	nA
Logic "1" Current (V_{INH} = 5 V) $\overline{PD}$	0		190	µA
Logic "0" Current (V_{INL} = 0 V) $\overline{PD}$	–320		–70	µA

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} Supply Range, T_R = T_F = 4 ns, F_{CLK} = 8 MHz unless otherwise noted.)

Parameter	Min	Typ	Max	Units
Clock Pulse Width (T_{WH})	12.0			ns
Clock Period (T_C)	32.0			ns
Setup Time SDATA vs. Clock (T_{DS})	6.5			ns
Setup Time $\overline{DATEN}$ vs. Clock (T_{ES})	17.0			ns
Hold Time SDATA vs. Clock (T_{DH})	5.0			ns
Hold Time $\overline{DATEN}$ vs. Clock (T_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{DATEN}$, Clock (T_R, T_F)			10	ns

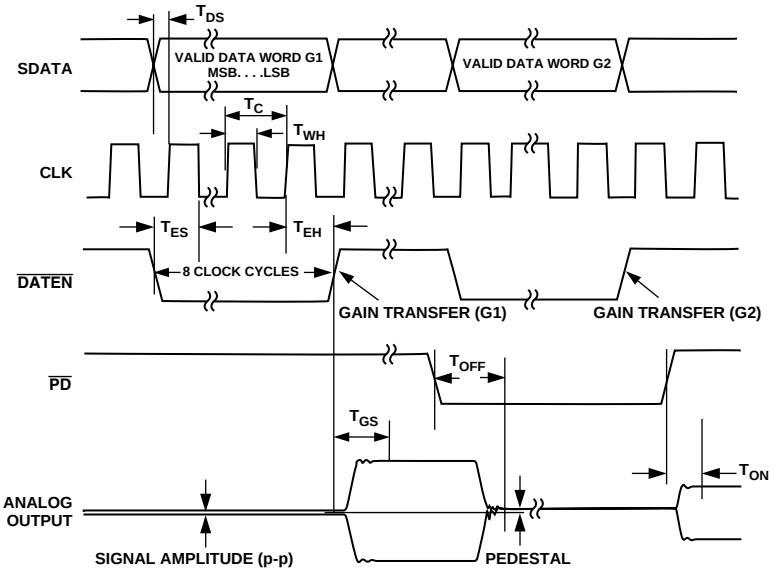

Figure 2. Serial Interface Timing

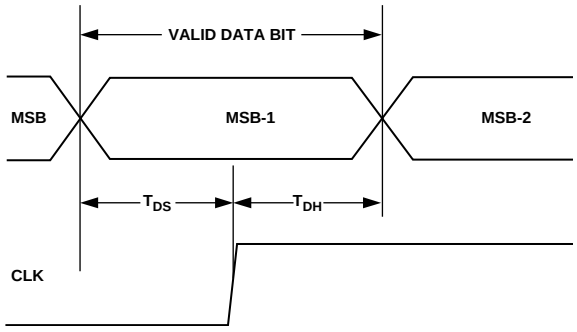

Figure 3.

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $+V_S$
- Pins 7, 8, 9, 17, 20 . . . . . –0.8 V to +13 V

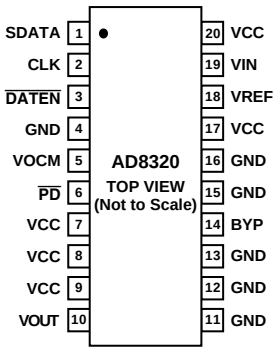
Input Voltages
- Pins 19 . . . . . ±3 V
- Pins 1, 2, 3, 6 . . . . . –0.8 V to +5 V

Internal Power Dissipation
- Small Outline (RP) . . . . . 1.3 W

Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 seconds . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	θ_{JA}	Package Option
AD8320ARP	–40°C to +85°C	20-Lead Thermally Enhanced Power SOIC*	53°C/W	RP-20
AD8320-EB		Evaluation Board		

*Shipped in tubes (38 pieces/tube) and dry packed per J-STD-020.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8320 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Function	Description
1	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
2	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0 to 1 transition latches the data bit and a 1 to 0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
3	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0 to 1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1 to 0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
4, 11, 12, 13, 15, 16	GND	Common External Ground Reference.
5	VOCM	VCC/2 Reference Pin. A dc output reference level that is equal to 1/2 of the supply voltage (VCC). This port should be externally ac decoupled (0.1 µF cap).
6	$\overline{\text{PD}}$	Power-Down Low Logic Input. A Logic 0 powers down (shuts off) the power amplifier disabling the output signal and enabling the reverse amplifier. A Logic 1 enables the output power amplifier and disables the reverse amplifier.
7, 8, 9, 17, 20	VCC	Common Positive External Supply Voltage.
10	VOUT	Output Signal Port. DC biased to approximately VCC/2.
14	BYP	Internal Bypass. This pin must be externally ac decoupled (0.1 µF cap).
18	VREF	Input Reference Voltage (typically 1.9 V at 27°C). This port should be externally ac decoupled (0.1 µF cap).
19	VIN	Analog Voltage Input Signal Port. DC biased to VREF voltage.

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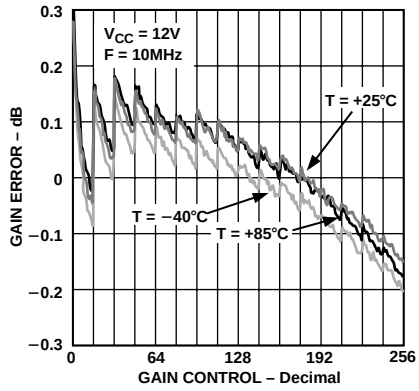

Figure 4. Gain Error vs. Gain Control at Various Temperatures

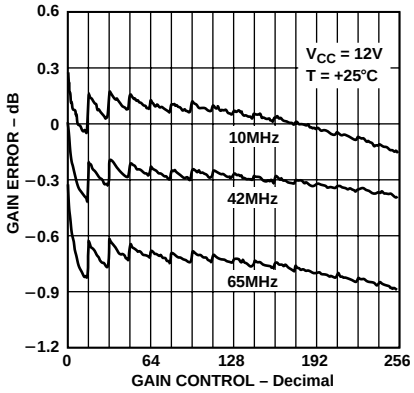

Figure 5. Gain Error vs. Gain Control at Various Frequencies

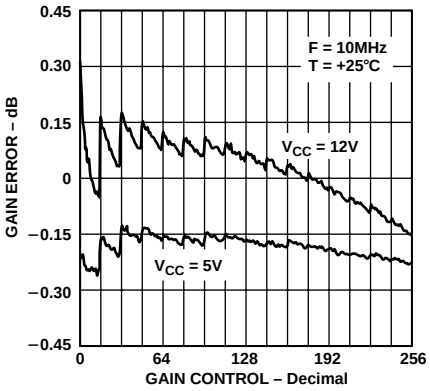

Figure 6. Gain Error vs. Gain Control at Different Supply Voltages

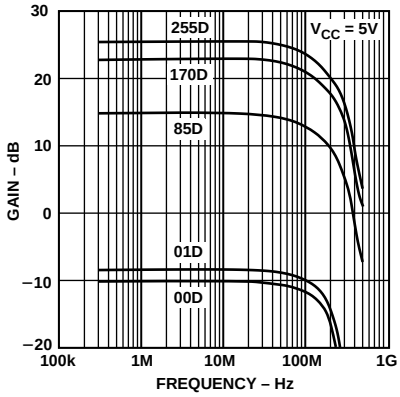

Figure 7. AC Response

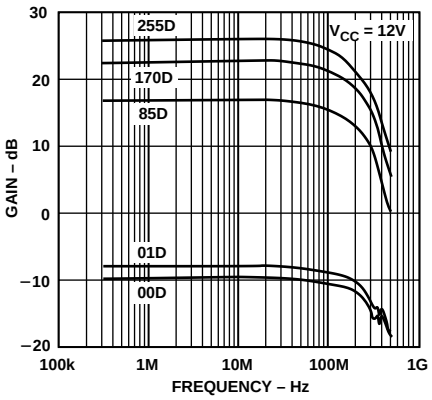

Figure 8. AC Response

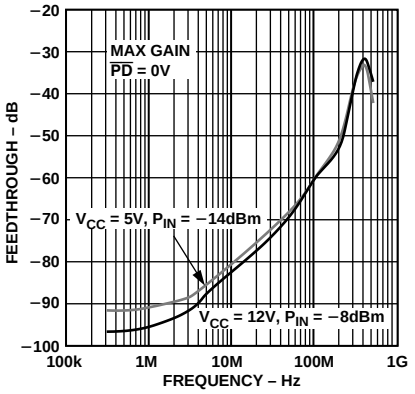

Figure 9. Input Signal Feedthrough vs. Frequency

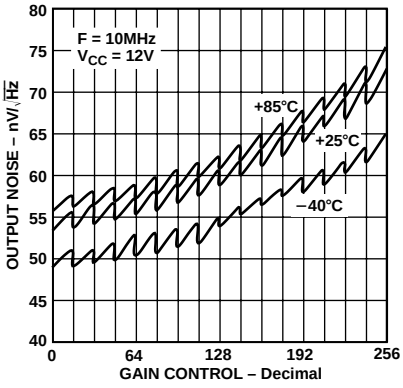

Figure 10. Output Referred Noise vs. Gain Control at Various Temperatures

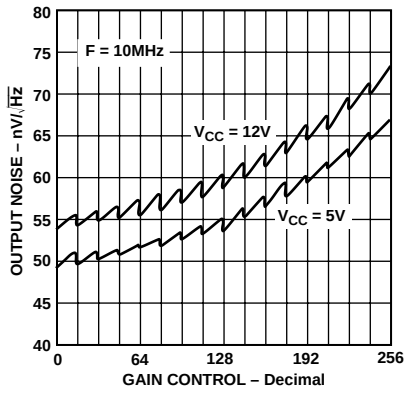

Figure 11. Output Referred Noise vs. Gain Control at Different Supply Voltages

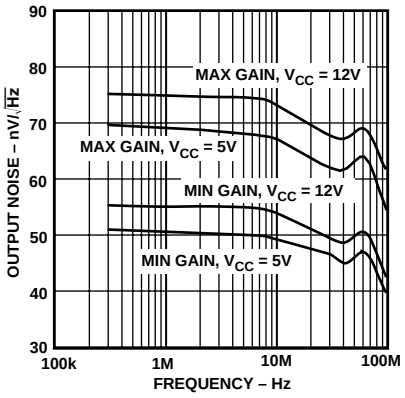

Figure 12. Output Referred Noise vs. Frequency

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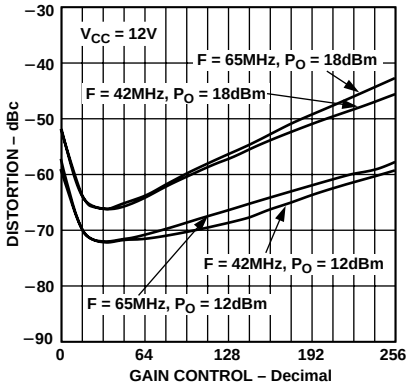

Figure 13. Worst Harmonic Distortion vs. Gain Control

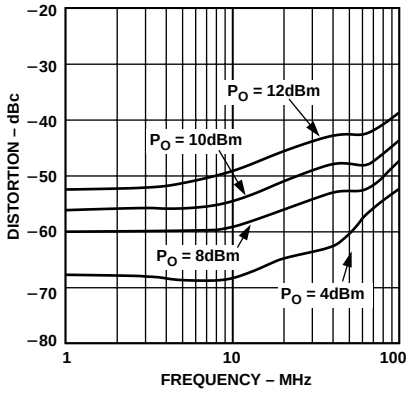

Figure 14. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 5 V

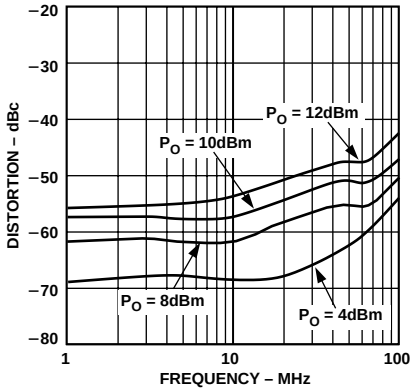

Figure 15. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 6 V

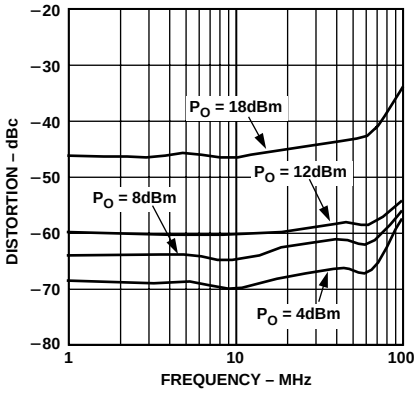

Figure 16. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 10 V

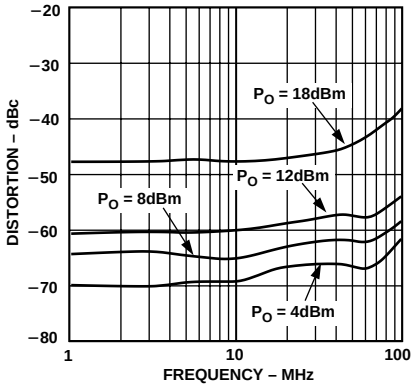

Figure 17. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 12 V

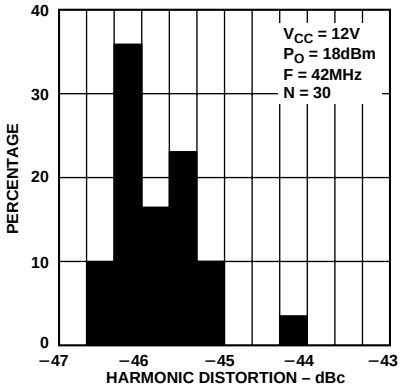

Figure 18. Distribution of Worst Harmonic Distortion

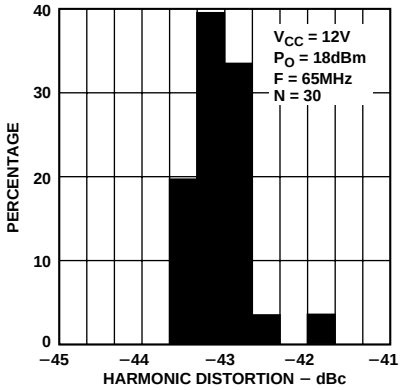

Figure 19. Distribution of Worst Harmonic Distortion

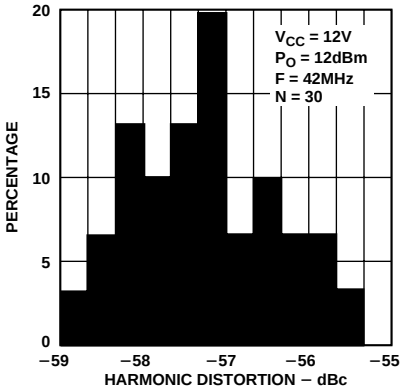

Figure 20. Distribution of Worst Harmonic Distortion

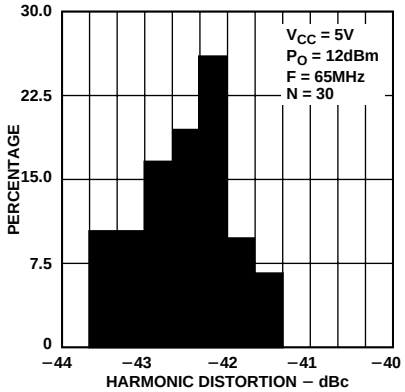

Figure 21. Distribution of Worst Harmonic Distortion

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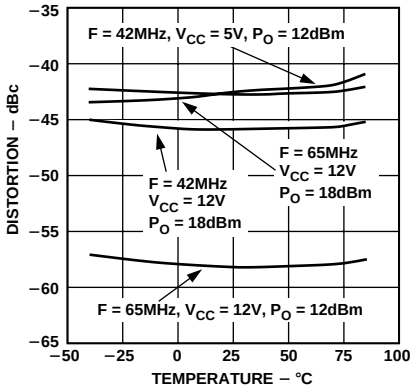

Figure 22. Harmonic Distortion vs. Temperature

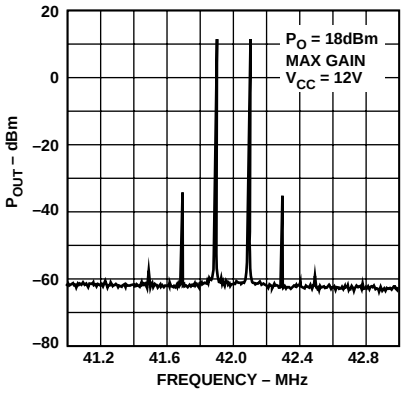

Figure 23. Two-Tone Intermodulation Distortion

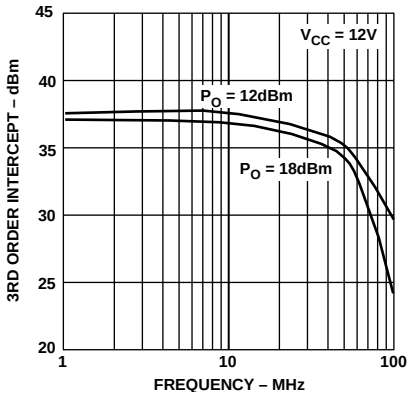

Figure 24. Third Order Intercept vs. Frequency

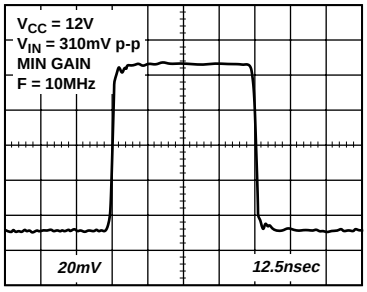

Figure 25. Transient Response

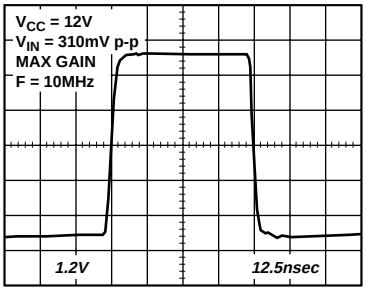

Figure 26. Transient Response

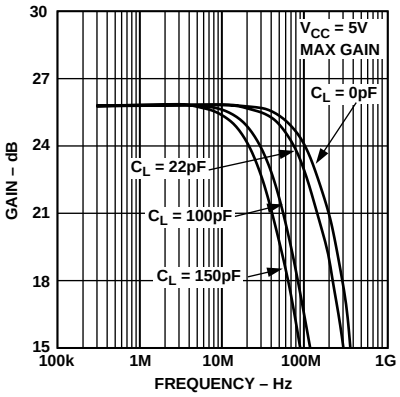

Figure 27. AC Response for Various Capacitive Loads

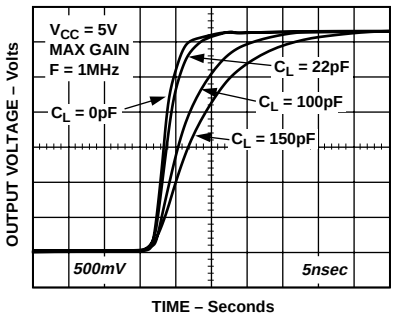

Figure 28. Transient Response for Various Capacitive Loads

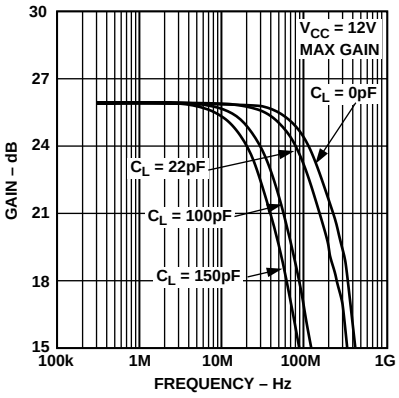

Figure 29. AC Response for Various Capacitive Loads

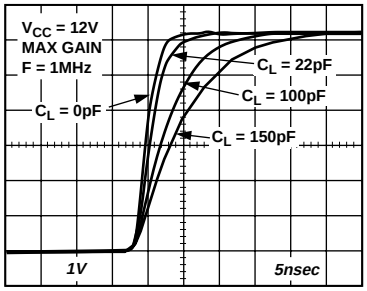

Figure 30. Transient Response for Various Capacitive Loads

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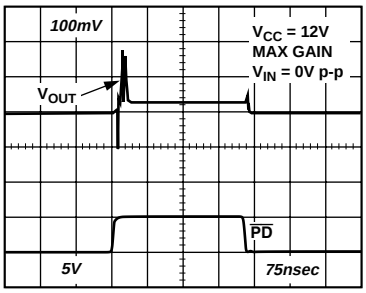

Figure 31. Power-Up/Power-Down Glitch

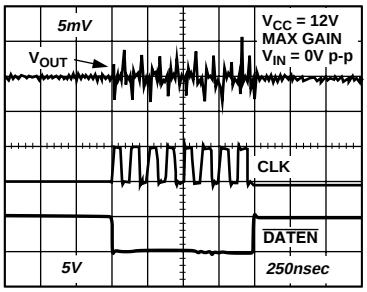

Figure 32. Clock Feedthrough

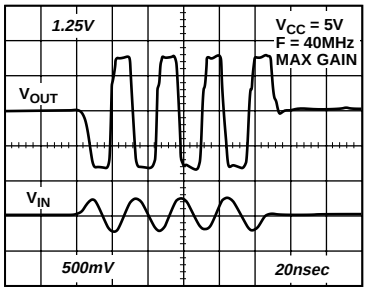

Figure 33. Overload Recovery

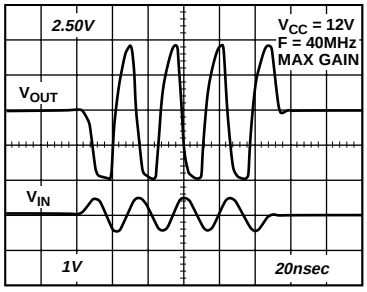

Figure 34. Overload Recovery

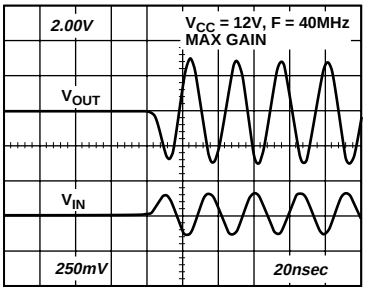

Figure 35. Output Settling Time Due to Input Change

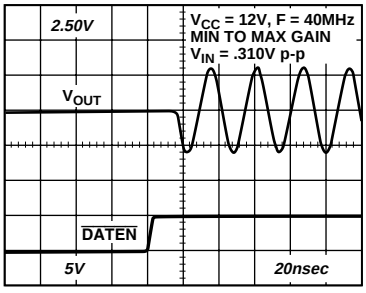

Figure 36. Output Settling Time Due to Gain Change

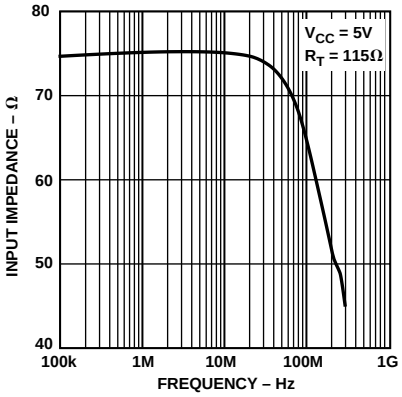

Figure 37. Input Impedance vs. Frequency

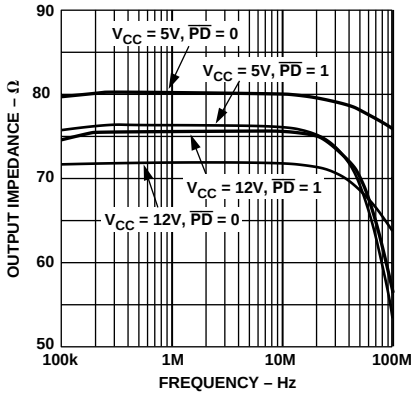

Figure 38. Output Impedance vs. Frequency

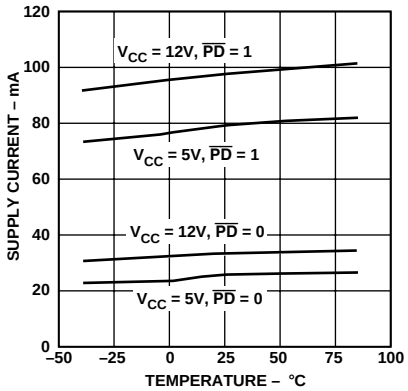

Figure 39. Supply Current vs. Temperature

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OPERATIONAL DESCRIPTION

The AD8320 is a digitally controlled variable gain power amplifier that is optimized for driving 75 Ω cable. A multifunctional bipolar device on single silicon, it incorporates all the analog features necessary to accommodate reverse path (upstream) high speed (5 MHz to 65 MHz) cable data modem and cable telephony requirements. The AD8320 has an overall gain range of 36 dB (–10 dB to 26 dB) and is capable of greater than 100 MHz of operation at output signal levels exceeding 18 dBm. Overall, when considering the device's wide gain range, low distortion, wide bandwidth and variable load drive, the device can be used in many variable gain block applications.

The digitally programmable gain is controlled by the three wire "SPI" compatible inputs. These inputs are called SDATA (serial data input port), $\overline{\text{DATEN}}$ (data enable low input port) and CLK (clock input port). See Pin Function Descriptions and Functional Block diagram. The AD8320 is programmed by an 8-bit "attenuator" word. These eight bits determine the 256 programmable gain settings. See attenuator core description below. The gain is linear in V/V/LSB and can be described by the following equation:

$$A_V = 0.316 + 0.077 \times Code \ (R_L = 75\ \Omega)$$

where *code* is the decimal equivalent of the 8-bit word. For example, if all 8 bits are at a logic "1," the decimal equivalent is 255 and A_V equals 19.95 V/V or 26 dB. The gain scaling factor is 0.077 V/V/LSB, with an offset of 0.316 V/V (–10.0 dB). Figure 40 shows the linear gain versus decimal code and Figure 41 shows the gain in dB versus decimal code. Note the nonlinearity that results when viewed in dB versus code. The dB step size increases as the attenuation increases (i.e., gain decreases) and reaches a maximum step size of approximately 1.9 dB (gain change between 01 and 00 decimal).

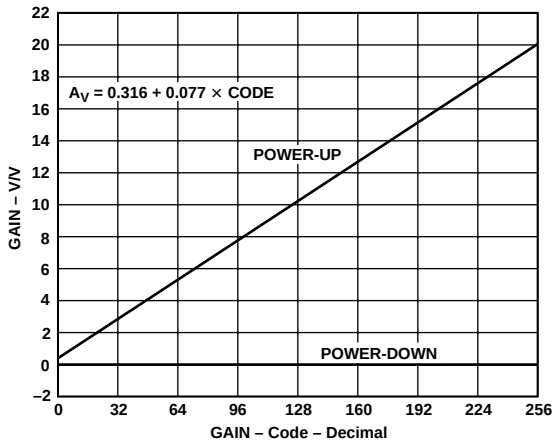

Figure 40. Linear Gain vs. Gain Control

The AD8320 is composed of three analog functions in the power-up or forward mode (Figure 42). The input inverter/buffer amplifier provides single-ended to differential output conversion. The output signals are nominally 180 degrees out of phase and equal in amplitude with a differential voltage gain of 2 (6 dB). Maintaining close to 180 degrees and equal amplitude is required for proper gain accuracy of the attenuator core over the specified operating frequency. The input buffer/inverter also provides equal dc voltages to the core inputs via the internal reference. This is required to ensure proper core linearity over the full specified power supply range (5 V to 12 V).

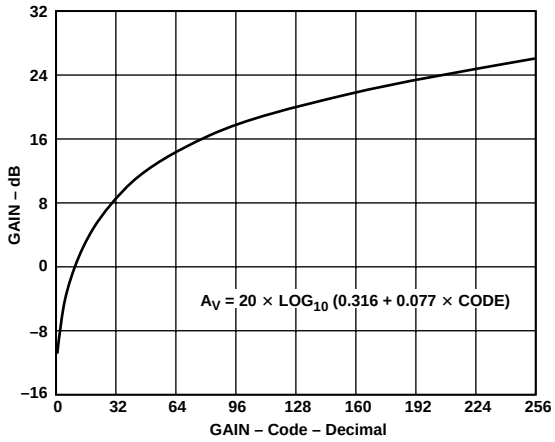

Figure 41. Log Gain vs. Gain Control

The attenuator core can be viewed as eight binarily weighted (differential in–differential out) transconductance (gm) stages with the "in phase" current outputs of all eight stages connected in parallel to their respective differential load resistors (not shown). The core *differential* output signals are also 180 degrees out of phase and equal in amplitude. The input stages are likewise parallel, connected to the inverting input amplifier and buffer outputs as shown. Nine bits plus of accuracy is achieved for all gain settings over the specified frequency, supply voltage and temperature range. The actual total core GM × RL attenuation is determined by which combination of binarily weighted gm stages are selected by the data latch. With 8 bits, 256 levels of attenuation can be programmed. This results in a 36 dB attenuation range (0 dB to –36 dB). See gain equation above.

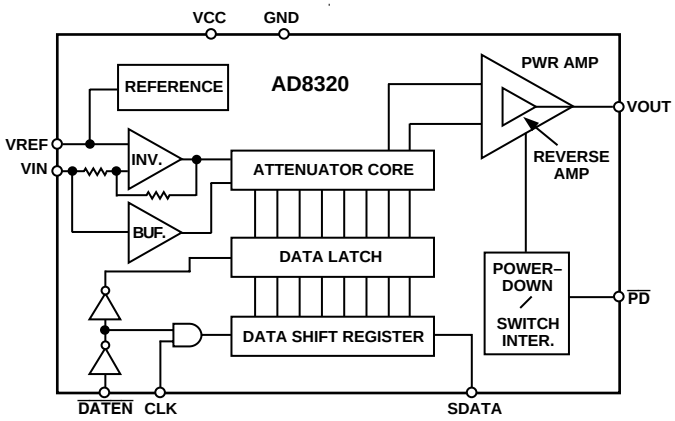

Figure 42. Functional Block Diagram

To update the AD8320 gain, the following digital load sequence is required. The attenuation setting is determined by the 8-bit word in the data latch. This 8-bit word is serially loaded (MSB first) into the shift register at each rising edge of the clock. See Figure 43. During this data load time (T), $\overline{\text{DATEN}}$ is low and the data latch is latched holding the previous (T – 1) data word keeping the attenuation level unchanged. After eight clock cycles the new data word is fully loaded and $\overline{\text{DATEN}}$ is switched high. This enables the data latch (becomes transparent) and the loaded register data is passed to the attenuator with the updated gain value. Also at this $\overline{\text{DATEN}}$ transition, the internal clock is disabled, thus inhibiting new serial input data.

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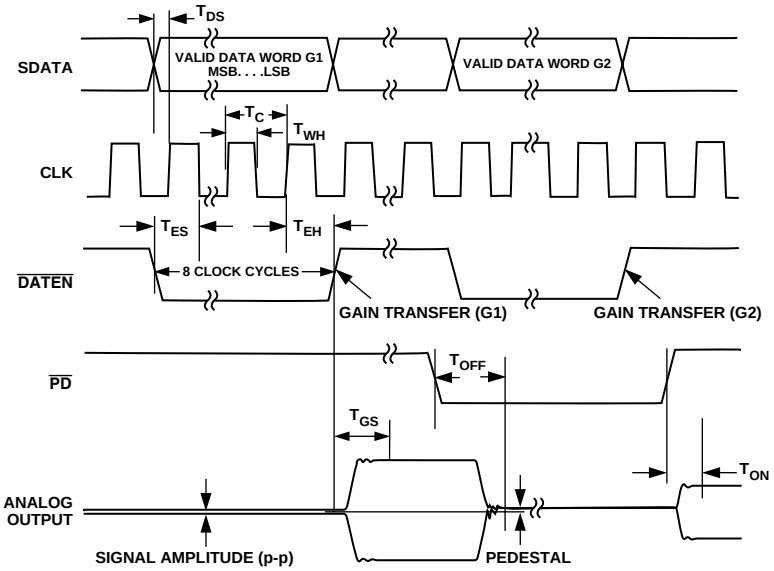

Figure 43. Serial Interface Timing

The power amplifier has two basic modes of operation; forward or power-up mode and reverse or power-down mode. In the power-up mode ($\overline{PD}$ = 1), the power amplifier stage is enabled and the differential output core signal is amplified by 20 dB. With a core attenuation range of 0 dB to –36 dB and 6 dB of input gain, the overall AD8320 gain range is 26 dB to –10 dB. In this mode, the single-ended output signal maintains a dc level of VCC/2. This dc output level provides for optimum large signal linearity and allows for dc coupling the output if necessary. The output stage is unique in that it maintains a dynamic output impedance of 75 Ω. This allows for a direct 75 Ω cable connection and results in 6 dB of added load power versus using a series 75 Ω back-termination resistor as required with traditional low output impedance amplifiers. The power amplifier will also drive lower or higher output loads, although the device's gain (not gain range) will change accordingly (see Applications section).

In the power-down mode ($\overline{PD}$ = 0), the power amplifier is turned off and a "reverse" amplifier (the inner triangle in Figure 42) is enabled. During this 1 to 0 transition, the output power amplifier's input stage is also disabled, resulting in no forward output signal (S21 is 0), although the attenuator core and input amplifier/buffer signals are not affected (S11 ≈ 0). The function of the reverse amplifier is to maintain 75 Ω and VCC/2 at the output port (VOUT) during power-down. This is required to minimize line reflections (S22 ≈ 0) and ensures proper filter operation for any forward mode device sharing the same bus (i.e., in a multiplexed configuration). (See Applications section.) In the time domain, as $\overline{PD}$ switches states, a transitional glitch and pedestal offset results. (See Figures 31 and 43.) The powered down supply current drops to 32 mA versus 97 mA (V_{CC} = 12 V) in power-up mode.

Generally, using the power-down low input ($\overline{PD}$) for switching allows for multiple devices to be multiplexed via splitters (N-1 off, 1 on) and reduces overall total power consumption as required for cable data applications. For cable telephony, the power-down current generally needs to be much lower during what is referred to as sleep and standby modes, and VCC supply switching via PFETS or equivalent, as described in the applications section, would be required.

APPLICATIONS

The AD8320 is primarily intended to be used as the return path (also called upstream path) line driver in cable modem and cable telephony applications. Data to be transmitted is modulated in either QPSK or QAM format. This is done either in DSP or by a dedicated QPSK/QAM modulator such as the AD9853.

The amplifier receives its input signal either from the dedicated QPSK/QAM modulator or from a DAC. In both cases, the signal must be low-pass filtered before being applied to the line driving amplifier.

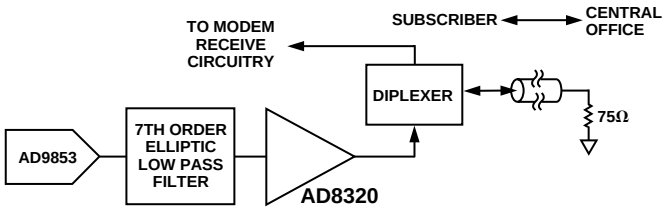

Figure 44. Block Diagram of Cable Modem's Upstream Driver Section

The amplifier drives the line through a diplexer. The insertion loss of a diplexer is typically –3 dB. As a result, the line driver must deliver a power level roughly 3 dB greater than required by the applicable cable modem standard so that diplexer losses are canceled out.

Because the distance to the central office varies from subscriber to subscriber, signals from different subscribers will be attenuated by differing amounts. As a result, the line driver is required to vary its gain so that all signals arriving at the central office have the same amplitude.

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Basic Connection

Figure 45 shows the basic schematic for operating the AD8320. Because the amplifier operates from a single supply, the input signal must be ac-coupled using a 0.1 µF capacitor. The input pin has a bias level of about 1.9 V. This bias level is available on the VREF pin (Pin 18) and can be used to externally bias signals if dc-coupling is desired. Under all conditions, a 0.1 µF decoupling capacitor must be connected to the VREF pin. If the VREF voltage is to be used externally, it should be buffered first.

The VIN pin of the AD8320 (Pin 19) has an input impedance of 220 Ω. Typically, in video applications, 75 Ω termination is favored. As a result, an external shunt resistance (R1) to ground of 115 Ω is required to create an overall input impedance of 75 Ω. If 50 Ω termination is required, a 64.9 Ω shunt resistor should be used. Note, to avoid dc loading of the VIN pin, the ac-coupling capacitor should be placed between the input pin and the shunt resistor as shown in Figure 45.

On the output side, the VOUT pin also has a dc bias level. In this case the bias level is midway between the supply voltage and ground. The output signal must therefore be ac-coupled before being applied to the load. The dc bias voltage is available on the VOCM pin (Pin 5) and can be used in dc-coupled applications. This node must be decoupled to ground using a 0.1 µF capacitor. If the VOCM voltage is to be used externally, it should be buffered.

Since the AD8320 has a dynamic output impedance of 75 Ω, no external back termination resistor is required. If the output signal is being evaluated on 50 Ω test equipment such as a spectrum analyzer, a 75 Ω to 50 Ω adapter (commonly called a pad) should be used to maintain a properly matched circuit.

Varying the Gain

The gain of the AD8320 can be varied over a range of 36 dB, from –10 dB to +26 dB, by varying the 8-bit gain setting word.

The timing diagram for AD8320's serial interface is shown in Figure 43.

The write cycle to the device is initiated by the falling edge of $\overline{\text{DATEN}}$. This is followed by eight clock pulses that clock in the control word. Because the clock signal is level triggered, data is effectively clocked on the falling edge of CLK.

After the control word has been clocked in, the $\overline{\text{DATEN}}$ line goes back high, allowing the gain to be updated (this takes about 30 ns).

The relationship between gain and control word is given by the equation:

$$Gain\ (V/V) = 0.077 \times Code + 0.316$$

where *code* is the decimal equivalent of the gain control word (0 to 255).

The gain in dB is given by the equation:

$$Gain\ (dB) = 20 \log_{10} (0.077 \times Code + 0.316)$$

The digital interface also contains an asynchronous power-down mode. The normally high $\overline{\text{PD}}$ line can be pulled low at any time. This turns off the output signal after 45 ns, and reduces the quiescent current to between 25 mA and 32 mA (depending upon the power supply voltage). In this mode, the programmed gain is maintained.

Clock Line Feedthrough

Clock feedthrough results in a 5 mV p-p signal appearing superimposed on the output signal (see Figure 32). If this impinges upon the dynamic range of the application, the clock signal should be noncontinuous, i.e., should only be turned on for eight cycles during programming.

Power Supply and Decoupling

The AD8320 should be powered with a good quality (i.e., low noise) single supply of between +5 V and +12 V. In order to achieve an output power level of +18 dBm (6.2 V p-p) into

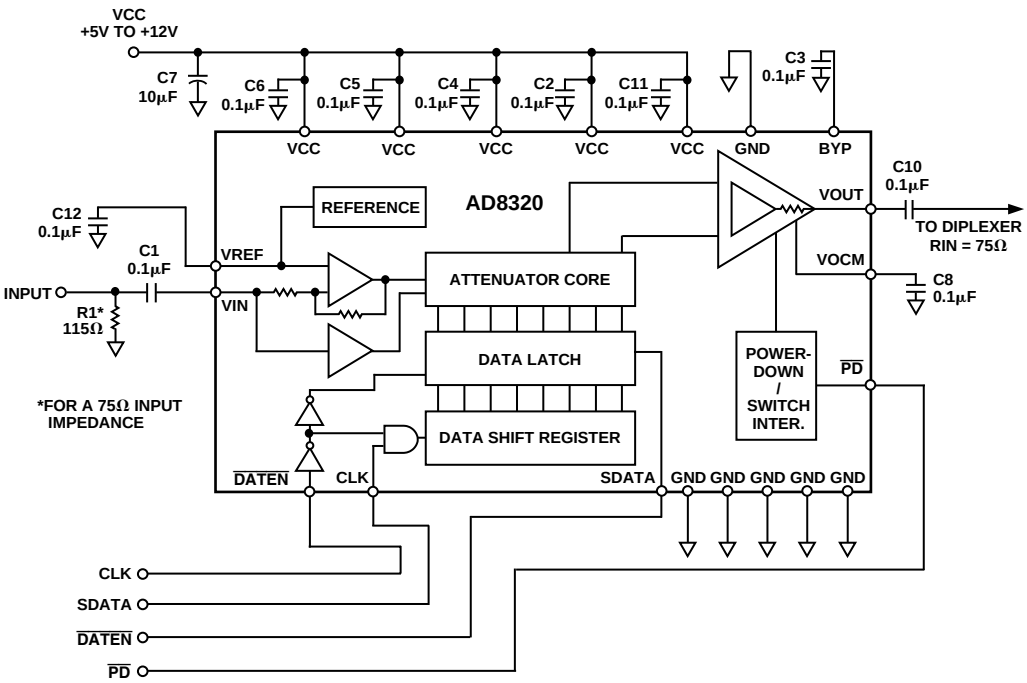

Figure 45. Basic Connection

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75 Ω, a supply voltage of at least +10 V is required. To achieve a signal level of +12 dBm (about 3.1 V p-p) into 75 Ω, a minimum supply level of +5 V is required. However, for the lowest possible distortion, the power supply voltage should be raised as high as possible. In varying the power supply from +5 V to +12 V, the quiescent current increases from 80 mA to 97 mA.

Careful attention must be paid to decoupling the power supply pins. A 10 µF capacitor, located fairly close to the device, is required to provide good decoupling for lower frequency signals. In addition, five 0.1 µF decoupling capacitors should be located close to each of the five power supply pins (7, 8, 9, 17 and 20). A 0.1 µF capacitor must also be connected to the pin labeled BYP (Pin 14), to provide decoupling to an internal node of the device. All six ground pins should be connected to a low impedance ground plane.

Alternative Power-Down Mode

As previously mentioned, the AD8320 can be put into a low power sleep mode by pulling the $\overline{PD}$ pin low. If lower power consumption is required during power-down mode, an alternative scheme can be used as shown in Figure 46.

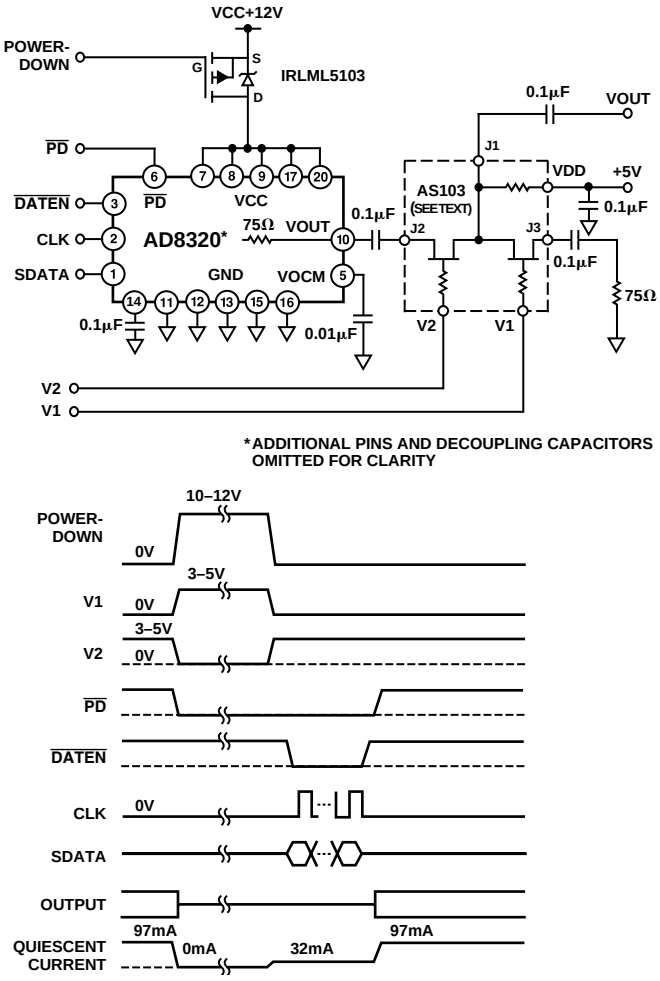

Figure 46. Alternative Power-Down Mode with Timing

A HEXFET power MOSFET (International Rectifier part number IRLML5103) is used to turn on and off the current to the supply pins of the AD8320. Under normal operating conditions, the gate (labeled POWER-DOWN) should be grounded. Pulling the gate to within 2 V of the supply will open the switch and reduce the current to the amplifier to zero.

In cable modem and cable telephony applications the modem must always present an output impedance of 75 Ω to the line. This forces the line driver to always present a 75 Ω impedance to the diplexer. In this application, a single pole double throw RF switch (AS103, Alpha Semiconductor) is used to switch in an external 75 Ω impedance when the AD8320 is turned off. This resistor then mimics the dynamic output impedance of the AD8320. TTL or CMOS logic can be used to drive the two voltages driving the RF switch (V1 and V2).

Before the AD8320 is turned back on again, the gain needs to be set to a known level. This can be done by holding the $\overline{PD}$ pin of the AD8320 low after POWER-DOWN has gone high. While $\overline{PD}$ is held low, the 8-bit serial data stream can be clocked into the AD8320. During this time the quiescent current will increase to 32 mA. However, this time period can be as small as about 1 µs. In this mode the output settles about 45 ns after the rising edge of $\overline{PD}$.

Alternatively, if $\overline{DATEN}$ is held low as the AD8320 is powered on, the device will power up in minimum gain. In this mode, the output settles after about 200 µs. Note that for both cases, the capacitor on VOCM has been reduced from 0.1 µF to 0.01 µF to facilitate a faster turn-on time. All other capacitors in the circuit should be connected as shown in Figure 45.

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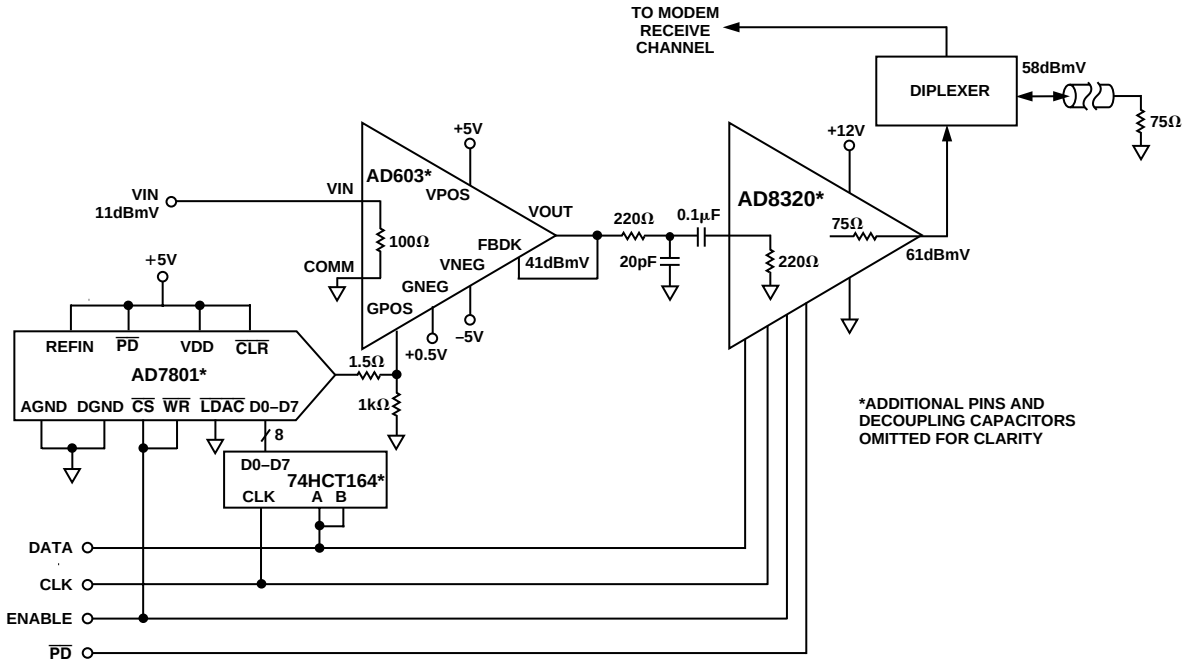

Figure 47. Enhanced Dynamic Range Circuit

Enhanced Dynamic Range Application

The AD8320 can be combined with the AD603 to give additional dynamic range as shown in Figure 47. The AD603 is a voltage controlled variable gain amplifier. The gain of the AD603 is determined by the difference in voltage between the GPOS and GNEG pins. This differential voltage has a range of ±0.5 V. In this example, the voltage on GNEG is tied to +0.5 V. As the voltage on GPOS is varied from 0 V to 1 V, the gain of the AD603 changes from –10 dB to +30 dB with a slope of 25 mV/dB (i.e., linear in dB). The gain control voltage is supplied by the AD7801 DAC. The output voltage of the DAC (0 V to +2.5 V) is divided down to fit the 0 V to 1 V range of the AD603 using a resistor attenuator network.

In order that the same gain control word can be used for both the AD603 and the AD8320, the serial data stream is converted to the parallel format of the AD7801 DAC using a serial-to-parallel shift register. The rising edge of the enable pulse simultaneously updates both amplifiers.

As the control word is varied from 00Dec to 255Dec, the gain of the signal chain varies from –26 dB to +50 dB (there is 6 dB of attenuation between AD603 and AD8320). In practice, this circuit is not usable at the lower end of the gain range due to the small input signal (11 dBmV or about 10 mV p-p). Figure 48 shows the spectrum of the output signal at a frequency of 42 MHz and an output level of 61 dBmV (3.1 V p-p, max gain).

The gain vs. code transfer function of the two amplifiers along with the overall gain is shown in Figure 49. The overall gain transfer function combines a linear in dB transfer function with a linear in Volts/Volt transfer function. It is clear from Figure 49 that the overall gain transfer function can be considered to be approximately linear in dB over the top 50 dB of its range.

Figure 48. Output Spectrum of Enhanced Dynamic Range Circuit (Output Level = 61 dBmV, Frequency = 42 MHz)

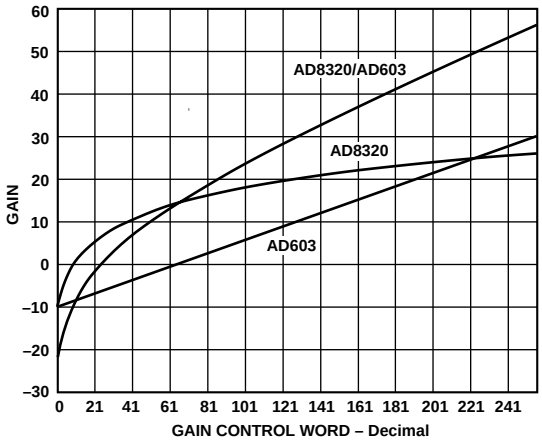

Figure 49. Gain Transfer Function of Enhanced Dynamic Range Circuit

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Varying Gain by Varying Load Impedance

As already mentioned, the AD8320 has a dynamic output impedance of 75 Ω. The specified gain range assumes that the output is terminated with a 75 Ω load impedance. Varying the load impedance allows the gain to be varied, up to a maximum of twice the specified gain (for $R_L = \infty$). The variation in gain with load resistance is shown in Figure 50 for the case of a gain control word of 255Dec (i.e., max gain).

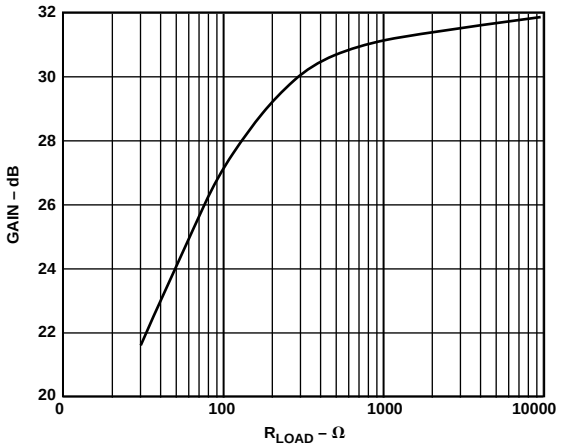

Figure 50. Gain vs. R_{LOAD} (Gain Control Word = 255Dec)

The gain can be described by the following equation:

$$A_V = 20 \log_{10} \left[\left(\frac{2 R_{LOAD}}{R_{LOAD} + 75} \right) (0.316 + 0.077 \times Code) \right]$$

where *Code* is the decimal equivalent of the 8-bit word.

Evaluation Board

A two layer evaluation board for the AD8320 is available (part number AD8320-EB). This board has been carefully laid out and tested to demonstrate the specified high speed performance of the device. Figure 51 shows the schematic of the evaluation board. The silkscreen for the component side layer is shown in Figure 52. The layout of the board is shown in Figure 53 and Figure 54.

The evaluation board package includes a fully populated board with BNC-type connectors along with Windows®-based software for controlling the board from a PC's printer port via a standard printer cable.

A prototyping area is provided to allow for additional circuitry on the board. The single supply and ground to the board are brought over to this area and are available on two strips. There are also two extra strips available on the prototyping area which can be used for additional power supplies.

The board should be powered with a good quality (i.e., low noise) single supply of between +5 V and +12 V. Extensive decoupling is provided on the board. A 10 µF capacitor, located fairly close to the device, provides good decoupling for lower frequency signals. In addition, and more importantly, five 0.1 µF decoupling capacitors are located close to each of the five power supply pins (7, 8, 9, 17 and 20).

Controlling the Evaluation Board from a PC

The evaluation board ships with Windows-based control software. A standard printer cable can be used to connect the evaluation board to a PC's printer port (also called parallel port). The cable length should be kept to less than about 5 feet. The wiring of a standard printer cable, with respect to the signal lines that are used in this application, is shown in Figure 55. Although the software controls the evaluation board via the PC's parallel port, the AD8320 digital interface is serial. Three of the parallel port's eight bits (and one digital ground line) are used to implement this serial interface. A fourth bit is used to control the $\overline{PD}$ pin.

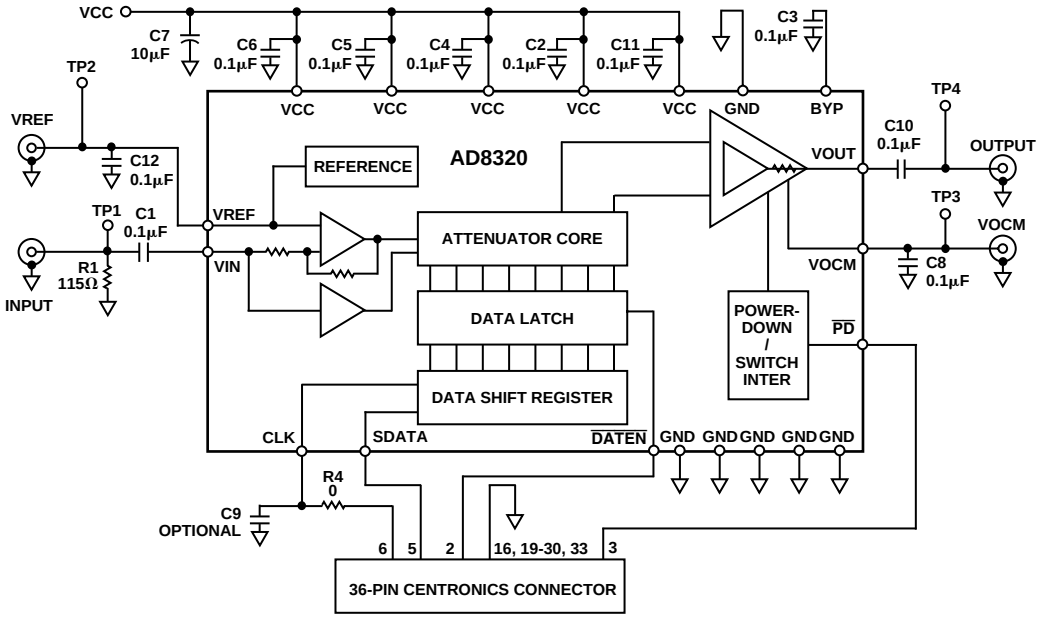

Figure 51. Evaluation Board Schematic

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The control software requires Windows 3.1 or later to operate. To install the software, insert the disk labeled "Disk # 1 of 2" in the PC and run the file called SETUP.EXE. Additional installation instructions will be given on-screen. Before beginning installation, it is important to close any other Windows applications that are running.

When you launch the installed control software from Windows, you will be asked to select the printer port you are using. Most modern PCs have only one printer port, usually called LPT1. However, some laptop computers use the PRN port.

Figure 56 shows the main screen of the control software. Using the slider, you can set any gain in the AD8320's 36 dB range. The gain is displayed on-screen in dB and V/V. The 8-bit gain setting byte is also displayed, in binary, hexadecimal and decimal.

Each time the slider is moved, the software automatically sends and latches the required 8-bit data stream to the AD8320. You can power down or reset the device simply by clicking the appropriate buttons. The software also offers one volatile storage location that can be used to store a particular gain. This functions in the same way as the memory on a pocket calculator.

Overshoot on PC Printer Ports' Data Lines

The data lines on some printer ports have excessive overshoot. Overshoot on the pin used as the serial clock (Pin 6 on the D-Sub-25 connector) can cause communication problems. This overshoot can be eliminated by applying mild filtering to the CLK line on the evaluation board. This can be done by putting a small series resistor on the CLK line, combined with a capacitor to ground. Pads are provided (C9, R4) on the component side of the evaluation board to allow easy insertion of these devices. Determining the size of these values will take some experimentation. Depending upon the overshoot from the printer port, this capacitor may need to be as large as 0.01 µF, while the resistor is typically in the 50 Ω to 100 Ω range.

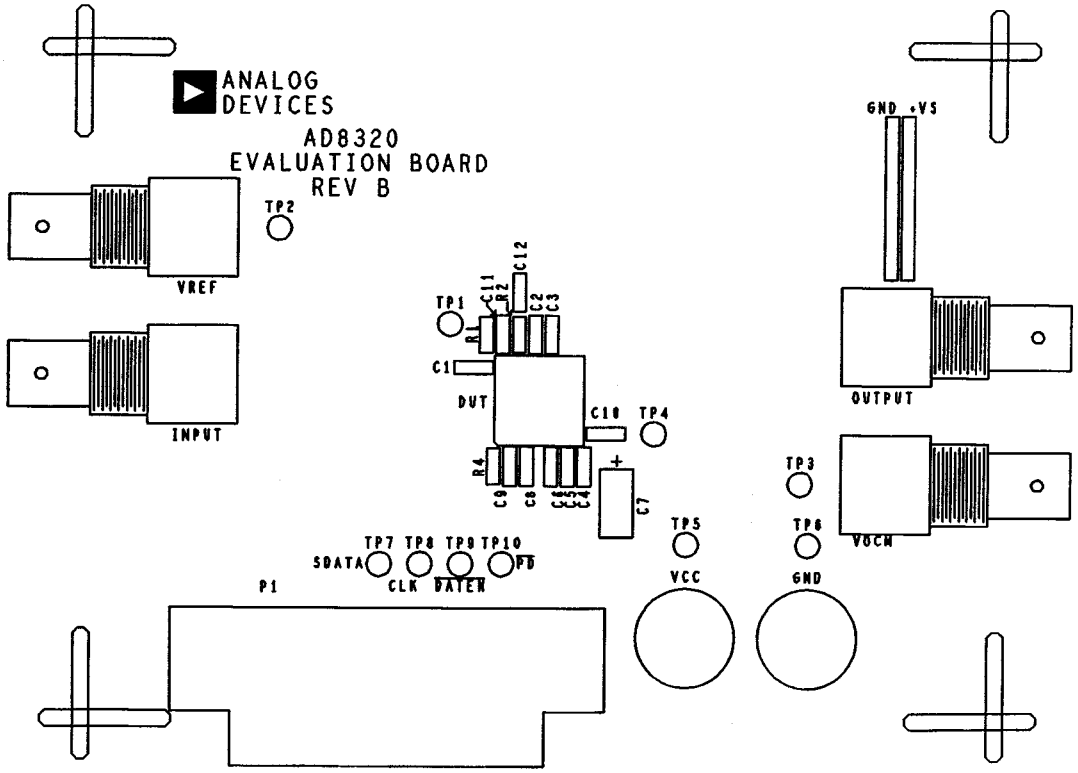

Figure 52. Evaluation Board Silkscreen (Component Side)

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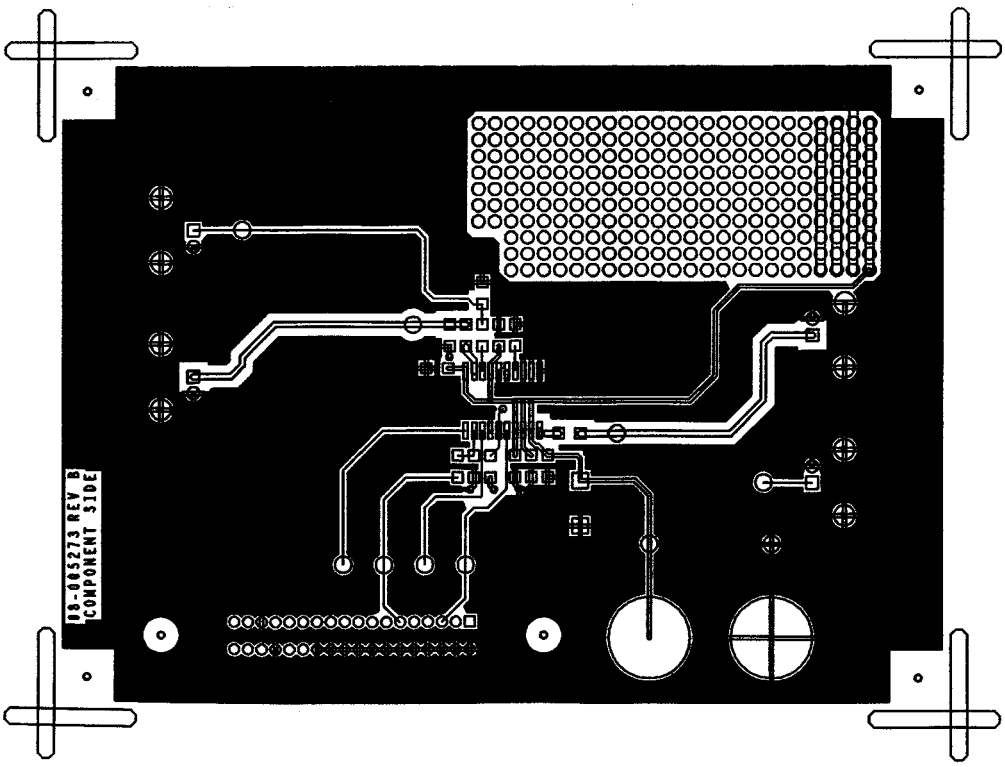

Figure 53. Evaluation Board Layout (Component Side)

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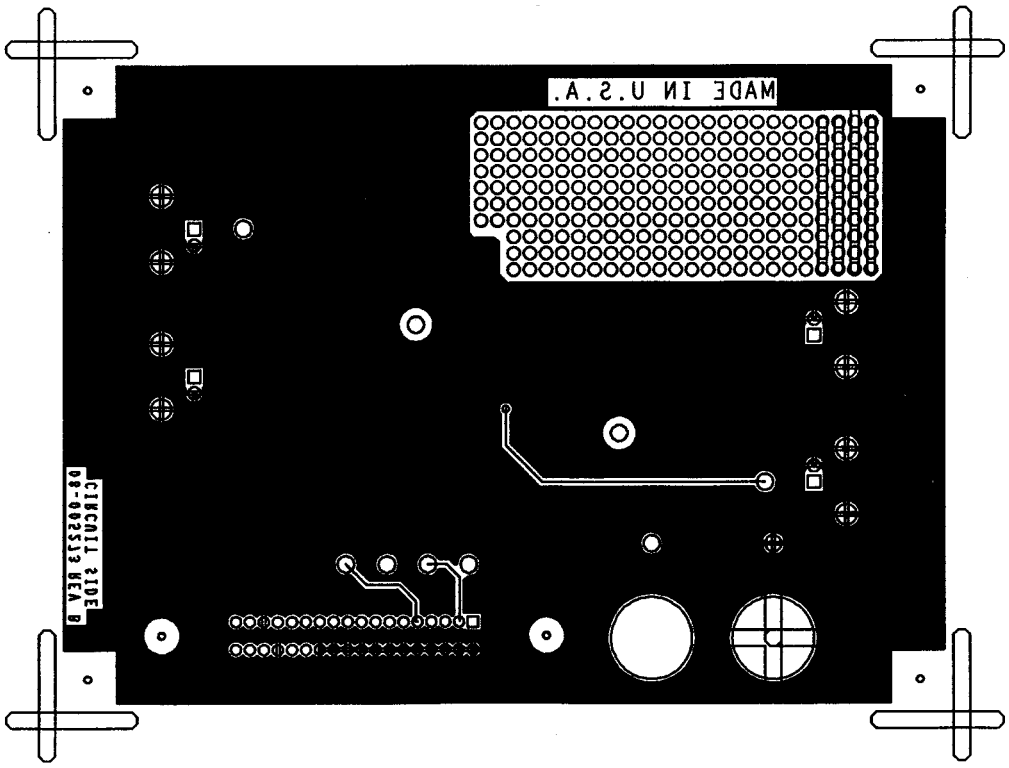
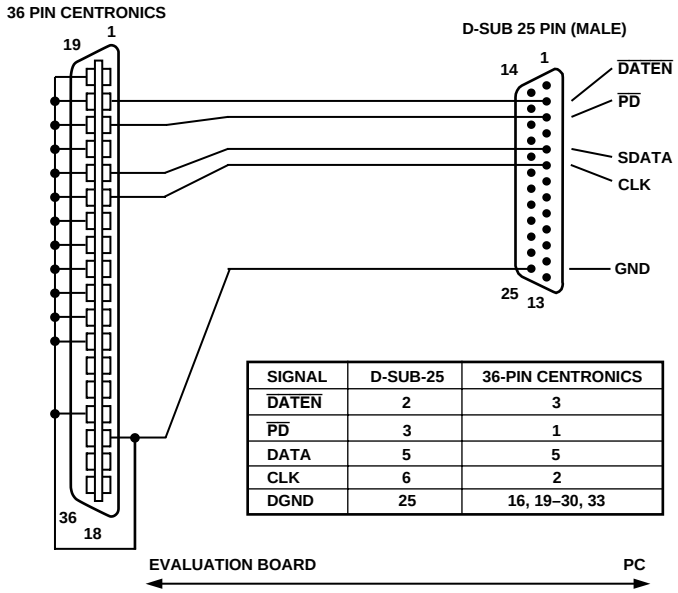


Figure 54. Evaluation Board Layout (Solder Side)



SIGNAL	D-SUB-25	36-PIN CENTRONICS
$\overline{\text{DATEN}}$	2	3
$\overline{\text{PD}}$	3	1
DATA	5	5
CLK	6	2
DGND	25	16, 19–30, 33

Figure 55. Interconnection Between AD8320EB and PC Printer Port

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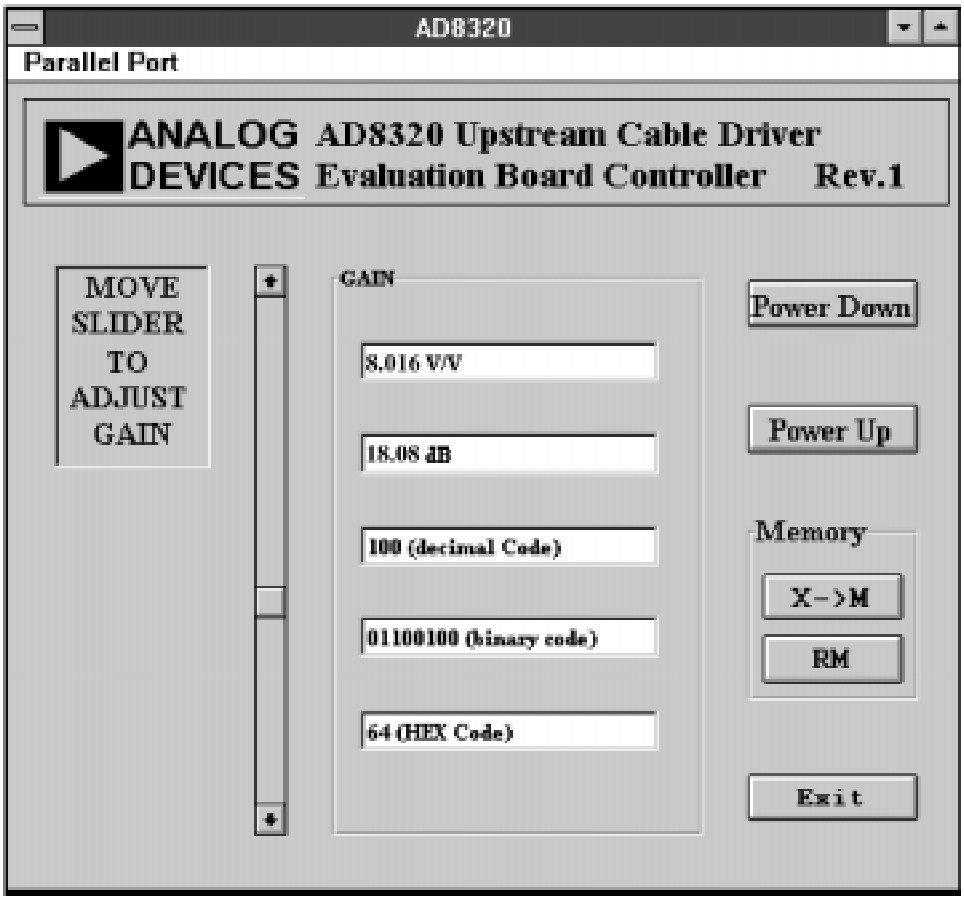

Figure 56. Screen Display of Windows-Based Control Software

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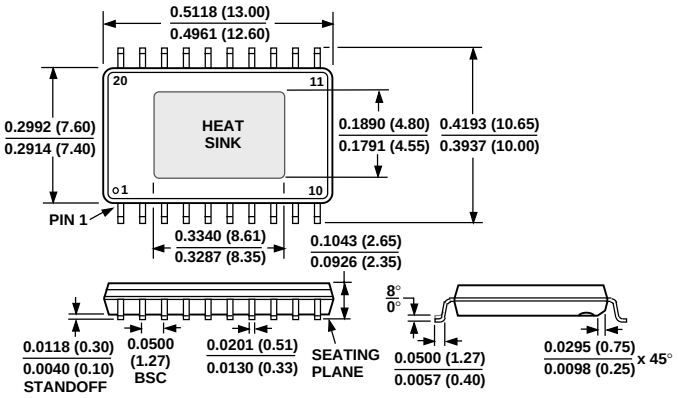
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thermally Enhanced Power Small Outline Package (RP-20)



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