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**1/04—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V, $I_{OUT}$ = virtual GND, GND = 0 V, $V_{REF}$ = −10 V to 10 V, $T_A$ = full operating temperature range, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| STATIC PERFORMANCE[1] | | | | | | |
| Resolution | N | AD5546, 1 LSB = $V_{REF}/2^{16}$ = 153 µV at $V_{REF}$ = 10 V | | 16 | | Bits |
| | | AD5556, 1 LSB = $V_{REF}/2^{14}$ = 610 µV at $V_{REF}$ = 10 V | | 14 | | Bits |
| Relative Accuracy | INL | Grade: AD5556C | | | ±1 | LSB |
| | | Grade: AD5546B | | | ±2 | LSB |
| | | Grade: AD5546C | | | ±1 | LSB |
| Differential Nonlinearity | DNL | Monotonic | | | ±1 | LSB |
| Output Leakage Current | $I_{OUT}$ | Data = zero scale, $T_A$ = 25°C | | | 10 | nA |
| | | Data = zero scale, $T_A$ = $T_A$ maximum | | | 20 | nA |
| Full-Scale Gain Error | $G_{FSE}$ | Data = full scale | | ±1 | ±4 | mV |
| Bipolar Mode Gain Error | $G_E$ | Data = full scale | | ±1 | ±4 | mV |
| Bipolar Mode Zero-Scale Error | $G_{ZSE}$ | Data = full scale | | ±1 | ±2.5 | mV |
| Full-Scale Tempco[2] | $TCV_{FS}$ | | | 1 | | ppm/°C |
| REFERENCE INPUT | | | | | | |
| $V_{REF}$ Range | $V_{REF}$ | | −18 | | +18 | V |
| REF Input Resistance | REF | | 4 | 5 | 6 | kΩ |
| R1 and R2 Resistance | R1 and R2 | | 4 | 5 | 6 | kΩ |
| R1-to-R2 Mismatch | Δ(R1 to R2) | | | ±0.5 | ±1.5 | Ω |
| Feedback and Offset Resistance | $R_{FB}$, $R_{OFS}$ | | 8 | 10 | 12 | kΩ |
| Input Capacitance[2] | $C_{REF}$ | | | 5 | | pF |
| ANALOG OUTPUT | | | | | | |
| Output Current | $I_{OUT}$ | Data = full scale | | 2 | | mA |
| Output Capacitance[2] | $C_{OUT}$ | Code dependent | | 200 | | pF |
| LOGIC INPUT AND OUTPUT | | | | | | |
| Logic Input Low Voltage | $V_{IL}$ | $V_{DD}$ = 5 V | | | 0.8 | V |
| | | $V_{DD}$ = 3 V | | | 0.4 | V |
| Logic Input High Voltage | $V_{IH}$ | $V_{DD}$ = 5 V | 2.4 | | | V |
| | | $V_{DD}$ = 3 V | 2.1 | | | V |
| Input Leakage Current | $I_{IL}$ | | | | 10 | µA |
| Input Capacitance[2] | $C_{IL}$ | | | | 10 | pF |
| INTERFACE TIMING[2, 3] | | | | | | |
| Data to $\overline{WR}$ Setup Time | $t_{DS}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| Data to $\overline{WR}$ Hold Time | $t_{DH}$ | $V_{DD}$ = 5 V | 0 | | | ns |
| | | $V_{DD}$ = 3 V | 0 | | | ns |
| $\overline{WR}$ Pulse Width | $t_{\overline{WR}}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| LDAC Pulse Width | $t_{LDAC}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\overline{RS}$ Pulse Width | $t_{RS}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| $\overline{WR}$ to LDAC Delay Time | $t_{LWD}$ | $V_{DD}$ = 5 V | 0 | | | ns |
| | | $V_{DD}$ = 3 V | 0 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 2.7 | | 5.5 | V |
| Positive Supply Current | $I_{DD}$ | Logic inputs = 0 V | | | 10 | μA |
| Power Dissipation | $P_{DISS}$ | Logic inputs = 0 V | | | 0.055 | mW |
| Power Supply Sensitivity | $P_{SS}$ | $\Delta V_{DD}$ = ±5% | | | 0.003 | %/% |
| AC CHARACTERISTICS[4] | | | | | | |
| Output Voltage Settling Time | $t_S$ | To ±0.1% of full scale, data cycles from zero scale to full scale to zero scale | | 0.5 | | μs |
| Reference Multiplying BW | BW | $V_{REF}$ = 100 mV rms, data = full scale, C6 =5.6 pF[5] | | 6.8 | | MHz |
| DAC Glitch Impulse | Q | $V_{REF}$ = 0 V, midscale minus 1 to midscale | | –3 | | nV-s |
| Multiplying Feedthrough Error | $V_{OUT}/V_{REF}$ | $V_{REF}$ = 100 mV rms, f = 10 kHz | | 79 | | dB |
| Digital Feedthrough | $Q_D$ | $\overline{WR}$ = 1, LDAC toggles at 1 MHz | | 7 | | nV-s |
| Total Harmonic Distortion | THD | $V_{REF}$ = 5 V p-p, data = full-scale, f = 1 kHz | | –103 | | dB |
| Output Noise Density | $e_N$ | f = 1 kHz, BW = 1 Hz | | 12 | | nV/rt Hz |

[1] All static performance tests (except $I_{OUT}$) are performed in a closed-loop system, using an external precision OP97 I-V converter amplifier. The AD554x RFB terminal is tied to the amplifier output. The op amp +IN is grounded, and the DAC $I_{OUT}$ is tied to the op amp –IN. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and are not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-V converter amplifier except for THD where an AD8065 was used.
[5] C6 is the C6 capacitor shown in Figure 20.

## TIMING DIAGRAM

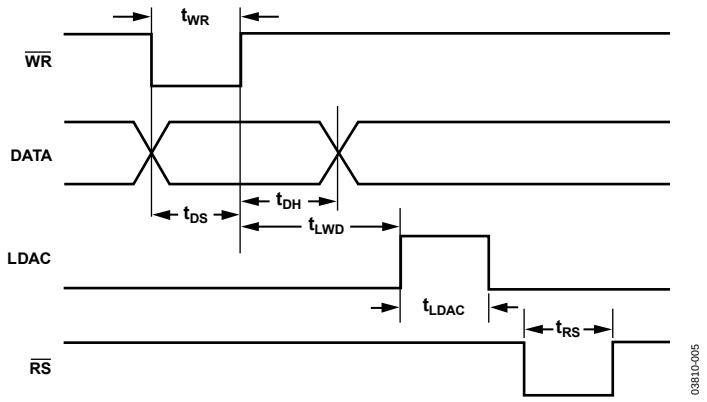



*Figure 3. AD5546/AD5556 Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V, +8 V |
| $R_{FB}$, $R_{OFS}$, R1, $R_{COM}$, and REF to GND | −18 V, 18 V |
| Logic Inputs to GND | −0.3 V, +8 V |
| V ($I_{OUT}$) to GND | −0.3 V, $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies | ±50 mA |
| Thermal Resistance ($\theta_{JA}$) | 128°C |
| Maximum Junction Temperature ($T_{J\ MAX}$) | 150°C |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature: | |
| Vapor Phase, 60 s | 215°C |
| Infrared, 15 s | 220°C |
| Package Power Dissipation | $(T_{J\ MAX} - T_A)/\theta_{JA}$ |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

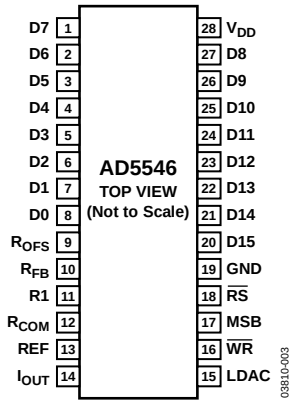



*Figure 4. AD5546 Pin Configuration*

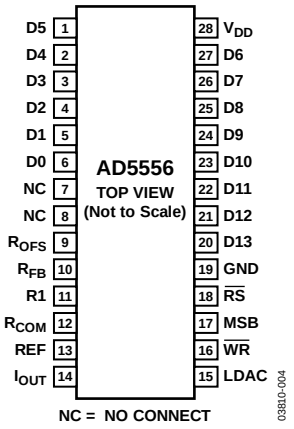



*Figure 5. AD5556 Pin Configuration*

**Table 3. AD5546 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 to 8 | D7 to D0 | Digital Input Data Bits[D7: D0]. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 9 | $R_{OFS}$ | Bipolar Offset Resistor. Accepts up to ±18 V. In two-quadrant mode, ties to $R_{FB}$. In four-quadrant mode, ties to R1 and the external reference. |
| 10 | $R_{FB}$ | Internal Matching Feedback Resistor. Connects to the output of an external op amp for I-V conversion. |
| 11 | R1 | Four-Quadrant Resistor R1. In two-quadrant mode, shorts to the REF pin. In four-quadrant mode, ties to $R_{OFS}$. |
| 12 | $R_{COM}$ | Center Tap Point of Two Four-Quadrant Resistors, R1 and R2. In four-quadrant mode, ties to the inverting node of the reference amplifier. In two-quadrant mode, shorts to the REF pin. |
| 13 | REF | DAC Reference Input in Two-Quadrant Mode and R2 Terminal in Four-Quadrant Mode. In two-quadrant mode, this pin is the reference input with constant input resistance vs. code. In four-quadrant mode, this pin is driven by the external reference amplifier. |
| 14 | $I_{OUT}$ | DAC Current Output. Connects to the inverting node of an external op amp for I-V conversion. |
| 15 | LDAC | Digital Input Load DAC Control. Signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 16 | $\overline{WR}$ | Write Control Digital Input in Active Low. Transfers shift-register data to the DAC register on the rising edge. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 17 | MSB | Power-On Reset State. MSB = 0 resets at zero scale; MSB = 1 resets at midscale. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 18 | $\overline{RS}$ | Reset in Active Low. Resets to zero scale if MSB = 0, and resets to midscale if MSB = 1. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 19 | GND | Analog and Digital Grounds. |
| 20 to 21 | D15 to D14 | Digital Input Data Bits[D15:D14]. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 22 to 27 | D13 to D8 | Digital Input Data Bits[D13:D8]. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 28 | $V_{DD}$ | Positive Power Supply Input. Specified range of operation: 2.7 V to 5.5 V. |

**Table 4. AD5556 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 to 6 | D5 to D0 | Digital Input Data Bits[D5:D0]. The signal level must be ≤ $V_{DD}$+0.3 V. |
| 7 to 8 | NC | No Connection. The user should not connect anything other than dummy pads on these terminals. |
| 9 | $R_{OFS}$ | Bipolar Offset Resistor. Accepts up to ±18 V. In two-quadrant mode, ties to RFB. In four-quadrant mode, ties to R1 and the external reference. |
| 10 | $R_{FB}$ | Internal Matching Feedback Resistor. Connects to the output of an external op amp for I-V conversion. |
| 11 | R1 | Four-Quadrant Resistor R1. In two-quadrant mode, shorts to the REF pin. In four-quadrant mode, ties to $R_{OFS}$. |
| 12 | $R_{COM}$ | Center Tap Point of Two Four-Quadrant Resistors, R1 and R2. In four-quadrant mode, ties to the inverting node of the reference amplifier. In two-quadrant mode, shorts to the REF pin. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 13 | REF | DAC Reference Input in Two-Quadrant Mode and R2 Terminal in Four-Quadrant Mode. In two-quadrant mode, this pin is the reference input with constant input resistance vs. code. In four-quadrant mode, this pin is driven by the external reference amplifier. |
| 14 | $I_{OUT}$ | DAC Current Output. Connects to the inverting node of an external op amp for I-V conversion. |
| 15 | LDAC | Digital Input Load DAC Control. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 16 | $\overline{WR}$ | Write Control Digital Input in Active Low. Transfers shift-register data to the DAC register on the rising edge. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 17 | MSB | Power On Reset State. MSB = 0 resets at zero scale; MSB = 1 resets at midscale. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 18 | $\overline{RS}$ | Reset in Active Low. Resets to zero scale if MSB = 0 and resets to midscale if MSB = 1. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 19 | GND | Analog and Digital Grounds. |
| 20 to 27 | D13 to D6 | Digital Input Data Bits[D13:D6]. The signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 28 | $V_{DD}$ | Positive Power Supply Input. Specified range of operation: 2.7 V to 5.5 V. |

# TYPICAL PERFORMANCE CHARACTERISTICS

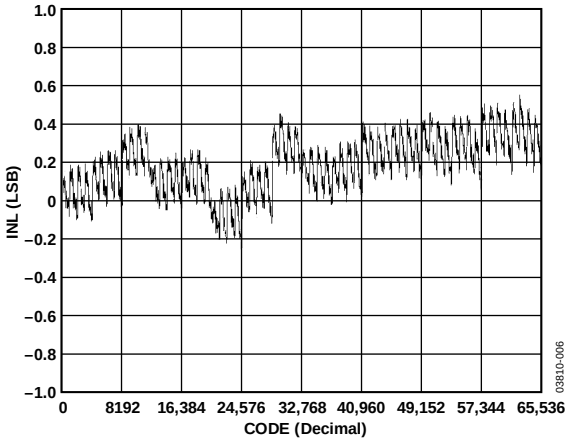



Figure 6. AD5546 Integral Nonlinearity Error

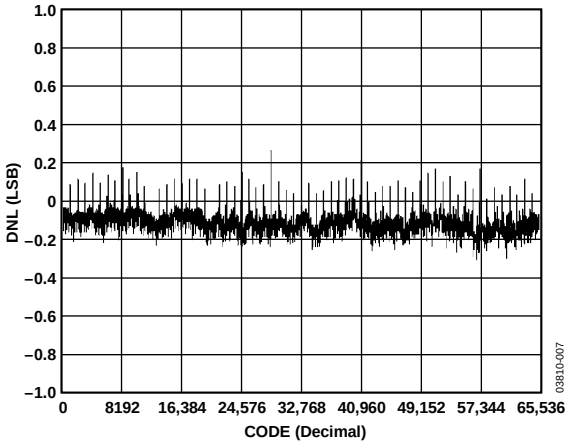



Figure 7. AD5546 Differential Nonlinearity Error

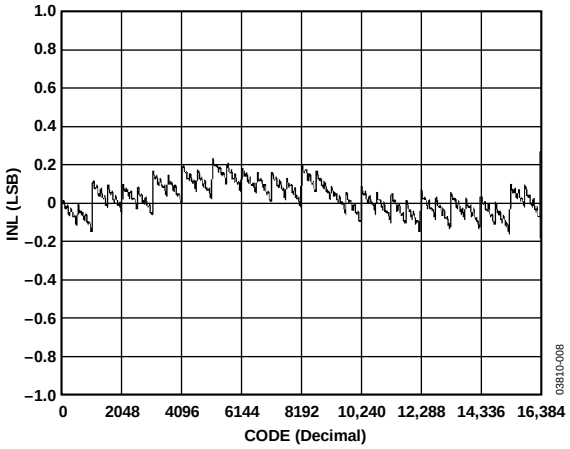



Figure 8. AD5556 Integral Nonlinearity Error

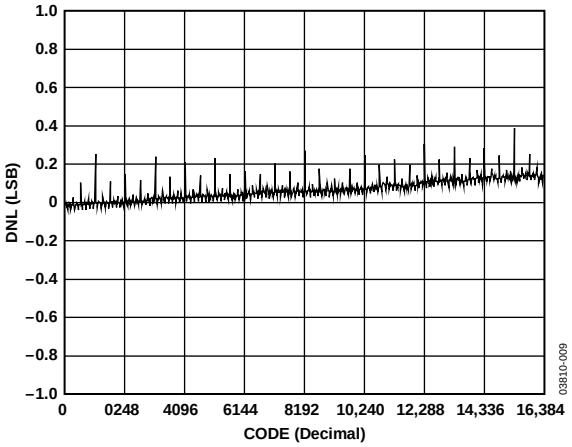



Figure 9. AD5556 Differential Nonlinearity Error

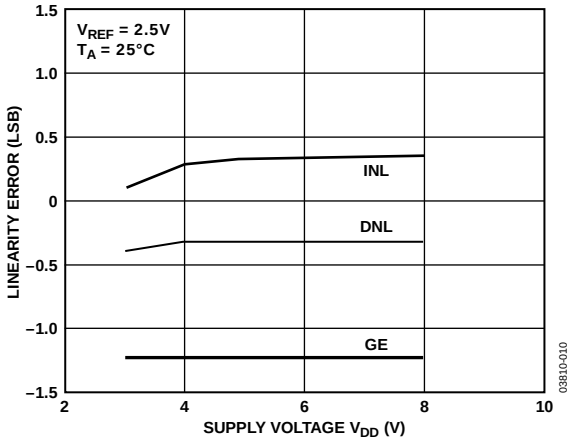



Figure 10. Linearity Error vs. $V_{DD}$

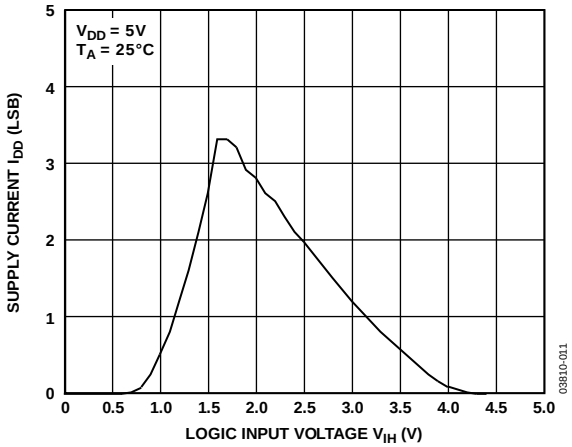



Figure 11. Supply Current vs. Logic Input Voltage

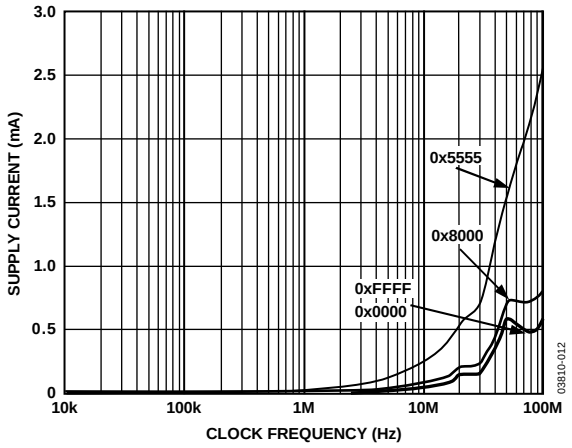



Figure 12. AD5546 Supply Current vs. Clock Frequency

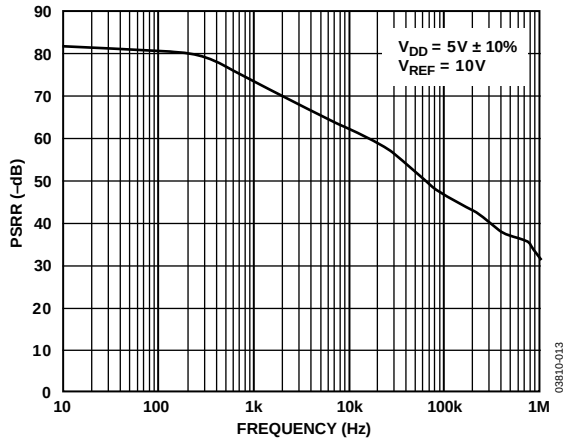



Figure 13. Power Supply Rejection Ratio vs. Frequency

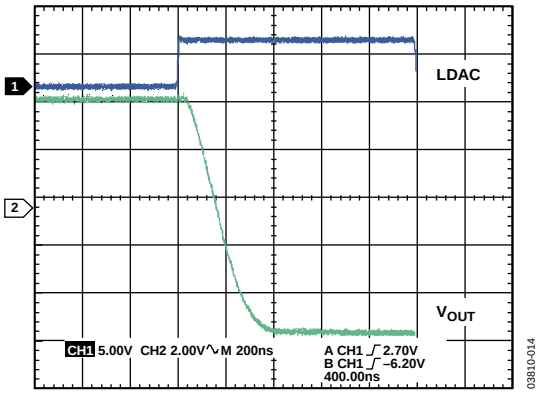



Figure 14. Settling Time from Full Scale to Zero Scale

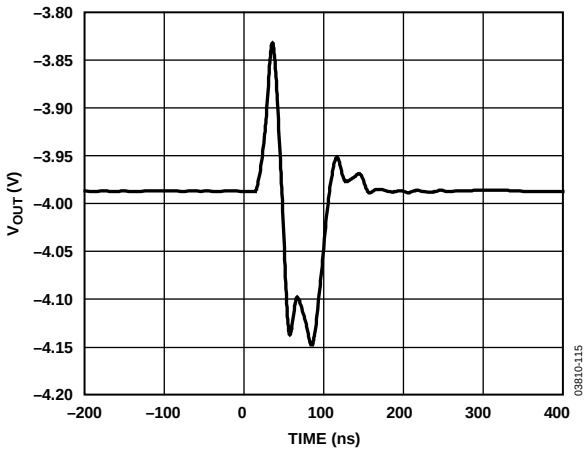



Figure 15. AD5546 Midscale Transition

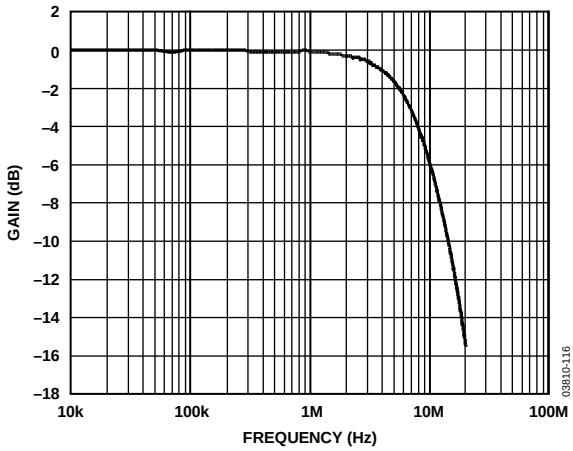



Figure 16. AD5546 Unipolar Reference Multiplying Bandwidth

# CIRCUIT OPERATION

## DIGITAL-TO-ANALOG (DAC) CONVERTER SECTION

The AD5546/AD5556 are 16-/14-bit multiplying, current output, and parallel input DACs. The devices operate from a single 2.7 V to 5.5 V supply and provide both unipolar 0 V to $-V_{REF}$, or 0 V to $+V_{REF}$, and bipolar $\pm V_{REF}$ output ranges from a –18 V to +18 V reference. In addition to the precision conversion $R_{FB}$ commonly found in current output DACs, there are three additional precision resistors for four-quadrant bipolar applications.

The AD5546/AD5556 consist of two groups of precision R-2R ladders, which make up the 12/10 LSBs, respectively. Furthermore, the four MSBs are decoded into 15 segments of resistor value 2R. Figure 17 shows the architecture of the 16-bit AD5546. Each of the 16 segments in the R-2R ladder carries an equally weighted current of one-sixteenth of full scale. The feedback resistor, $R_{FB}$, and four-quadrant resistor, $R_{OFS}$, have values of 10 kΩ. Each four-quadrant resistor, R1 and R2, equals 5 kΩ. In four-quadrant operation, R1, R2, and an external op amp work together to invert the reference voltage and apply it to the REF input. With $R_{OFS}$ and $R_{FB}$ connected as shown in Figure 2, the output can swing from $-V_{REF}$ to $+V_{REF}$.

The reference voltage inputs exhibit a constant input resistance of 5 kΩ ±20%. The DAC output, $I_{OUT}$, impedance is code dependent. External amplifier choice should take into account the variation of the AD5546/AD5556 output impedance. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. To maintain good analog performance, it is recommended to bypass the power supply with a 0.01 µF to 0.1 µF ceramic or chip capacitor in parallel with a 1 µF tantalum capacitor. Also, to minimize gain error, PCB metal traces between $V_{REF}$ and $R_{FB}$ should match.

Every code change of the DAC corresponds to a step function; gain peaking at each output step may occur if the op amp has limited GBP and excessive parasitic capacitance present at the op amp inverting node. A compensation capacitor, therefore, may be needed between the I-V op amp inverting and output nodes to smooth the step transition. Such a compensation capacitor should be found empirically, but a 20 pF capacitor is generally adequate for the compensation.

The $V_{DD}$ power is used primarily by the internal logic and to drive the DAC switches. Note that the output precision degrades if the operating voltage falls below the specified voltage. The user should also avoid using switching regulators because device power supply rejection degrades at higher frequencies.

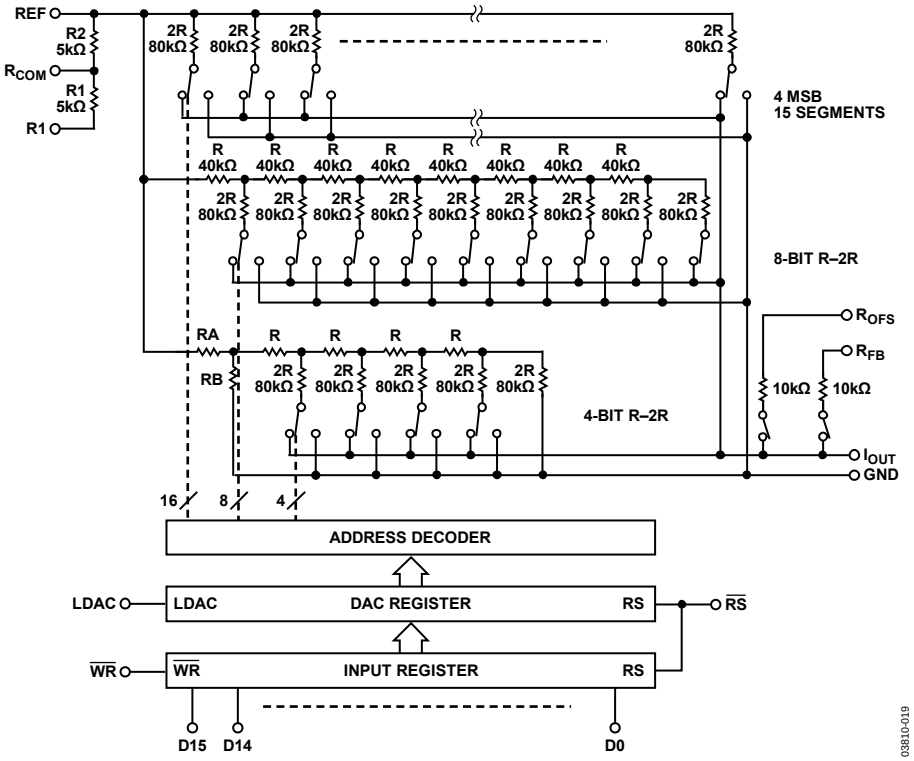



*Figure 17. 16-Bit AD5546 Equivalent R-2R DAC Circuit with Digital Section*

## DIGITAL SECTION

The AD5546/AD5556 have 16-/14-bit parallel inputs. The devices are double buffered with 16-/14-bit registers. The double-buffered feature allows the update of several AD5546/AD5556 simultaneously. For the AD5546, the input register is loaded directly from a 16-bit controller bus when the $\overline{WR}$ pin is brought low. The DAC register is updated with data from the input register when LDAC is brought high. Updating the DAC register updates the DAC output with the new data (see Figure 17). To make both registers transparent, tie $\overline{WR}$ low and LDAC high. The asynchronous $\overline{RS}$ pin resets the part to zero scale if the MSB pin = 0 and to midscale if the MSB pin = 1.

**Table 5. AD5546 Parallel Input Data Format**

| | MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit Position | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Data Word | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 6. AD5556 Parallel Input Data Format**

| | MSB | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit Position | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Data Word | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 7. Control Inputs**

| $\overline{RS}$ | $\overline{WR}$ | LDAC | Register Operation |
|---|---|---|---|
| 0 | X[1] | X[1] | Reset output to 0, with MSB pin = 0 and to midscale with MSB pin = 1. |
| 1 | 0 | 0 | Load input register with data bits. |
| 1 | 1 | 1 | Load DAC register with the contents of the input register. |
| 1 | 0 | 1 | Input and DAC registers are transparent. |
| 1 | ⎍ | ⎍ | When LDAC and $\overline{WR}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse. |
| 1 | 1 | 0 | No register operation. |

[1] X = don't care.

## ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND) and $V_{DD}$, as shown in Figure 18. As a result, the voltage level of the logic input should not be greater than the supply voltage.

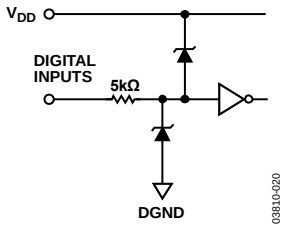



*Figure 18. Equivalent ESD Protection Circuits*

## AMPLIFIER SELECTION

In addition to offset voltage, the bias current is important in op amp selection for precision current output DACs. An input bias current of 30 nA in the op amp contributes to 1 LSB in the AD5546's full-scale error. The OP1177 and AD8628 op amps are good candidates for the I-V conversion.

## REFERENCE SELECTION

The initial accuracy and the rated output of the voltage reference determine the full span adjustment. The initial accuracy is usually a secondary concern in precision because it can be trimmed. Figure 23 shows an example of a trimming circuit. The zero scale error can also be minimized by standard op amp nulling techniques.

The voltage reference temperature coefficient (TC) and long-term drift are primary considerations. For example, a 5 V reference with a TC of 5 ppm/°C means that the output changes by 25 μV per degree Celsius. As a result, the reference that operates at 55°C contributes an additional 750 μV full-scale error.

Similarly, the same 5 V reference with a ±50 ppm long-term drift means that the output may change by ±250 μV over time. Therefore, it is practical to calibrate a system periodically to maintain its optimum precision.

# APPLICATIONS INFORMATION

## UNIPOLAR MODE

### *Two-Quadrant Multiplying Mode, $V_{OUT}$ = 0 V to $-V_{REF}$*

The AD5546/AD5556 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op amp to convert the unipolar mode of output voltage to

AD5546

$$V_{OUT} = -V_{REF} \times D/65{,}536 \quad (1)$$

AD5556

$$V_{OUT} = -V_{REF} \times D/16{,}384 \quad (2)$$

where $D$ is the decimal equivalent of the input code.

The output voltage polarity is opposite to the $V_{REF}$ polarity in this case (see Figure 19). Table 8 shows the negative output vs. code for the AD5546.

**Table 8. AD5546 Unipolar Mode Negative Output vs. Code**

| D in Binary | $V_{OUT}$ (V) |
|---|---|
| 1111 1111 1111 1111 | $-V_{REF}(65{,}535/65{,}536)$ |
| 1000 0000 0000 0000 | $-V_{REF}/2$ |
| 0000 0000 0000 0001 | $-V_{REF}(1/65{,}536)$ |
| 0000 0000 0000 0000 | 0 |

### *Two-Quadrant Multiplying Mode, $V_{OUT}$ = 0 V to $+V_{REF}$*

The AD5546/AD5556 are designed to operate with either positive or negative reference voltages. As a result, positive output can be achieved with an additional op amp, (see Figure 20), and the output becomes

AD5546

$$V_{OUT} = +V_{REF} \times D/65{,}536 \quad (3)$$

AD5556

$$V_{OUT} = +V_{REF} \times D/16{,}384 \quad (4)$$

Table 9 shows the positive output vs. code for the AD5546.

**Table 9. AD5546 Unipolar Mode Positive Output vs. Code**

| D in Binary | $V_{OUT}$ (V) |
|---|---|
| 1111 1111 1111 1111 | $+V_{REF}(65{,}535/65{,}536)$ |
| 1000 0000 0000 0000 | $+V_{REF}/2$ |
| 0000 0000 0000 0001 | $+V_{REF}(1/65{,}536)$ |
| 0000 0000 0000 0000 | 0 |

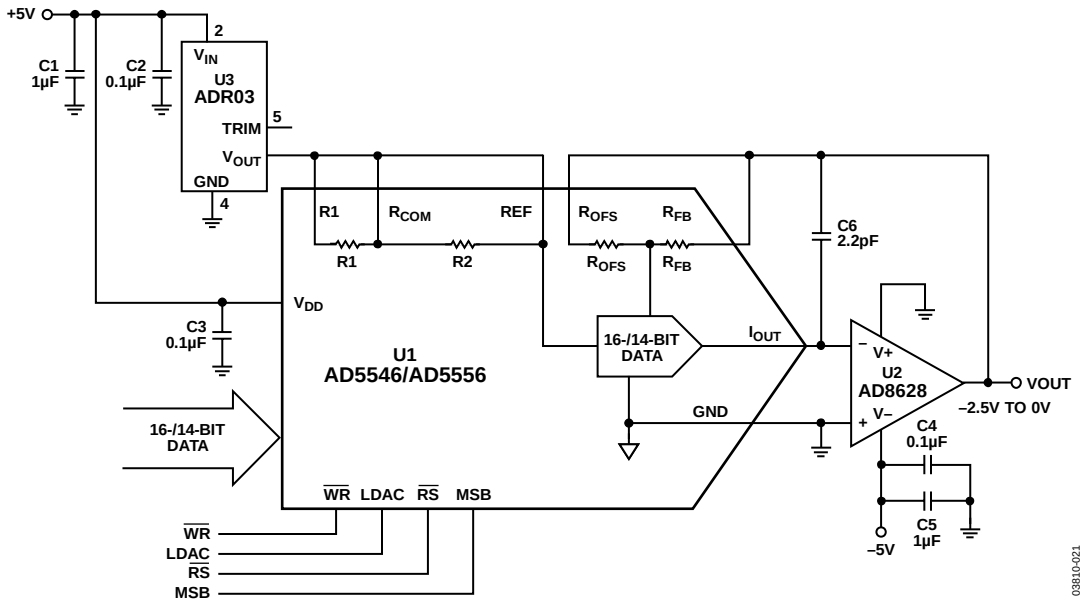



*Figure 19. Unipolar Two-Quadrant Multiplying Mode, $V_{OUT}$ = 0 to $-V_{REF}$*

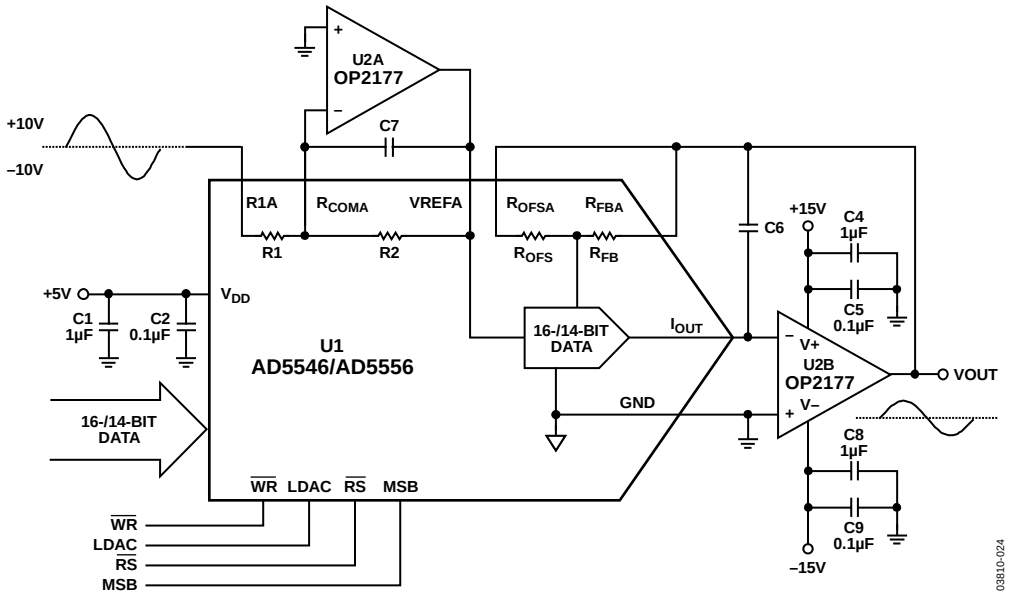



*Figure 20. Unipolar Two-Quadrant Multiplying Mode, $V_{OUT}$ = 0 to +$V_{REF}$*

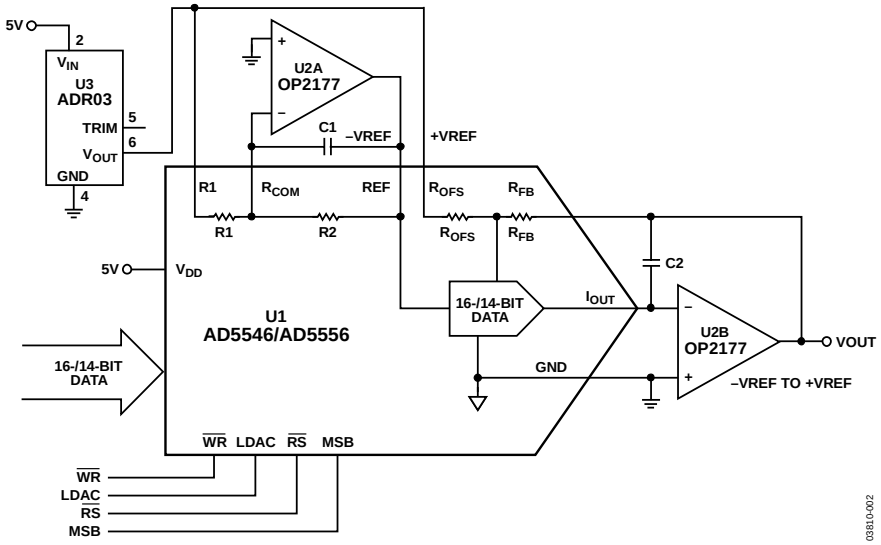



*Figure 21. Four-Quadrant Multiplying Mode, $V_{OUT}$ = –$V_{REF}$ to +$V_{REF}$*

## BIPOLAR MODE

### *Four-Quadrant Multiplying Mode, $V_{OUT}$ = –$V_{REF}$ to +$V_{REF}$*

The AD5546/AD5556 contain on-chip all the four-quadrant resistors necessary for the precision bipolar multiplying operation. Such a feature minimizes the number of exponent components to only a voltage reference, dual op amp, and compensation capacitor (see Figure 21). For example, with a 10 V reference, the circuit yields a precision, bipolar –10 V to +10 V output.

AD5546

$$V_{OUT} = (D/32768 - 1) \times V_{REF} \quad (5)$$

AD5556

$$V_{OUT} = (D/16384 - 1) \times V_{REF} \quad (6)$$

Table 10 shows some of the results for the 16-bit AD5546.

**Table 10. AD5546 Output vs. Code**

| D in Binary | $V_{OUT}$ |
|---|---|
| 1111 1111 1111 1111 | $+V_{REF}(32,767/32,768)$ |
| 1000 0000 0000 0001 | $+V_{REF}(1/32,768)$ |
| 1000 0000 0000 0000 | 0 |
| 0111 1111 1111 1111 | $-V_{REF}(1/32,768)$ |
| 0000 0000 0000 0000 | $-V_{REF}$ |

## AC REFERENCE SIGNAL ATTENUATOR

Besides handling digital waveforms decoded from parallel input data, the AD5546/AD5556 handle equally well low frequency ac reference signals for signal attenuation, channel equalization, and waveform generation applications. The maximum signal range can be up to ±18 V (see Figure 22).

## SYSTEM CALIBRATION

The initial accuracy of the system can be adjusted by trimming the voltage reference ADR0x with a digital potentiometer (see Figure 23). The AD5170 provides an OTP (one time programmable), 8-bit adjustment that is ideal and reliable for such calibration. The Analog Devices, Inc., OTP digital potentiometer comes with programmable software that simplifies the factory calibration process.

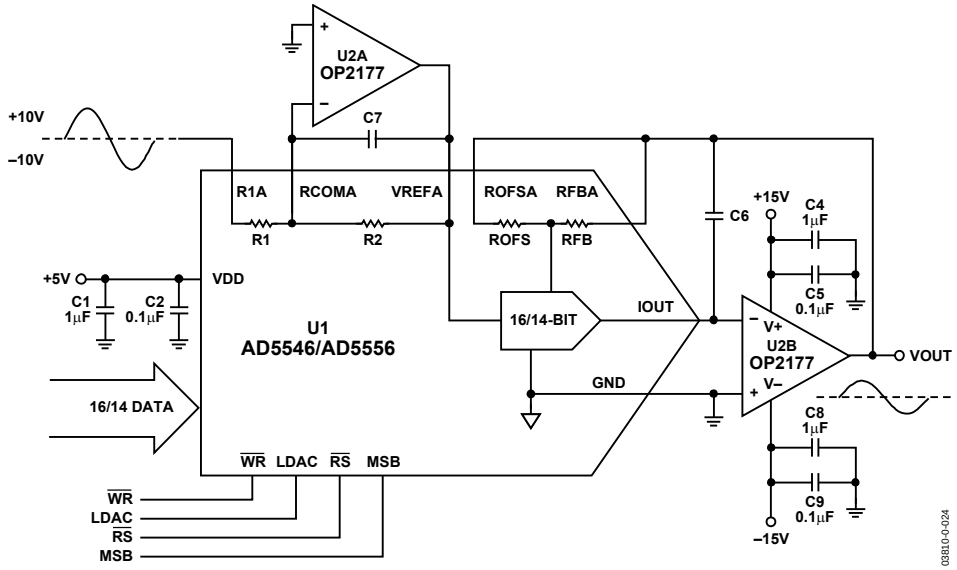



*Figure 22. Signal Attenuator with AC Reference*

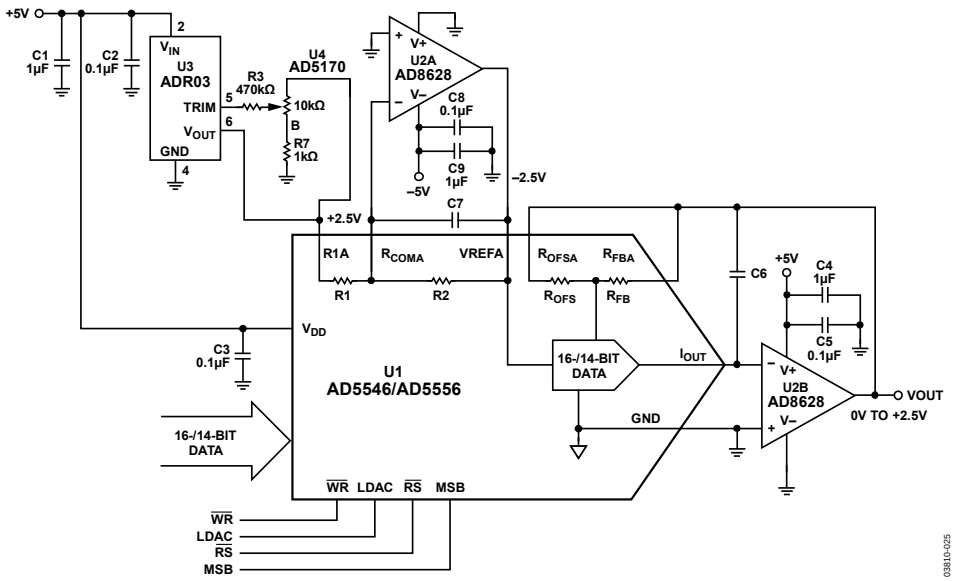



*Figure 23. Full Span Calibration*

## REFERENCE SELECTION

When selecting a reference for use with the AD55xx series of current output DACs, pay attention to the output voltage temperature coefficient specification of the reference. Choosing a precision reference with a low output temperature coefficient minimizes error sources. Table 11 lists some of the references available from Analog Devices that are suitable for use with this range of current output DACs.

## AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output because of the bias current flowing in the feedback resistor, $R_{FB}$.

Common-mode rejection of the op amp is important in voltage-switching circuits because it produces a code-dependent error at the voltage output of the circuit.

Provided that the DAC switches are driven from true wideband low impedance sources, they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the $V_{REF}$ node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Analog Devices offers a wide range of amplifiers for both precision dc and ac applications, as listed in Table 12 and Table 13.

**Table 11. Suitable Analog Devices Precision References**

| Part No. | Output Voltage (V) | Initial Tolerance (%) | Maximum Temperature Drift (ppm/°C) | $I_{SS}$ (mA) | Output Noise (µV p-p) | Package(s) |
|---|---|---|---|---|---|---|
| ADR01 | 10 | 0.05 | 3 | 1 | 20 | SOIC-8 |
| ADR01 | 10 | 0.05 | 9 | 1 | 20 | TSOT-5, SC70-5 |
| ADR02 | 5.0 | 0.06 | 3 | 1 | 10 | SOIC-8 |
| ADR02 | 5.0 | 0.06 | 9 | 1 | 10 | TSOT-5, SC70-5 |
| ADR03 | 2.5 | 0.1 | 3 | 1 | 6 | SOIC-8 |
| ADR03 | 2.5 | 0.1 | 9 | 1 | 6 | TSOT-5, SC70-5 |
| ADR06 | 3.0 | 0.1 | 3 | 1 | 10 | SOIC-8 |
| ADR06 | 3.0 | 0.1 | 9 | 1 | 10 | TSOT-5, SC70-5 |
| ADR420 | 2.048 | 0.05 | 3 | 0.5 | 1.75 | SOIC-8, MSOP-8 |
| ADR421 | 2.50 | 0.04 | 3 | 0.5 | 1.75 | SOIC-8, MSOP-8 |
| ADR423 | 3.00 | 0.04 | 3 | 0.5 | 2 | SOIC-8, MSOP-8 |
| ADR425 | 5.00 | 0.04 | 3 | 0.5 | 3.4 | SOIC-8, MSOP-8 |
| ADR431 | 2.500 | 0.04 | 3 | 0.8 | 3.5 | SOIC-8, MSOP-8 |
| ADR435 | 5.000 | 0.04 | 3 | 0.8 | 8 | SOIC-8, MSOP-8 |
| ADR391 | 2.5 | 0.16 | 9 | 0.12 | 5 | TSOT-5 |
| ADR395 | 5.0 | 0.10 | 9 | 0.12 | 8 | TSOT-5 |

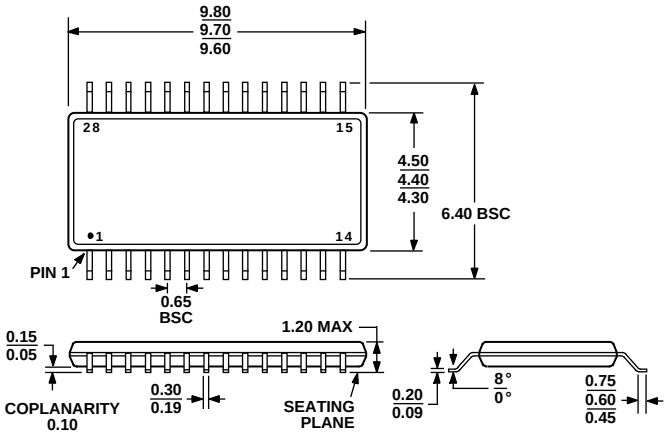
Table 12. Suitable Analog Devices Precision Op Amps

| Part No. | Supply Voltage (V) | $V_{OS}$ Maximum (µV) | $I_B$ Maximum (nA) | 0.1 Hz to 10 Hz Noise (µV p-p) | Supply Current (µA) | Package(s) |
|---|---|---|---|---|---|---|
| OP97 | ±2 to ±20 | 25 | 0.1 | 0.5 | 600 | SOIC-8 , PDIP-8 |
| OP1177 | ±2.5 to ±15 | 60 | 2 | 0.4 | 500 | MSOP-8, SOIC-8 |
| AD8675 | ±5 to ±18 | 75 | 2 | 0.1 | 2300 | MSOP-8, SOIC-8 |
| AD8671 | ±5 to ±15 | 75 | 12 | 0.077 | 3000 | MSOP-8, SOIC-8 |
| ADA4004-1 | ±5 to ±15 | 125 | 90 | 0.1 | 2000 | SOIC-8, SOT-23-5 |
| AD8603 | 1.8 to 5 | 50 | 0.001 | 2.3 | 40 | TSOT-5 |
| AD8607 | 1.8 to 5 | 50 | 0.001 | 2.3 | 40 | MSOP-8, SOIC-8 |
| AD8605 | 2.7 to 5 | 65 | 0.001 | 2.3 | 1000 | WLCSP-5, SOT-23-5 |
| AD8615 | 2.7 to 5 | 65 | 0.001 | 2.4 | 2000 | TSOT-23-5 |
| AD8616 | 2.7 to 5 | 65 | 0.001 | 2.4 | 2000 | MSOP-8, SOIC-8 |

Table 13. Suitable Analog Devices High Speed Op Amps

| Part No. | Supply Voltage (V) | BW @ ACL (MHz) | Slew Rate (V/µs) | $V_{OS}$ (Max) (µV) | $I_B$ (Max) (nA) | Package(s) |
|---|---|---|---|---|---|---|
| AD8065 | 5 to 24 | 145 | 180 | 1500 | 0.006 | SOIC-8, SOT-23-5 |
| AD8066 | 5 to 24 | 145 | 180 | 1500 | 0.006 | SOIC-8, MSOP-8 |
| AD8021 | 5 to 24 | 490 | 120 | 1000 | 10,500 | SOIC-8, MSOP-8 |
| AD8038 | 3 to 12 | 350 | 425 | 3000 | 750 | SOIC-8, SC70-5 |
| ADA4899-1 | 5 to 12 | 600 | 310 | 35 | 100 | LFCSP-8, SOIC-8 |
| AD8057 | 3 to 12 | 325 | 1000 | 5000 | 500 | SOT-23-5, SOIC-8 |
| AD8058 | 3 to 12 | 325 | 850 | 5000 | 500 | SOIC-8, MSOP-8 |
| AD8061 | 2.7 to 8 | 320 | 650 | 6000 | 350 | SOT-23-5, SOIC-8 |
| AD8062 | 2.7 to 8 | 320 | 650 | 6000 | 350 | SOIC-8, MSOP-8 |
| AD9631 | ±3 to ±6 | 320 | 1300 | 10,000 | 7000 | SOIC-8, PDIP-8 |

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-153-AE

*Figure 24. 28-Lead Thin Shrink Small Outline Package [TSSOP]*
*RU-28*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | RES (Bit) | DNL (LSB) | INL (LSB) | Temperature Range (°C) | Package Description | Package Option | Ordering Quantity |
|---|---|---|---|---|---|---|---|
| AD5546BRU | 16 | ±1 | ±2 | −40 to +125 | 28-Lead TSSOP | RU-28 | 50 |
| AD5546BRU-REEL7 | 16 | ±1 | ±2 | −40 to +125 | 28-Lead TSSOP | RU-28 | 1,000 |
| AD5546BRUZ | 16 | ±1 | ±2 | −40 to +125 | 28-Lead TSSOP | RU-28 | 50 |
| AD5546BRUZ-REEL7 | 16 | ±1 | ±2 | −40 to +125 | 28-Lead TSSOP | RU-28 | 1,000 |
| AD5546CRUZ | 16 | ±1 | ±1 | −40 to +125 | 28-Lead TSSOP | RU-28 | 50 |
| AD5546CRUZ-REEL7 | 16 | ±1 | ±1 | −40 to +125 | 28-Lead TSSOP | RU-28 | 1,000 |
| AD5556CRU | 14 | ±1 | ±1 | −40 to +125 | 28-Lead TSSOP | RU-28 | 50 |
| AD5556CRU-REEL7 | 14 | ±1 | ±1 | −40 to +125 | 28-Lead TSSOP | RU-28 | 1,000 |
| AD5556CRUZ | 14 | ±1 | ±1 | −40 to +125 | 28-Lead TSSOP | RU-28 | 50 |
| EVAL-AD5546SDZ | | | | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.

## NOTES

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