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## REVISION HISTORY

### 1/16—Rev. D to Rev. E

Deleted Positive Output Voltage Section and Figure 53; Renumbered Sequentially.....	20
Changes to Adding Gain Section .....	21
Changed ADSP-21xx-to-AD5424/AD5433/AD5445 Interface Section to ADSP-2191M-to-AD5424/AD5433/AD5445 Interface Section and ADSP-BF5xx-to-AD5424/AD5433/ AD5445 Interface Section to Blackfin Processor-to-AD5424/ AD5433/AD5445 Interface Section .....	23
Changes to Figure 55 and Figure 57.....	23
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### 4/13—Rev. C to Rev. D

Changes to Figure 4 and Table 4.....	7
Changes to Figure 6 and Table 5.....	8
Changes to Figure 8 and Table 6.....	9
Updated Outline Dimensions .....	25
Changes to Ordering Guide .....	26

### 12/12—Rev. B to Rev. C

Changes to General Description Section .....	1
Added Note 2 to Table 1 .....	4
Added EPAD Note to Table 4 and EPAD Note to Figure 4.....	7
Added EPAD Note to Table 5 and EPAD Note to Figure 6.....	8

Added EPAD Note to Table 6 and EPAD Note to Figure 8.....	9
Deleted the Evaluation Board for AD5424/AD5433/AD5445 Section and Power Supplies for Evaluation Board Section.....	23
Deleted Figure 59; Renumbered Sequentially .....	24
Deleted Figure 60 and Figure 61 .....	25
Changes to Ordering Guide .....	26
Deleted Figure 62 and Table 12; Renumbered Sequentially .....	26

### 8/09—Rev. A to Rev. B

Updated Outline Dimensions .....	28
Changes to Ordering Guide .....	29

### 3/05—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Specifications.....	4
Changes to Figure 49.....	17
Changes to Figure 50.....	18
Changes to Figure 51, Figure 52, and Figure 54.....	19
Added Microprocessor Interfacing Section .....	22
Added Figure 59 .....	24
Added Figure 60 .....	25

### 10/03—Initial Version: Revision 0

## SPECIFICATIONS

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 10\text{ V}$ ,  $I_{OUT2} = 0\text{ V}$ . Temperature range for Y version:  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. DC performance measured with [OP177](#) and ac performance measured with [AD8038](#), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
<a href="#">AD5424</a>					
Resolution			8	Bits	Guaranteed monotonic
Relative Accuracy			$\pm 0.25$	LSB	
Differential Nonlinearity			$\pm 0.5$	LSB	
<a href="#">AD5433</a>					
Resolution			10	Bits	Guaranteed monotonic
Relative Accuracy			$\pm 0.5$	LSB	
Differential Nonlinearity			$\pm 1$	LSB	
<a href="#">AD5445</a>					
Resolution			12	Bits	Guaranteed monotonic
Relative Accuracy			$\pm 1$	LSB	
Differential Nonlinearity			$-1/+2$	LSB	
Gain Error			$\pm 10$	mV	
Gain Error Temperature Coefficient <sup>1</sup>		$\pm 5$		ppm FSR/ $^{\circ}\text{C}$	
Output Leakage Current <sup>1</sup>			$\pm 10$	nA	Data = 0x0000, $T_A = 25^{\circ}\text{C}$ , $I_{OUT1}$
			$\pm 20$	nA	Data = 0x0000, $T = -40^{\circ}\text{C to }+125^{\circ}\text{C}$ , $I_{OUT1}$
REFERENCE INPUT <sup>1</sup>					
Reference Input Range		$\pm 10$		V	
$V_{REF}$ Input Resistance	8	10	12	k $\Omega$	Input resistance TC = $-50\text{ ppm}/^{\circ}\text{C}$
$R_{FB}$ Resistance	8	10	12	k $\Omega$	Input resistance TC = $-50\text{ ppm}/^{\circ}\text{C}$
Input Capacitance					
Code Zero Scale		3	6	pF	
Code Full Scale		5	8	pF	
DIGITAL INPUTS/OUTPUT <sup>1</sup>					
Input High Voltage, $V_{IH}$	1.7			V	
Input Low Voltage, $V_{IL}$			0.6	V	
Output High Voltage, $V_{OH}$	$V_{DD} - 1$			V	$V_{DD} = 4.5\text{ V to }5\text{ V}$ , $I_{SOURCE} = 200\text{ }\mu\text{A}$
	$V_{DD} - 0.5$			V	$V_{DD} = 2.5\text{ V to }3.6\text{ V}$ , $I_{SOURCE} = 200\text{ }\mu\text{A}$
Output Low Voltage, $V_{OL}$			0.4	V	$V_{DD} = 4.5\text{ V to }5\text{ V}$ , $I_{SINK} = 200\text{ }\mu\text{A}$
			0.4	V	$V_{DD} = 2.5\text{ V to }3.6\text{ V}$ , $I_{SINK} = 200\text{ }\mu\text{A}$
Input Leakage Current, $I_{IL}$			1	$\mu\text{A}$	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE <sup>1</sup>					
Reference Multiplying Bandwidth		10		MHz	$V_{REF} = \pm 3.5\text{ V}$ ; DAC loaded all 1s
Output Voltage Settling Time					$V_{REF} = \pm 3.5\text{ V}$ , $R_{LOAD} = 100\text{ }\Omega$ , DAC latch alternately loaded with 0s and 1s
Measured to $\pm 16\text{ mV}$ of full scale		30	60	ns	
Measured to $\pm 4\text{ mV}$ of full scale		35	70	ns	
Measured to $\pm 1\text{ mV}$ of full scale		80	120	ns	
Digital Delay		20	40	ns	Interface delay time
10% to 90% Settling Time		15	30	ns	Rise and fall time, $V_{REF} = 10\text{ V}$ , $R_{LOAD} = 100\text{ }\Omega$
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, $V_{REF} = 0\text{ V}$
Multiplying Feedthrough Error					DAC latch loaded with all 0s, $V_{REF} = \pm 3.5\text{ V}$
		70		dB	Reference = 1 MHz
		48		dB	Reference = 10 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Capacitance					
I <sub>OUT1</sub>		12	17	pF	All 0s loaded
		25	30	pF	All 1s loaded
I <sub>OUT2</sub>		22	25	pF	All 0s loaded
		10	12	pF	All 1s loaded
Digital Feedthrough		1		nV-s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Analog THD		81		dB	V <sub>REF</sub> = 3.5 V p-p, all 1s loaded, f = 100 kHz
Digital THD					Clock = 10 MHz, V <sub>REF</sub> = 3.5 V
50 kHz f <sub>OUT</sub>		65		dB	
Output Noise Spectral Density <sup>2</sup>		25		nV/Hz	At 1 kHz
SFDR Performance (Wide Band)					AD5445, V <sub>REF</sub> = 3.5 V
Clock = 10 MHz					
500 kHz f <sub>OUT</sub>		55		dB	
100 kHz f <sub>OUT</sub>		63		dB	
50 kHz f <sub>OUT</sub>		65		dB	
Clock = 25 MHz					
500 kHz f <sub>OUT</sub>		50		dB	
100 kHz f <sub>OUT</sub>		60		dB	
50 kHz f <sub>OUT</sub>		62		dB	
SFDR Performance (Narrow Band)					AD5445, V <sub>REF</sub> = 3.5 V
Clock = 10 MHz					
500 kHz f <sub>OUT</sub>		73		dB	
100 kHz f <sub>OUT</sub>		80		dB	
50 kHz f <sub>OUT</sub>		82		dB	
Clock = 25 MHz					
500 kHz f <sub>OUT</sub>		70		dB	
100 kHz f <sub>OUT</sub>		75		dB	
50 kHz f <sub>OUT</sub>		80		dB	
Intermodulation Distortion					AD5445, V <sub>REF</sub> = 3.5 V
Clock = 10 MHz					
f <sub>1</sub> = 400 kHz, f <sub>2</sub> = 500 kHz		65		dB	
f <sub>1</sub> = 40 kHz, f <sub>2</sub> = 50 kHz		72		dB	
Clock = 25 MHz					
f <sub>1</sub> = 400 kHz, f <sub>2</sub> = 500 kHz		51		dB	
f <sub>1</sub> = 40 kHz, f <sub>2</sub> = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I <sub>DD</sub>			0.6	μA	T <sub>A</sub> = 25°C, logic inputs = 0 V or V <sub>DD</sub>
		0.4	5	μA	Logic inputs = 0 V or V <sub>DD</sub> , T = -40°C to +125°C
Power Supply Sensitivity			0.001	%/%	ΔV <sub>DD</sub> = ±5%

<sup>1</sup> Guaranteed by design, not subject to production test.

<sup>2</sup> Specification measured with OP27.

## TIMING CHARACTERISTICS

All input signals are specified with  $t_r = t_f = 1$  ns (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .  $V_{DD} = 2.5$  V to 5.5 V,  $V_{REF} = 10$  V,  $I_{OUT2} = 0$  V; temperature range for Y version:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter <sup>1</sup>	$V_{DD} = 2.5$ V to 5.5 V	$V_{DD} = 4.5$ V to 5.5 V	Unit	Test Conditions/Comments
$t_1$	0	0	ns min	R/W to $\overline{CS}$ setup time
$t_2$	0	0	ns min	R/W to $\overline{CS}$ hold time
$t_3$	10	10	ns min	$\overline{CS}$ low time (write cycle)
$t_4$	6	6	ns min	Data setup time
$t_5$	0	0	ns min	Data hold time
$t_6$	5	5	ns min	R/W high to $\overline{CS}$ low
$t_7$	9	7	ns min	$\overline{CS}$ min high time
$t_8$	20	10	ns typ	Data access time
	40	20	ns max	
$t_9$	5	5	ns typ	Bus relinquish time
	10	10	ns max	

<sup>1</sup> Guaranteed by design, not subject to production test.

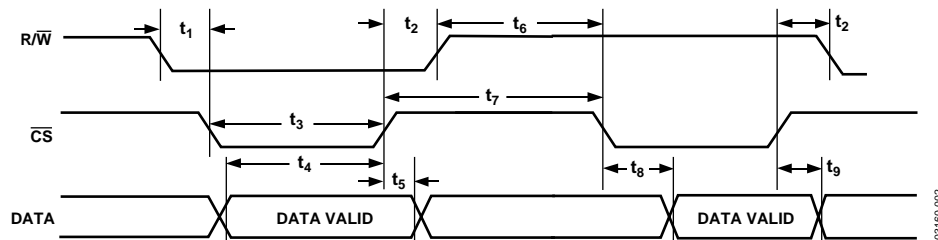


Figure 2. Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_{REF}$ , $R_{FB}$ to GND	-12 V to +12 V
$I_{OUT1}$ , $I_{OUT2}$ to GND	-0.3 V to +7 V
Logic Inputs and Output <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Extended Industrial (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP $\theta_{JA}$ Thermal Impedance	150°C/W
20-Lead TSSOP $\theta_{JA}$ Thermal Impedance	143°C/W
20-Lead LFCSP $\theta_{JA}$ Thermal Impedance	135°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

<sup>1</sup> Overvoltages at  $\overline{DBx}$ ,  $\overline{CS}$ , and  $R/\overline{W}$ , are clamped by internal diodes.

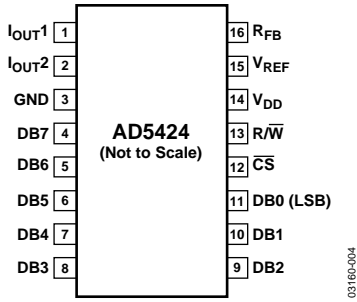
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



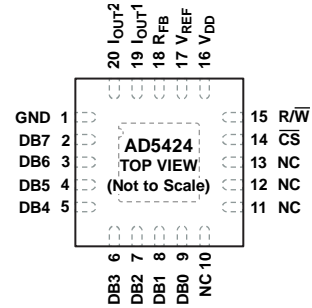
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



03160-004

Figure 3. AD5424 Pin Configuration (TSSOP)



03160-105

- NOTES  
 1. NC = NO CONNECT.  
 2. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 4. AD5424 Pin Configuration (LFCSP)

Table 4. AD5424 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	19	I <sub>OUT1</sub>	DAC Current Output.
2	20	I <sub>OUT2</sub>	DAC Analog Ground. This pin must normally be tied to the analog ground of the system.
3	1	GND	Ground.
4 to 11	2 to 9	DB7 to DB0	Parallel Data Bits 7 to 0.
	10 to 13	NC	No Internal Connection.
12	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with $R/\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
13	15	$R/\overline{W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
14	16	V <sub>DD</sub>	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
15	17	V <sub>REF</sub>	DAC Reference Voltage Input Terminal.
16	18	R <sub>FB</sub>	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

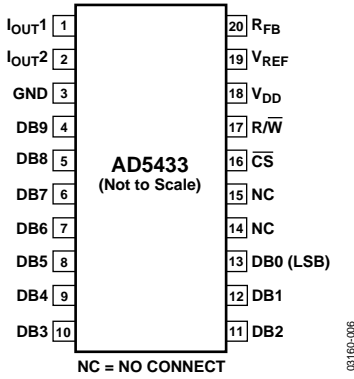
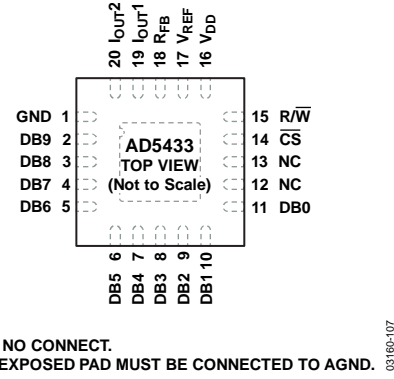


Figure 5. AD5433 Pin Configuration (TSSOP)



NOTES  
 1. NC = NO CONNECT.  
 2. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 6. AD5433 Pin Configuration (LFCSP)

Table 5. AD5433 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	19	I <sub>OUT1</sub>	DAC Current Output.
2	20	I <sub>OUT2</sub>	DAC Analog Ground. This pin must normally be tied to the analog ground of the system.
3	1	GND	Ground.
4 to 13	2 to 11	DB9 to DB0	Parallel Data Bits 9 to 0.
14, 15	12, 13	NC	Not Internally Connected.
16	14	$\overline{CS}$	Chip Select Input. Active low. Use in conjunction with $\overline{R/W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	$\overline{R/W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	16	V <sub>DD</sub>	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V <sub>REF</sub>	DAC Reference Voltage Input Terminal.
20	18	R <sub>FB</sub>	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

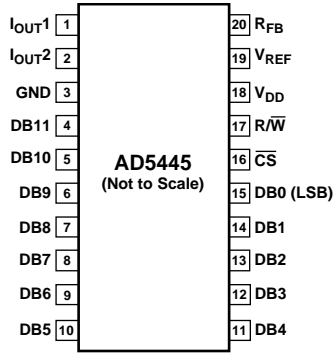
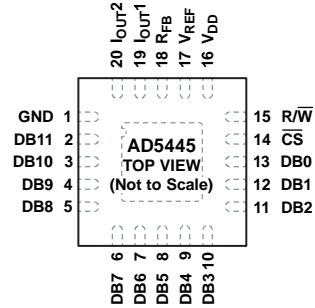


Figure 7. AD5445 Pin Configuration (TSSOP)



NOTES  
1. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 8. AD5445 Pin Configuration (LFCSP)

Table 6. AD5445 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	19	I <sub>OUT1</sub>	DAC Current Output.
2	20	I <sub>OUT2</sub>	DAC Analog Ground. This pin must normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4 to 15	2 to 13	DB11 to DB0	Parallel Data Bits 11 to 0.
16	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with $\overline{R/W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	$\overline{R/W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	16	V <sub>DD</sub>	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V <sub>REF</sub>	DAC Reference Voltage Input Terminal.
20	18	R <sub>FB</sub>	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.



TYPICAL PERFORMANCE CHARACTERISTICS

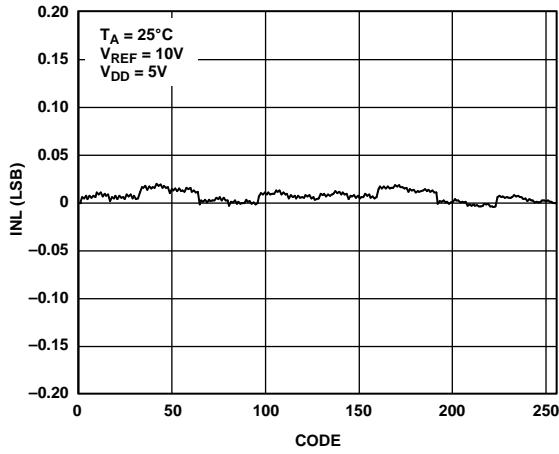


Figure 9. INL vs. Code (8-Bit DAC)

03160-010

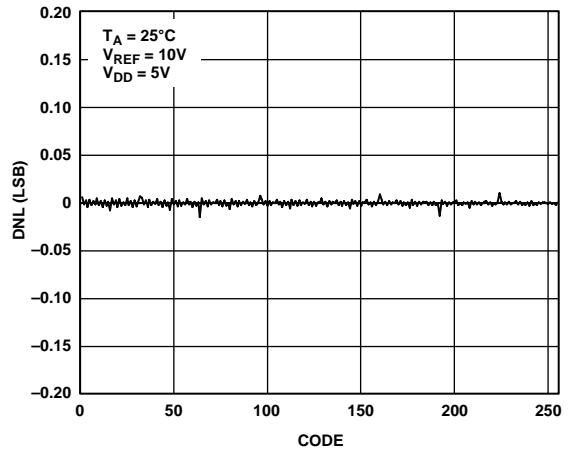


Figure 12. DNL vs. Code (8-Bit DAC)

03160-013

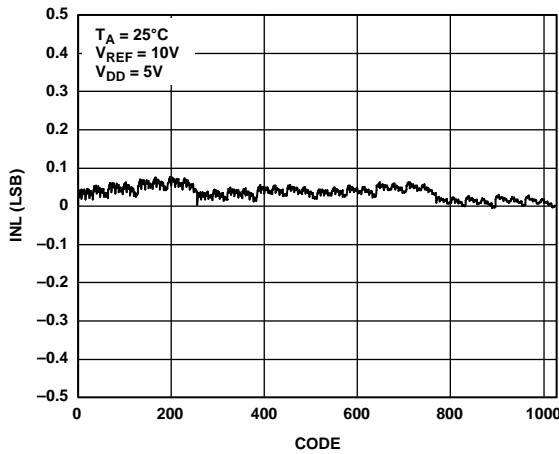


Figure 10. INL vs. Code (10-Bit DAC)

03160-011

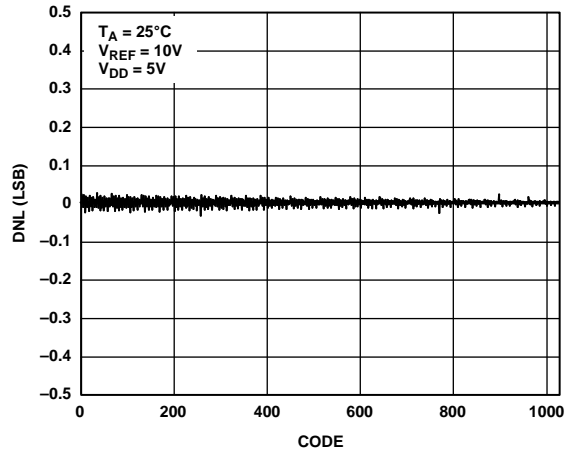


Figure 13. DNL vs. Code (10-Bit DAC)

03160-014

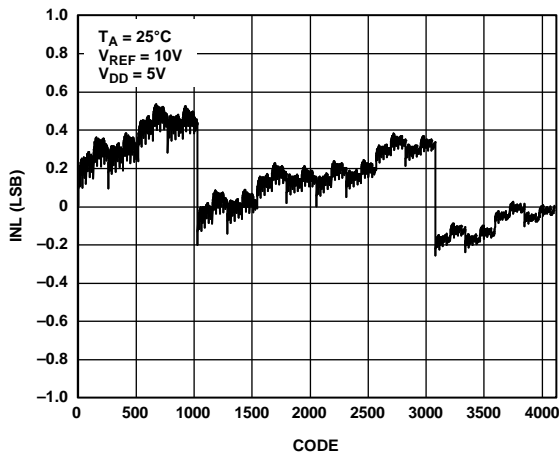


Figure 11. INL vs. Code (12-Bit DAC)

03160-012

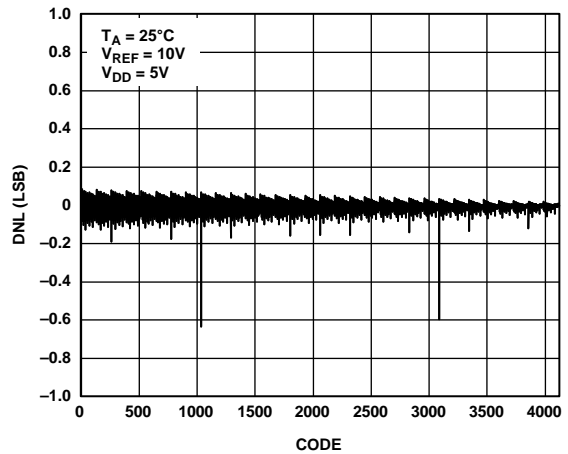


Figure 14. DNL vs. Code (12-Bit DAC)

03160-015

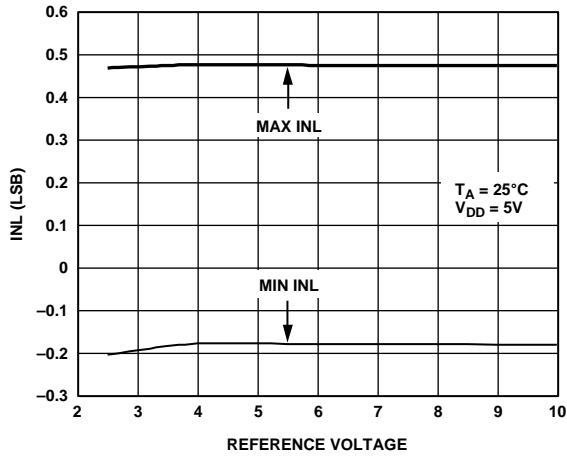


Figure 15. INL vs. Reference Voltage, AD5445

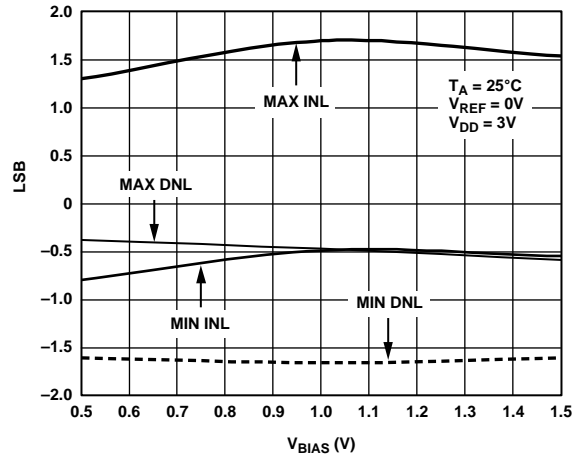


Figure 18. Linearity vs.  $V_{BIAS}$  Voltage Applied to  $I_{OUT2}$ , AD5445

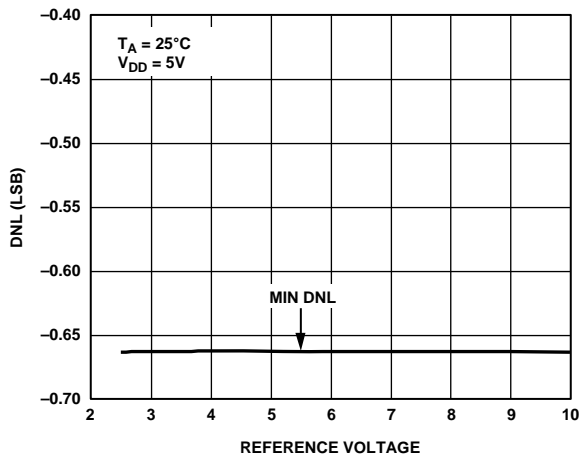


Figure 16. DNL vs. Reference Voltage, AD5445

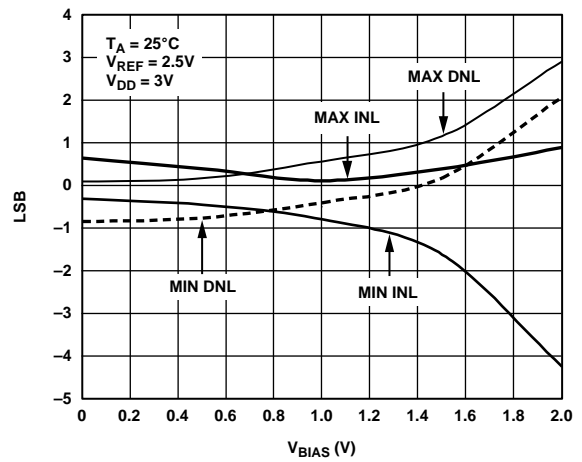


Figure 19. Linearity vs.  $V_{BIAS}$  Voltage Applied to  $I_{OUT2}$ , AD5445

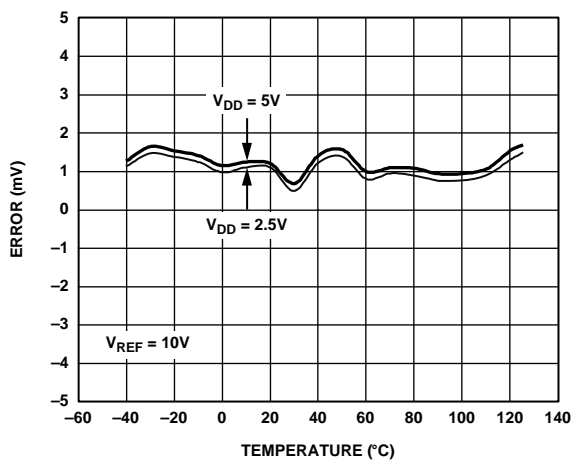


Figure 17. Gain Error vs. Temperature

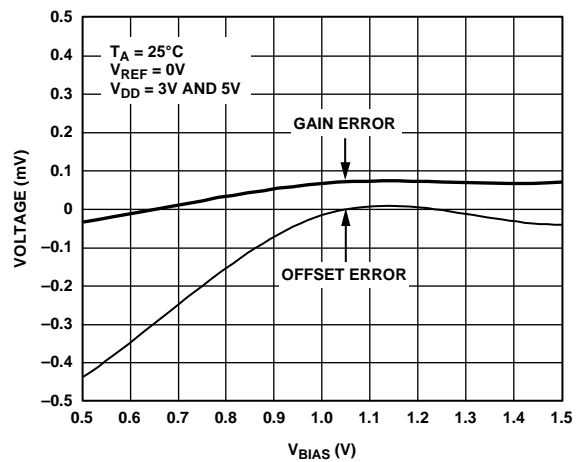


Figure 20. Gain and Offset Errors vs.  $V_{BIAS}$  Voltage Applied to  $I_{OUT2}$

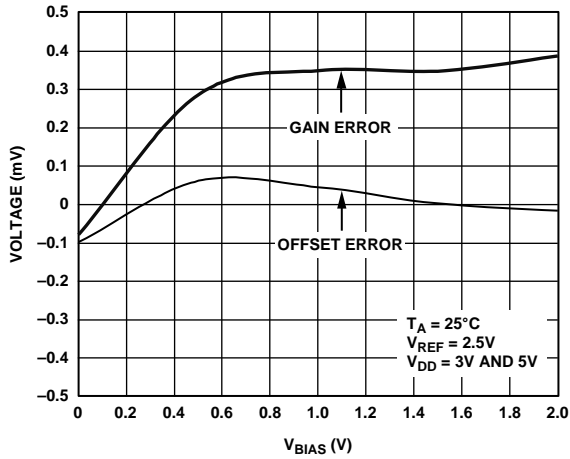


Figure 21. Gain and Offset Errors vs.  $V_{BIAS}$  Voltage Applied to  $I_{out2}$

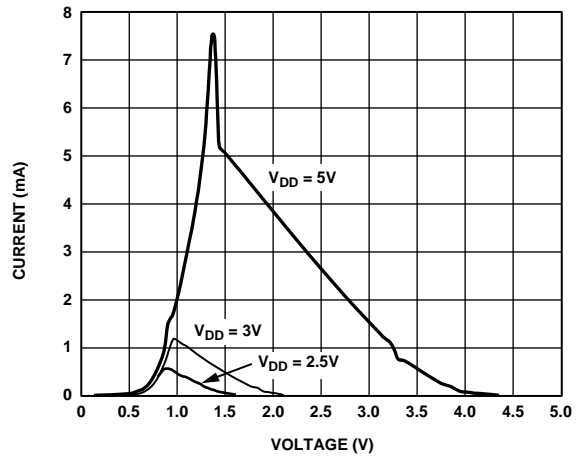


Figure 24. Supply Current vs. Logic Input Voltage (Driving DB0 to DB11, All Other Digital Inputs at Supplies)

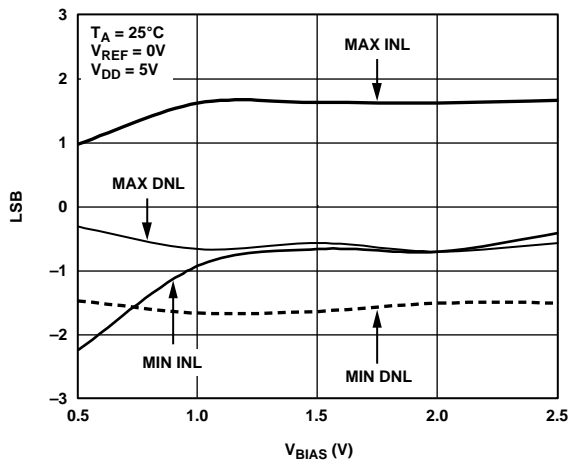


Figure 22. Linearity vs.  $V_{BIAS}$  Voltage Applied to  $I_{out2}$ , AD5445

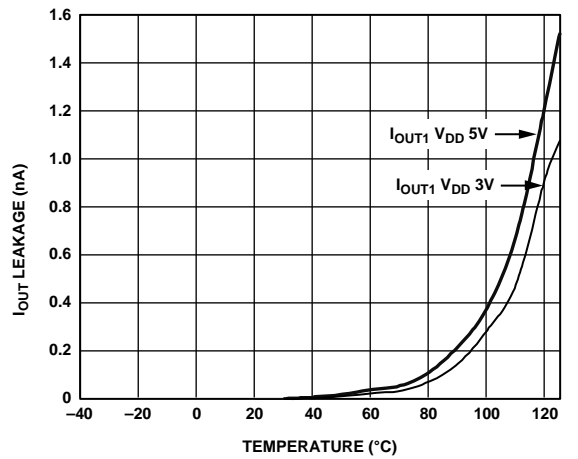


Figure 25.  $I_{out1}$  Leakage Current vs. Temperature

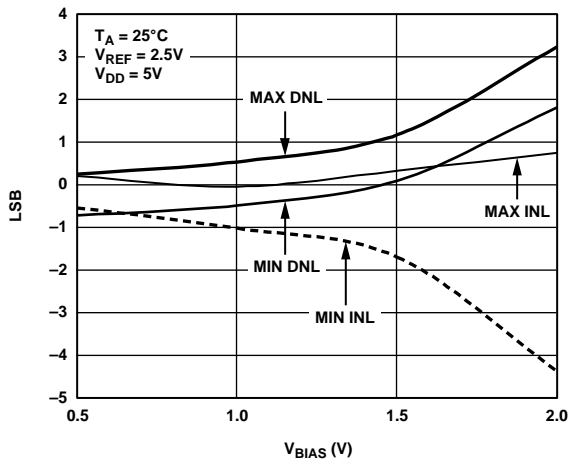


Figure 23. Linearity vs.  $V_{BIAS}$  Voltage Applied to  $I_{out2}$ , AD5445

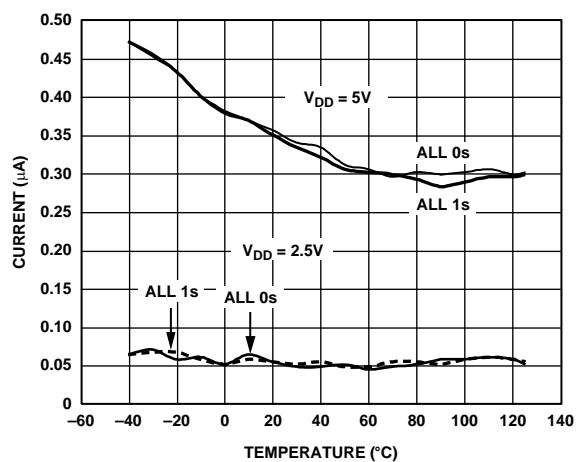


Figure 26. Supply Current vs. Temperature

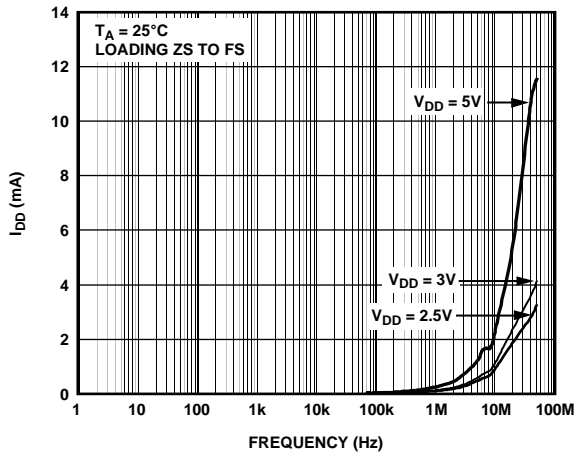


Figure 27. Supply Current vs. Update Rate

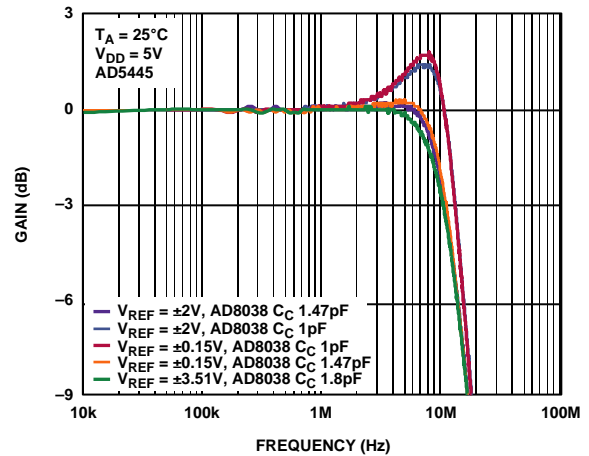


Figure 30. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

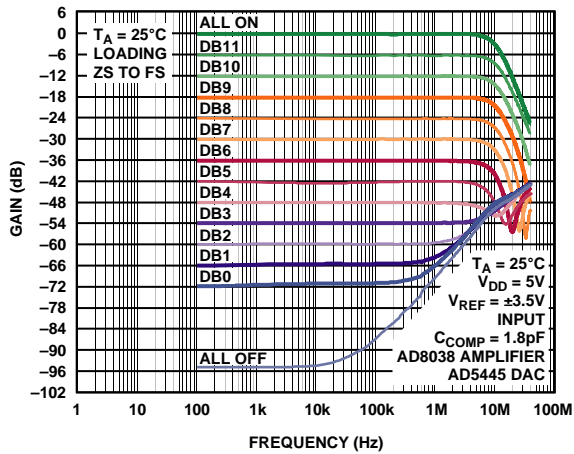


Figure 28. Reference Multiplying Bandwidth vs. Frequency and Code

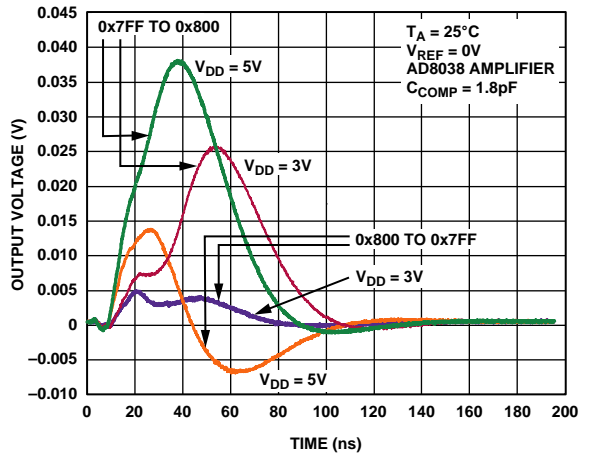


Figure 31. Midscale Transition,  $V_{REF} = 0\text{ V}$

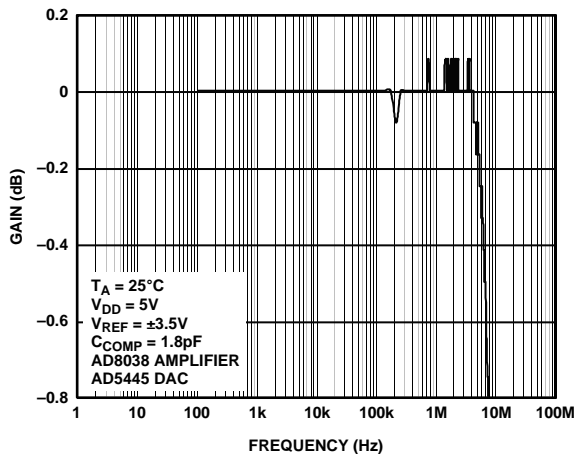


Figure 29. Reference Multiplying Bandwidth—All 1s Loaded

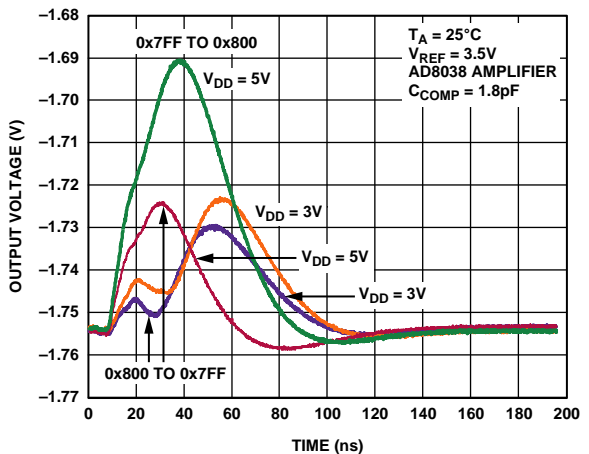


Figure 32. Midscale Transition,  $V_{REF} = 3.5\text{ V}$

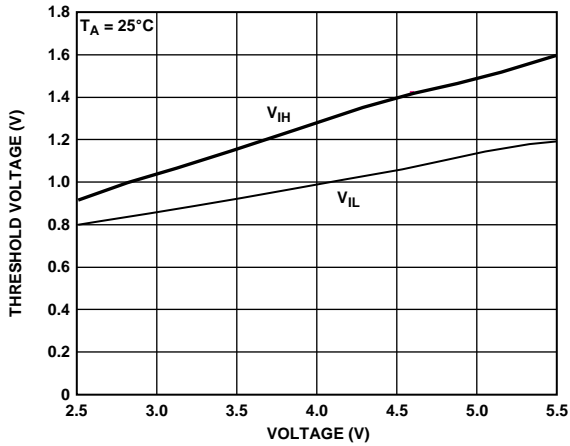


Figure 33. Threshold Voltages vs. Supply Voltage

03160-062

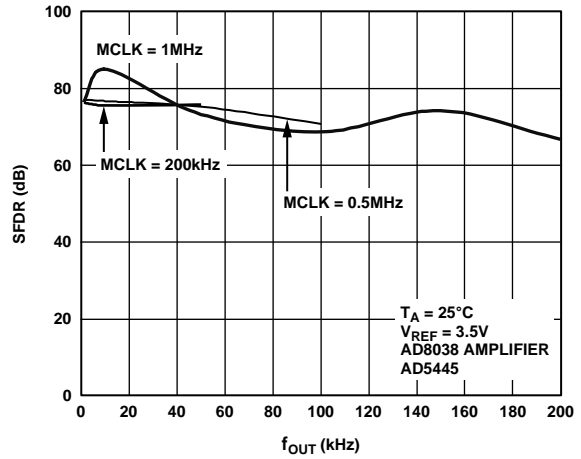


Figure 36. Wideband SFDR vs.  $f_{OUT}$  Frequency

03160-036

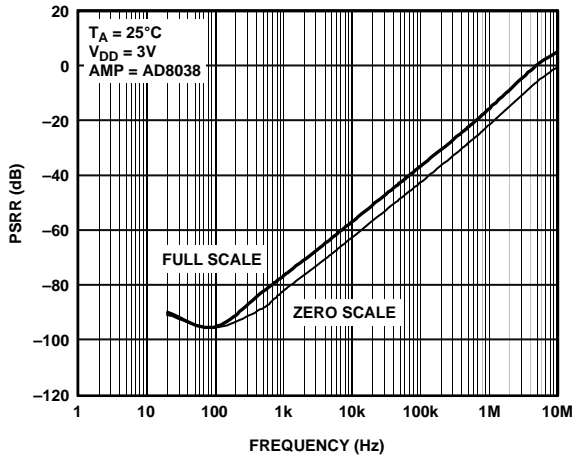


Figure 34. Power Supply Rejection vs. Frequency

03160-034

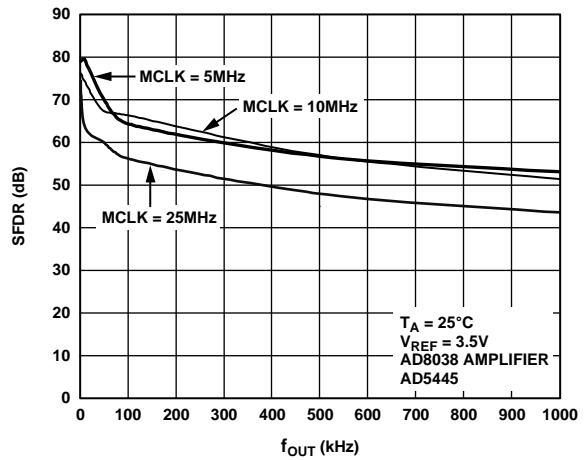


Figure 37. Wideband SFDR vs.  $f_{OUT}$  Frequency

03160-037

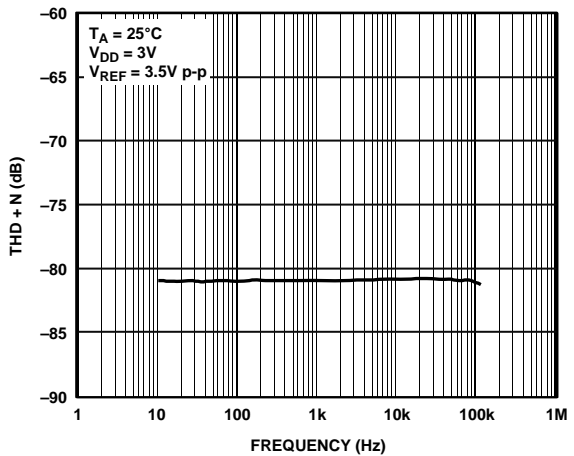


Figure 35. THD and Noise vs. Frequency

03160-035

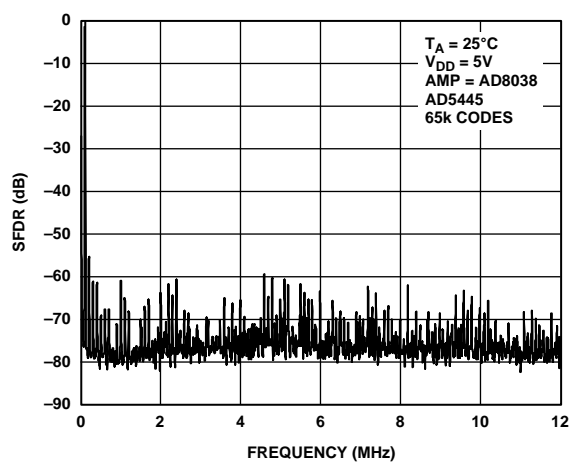


Figure 38. Wideband SFDR,  $f_{OUT} = 100$  kHz, Clock = 25 MHz

03160-038

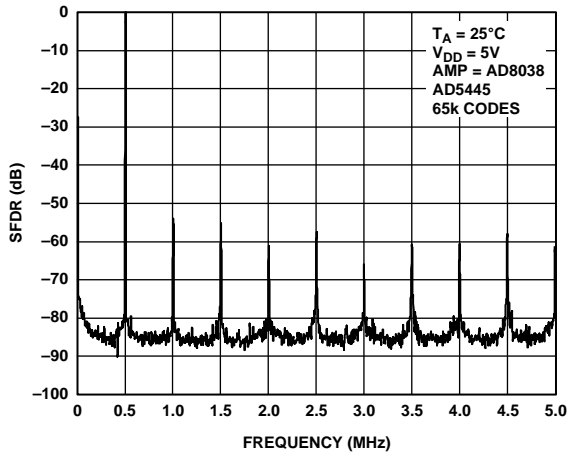


Figure 39. Wideband SFDR,  $f_{OUT} = 500$  kHz, Clock = 10 MHz

03160-039

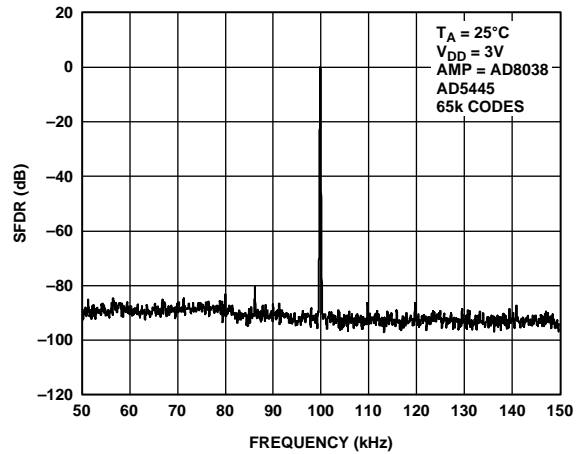


Figure 42. Narrow-Band SFDR,  $f_{OUT} = 100$  kHz, MCLK = 25 MHz

03160-042

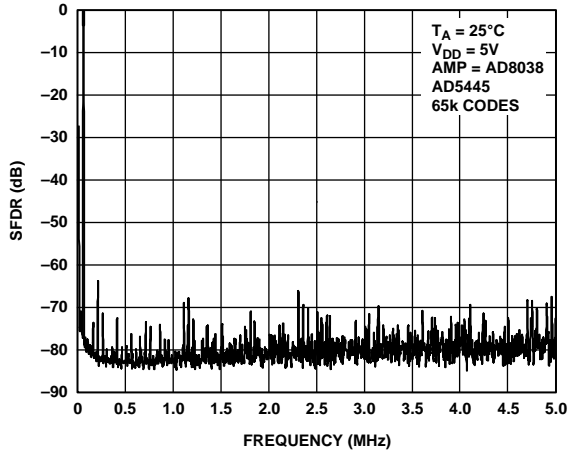


Figure 40. Wideband SFDR,  $f_{OUT} = 50$  kHz, Clock = 10 MHz

03160-040

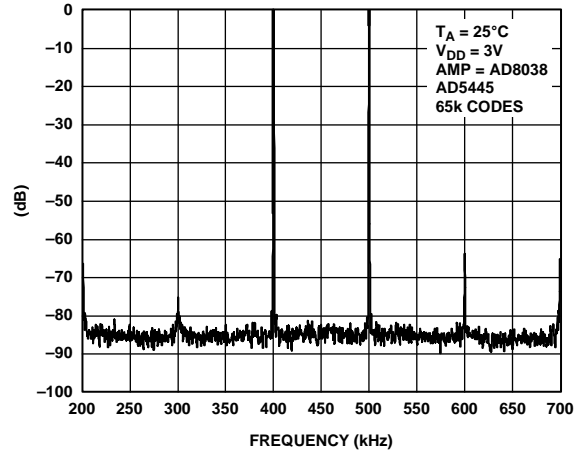


Figure 43. Narrow-Band IMD,  $f_{OUT} = 400$  kHz, 500 kHz, Clock = 10 MHz

03160-043

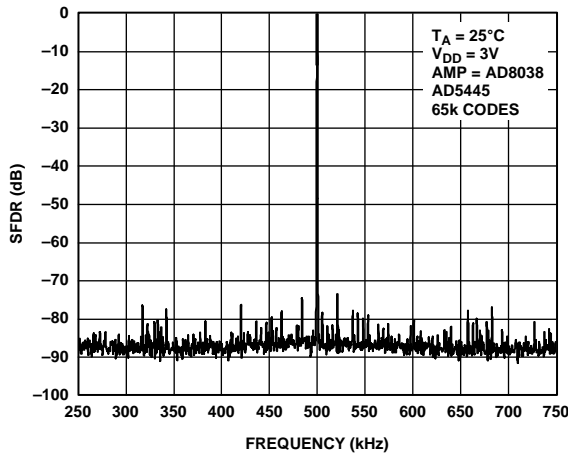


Figure 41. Narrow-Band Spectral Response,  $f_{OUT} = 500$  kHz, Clock = 25 MHz

03160-041

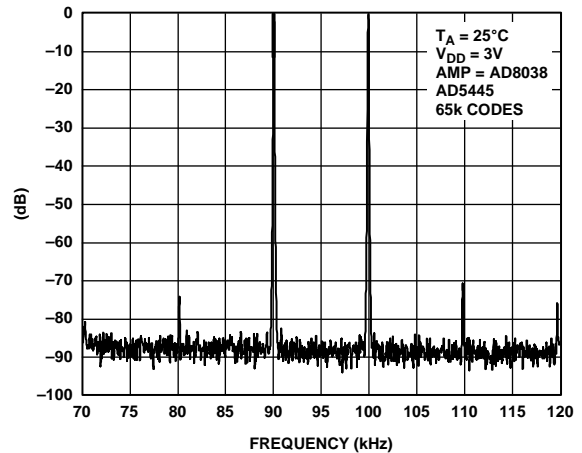


Figure 44. Narrow-Band IMD,  $f_{OUT} = 90$  kHz, 100 kHz, Clock = 10 MHz

03160-044

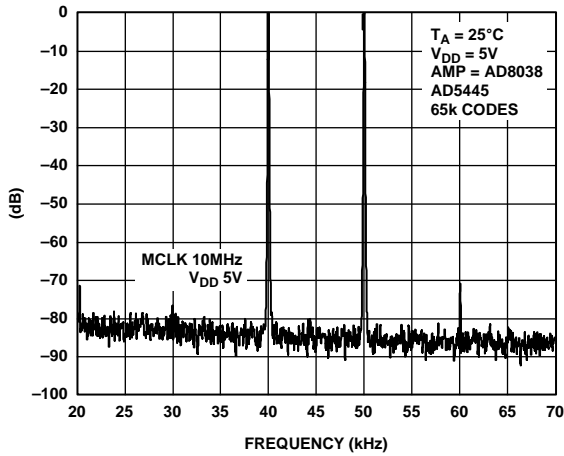


Figure 45. Narrow-Band IMD,  $f_{OUT} = 40\text{ kHz}, 50\text{ kHz}$ , Clock = 10 MHz

03160-045

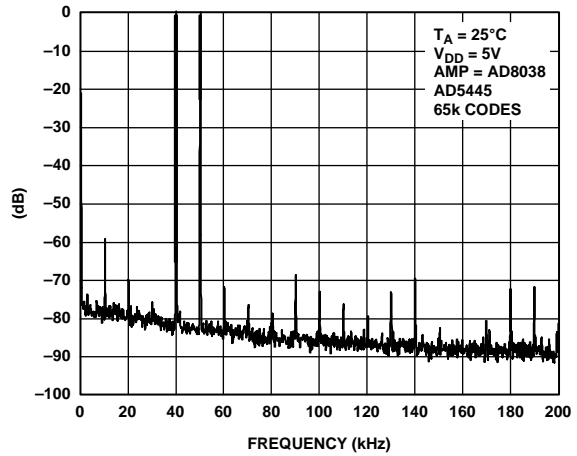


Figure 47. Wideband IMD,  $f_{OUT} = 60\text{ kHz}, 50\text{ kHz}$ , Clock = 10 MHz

03160-047

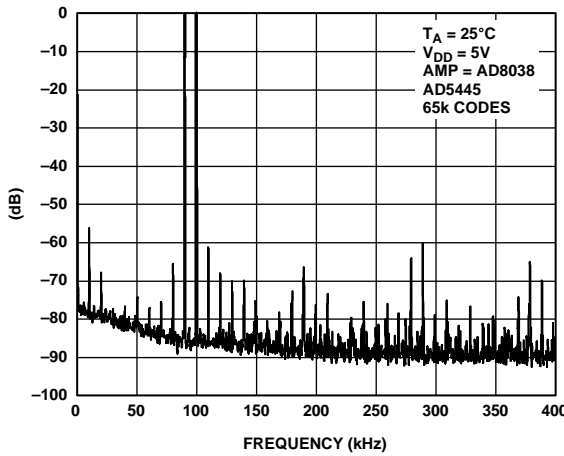


Figure 46. Wideband IMD,  $f_{OUT} = 90\text{ kHz}, 100\text{ kHz}$ , Clock = 25 MHz

03160-046

## TERMINOLOGY

### Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting zero scale and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

### Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $-1$  LSB maximum over the operating temperature range ensures monotonicity.

### Gain Error

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is  $V_{REF} - 1$  LSB. Gain error of the DACs is adjustable to 0 with external resistance.

### Output Leakage Current

Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the  $I_{OUT1}$  terminal, it can be measured by loading all 0s to the DAC and measuring the  $I_{OUT1}$  current. Minimum current flows in the  $I_{OUT2}$  line when the DAC is loaded with all 1s.

### Output Capacitance

Capacitance from  $I_{OUT1}$ , or  $I_{OUT2}$ , to AGND.

### Output Current Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a  $100\ \Omega$  resistor to ground.

The settling time specification includes the digital delay from the CS rising edge to the full-scale output change.

### Digital-to-Analog Glitch Impulse

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA seconds or nV seconds, depending upon whether the glitch is measured as a current or voltage signal.

### Digital Feedthrough

When the device is not selected, high frequency logic activity on the device digital inputs can be capacitively coupled through the device to show up as noise on the  $I_{OUT}$  pins and subsequently in the following circuitry. This noise is called digital feedthrough.

### Multiplying Feedthrough Error

This is the error due to capacitive feedthrough from the DAC reference input to the DAC  $I_{OUT1}$  terminal when all 0s are loaded to the DAC.

### Total Harmonic Distortion (THD)

The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second to fifth.

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}$$

### Digital Intermodulation Distortion

Second-order intermodulation distortion (IMD) measurements are the relative magnitude of the  $f_a$  and  $f_b$  tones generated digitally by the DAC and the second-order products at  $2f_a - f_b$  and  $2f_b - f_a$ .

### Spurious-Free Dynamic Range (SFDR)

SFDR is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. It is measured by the difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or  $f_s/2$ ). Narrow-band SFDR is a measure of SFDR over an arbitrary window size, in this case, 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is a digitally generated sine wave.



## THEORY OF OPERATION

The **AD5424**, **AD5433**, and **AD5445** are 8-, 10-, and 12-bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-bit **AD5424** is shown in Figure 48. The matching feedback resistor  $R_{FB}$  has a value of  $R$ . The value of  $R$  is typically  $10\text{ k}\Omega$  (minimum  $8\text{ k}\Omega$  and maximum  $12\text{ k}\Omega$ ). If  $I_{OUT1}$  and  $I_{OUT2}$  are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at  $V_{REF}$  is always constant and nominally of resistance value  $R$ . The DAC output ( $I_{OUT}$ ) is code-dependent, producing various resistances and capacitances. External amplifier choice must take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

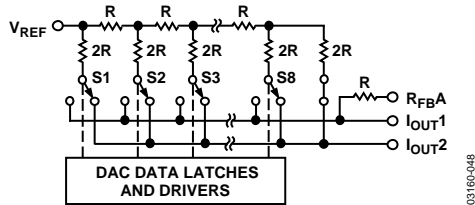


Figure 48. Simplified Ladder

Access is provided to the  $V_{REF}$ ,  $R_{FB}$ ,  $I_{OUT1}$ , and  $I_{OUT2}$  terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, 4-quadrant multiplication in bipolar mode or in single-supply modes of operation. Note that a matching switch is used in series with the internal  $R_{FB}$  feedback resistor. If users attempt to measure  $R_{FB}$ , power must be applied to  $V_{DD}$  to achieve continuity.

## CIRCUIT OPERATION

### Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 49.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times \frac{D}{2^n}$$

where  $D$  is the fractional representation of the digital word loaded to the DAC and  $n$  is the resolution of the DAC.

$$\begin{aligned} D &= 0 \text{ to } 255 \text{ (8-bit AD5424)} \\ &= 0 \text{ to } 1023 \text{ (10-bit AD5433)} \\ &= 0 \text{ to } 4095 \text{ (12-bit AD5445)} \end{aligned}$$

Note that the output voltage polarity is opposite to the  $V_{REF}$  polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The  $V_{DD}$  power pin is only used by the internal digital logic to drive the DAC switches' on and off states.

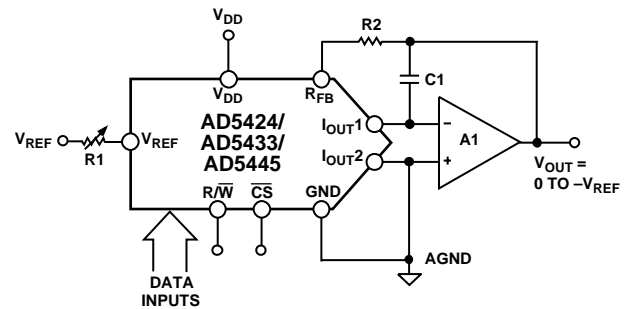
These DACs are also designed to accommodate ac reference input signals in the range of  $-10\text{ V}$  to  $+10\text{ V}$ .

With a fixed  $10\text{ V}$  reference, the circuit shown in Figure 49 gives a unipolar  $0\text{ V}$  to  $-10\text{ V}$  output voltage swing. When  $V_{IN}$  is an ac signal, the circuit performs 2-quadrant multiplication.

Table 7 shows the relationship between digital code and expected output voltage for unipolar operation (**AD5424**, 8-bit device).

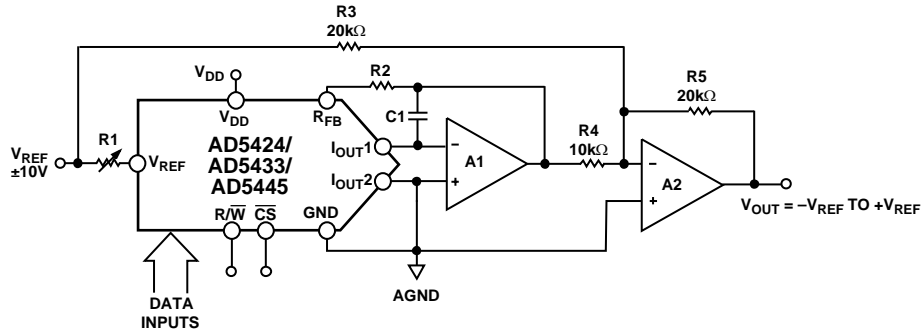
Table 7. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF} (255/256)$
1000 0000	$-V_{REF} (128/256) = -V_{REF}/2$
0000 0001	$V_{REF} (1/256)$
0000 0000	$V_{REF} (0/256) = 0$



- NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
  2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 49. Unipolar Operation



- NOTES:
1. R1 AND R2 ARE USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR  $V_{OUT} = 0V$  WITH CODE 10000000 LOADED TO DAC.
  2. MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R3 AND R4.
  3. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER.

03160-050

Figure 50. Bipolar Operation (4-Quadrant Multiplication)

**BIPOLAR OPERATION**

In some applications, it can be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors, as shown in Figure 50. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage, results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ( $V_{OUT} = -V_{REF}$ ) to midscale ( $V_{OUT} = 0V$ ) to full scale ( $V_{OUT} = +V_{REF}$ ).

$$V_{OUT} = (V_{REF} \times D / 2^{n-1}) - V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

- D = 0 to 255 (8-bit AD5424)
- = 0 to 1023 (10-bit AD5433)
- = 0 to 4095 (12-bit AD5445)

When  $V_{IN}$  is an ac signal, the circuit performs 4-quadrant multiplication.

Table 8 shows the relationship between digital code and the expected output voltage for bipolar operation (AD5424, 8-bit device).

Table 8. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	+ $V_{REF}$ (127/128)
1000 0000	0
0000 0001	- $V_{REF}$ (127/128)
0000 0000	- $V_{REF}$ (128/128)

**Stability**

In the I-to-V configuration, the  $I_{OUT}$  of the DAC and the inverting node of the op amp must be connected as closely as possible and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking can occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in closed-loop applications.

An optional compensation capacitor, C1, can be added in parallel with  $R_{FB}$  for stability, as shown in Figure 49 and Figure 50. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 must be found empirically, but 1 pF to 2 pF is generally adequate for compensation.

## SINGLE-SUPPLY APPLICATIONS

### Current Mode Operation

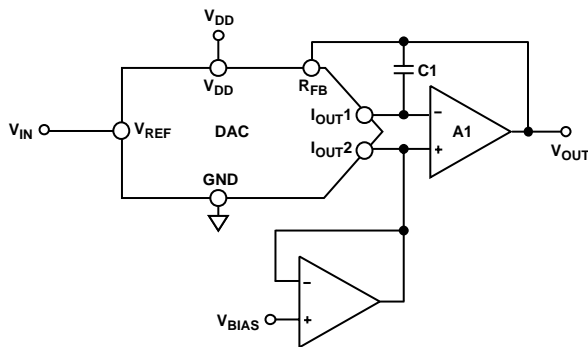
The current mode circuit in Figure 51 shows a typical circuit for operation with a single 2.5 V to 5 V supply.  $I_{OUT2}$  and therefore  $I_{OUT1}$  is biased positive by the amount applied to  $V_{BIAS}$ . In this configuration, the output voltage is given by

$$V_{OUT} = [D \times (R_{FB}/R_{DAC}) \times (V_{BIAS} - V_{IN})] + V_{BIAS}$$

As  $D$  varies from 0 to 255 (AD5424), 0 to 1023 (AD5433), or 0 to 4095 (AD5445), the output voltage varies from

$$V_{OUT} = V_{BIAS} \text{ to } V_{OUT} = 2V_{BIAS} - V_{IN}$$

$V_{BIAS}$  must be a low impedance source capable of sinking and sourcing all possible variations in current at the  $I_{OUT2}$  terminal.



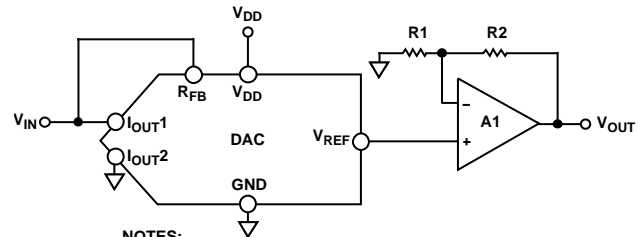
- NOTES:
1. ADDITIONAL PINS OMITTED FOR CLARITY
  2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 51. Single-Supply Current Mode Operation

It is important to note that  $V_{IN}$  is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, there on resistance differs and the linearity of the DAC degrades.

### Voltage Switching Mode of Operation

Figure 52 shows these DACs operating in the voltage-switching mode. The reference voltage,  $V_{IN}$ , is applied to the  $I_{OUT1}$  pin,  $I_{OUT2}$  is connected to AGND, and the output voltage is available at the  $V_{REF}$  terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is a voltage at a constant impedance (the DAC ladder resistance), thus an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. Therefore, the voltage input must be driven from a low impedance source.



- NOTES:
1. ADDITIONAL PINS OMITTED FOR CLARITY
  2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 52. Single-Supply Voltage-Switching Mode Operation

It is important to note that  $V_{IN}$  is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, there on resistance differs, which degrades the linearity of the DAC. See Figure 18 to Figure 23. Also,  $V_{IN}$  must not go negative by more than 0.3 V; otherwise, an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

**ADDING GAIN**

In applications where the output voltage is required to be greater than  $V_{IN}$ , gain can be added with an additional external amplifier or it can be achieved in a single stage. It is important to consider the effect of the temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the  $R_{FB}$  resistor causes mismatches in the temperature coefficients and results in larger gain temperature coefficient errors. Instead, the circuit shown in Figure 53 is a recommended method of increasing the gain of the circuit.  $R_1$ ,  $R_2$ , and  $R_3$  must have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains greater than 1 are required. Note that  $R_{FB} \gg R_2 \parallel R_3$  and take into consideration a gain error percentage of  $100 \times (R_2 \parallel R_3) / R_{FB}$ .

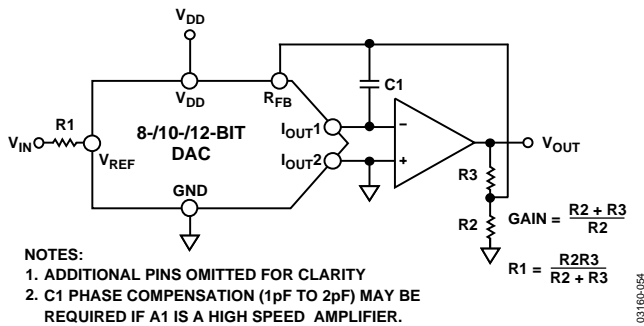


Figure 53. Increasing the Gain of the Current Output DAC

**DACS USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT**

Current steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp and  $R_{FB}$  is used as the input resistor, as shown in Figure 54, then the output voltage is inversely proportional to the digital input fraction,  $D$ .

For  $D = 1 - 2^{-n}$  the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1 - 2^{-n})$$

As  $D$  is reduced, the output voltage increases. For small values of  $D$ , it is important to ensure that the amplifier does not saturate and that the required accuracy is met.

For example, in the circuit shown in Figure 54, an 8-bit DAC driven with the binary code 0x10 (00010000), that is, 16 decimal, must cause the output voltage to be  $16 \times V_{IN}$ . However, if the DAC has a linearity specification of  $\pm 0.5$  LSB, then  $D$  can in fact have a weight anywhere in the range  $15.5/256$  to  $16.5/256$  so that the possible output voltage falls in the range  $15.5 V_{IN}$  to  $16.5 V_{IN}$ —an error of 3% even though the DAC itself has a maximum error of 0.2%.

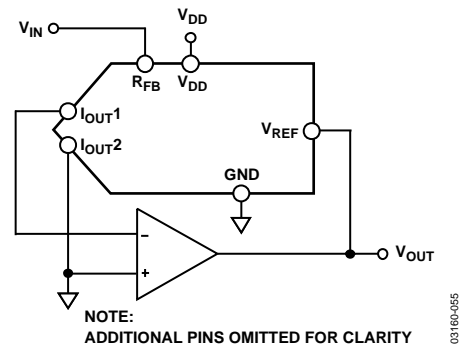


Figure 54. Current-Steering DAC Used as a Divider or Programmable Gain Element

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction,  $D$ , of the current into the  $V_{REF}$  terminal is routed to the  $I_{OUT1}$  terminal, the output voltage has to change as follows:

$$Output\ Error\ Voltage\ due\ to\ DAC\ Leakage = (Leakage \times R)/D$$

where  $R$  is the DAC resistance at the  $V_{REF}$  terminal.

For a DAC leakage current of 10 nA,  $R = 10$  k $\Omega$ , and a gain (that is,  $1/D$ ) of 16, the error voltage is 1.6 mV.

Table 9. Suitable ADI Precision References

Device No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I <sub>SS</sub> (mA)	Output Noise (μV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC
ADR435	5	0.04	3	0.8	8	SOIC
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 10. Suitable ADI Precision Op Amps

Device No.	Supply Voltage (V)	V <sub>OS</sub> (Max) (μV)	I <sub>B</sub> (Max) (nA)	0.1 Hz to 10 Hz Noise (μV p-p)	Supply Current (μA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC

Table 11. Suitable ADI High Speed Op Amps

Device No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/μs)	V <sub>OS</sub> (Max) (μV)	I <sub>B</sub> (Max) (nA)	Package
AD8065	5 to 24	145	180	1500	6000	SOIC, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1000	10500	SOIC, MSOP
AD8038	3 to 12	350	425	3000	750	SOIC, SC70-5
AD9631	±3 to ±6	320	1300	10000	7000	SOIC

## REFERENCE SELECTION

When selecting a reference for use with the [AD5424/AD5433/AD5445](#) family of current output DACs, pay attention to the output voltage temperature coefficient specification of the reference. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient must be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature must be less than 78 ppm/°C.

A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized. Table 9 suggests some references available from Analog Devices that are suitable for use with this range of current output DACs.

## AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code dependent output resistance of the DAC) of the circuit. A change in the noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be non-monotonic. In general, the input offset voltage must be <1/4 LSB to ensure monotonic behavior when stepping through codes.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing into the feedback resistor, R<sub>FB</sub>. Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, since it produces a code dependent error at the voltage output of the circuit. Most op amps have adequate common mode rejection for use at 8-, 10-, and 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources ( $V_{IN}$  and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the  $V_{REF}$  node (voltage output node in this application) of the DAC. This is done by using low inputs capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turns requires an amplifier that can handle rail-to-rail signals. There is a large range of single-supply amplifiers available from Analog Devices.

**PARALLEL INTERFACE**

Data is loaded to the AD5424/AD5433/AD5445 in the format of an 8-, 10-, or 12-bit parallel word. Control lines  $\overline{CS}$  and  $R/\overline{W}$  allow data to be written to or read from the DAC register. A write event takes place when  $\overline{CS}$  and  $R/\overline{W}$  are brought low, data available on the data lines fills the shift register, and the rising edge of  $\overline{CS}$  latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent, thus a write sequence must consist of a falling and rising edge on  $\overline{CS}$  to ensure that data is loaded to the DAC register and its analog equivalent is reflected on the DAC output.

A read event takes place when  $R/\overline{W}$  is held high and  $\overline{CS}$  is brought low. New data is loaded from the DAC register back to the input register and out onto the data line where it can be read back to the controller for verification or diagnostic purposes.

**MICROPROCESSOR INTERFACING**

**ADSP-2191M-to-AD5424/AD5433/AD5445 Interface**

Figure 55 shows the AD5424/AD5433/AD5445 interfaced to the ADSP-2191M as a memory-mapped device. A single wait state can be necessary to interface the AD5424/AD5433/AD5445 to the ADSP-2191M, depending on the clock speed of the DSP. The wait state can be programmed via the data memory wait state control register of the ADSP-2191M (see the ADSP 21xx Processors: Manuals for details).

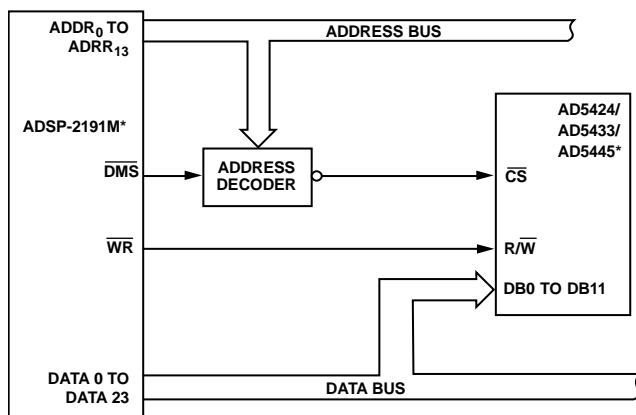


Figure 55. ADSP-2191M-to-AD5424/AD5433/AD5445 Interface

**8xC51-to-AD5424/AD5433/AD5445 Interface**

Figure 56 shows the interface between the AD5424/AD5433/AD5445 and the 8xC51 family of DSPs. To facilitate external data memory access, the address latch enable (ALE) mode is enabled. The low byte of the address is latched with this output pulse during access to external memory. AD0 to AD7 are the multiplexed low order addresses and data bus and require strong internal pull-ups when emitting 1s. During access to external memory, A8 to A15 are the high order address bytes. Since these ports are open drained, they also require strong internal pull-ups when emitting 1s.

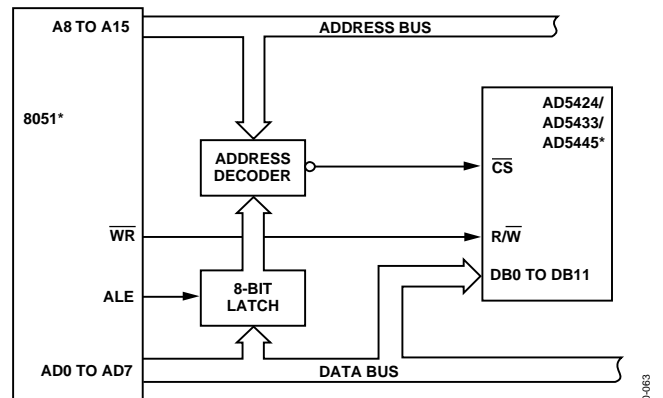


Figure 56. 8xC51-to-AD5424/AD5433/AD5445 Interface

**Blackfin Processor-to-AD5424/AD5433/AD5445 Interface**

Figure 57 shows a typical interface between the AD5424/AD5433/AD5445 and the Blackfin processor family of DSPs. The asynchronous memory write cycle of the processor drives the digital inputs of the DAC. The AMSx line is actually four memory select lines. Internal ADDR lines are decoded into AMS<sub>3-0</sub>, these lines are then inserted as chip selects. The rest of the interface is a standard handshaking operation.

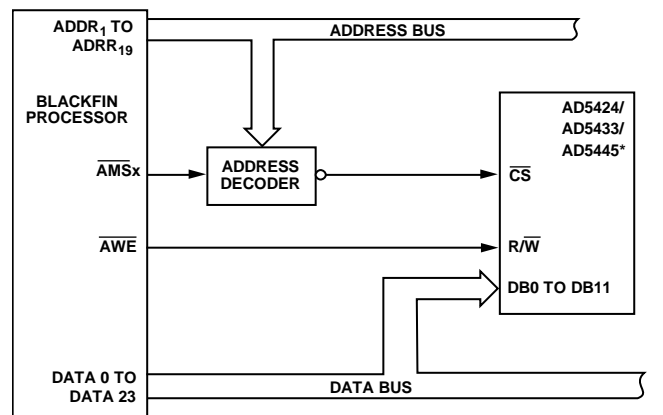


Figure 57. Blackfin Processor-to-AD5424/AD5433/AD5445 Interface

## PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board on which the AD5424/AD5433/AD5445 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

These DACs must have ample supply bypassing of 10  $\mu\text{F}$  in parallel with 0.1  $\mu\text{F}$  on the supply, located as close to the package as possible and ideally right up against the device. The 0.1  $\mu\text{F}$  capacitor must have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum or electrolytic capacitors must also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Shield fast switching signals such as clocks with digital ground to avoid radiating noise to other parts of the board and must never be run near the reference inputs.

Avoid crossover of digital and analog signals. Running traces on opposite sides of the board at right angles to each other reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, while signal traces are placed on the solder side.

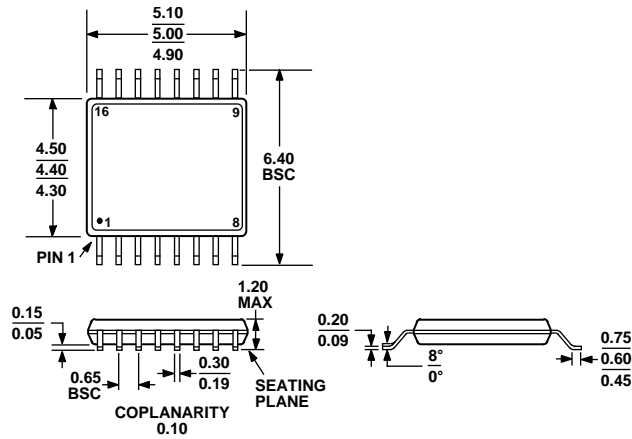
It is good practice to employ compact, minimum lead length PCB layout design. Ensure that leads to the input are as short as possible to minimize IR drops and stray inductance.

Match the PCB metal traces between  $V_{\text{REF}}$  and  $R_{\text{FB}}$  to minimize gain error. To maximize high frequency performance, locate the I-to-V amplifier as close to the device as possible.

Table 12. Overview of the AD5424/AD5433/AD5445 and Related Multiplying DACs

Part No.	Resolution	No. DACs	INL(LSB)	Interface	Package	Features
AD5424	8	1	$\pm 0.25$	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5426	8	1	$\pm 0.25$	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	$\pm 0.25$	Parallel	RU-20	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5429	8	2	$\pm 0.25$	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	$\pm 0.25$	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	$\pm 0.5$	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	$\pm 0.5$	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5439	10	2	$\pm 0.5$	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	$\pm 0.5$	Parallel	RU-24	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5451	10	1	$\pm 0.25$	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	$\pm 1$	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	$\pm 0.5$	Serial	RM-8	50 MHz serial interface
AD5415	12	2	$\pm 1$	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	$\pm 1$	Parallel	CP-40	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5445	12	2	$\pm 1$	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5447	12	2	$\pm 1$	Parallel	RU-24	10 MHz BW, 17 ns $\overline{\text{CS}}$ pulse width
AD5449	12	2	$\pm 1$	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	$\pm 0.5$	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	$\pm 1$	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	$\pm 2$	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	$\pm 1$	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	$\pm 1$	Parallel	RU-28	4 MHz BW, 20 ns $\overline{\text{WR}}$ pulse width
AD5555	14	2	$\pm 1$	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	$\pm 1$	Parallel	RU-38	4 MHz BW, 20 ns $\overline{\text{WR}}$ pulse width
AD5543	16	1	$\pm 2$	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	$\pm 2$	Parallel	RU-28	4 MHz BW, 20 ns $\overline{\text{WR}}$ pulse width
AD5545	16	2	$\pm 2$	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	$\pm 2$	Parallel	RU-38	4 MHz BW, 20 ns $\overline{\text{WR}}$ pulse width

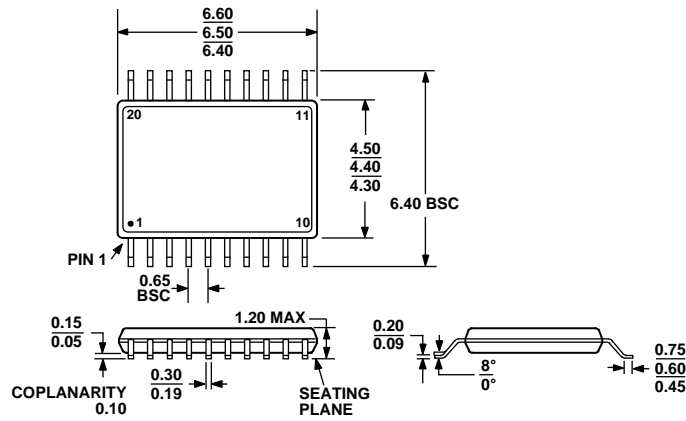
# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 58. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

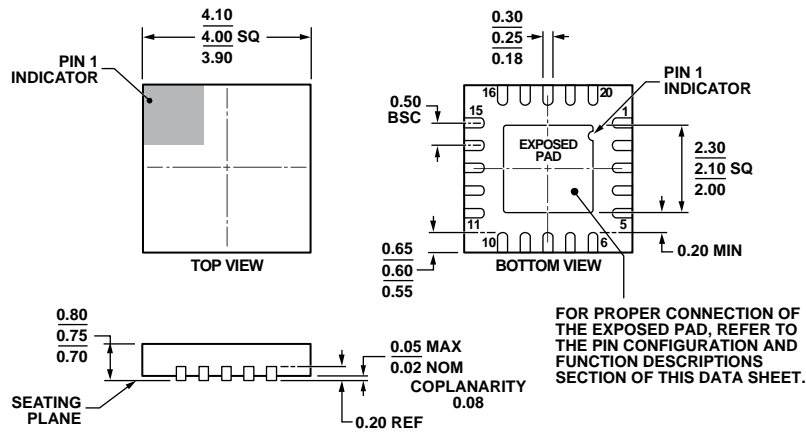


COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 59. 20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

Dimensions shown in millimeters





COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 60. 20-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 4 mm × 4 mm Body, Very Thin Quad  
 (CP-20-6)  
 Dimensions shown in millimeters

0816-2010-B

**ORDERING GUIDE**

Model <sup>1</sup>	Resolution (Bits)	INL (LSB)	Temperature Range	Package Description	Package Option
AD5424YRU	8	±0.25	-40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ	8	±0.25	-40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ-REEL	8	±0.25	-40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ-REEL7	8	±0.25	-40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YCPZ	8	±0.25	-40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5424YCPZ-REEL7	8	±0.25	-40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5433YRU	10	±0.5	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ	10	±0.5	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ-REEL	10	±0.5	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ-REEL7	10	±0.5	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YCPZ	10	±0.5	-40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5445YRU	12	±1	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ	12	±1	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ-REEL	12	±1	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ-REEL7	12	±1	-40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YCPZ	12	±1	-40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
EVAL-AD5445SDZ				Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

NOTES