I/Os Per Package[1]

ProASIC3E Devices	A3PE600		A3PE1500 [3]		A3PE3000 [3]	
ARM-Enabled ProASIC3E Devices	M7A3PE600		M7A3PE1500		M7A3PE3000	
	I/O Types					
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
PQ208	147	65	147	65	147	65
FG256	165	79	–	–	–	–
FG484	270	135	280	139	280	136
FG676	–	–	444	222	–	–
FG896	–	–	–	–	616	300

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to "Package Pin Assignments" starting on page 4-1 to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (V_{REF}) per minibank (group of I/Os).Refer to the "I/O Banks and I/O Standards Compatibility" section on page 2-28 for more information about V_{REF} and the use of minibanks*
6. *"G" indicates RoHS-compliant packages. Refer to the "ProASIC3E Ordering Information" on page iii for the location of the "G" in the part number.*

Packaging Tables

Pinout tables not published in this document will be added in future revisions of the datasheet. For updates, contact our local sales office.

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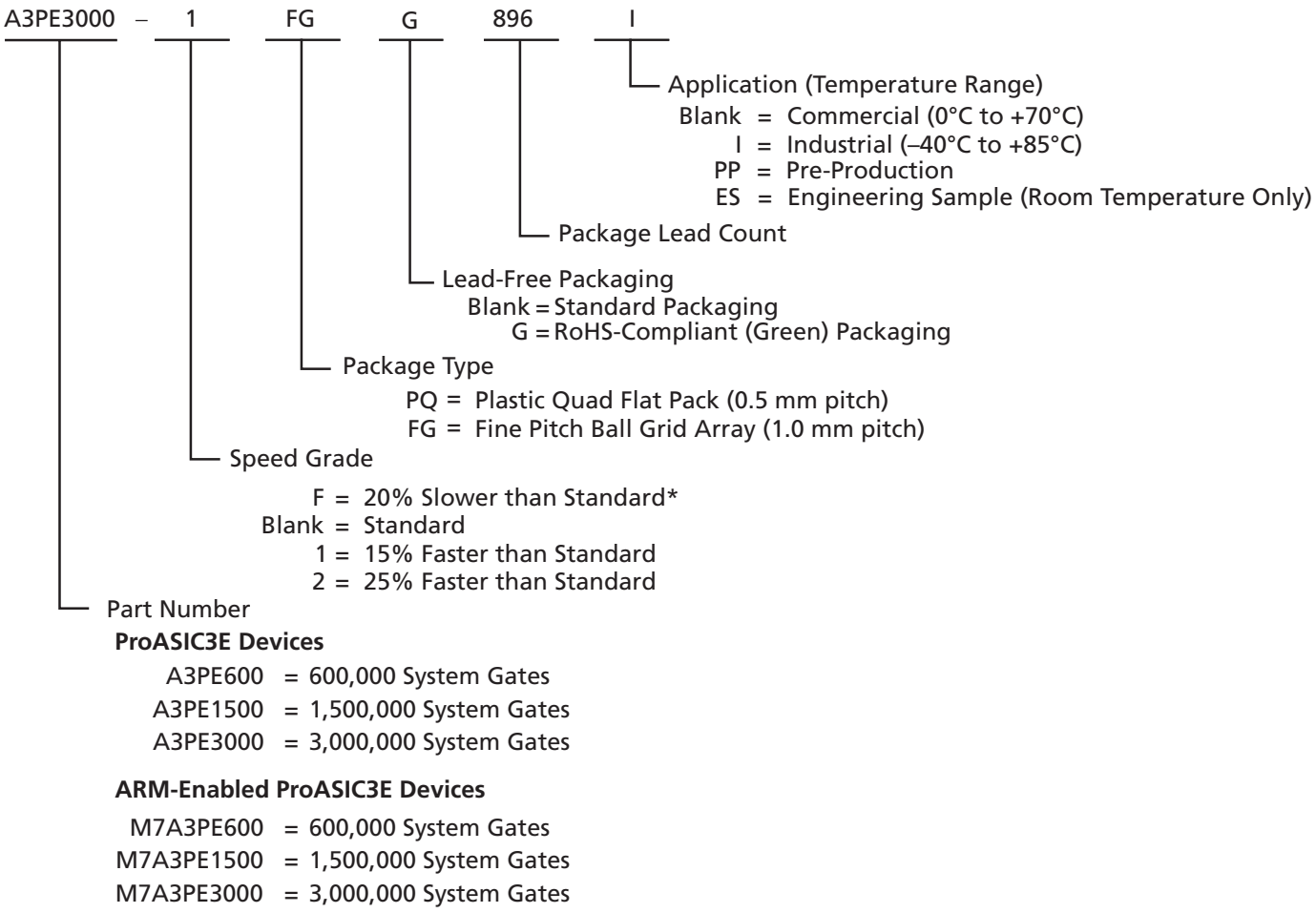
ProASIC3E Ordering Information



ProASIC3E Devices

A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ARM-Enabled ProASIC3E Devices

M7A3PE600 = 600,000 System Gates
M7A3PE1500 = 1,500,000 System Gates
M7A3PE3000 = 3,000,000 System Gates

Note: **The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*

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Temperature Grade Offerings

Package	A3PE600 M7A3PE600	A3PE1500 M7A3PE1500	A3PE3000 M7A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: *C = Commercial temperature range: 0°C to 70°C*
I = Industrial temperature range: –40°C to 85°C

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.	–1	–2
C[2]	✓	✓	✓	✓
I[3]	–	✓	✓	✓

Notes:

1. *The DC and switching characteristics for the –F speed grade targets are based only on simulation.*
   The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.
2. *C = Commercial temperature range: 0°C to 70°C*
3. *I = Industrial temperature range: –40°C to 85°C*

Datasheet references made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M7.

Contact your local Actel representative for device availability (http://www.actel.com/contact/default.aspx).

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Introduction and Overview

General Description

ProASIC3E, the third-generation family of Actel Flash FPGAs, offers performance, density, and features beyond those of the ProASIC[PLUS]® family. Nonvolatile Flash technology gives ProASIC3E devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 616 user I/Os.

All ProASIC3E devices support the ARM7 soft IP core, and the ARM-enabled devices have Actel ordering numbers that begin with M7A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based ProASIC3E devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Security

The nonvolatile, Flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile Flash programming can offer.

ProASIC3E devices utilize a 128-bit Flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3E device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An ProASIC3E device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based ProASIC3E FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

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Live at Power-Up

The Actel Flash-based ProASIC3E devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASIC3E devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3E device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3E devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

"I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3E Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of ProASIC3E FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3E devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3E devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3E family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate Flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3E devices via an IEEE 1532 JTAG interface.

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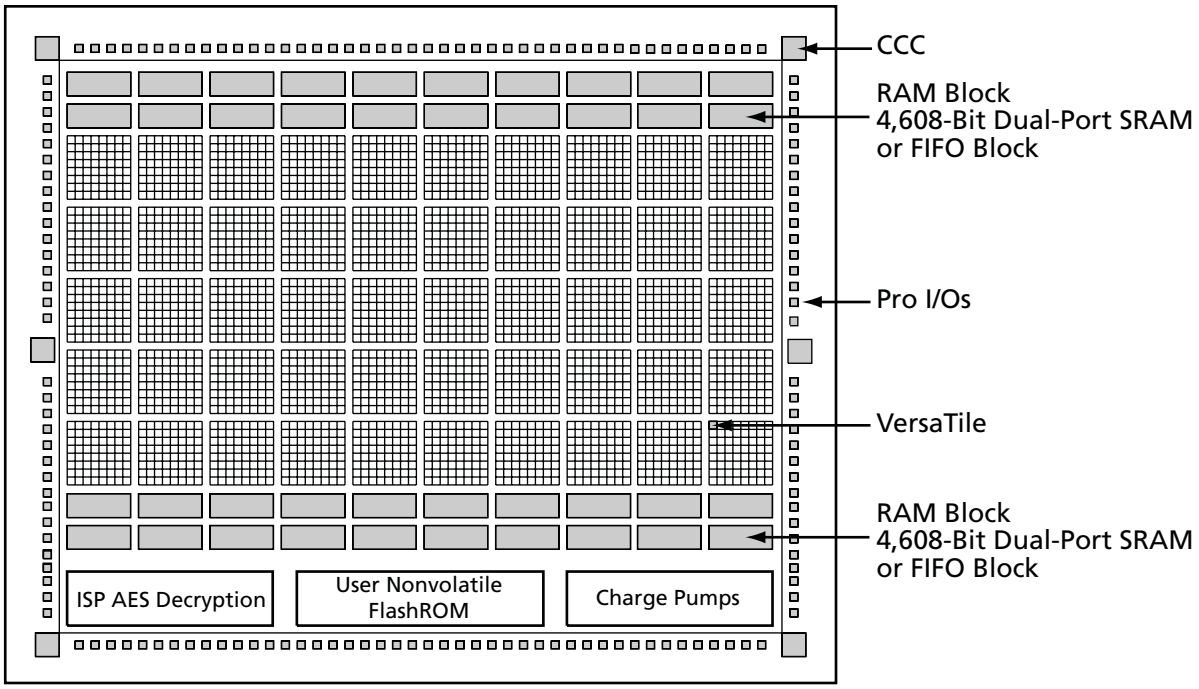

Figure 1-1 • **ProASIC3E Device Architecture Overview**

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

For more information about VersaTiles, refer to the "VersaTile" section on page 2-2.

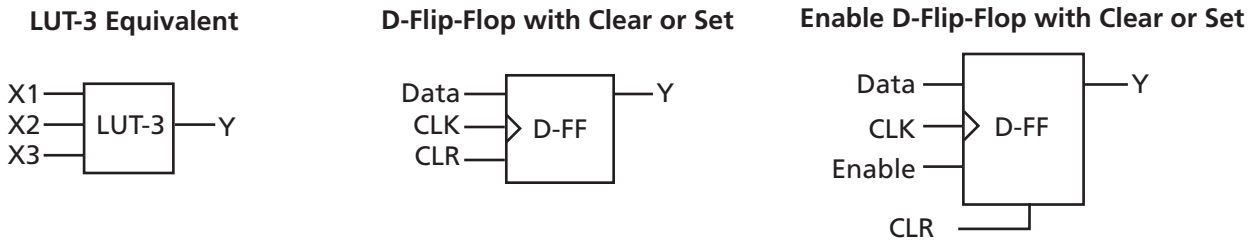

Figure 1-2 • **VersaTile Configurations**

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User Nonvolatile FlashROM

Actel ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3E development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access (refer to the "Clock Conditioning Circuits" section on page 2-13 for more information).

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns

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- 2 programmable delay types for clock skew minimization; refer to Figure 2-16 on page 2-17, Table 2-4 on page 2-18, and the "Features Supported on Every I/O" section on page 2-31 for more information.
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC})

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks (Figure 2-9 on page 2-9). The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. For more information, see Table 2-23 on page 2-49.

The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see Table 2-14 on page 2-30 for more information). Each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers (Figure 2-24 on page 2-33). These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, BLVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II). See the "DDR Module Specifications" section on page 3-56.

ProASIC3E banks support M-LVDS with 20 multi-drop points.

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Related Documents

Application Notes

ProASIC3/E I/O Usage Guide
http://www.actel.com/documents/PA3_E_IO_AN.pdf
In-System Programming (ISP) in ProASIC3/E Using FlashPro3
http://www.actel.com/documents/PA3_E_ISP_AN.pdf
ProASIC3/E FlashROM
http://www.actel.com/documents/PA3_E_FROM_AN.pdf
ProASIC3/E Security
http://www.actel.com/documents/PA3_E_Security_AN.pdf
ProASIC3/E SRAM/FIFO Blocks
http://www.actel.com/documents/PA3_E_SRAMFIFO_AN.pdf
Programming a ProASIC3/E Using a Microprocessor
http://www.actel.com/documents/PA3_E_Microprocessor_AN.pdf
UJTAG Applications in ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_UJTAG_AN.pdf
Using DDR for ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_DDR_AN.pdf
Using Global Resources in Actel ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_Global_AN.pdf
Power-Up/Down Behavior of ProASIC3/E Devices
http://www.actel.com/documents/ProASIC3_E_PowerUp_AN.pdf

For additional ProASIC3E application notes, go to http://www.actel.com/techdocs/an.aspx.

User's Guides

SmartGen Cores Reference Guide
http://www.actel.com/documents/genguide_ug.pdf
Designer User's Guide
http://www.actel.com/documents/designer_ug.pdf
ProASIC3/E Macro Library Guide
http://www.actel.com/documents/pa3_libguide_ug.pdf

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Device Architecture

Introduction

Flash Technology

Advanced Flash Switch

Unlike SRAM FPGAs, the ProASIC3E family uses a live at power-up ISP Flash switch as its programming element. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable programming to connect signal lines to the appropriate VersaTile inputs and outputs. In the Flash switch, two transistors share the floating gate, which stores the programming information (Figure 2-1). One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure VersaTile logic. It is also used to erase the floating gate. Dedicated high-performance lines are connected as required using the Flash switch for fast, low-skew, global signal distribution throughout the device core. Maximum core utilization is possible for virtually any design. The use of the Flash switch technology also removes the possibility of firm errors, which are increasingly common in SRAM-based FPGAs.

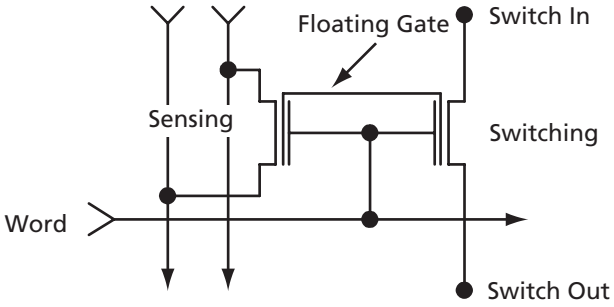

Figure 2-1 • **ProASIC3E Flash-Based Switch**

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Device Overview

The ProASIC3E device family consists of five distinct programmable architectural features (Figure 2-2):

- FPGA fabric/core (VersaTiles)
- Routing and clock resources (VersaNets)
- FlashROM
- Dedicated SRAM/FIFO memory
- Pro I/O structure

Core Architecture

VersaTile

The proprietary ProASIC3E family architecture provides granularity comparable to gate arrays. The ProASIC3E device core consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 2-3 on page 2-3, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate Flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a fourth input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions can be connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, SET/CLR is supported by a fourth input. The SET/CLR signal can only be routed to this fourth input over the VersaNet (global) network. However, if in the user's design the SET/CLR signal is not routed over the VersaNet network, a compile warning message will be given and the intended logic function will be implemented by two VersaTiles instead of one.

The output of the VersaTile is F2 (Figure 2-3 on page 2-3) when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources.

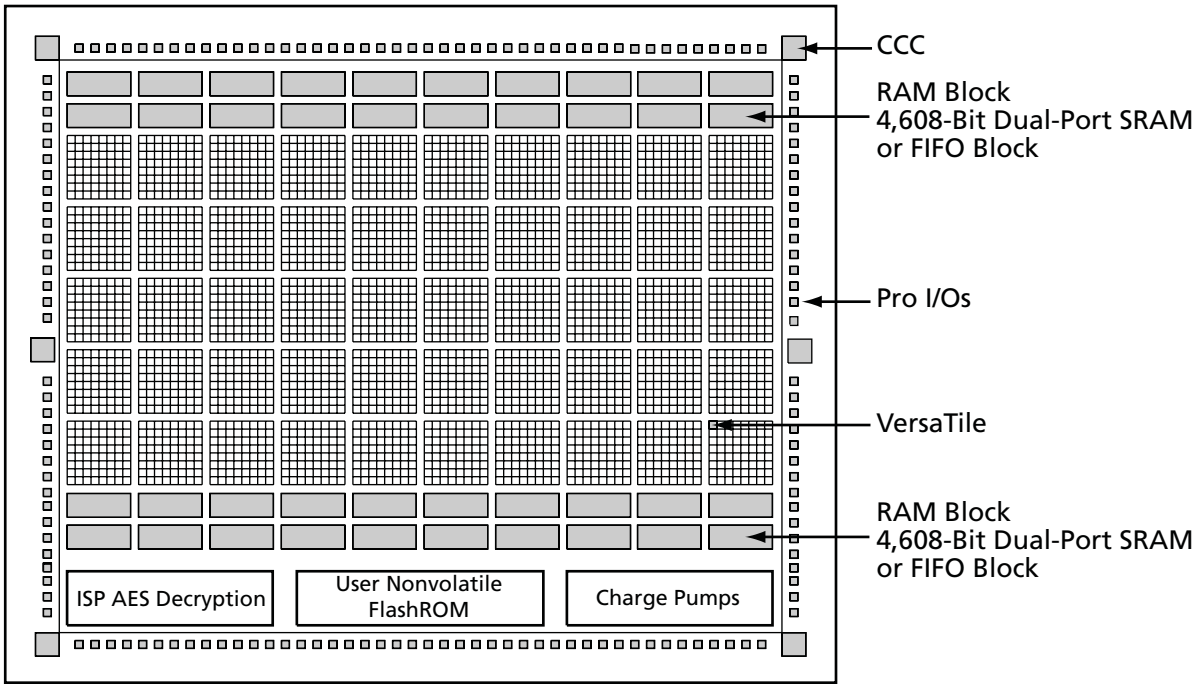

Figure 2-2 • **ProASIC3E Device Architecture Overview**

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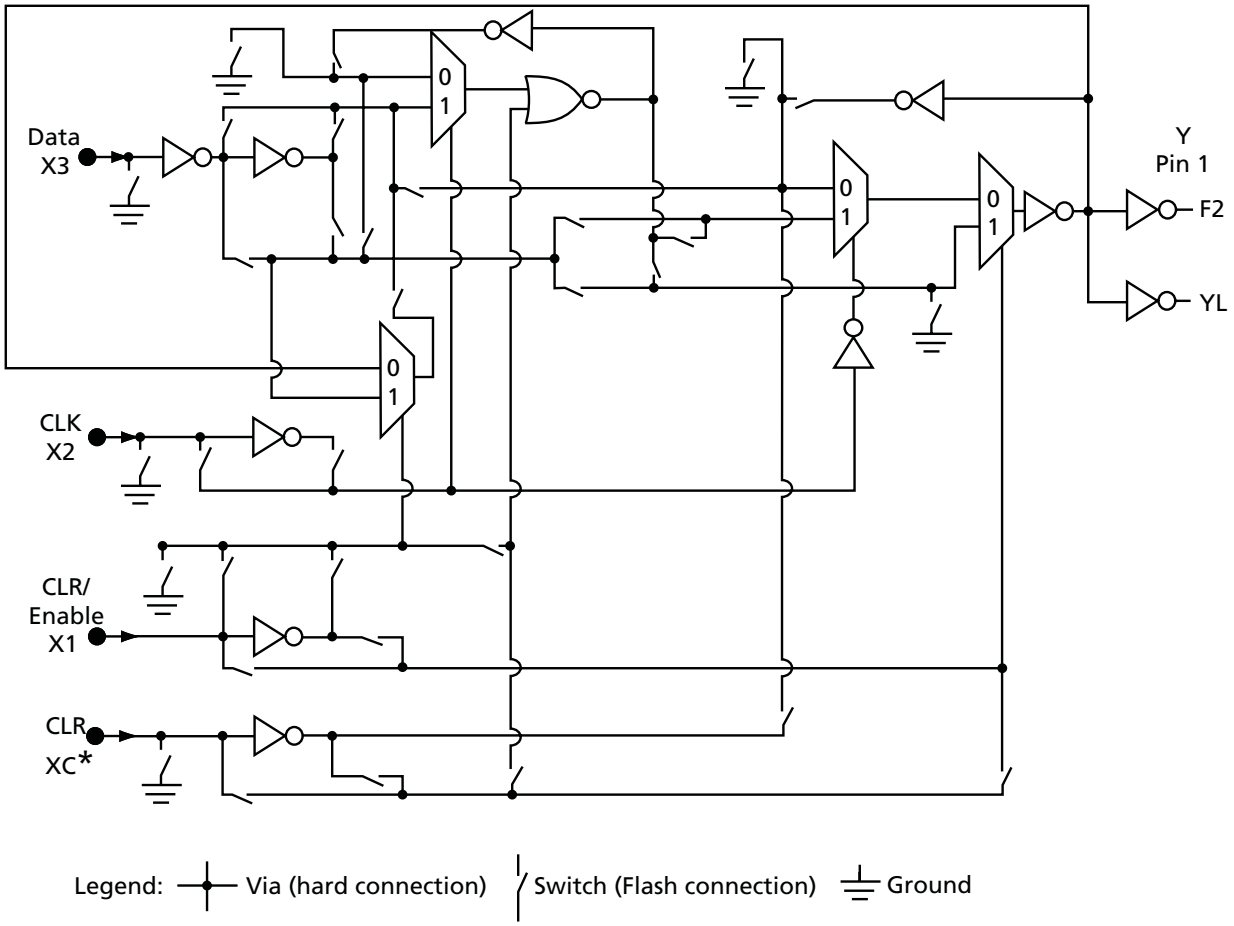

Note: **This input can only be connected to the global clock distribution network.*

Figure 2-3 • **ProASIC3E Core VersaTile**

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Array Coordinates

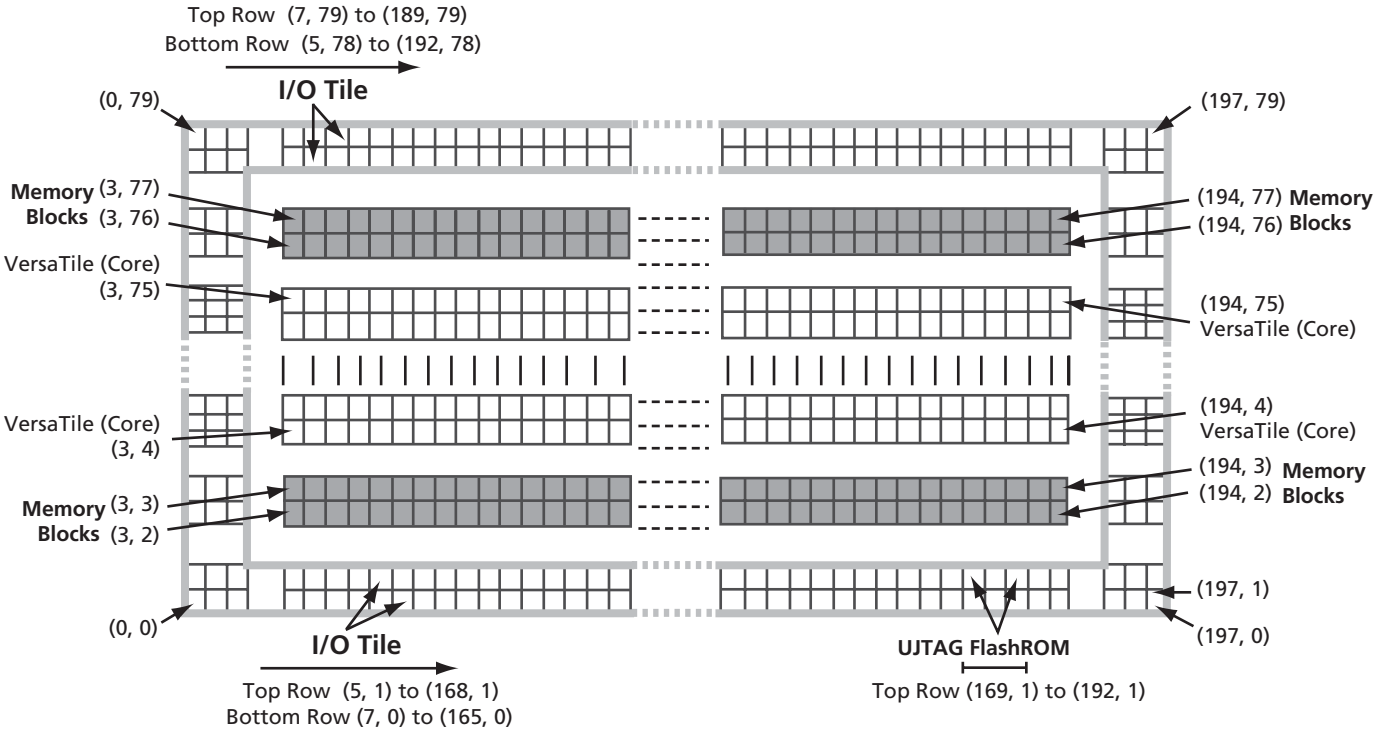
During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-1 provides array coordinates of core cells and memory blocks. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-1. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-4 illustrates the array coordinates of an A3PE600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for ProASIC3E software tools.

Table 2-1 • **ProASIC3E Array Coordinates**

	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
Device	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
A3PE600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
A3PE1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 127)
A3PE3000	3	6	450	173	(3, 2) or (3, 4)	(3, 174) or (3, 176)	(0, 0)	(453, 179)



Note: *The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

Figure 2-4 • **Array Coordinates for A3PE600**

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Routing Architecture

Routing Resources

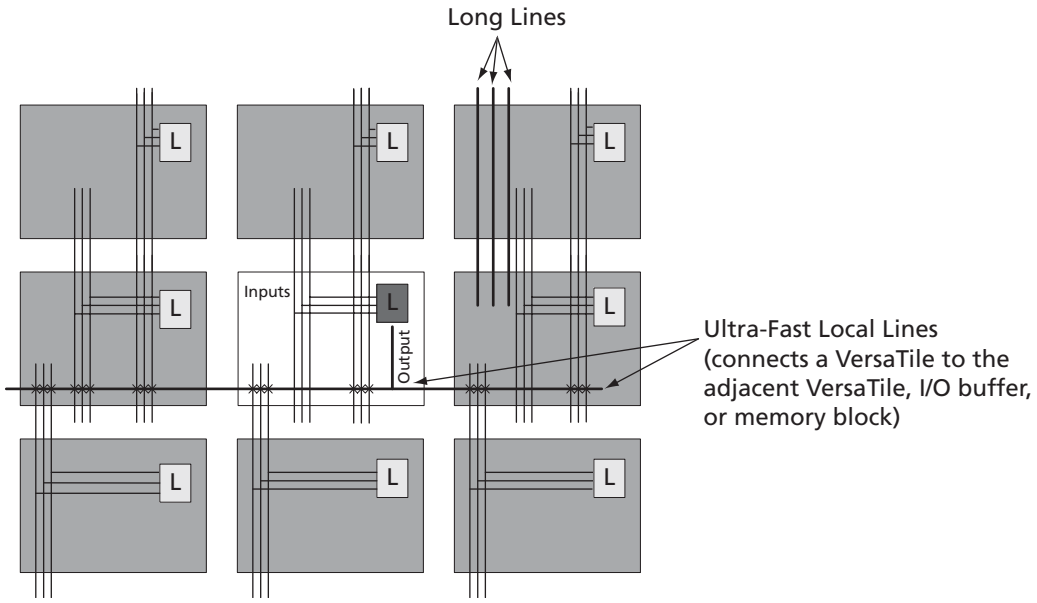
The routing structure of ProASIC3E devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very-long-line resources, and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-5). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaTile global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire ProASIC3E device (Figure 2-6 on page 2-6). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length +/–12 VersaTiles in the vertical direction and length +/–16 in the horizontal direction from a given core VersaTile (Figure 2-7 on page 2-7). Very long lines in ProASIC3E devices have been enhanced over those in previous ProASIC families. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-8 on page 2-8). These nets are typically used to distribute clocks, resets, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: *Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.*

Figure 2-5 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

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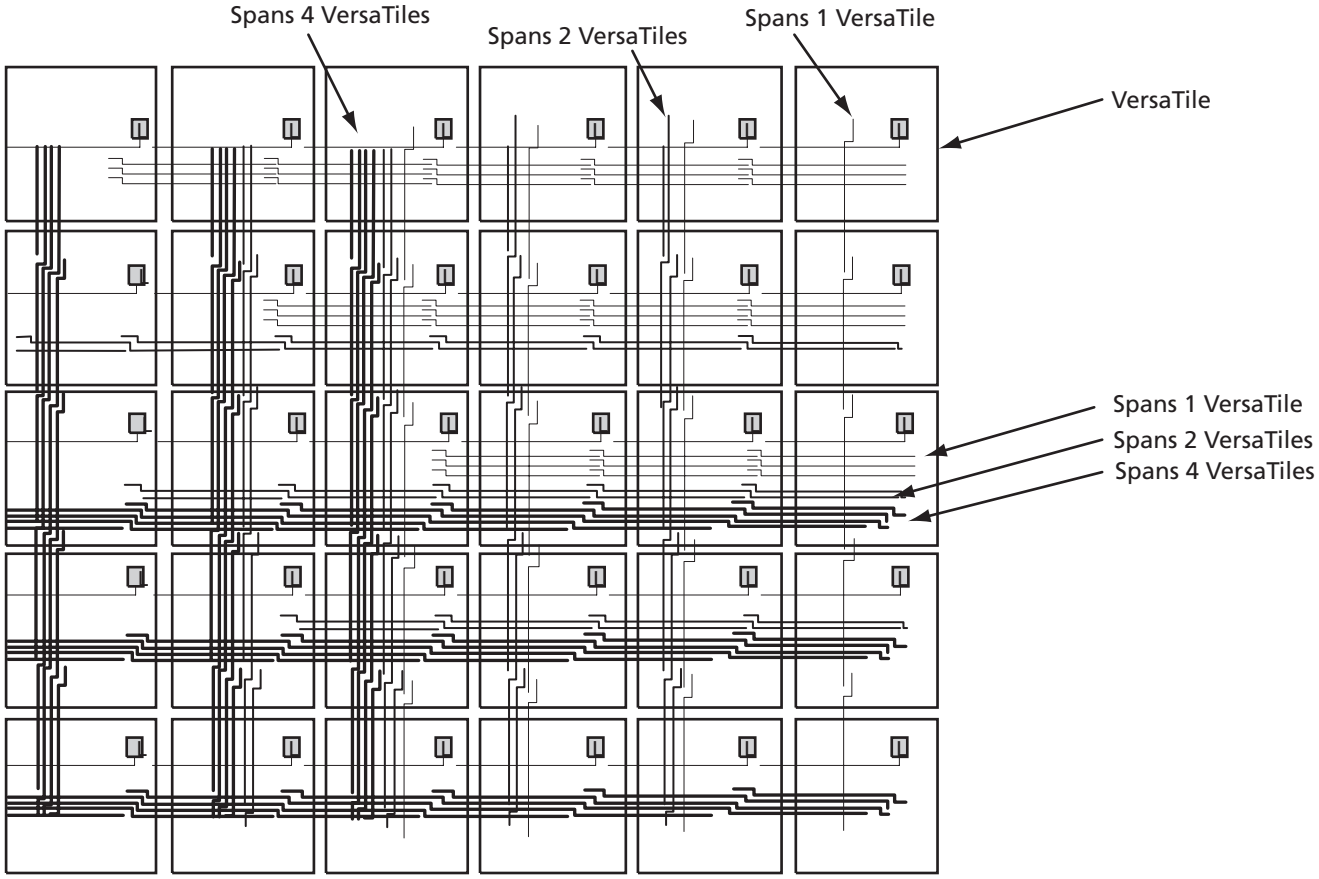

Figure 2-6 • **Efficient Long-Line Resources**

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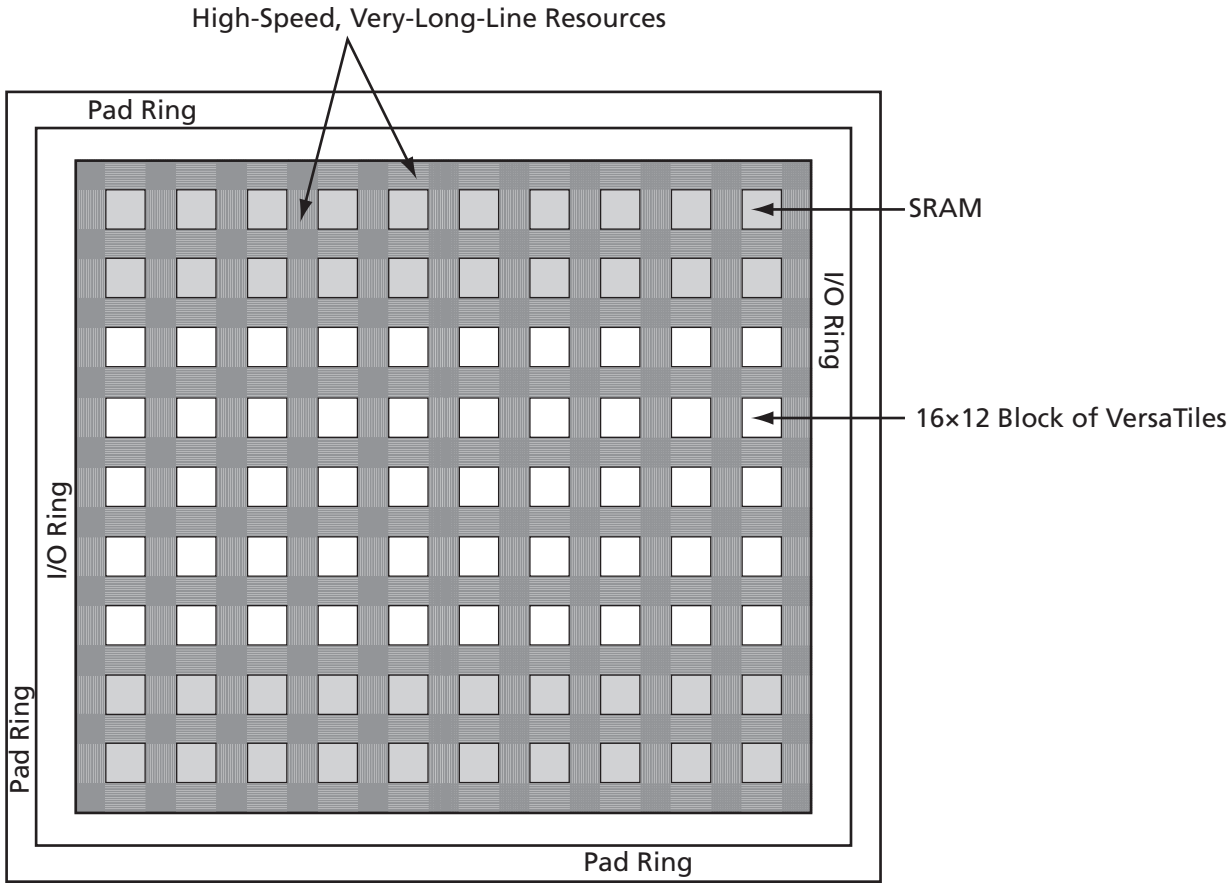

Figure 2-7 • **Very-Long-Line Resources**

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Clock Resources (VersaNets)

ProASIC3E devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs containing a phase-locked loop (PLL) core, delay lines, a phase shifter (0°, 90°, 180°, 270°), clock multipliers/dividers, and all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six total lines). The CCCs at the four corners each have access to three quadrant global lines in each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of ProASIC3E is the set of powerful and low-delay VersaNet global networks. ProASIC3E offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-8). In addition, ProASIC3E devices have three regional globals in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks, and a total of 18 globals on the device. Each of these networks contains spines and ribs that reach all the VersaTiles in the quadrants (Figure 2-9 on page 2-9). This flexible VersaNet global network architecture allows users to map up to 252 different internal/external clocks in a ProASIC3E device. Details on the VersaNet networks are given in Table 2-2 on page 2-9. The flexible use of the ProASIC3E VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

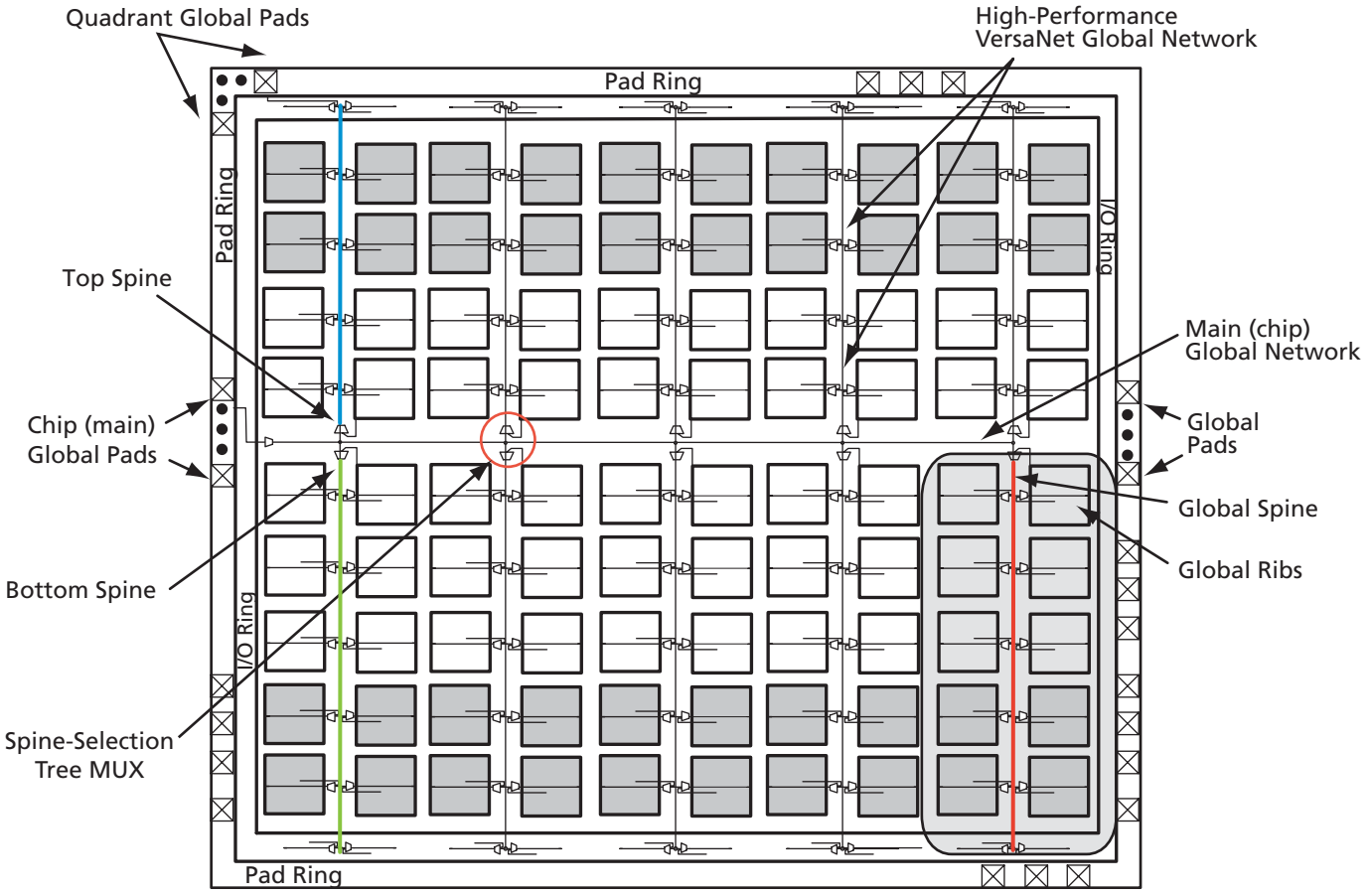

Figure 2-8 • **Overview of ProASIC3E VersaNet Global Network**

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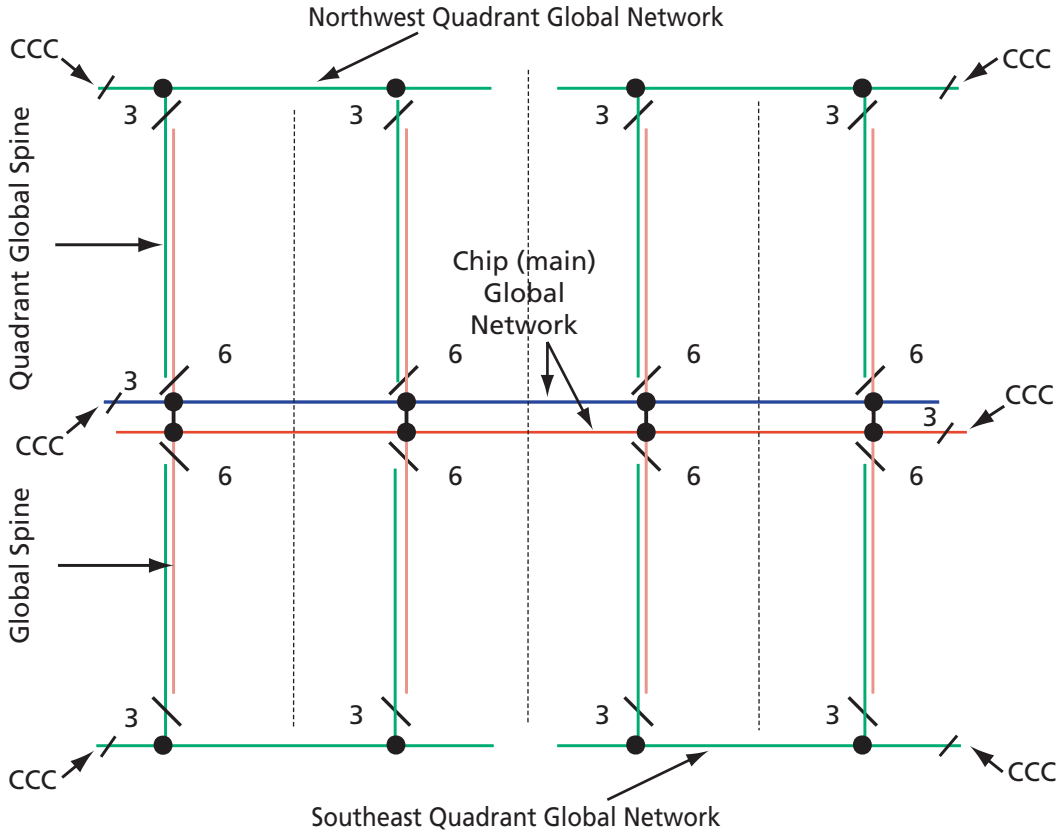

Figure 2-9 • **Global Network Architecture**

Table 2-2 • **ProASIC3E Globals/Spines/Rows by Device**

	A3PE600	A3PE1500	A3PE3000
Global Clock Networks (Trees)*	9	9	9
Clock Spines/Trees	12	20	28
Total Spines	108	180	252
VersaTiles in Each Top or Bottom Spine	1,120	1,888	2,656
Total VersaTiles	13,824	38,400	75,264
Rows in Each Top or Bottom Spine	36	60	84

Note: **There are six chip (main) globals and three globals per quadrant.*

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VersaNet Global Networks and Spine Access

The ProASIC3E architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles of the ProASIC3E device. There are nine global network resources in each device quadrant: three quadrant globals and six chip (main) global networks. Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 252 internal/external clocks (in an A3PE3000 device) or other high-fanout nets in ProASIC3E devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on ProASIC3E devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-9 on page 2-9).

The spines are the vertical branches of the global network tree, shown in Figure 2-10 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the ProASIC3E device (the "scope" of the spine; see Figure 2-8 on page 2-8). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or by another net defined by the user (Figure 2-11 on page 2-12). Quadrant spines can be driven from user I/Os on the north and south sides of the die. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-11 on page 2-12. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device.

For details on using spines in ProASIC3E devices, see the Actel application note *Using Global Resources in Actel ProASIC3/E Devices*.

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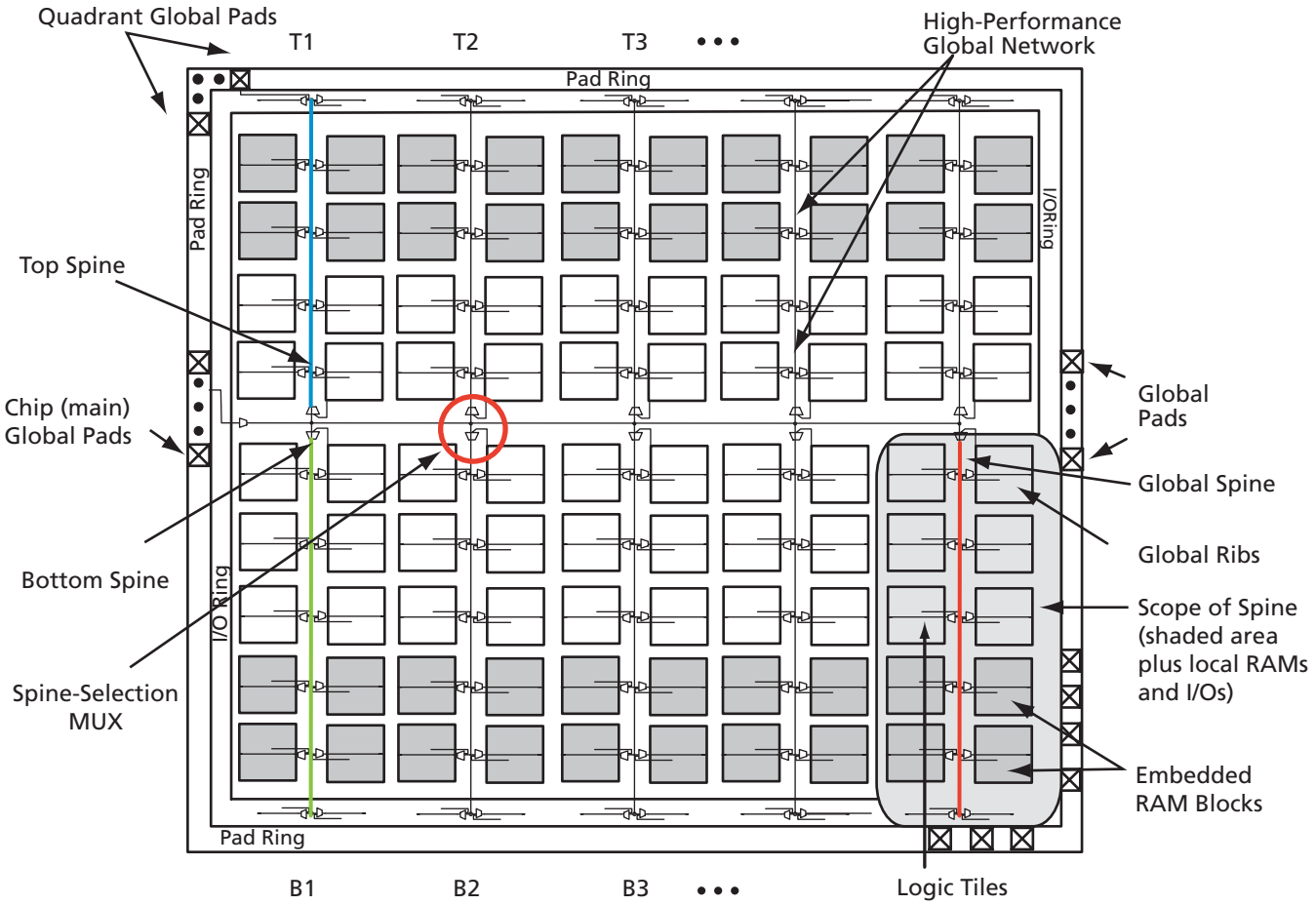

Figure 2-10 • **ProASIC3E Spines in a Global Clock Tree Network**

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Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-12 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel ProASIC3/E Devices* application note.

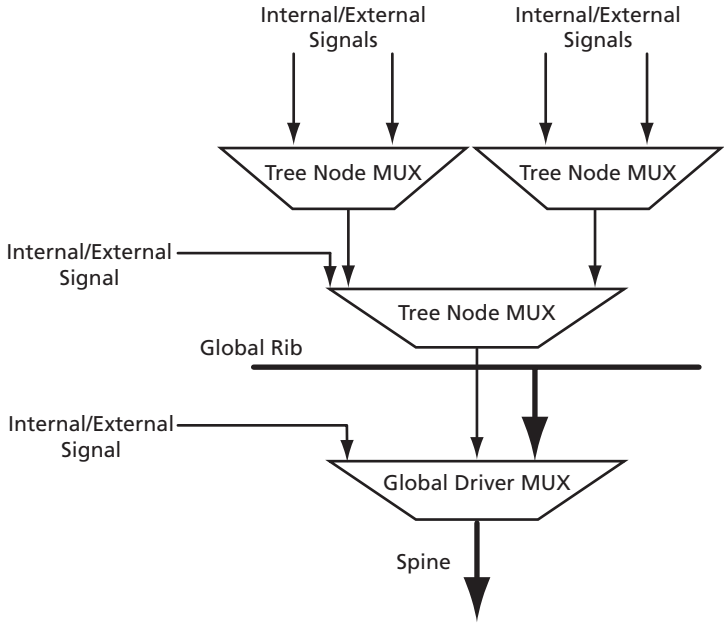

Figure 2-11 • **Spine Selection MUX of Global Tree**

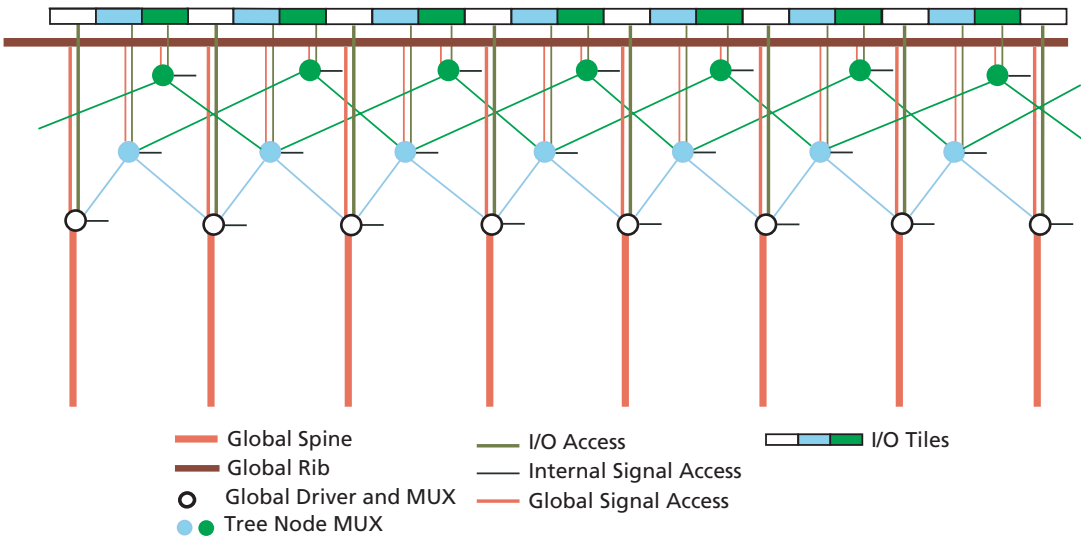

Figure 2-12 • **Clock Aggregation Tree Architecture**

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Clock Conditioning Circuits

Overview of Clock Conditioning Circuitry

In ProASIC3E devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, or CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and optionally the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-13 on page 2-14). Refer to the "PLL Macro" section on page 2-15 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via Flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the ProASIC3E device to permit parameter changes (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in Flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note and the "CCC Electrical Specifications" section on page 2-18 for more information.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS macros are composite macros that include an I/O macro driving a global buffer, which uses a hardwired connection.

The CLKBUF, CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

The CLKINT macro provides a global buffer function driven by the FPGA core.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by ProASIC3E devices. The available CLKBUF macros are described in the *ProASIC3/E Macro Library Guide*.

Global Buffer with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay. The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the ProASIC3E family. The available INBUF macros are described in the *ProASIC3/E Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

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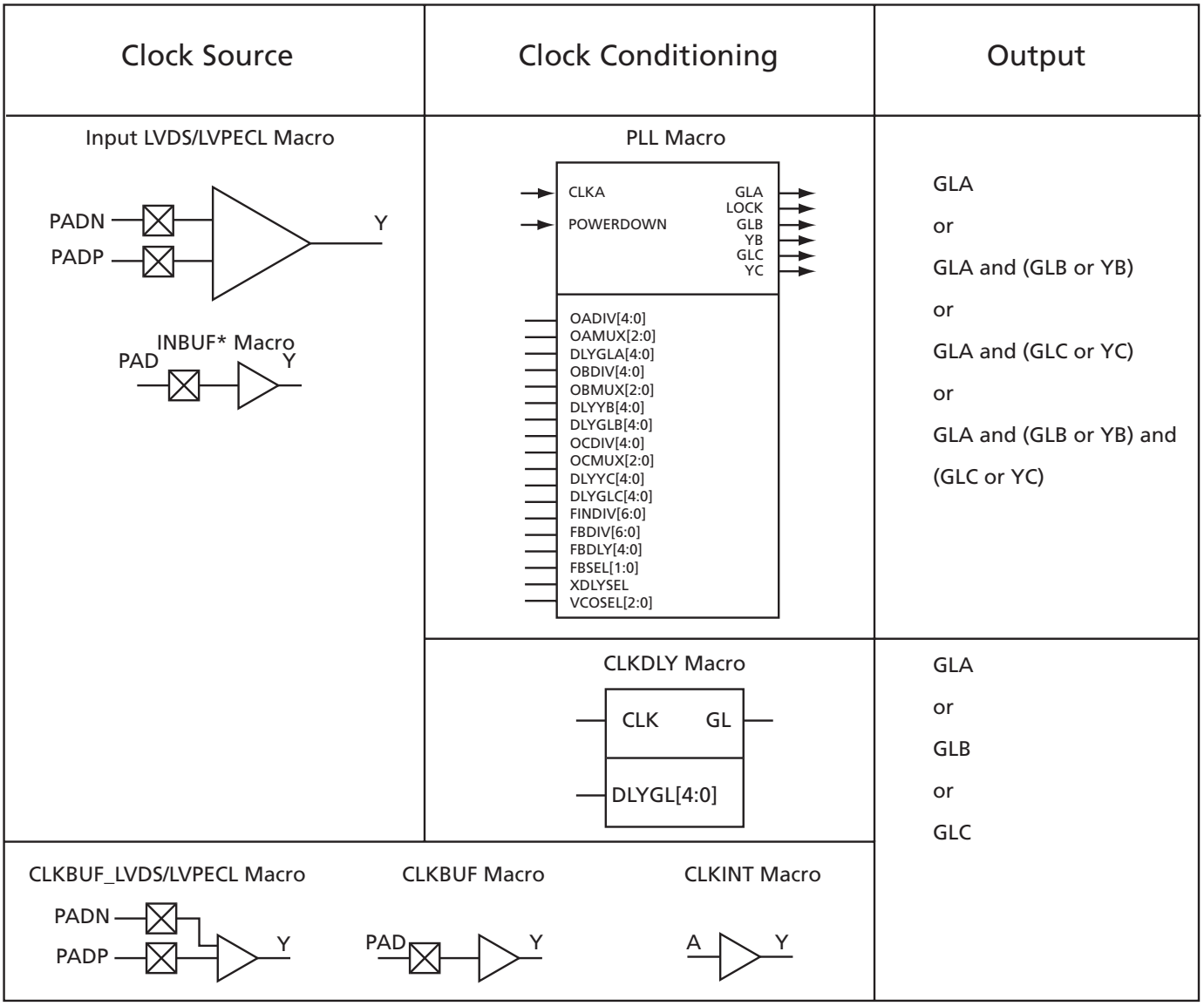

Notes:

1. *Visit the Actel website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-15 for signal descriptions.*
2. *Refer to the ProASIC3/E Macro Library Guide for more information.*
3. *Many standard-specific INBUF macros (for example, INBUF_LVDS) support the wide variety of single-ended and differential I/O standards supported by the ProASIC3E family. The available INBUF macros are described in the ProASIC3/E Macro Library Guide.*

Figure 2-13 • **ProASIC3E CCC Options**

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PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[0:2] package pins. Refer to Figure 2-14 on page 2-16 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL macro also provides power-down input and lock output signals. See Figure 2-16 on page 2-17 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is Powerdown On (active low).

Outputs:

- LOCK: indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-19 on page 2-19 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global network access, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

During power-up, the PLL outputs will toggle around the maximum frequency of the VCO gear selected. Toggle frequencies can range from 40 Mhz to 350 Mhz. This will continue as long as the clock input (CLKA) is constant (high or low). This can be prevented by LOW assertion of the POWERDOWN signal.

The visual PLL configuration in SmartGen, part of the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen also allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select the input clock source. SmartGen automatically instantiates the special macro, PLLINT, when needed.

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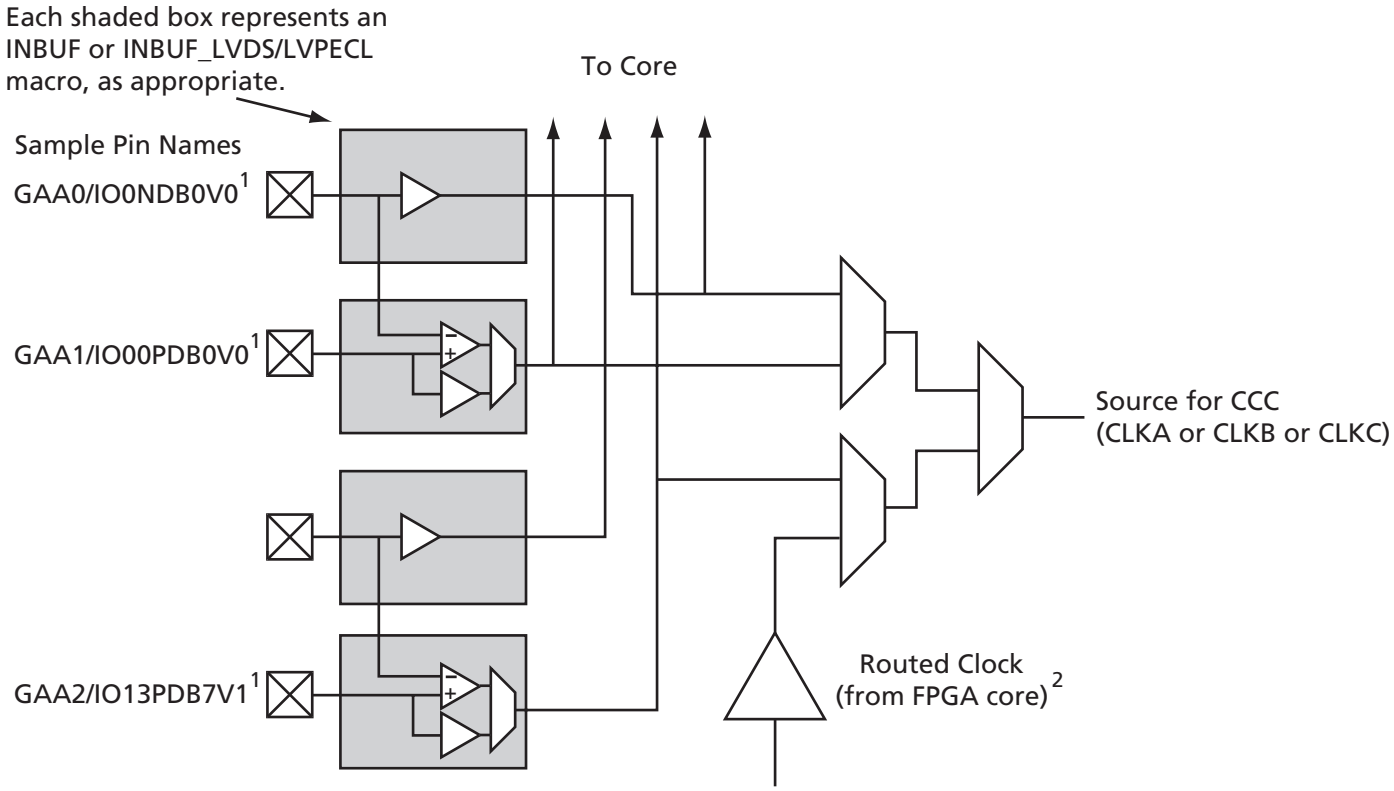

Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-50 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of a PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS/BLVDS/M-LVDS/DDR) in a relevant global pin location.
3.

Figure 2-14 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

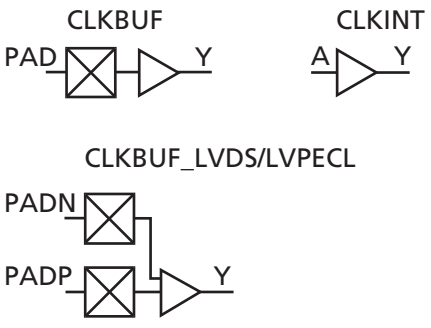

Figure 2-15 • **CLKBUF and CLKINT**

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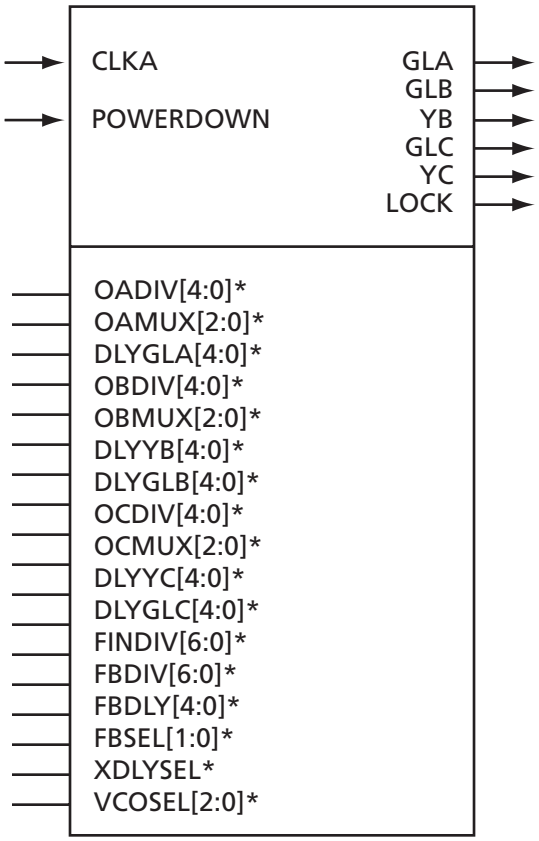
Table 2-3 • **Available ProASIC3E I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS25
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_PCIX
CLKBUF_GTL25
CLKBUF_GTL33
CLKBUF_GTLP25
CLKBUF_GTLP33
CLKBUF_HSTL_I
CLKBUF_HSTL_II
CLKBUF_SSTL3_I
CLKBUF_SSTL3_II
CLKBUF_SSTL2_I
CLKBUF_SSTL2_II
CLKBUF_LVDS[2]
CLKBUF_LVPECL

Notes:

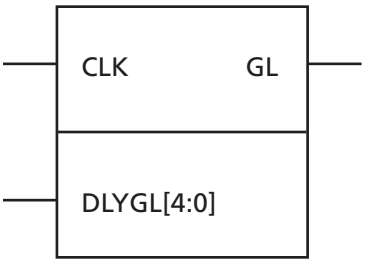
1. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology. For more details, refer to the ProASIC3/E Macro Library Guide.*
2. *BLVDS and M-LVDS standards are supported by CLKBUF_LVDS.*



Note: **Visit the Actel website for future application notes concerning the dynamic PLL.*

Figure 2-16 • **CCC/PLL Macro**

CLKDLY



Note: *The CLKDLY macro uses programmable delay element type 2.*

Figure 2-17 • **CLKDLY**

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CCC Electrical Specifications

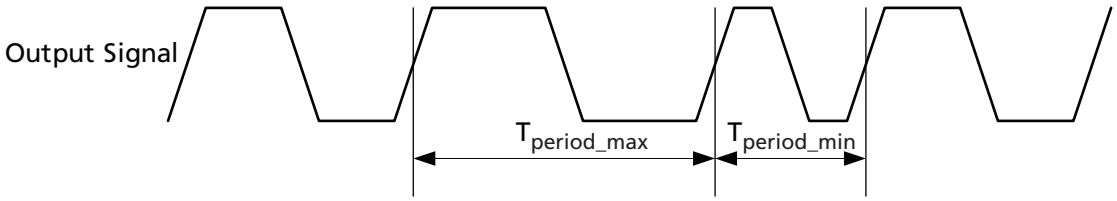
Timing Characteristics

Table 2-4 • **ProASIC3E CCC/PLL Specification**

Parameter		Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		350	MHz
Delay Increments in Programmable Delay Blocks1, 2			160		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter FCCC_OUT		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		0.50%		0.70%	
24 MHz to 100 MHz		1.00%		1.20%	
100 MHz to 250 MHz		1.75%		2.00%	
250 MHz to 350 MHz		2.50%		5.60%	
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter[3]	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1[1, 2]		0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[1, 2]		0.025		5.56	ns
Delay Range in Block: Fixed Delay[1, 2]			2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-6 on page 3-4 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V.*
3. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*



Note: *Peak-to-peak jitter measurements are defined by Tpeak-to-peak = Tperiod_max - Tperiod_min*

Figure 2-18 • **Peak-to-Peak Jitter Definition**

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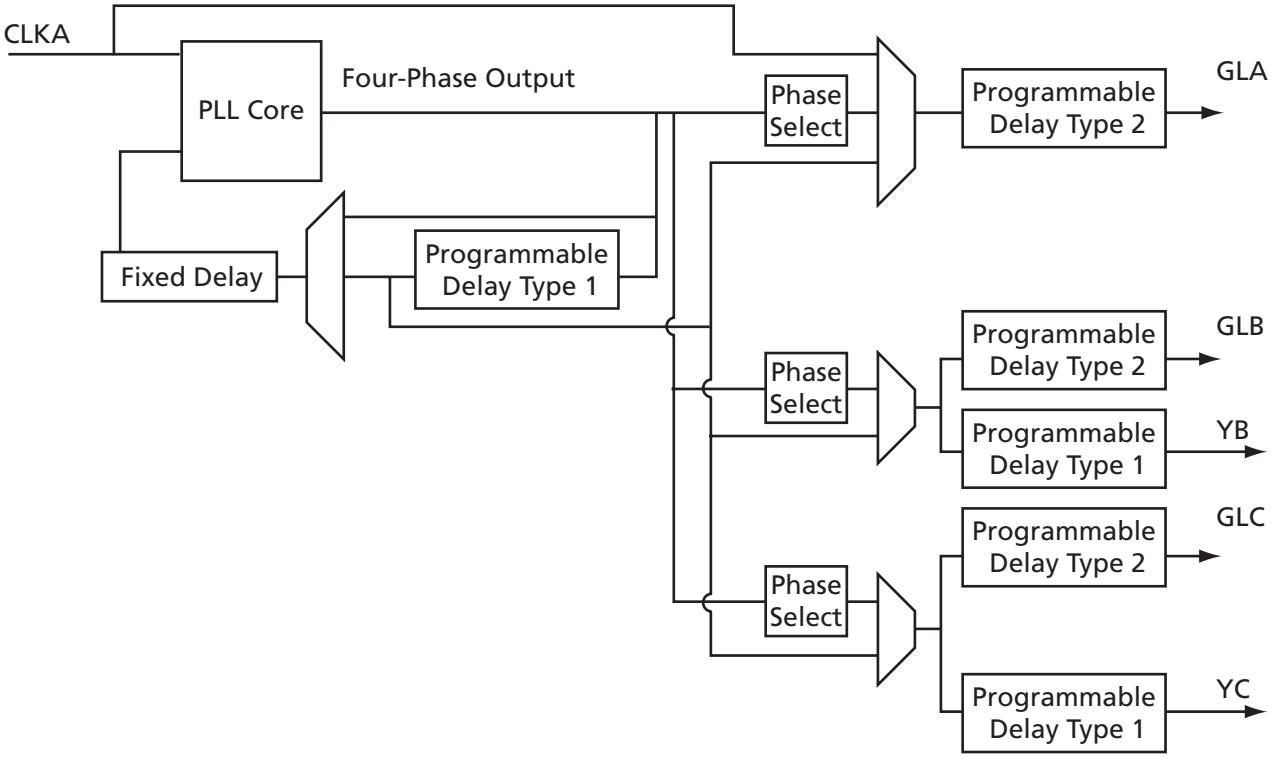
CCC Physical Implementation

The CCC is composed of the following (Figure 2-19):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay that advances/delays phase
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-19 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability

CCC Programming

The CCC block is fully configurable, either via static Flash configuration bits in the array, set by the user in the programming bitstream, or through an asynchronous dedicated shift register dynamically accessible from inside the ProASIC3E device. The dedicated shift register permits changes in parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note for more information.



Notes:

1. *Refer to the "Clock Conditioning Circuits" section on page 2-13 and Table 2-4 on page 2-18 for signal descriptions.*
2. *Clock divider and clock multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

Figure 2-19 • **PLL Block**

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Nonvolatile Memory (NVM)

Overview of User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip nonvolatile Flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the FlashROM from the FPGA core (Figure 2-20).

The FlashROM can only be programmed via the IEEE1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports synchronous read. The address is latched on the rising edge of the clock and the new output data is stable after the falling edge of the same clock cycle. Please refer to Figure 3-53 on page 3-79 for the timing diagram. The FlashROM can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

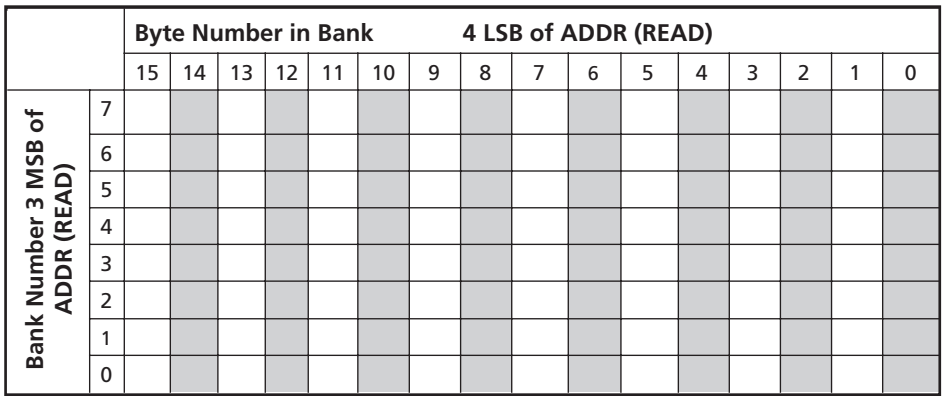

Figure 2-20 • **FlashROM Architecture**

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SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along the north and south sides of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz.

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—2 read, 2 write or 1 read, 1 write)
- 512×9, 256×18 (2-port RAM—1 read and 1 write)
- Sync write, sync pipelined / nonpipelined read

The ProASIC3E memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Block diagrams of the memory modules are illustrated in Figure 2-21 on page 2-22.

Simultaneous dual-port read/write and write/write operations at the same address are allowed when certain timing requirements are met.

During RAM operation, addresses are sourced by the user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-22 on page 2-23 for more information about the implementation of the embedded FIFO controller.

The ProASIC3E architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. For example, the write side size can be set to 256×18 and the read size to 512×9.

Both the write width and read width for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are: 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-5 on page 2-24.

When widths of one, two, or four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

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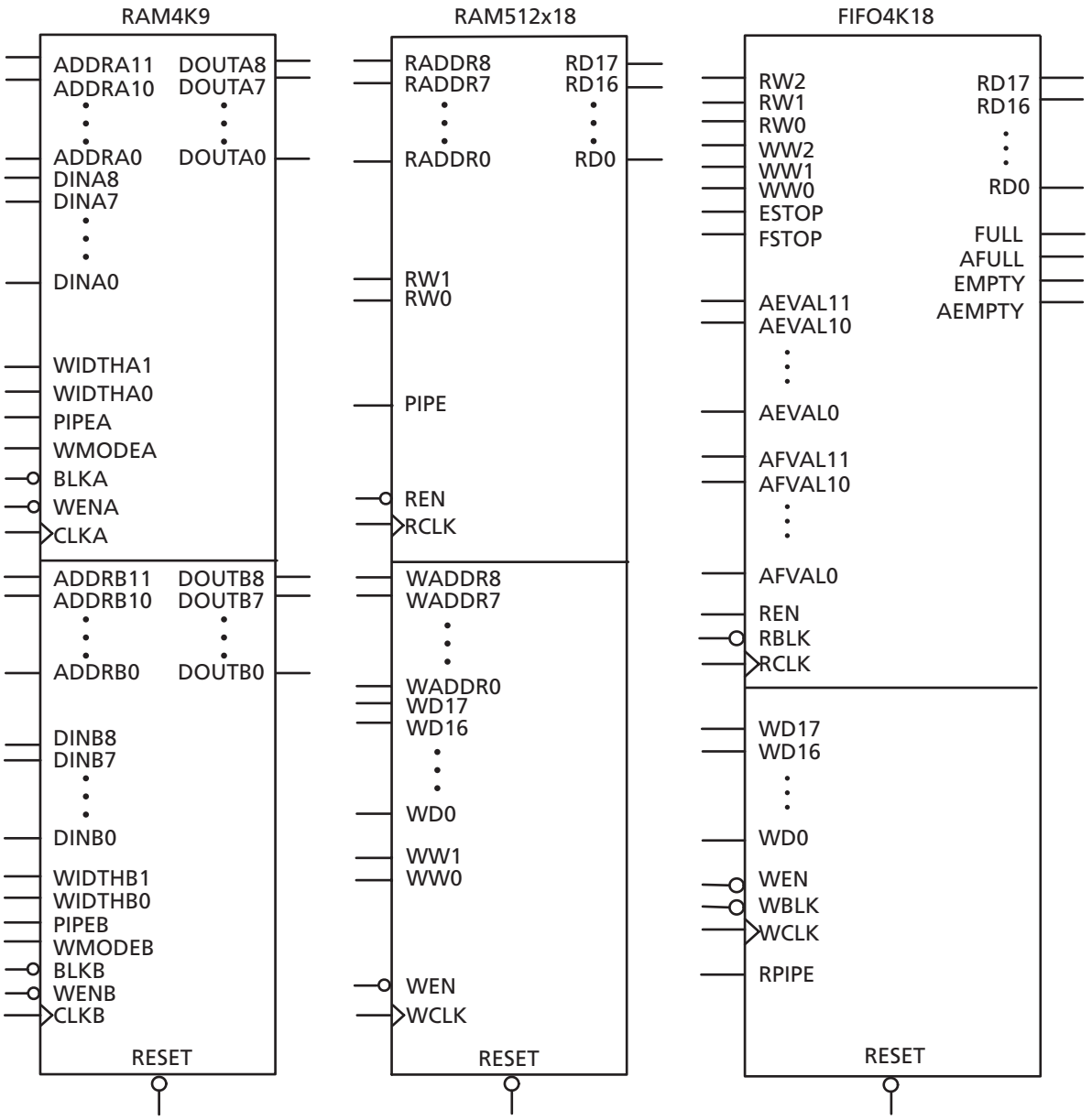

Figure 2-21 • **Supported Basic RAM Macros**

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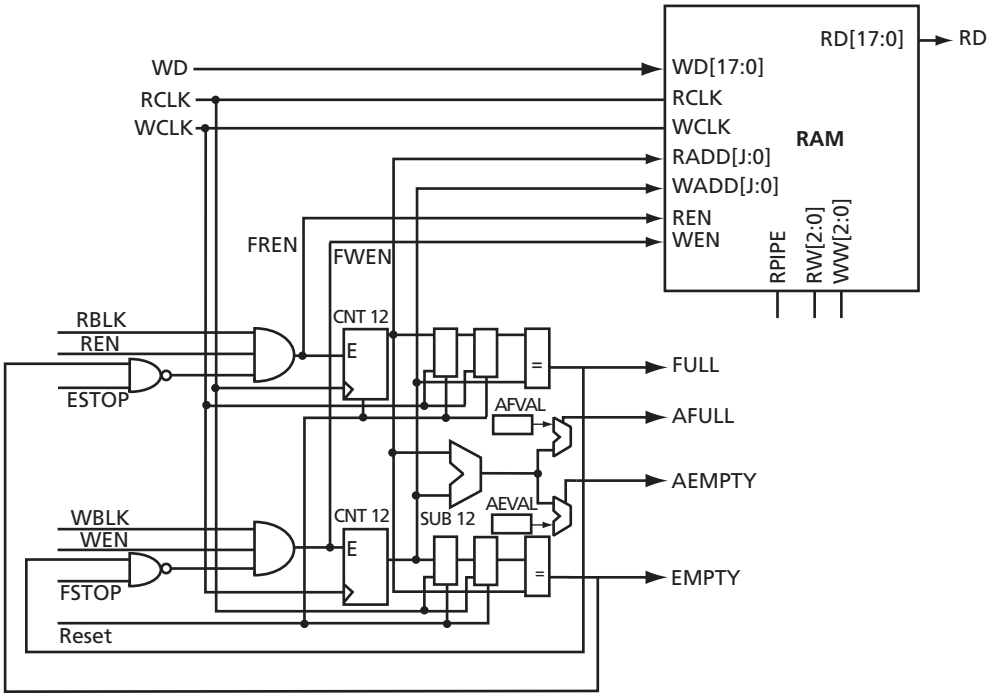

Figure 2-22 • **ProASIC3E RAM Block with Embedded FIFO Controller**

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Signal Descriptions for RAM4K9

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-5).

Table 2-5 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA[1:0]	WIDTHB[1:0]	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: *The aspect ratio settings are constant and cannot be changed on-the-fly.*

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, that port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A LOW on these signals indicates a write operation, and a HIGH indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A LOW on these signals makes the output retain data from the previous read. A HIGH indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero and disables reads and/or writes from the SRAM block as well as clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-94 on page 3-73 for the specifications.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-6).

Table 2-6 • **Address Pins Unused/Used for Various Supported Bus Widths**

	ADDRx	
D×W	Unused	Used
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: *The "x" in ADDRx implies A or B.*

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-7).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-7). The output data on unused pins is undefined.

Table 2-7 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

	DINx/DOUTx	
D×W	Unused	Used
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: *The "x" in DINx or DOUTx implies A or B.*

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Signal Descriptions for RAM512X18

RAM512X18 has slightly different behavior than RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-8).

Table 2-8 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They can be clocked on the rising or falling edge of WCLK and RCLK.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero and disables reads and/or writes from the SRAM block as well as clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-95 on page 3-74 for the specifications.

PIPE

This signal is used to specify pipelined read on the output. A LOW on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge and/or by separate clocks by port.

ProASIC3E devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the ProASIC3E development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from address to data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is high. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "DDR Module Specifications" section on page 3-56.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG 1532" section on page 2-54 and the *ProASIC3/E SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

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Signal Descriptions for FIFO4K18

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-9).

Table 2-9 • **Aspect Ratio Settings for WW[2:0]**

WW[2:0]	RW[2:0]	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when LOW. When the RBLK signal is HIGH, that port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A LOW on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array (Table 2-10).

While the RESET signal is active, read and write operations are disabled. As with any asynchronous RESET signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-96 on page 3-78 for the specifications.

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-10).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-10).

Table 2-10 • **Input Data Signal Usage for Different Aspect Ratios**

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	–

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes HIGH). A HIGH on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes HIGH). A HIGH on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-27.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts HIGH. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts HIGH. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-27.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the

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AEMPTY output will go HIGH. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go HIGH.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-27.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes HIGH). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes HIGH).

The FIFO counters in the ProASIC3E device start the count at zero, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at zero. An example application for ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1,500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case the AFVAL setting is based on the number of write data entries, and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16 instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Refer to the *ProASIC3/E SRAM/FIFO Blocks* application note for more information.

Pro I/Os

Introduction

ProASIC3E devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-11, Table 2-12, Table 2-13, and Table 2-14 on page 2-30 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, and weak pull-up and pull-down circuits. All I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-38 for possible implementations of 5 V tolerance.

Single-ended input buffers support both the Schmitt trigger and programmable delay options on a per-I/O basis.

All I/Os are in a known state during power-up and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3 for more information. During power-up, before reaching activation levels, the I/O input and output buffers are disabled, while the weak pull-up is enabled. Activation levels are described in Table 3-2 on page 3-2.

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I/O Tile

The ProASIC3E I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-24 on page 2-33). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-34 for more information).

As depicted in Figure 2-24 on page 2-33, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-33 for more information.

I/O Banks and I/O Standards Compatibility

I/Os are grouped into I/O voltage banks. There are eight I/O banks (two per side). Each I/O voltage bank has dedicated I/O supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-12 on page 2-29 shows the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-50.

Every I/O bank is divided into minibanks. Any user I/O in a V_{REF} minibank (a minibank is the region of scope of a V_{REF} pin) can be configured as a V_{REF} pin (Figure 2-23). Only one V_{REF} pin is needed to control the entire V_{REF} minibank. The location and scope of the V_{REF} minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-50.

Table 2-11 on page 2-29 shows the I/O standards supported by ProASIC3E devices and the corresponding voltage levels.

I/O standards are compatible if they answer the following:

- Their V_{CCI} and VMV values are identical
- Both of the standards need a V_{REF} and their V_{REF} values are identical

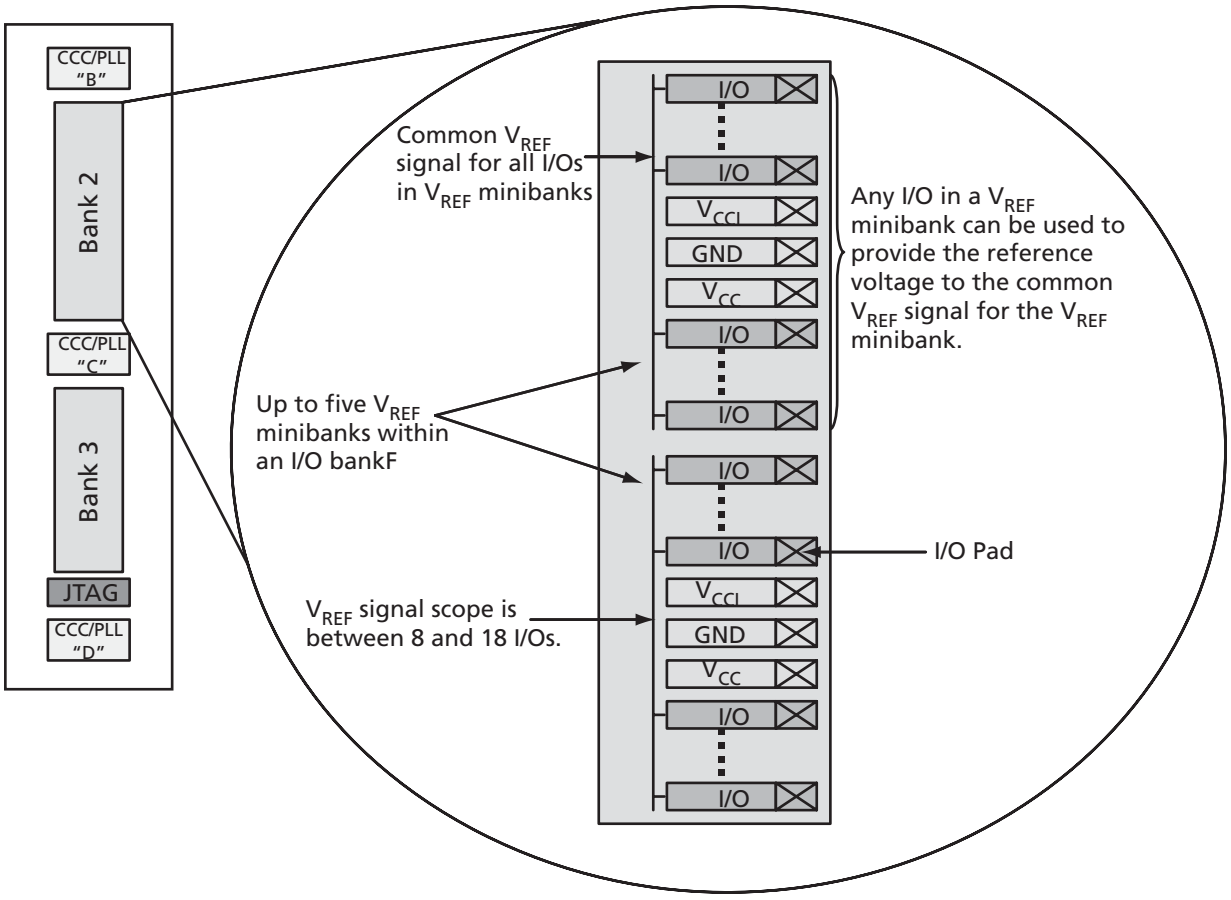

Figure 2-23 • **Typical ProASIC3E I/O Bank Detail Showing V_{REF} Minibanks**

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Table 2-11 • **ProASIC3E Supported I/O Standards**

	A3PE600	A3PE1500	A3PE3000
Single-Ended			
LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI/PCI-X	✓	✓	✓
Differential			
LVPECL, LVDS, BLVDS, M-LVDS	✓	✓	✓
Voltage-Referenced			
GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	✓	✓	✓

Table 2-12 • **V_{CCI} Voltages and Compatible ProASIC3E Standards**

V_{CCI} and VMV (typical)	**Compatible Standards**
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II), GTL+ 3.3, GTL 3.3, LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II), GTL+ 2.5, GTL 2.5, LVDS, DDR LVDS, BLVDS, and M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I), HSTL (Class II)

Table 2-13 • **V_{REF} Voltages and Compatible ProASIC3E Standards**

V_{REF} (typical)	**Compatible Standards**
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

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Table 2-14 • **Legal ProASIC3E I/O Usage Matrix within the Same Bank**

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI/PCI-X	GTL+ (3.3 V)	GTL+ (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS, BLVDS, and M-LVDS, DDR (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	–														
	0.80 V														
	1.00 V														
	1.50 V														
2.5 V	–														
	0.80 V														
	1.00 V														
	1.25 V														
1.8 V	–														
1.5 V	–														
	0.75 V														

Note: *White box: Allowable I/O standard combination*
Gray box: Illegal I/O standard combination

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Features Supported on Every I/O

Table 2-15 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-15 • **ProASIC3E I/O Features**

Feature	Description
Single-Ended and Voltage-Referenced Transmitter Features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os • Weak pull-up and pull-down • 2 slew rates • Skew between output buffer enable/disable time: 2 ns delay on the rising edge and 0 ns delay on the falling edge (see the "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-43 for more information). • 5 drive strengths • 5 V–tolerant receiver ("5 V Output Tolerance" section on page 2-41) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-41) • High performance (Table 2-16 on page 2-32)
Single-Ended Receiver Features	• ESD protection • Schmitt trigger option • Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-16 on page 2-32) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output induced noise.
Voltage-Referenced Differential Receiver Features	• Programmable delay: 0 ns if bypassed, 0.46 ns with '000' setting, 4.66 ns with '111' setting, 0.6-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-16 on page 2-32) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output induced noise.
CMOS-Style LVDS, BLVDS, M-LVDS, or LVPECL Transmitter	• 2 I/Os and external resistors are used to provide a CMOS-style LVDS, DDR LVDS, BLVDS, and M-LVDS/LVPECL transmitter solution. • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • High slew rate
LVDS, DDR LVDS, BLVDS, and M-LVDS/LVPECL Differential Receiver Features	• ESD protection • High performance (Table 2-16 on page 2-32) • Programmable Delay: 0 ns if bypassed, 0.46 ns with '000' setting, 4.66 ns with '111' setting, 0.6-ns intermediate delay increments (at 25°C, 1.5 V) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

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Table 2-16 • **Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected)**

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
M-LVDS	200 MHz
B LVDS	200 MHz
LVPECL	350 MHz

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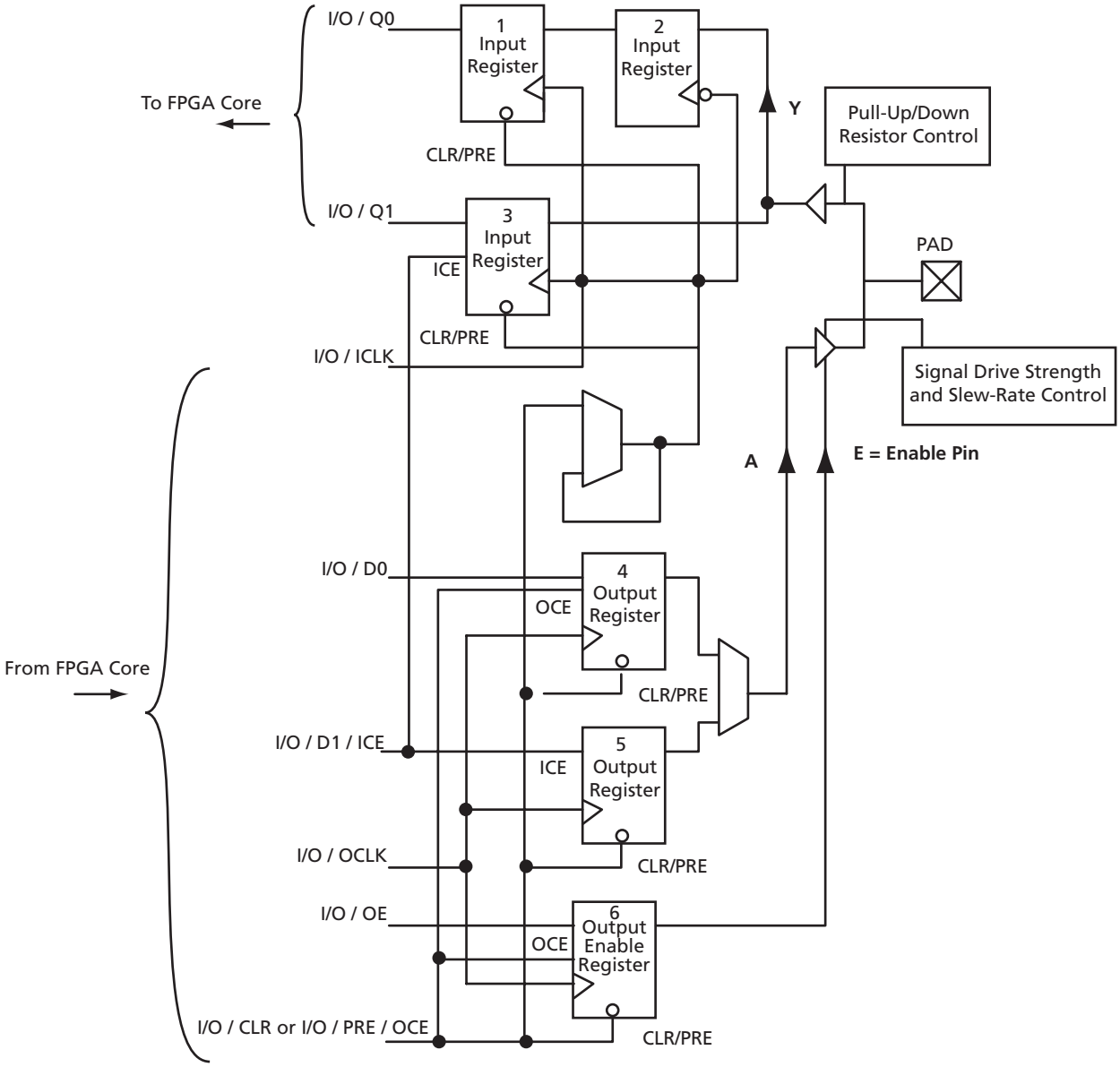
I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-24 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-24) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy certain rules. For more information, refer to the *ProASIC3/E I/O Usage Guide*.



Note: *ProASIC3E I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-34 for more information).*

Figure 2-24 • **I/O Block Logical Representation**

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Double Data Rate (DDR) Support

ProASIC3E devices support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making them very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. The DDR feature is primarily implemented in the FPGA core periphery and is not tied to a specific I/O technology or limited to any I/O standards.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-25. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on ProASIC3E devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-26 on page 2-35. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the Actel application note *Using DDR for ProASIC3/E Devices* for more information.

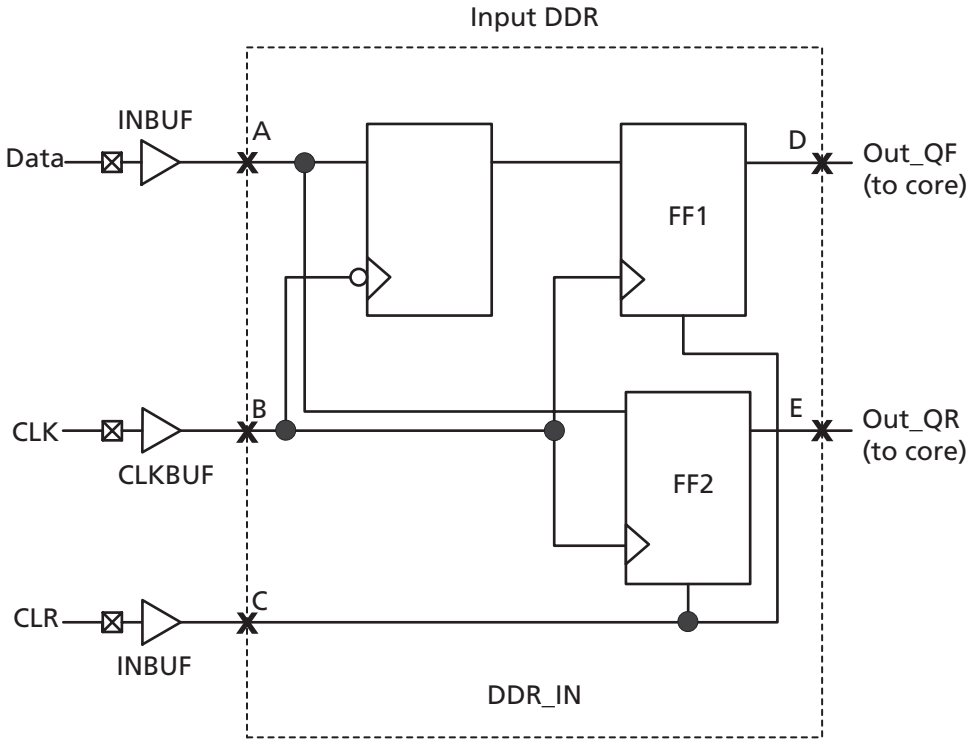

Figure 2-25 • **DDR Input Register Support in ProASIC3E Devices**

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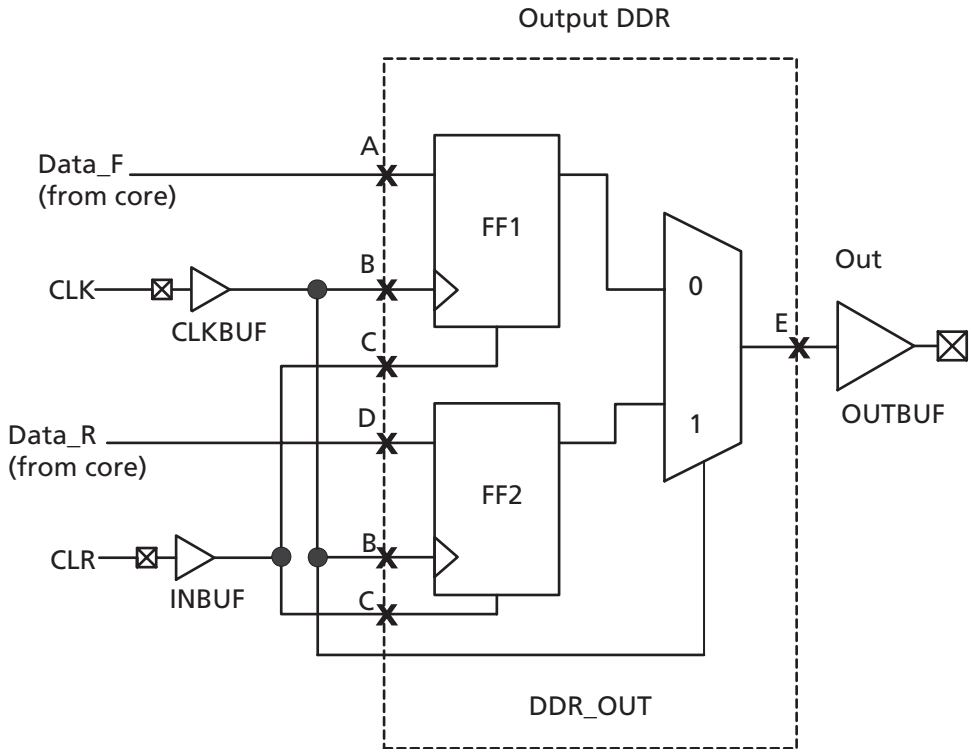

Figure 2-26 • **DDR Output Support in ProASIC3E Devices**

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Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in or from a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-17. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-17 • **Levels of Hot-Swap Support**

Hot-Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain ProASIC3E Devices	Compliance of ProASIC3E Devices
1	Cold-swap	No	–	–	–	System and card with Actel FPGA chip are powered down and the card is plugged into the system. Then the power supplies are turned on for the system but not for the FPGA on the card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	–	In PCI hot-plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/ removal)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on the bus. It is critical that the logic states set on the bus signal are not disturbed during card insertion/removal.	Compliant with 2 levels of staging (first-GND, second-all other pins)
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal are not disturbed during card insertion/removal.	Compliant with 2 levels of staging (first-GND, second-all other pins)

For ProASIC3E devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to ProASIC3E I/Os must have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This resistance is the transmitter resistance sending signal towards the ProASIC3E I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to achieve Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

- Grounds
- Powers, I/Os, and other pins

For boards and cards with three levels of staging, card power supplies must have time to reach their final value before the I/Os are connected. Pay attention to the sizing of power supply decoupling capacitors on the card to ensure that the power supplies are not overloaded with capacitance.

Cards with three levels of staging should have the following sequence:

- Grounds
- Powers
- I/Os and other pins

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Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

ProASIC3E devices support cold-sparing for all I/O configurations. Standards such as PCI that require I/O clamp diodes can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

Electrostatic Discharge (ESD) Protection

ProASIC3E devices are tested per JEDEC Standard JESD22-A114-B.

ProASIC3E devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

ProASIC3E devices are tested to the following models: the Human Body Model (HBM) with a tolerance of 2,000 V, the Machine Model (MM) with a tolerance of 250 V, and the Charged Device Model (CDM) with a tolerance of 200 V.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-18 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-18 • **I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V [3]	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [3]	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/LVPECL	No	Yes	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *In the SmartGen Core Reference Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.*

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5 V Input Tolerance

I/Os can support 5-V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V and LVCMOS 2.5 V / 5.0 V configurations are used (see Table 2-18 on page 2-37 for more details). There are four recommended solutions for achieving 5 V receiver tolerance (see Figure 2-27 to Figure 2-30 on page 2-40 for details of board and macro setups). All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design must ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

Here are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where Rtx_out_high = (V_{CCI} – V_{OH}) / I_{OH}, Rtx_out_low = V_{OL} / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 × 0.95 + 36 × 0.95 + 10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 × 0.95 + 390 × 0.95 + 10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin (rx) < 3.6 V* when the transmitter sends a logic 1. This range of Vin_dc (rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-4 on page 3-2.

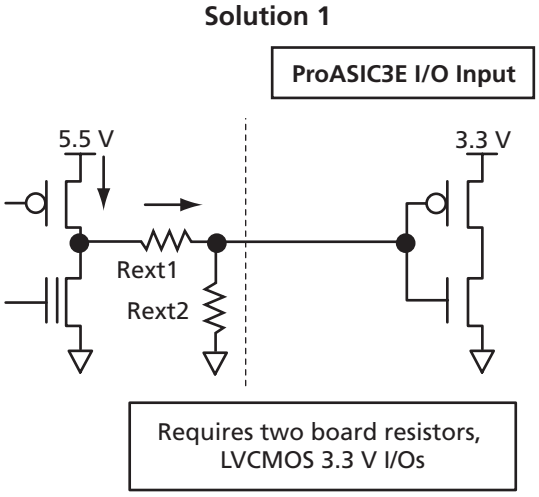

Figure 2-27 • **ProASIC3E Solution 1**

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Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-28. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

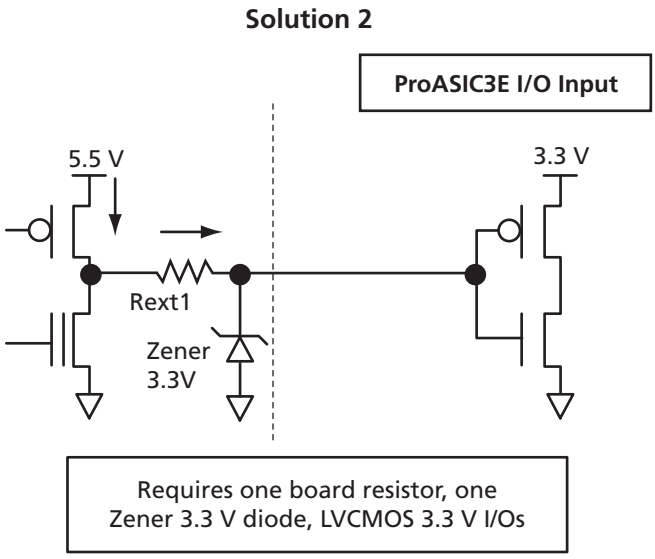

Figure 2-28 • **ProASIC3E Solution 2**

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Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-29. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

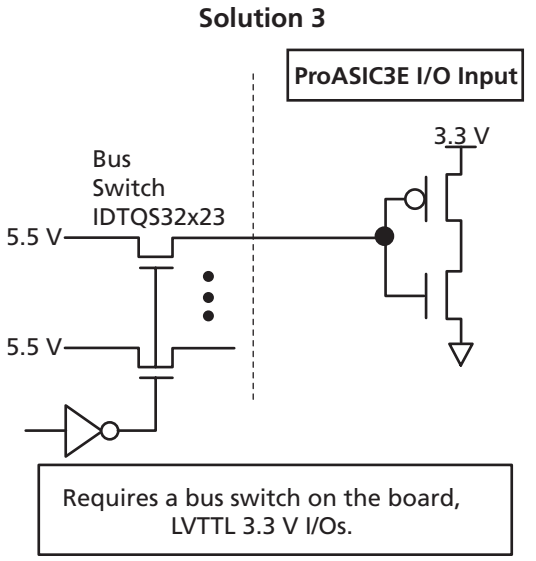

Figure 2-29 • **ProASIC3E Solution 3**

Solution 4

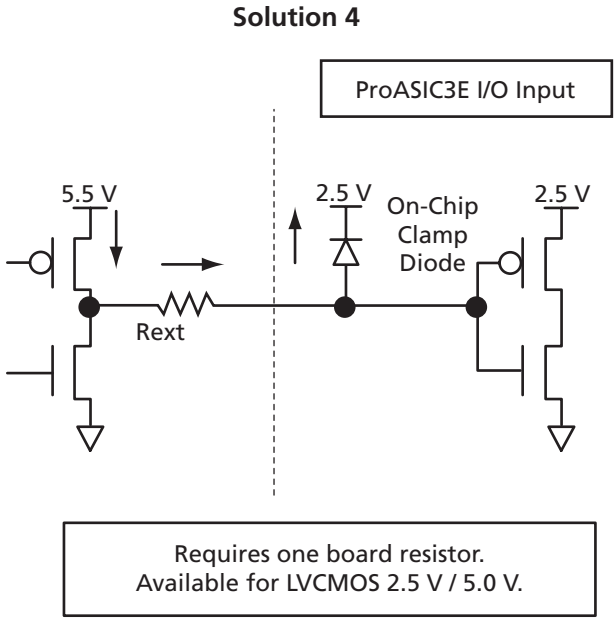

Figure 2-30 • **ProASIC3E Solution 4**

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Table 2-19 • **Comparison Table for 5 V–Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2, 3, 4, 5] • R = 47 Ω at T_J = 70°C • R = 150 Ω at T_J = 85°C • R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' • 52.7 mA at T_J = 70°C / 10-year lifetime • 16.5 mA at T_J = 85°C / 10-year lifetime • 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor of 1 / duty cycle. Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) × 52.7 mA = 5 × 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*
3. *At 70°C, customers could still use 420 Ω on every I/O.*
4. *At 85°C, a 5 V solution on every other I/O is permitted, since the resistance is lower (150 Ω) and the current is higher. Also, the designer can still use 420 Ω and use the solution on every I/O.*
5. *At 100°C, the 5 V solution on every I/O is permitted, since 420 Ω are used to limit the current to 5.9 mA.*

5 V Output Tolerance

ProASIC3E I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value, and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, ProASIC3E I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

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Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout

SSOs can cause signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and V_{CCI} dip noise. These two noise types are caused by rapidly changing currents through GND and V_{CCI} package pin inductances during switching activities (EQ 2-1 and EQ 2-2).

$$\text{Ground bounce noise voltage} = L(GND) \times di/dt \quad \textit{EQ 2-1}$$

$$V_{CCI} \text{ dip noise voltage} = L(V_{CCI}) \times di/dt \quad \textit{EQ 2-2}$$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to the SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

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Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

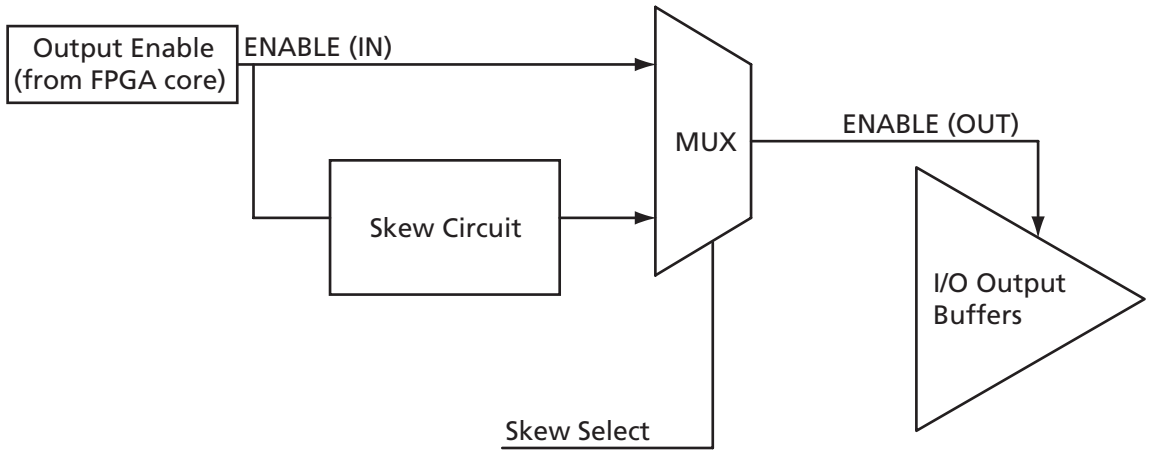

Figure 2-31 • **Block Diagram of Output Enable Path**

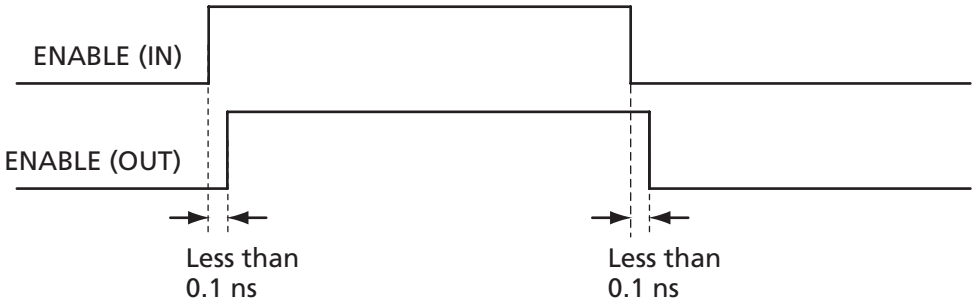

Figure 2-32 • **Timing Diagram (option 1: bypasses skew circuit)**

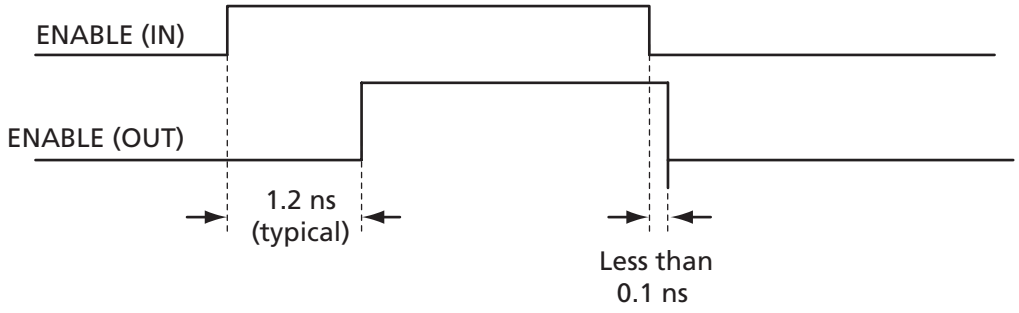

Figure 2-33 • **Timing Diagram (option 2: enables skew circuit)**

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At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter over-stress due to transmitter-to-transmitter current shorts. Figure 2-34 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-35 shows how bus contention is created, and Figure 2-36 on page 2-45 shows how it can be avoided with the skew circuit.

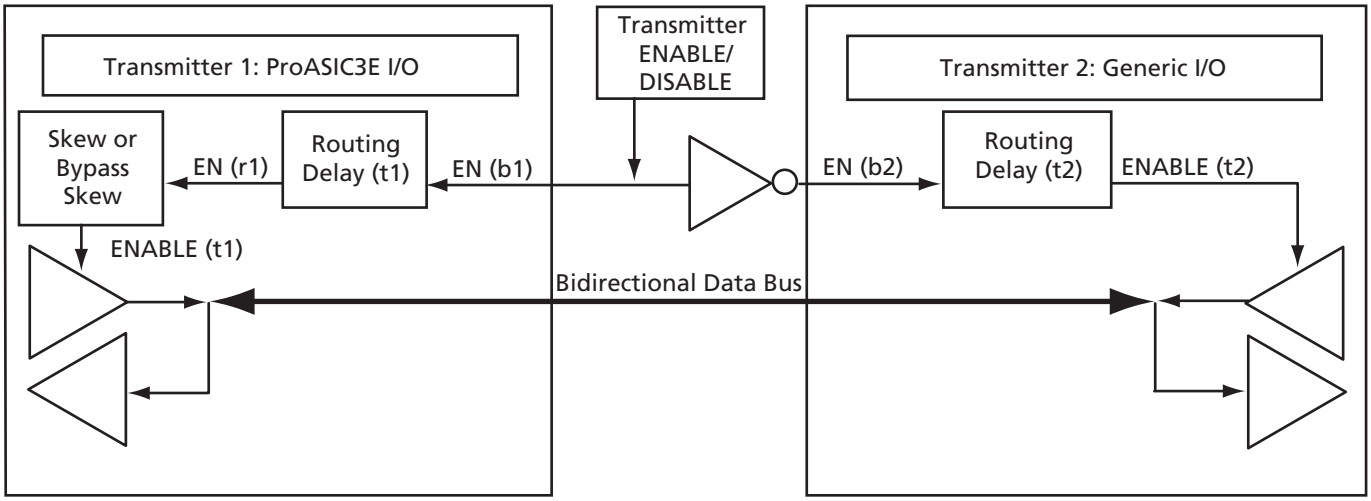

Figure 2-34 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using ProASIC3E Devices**

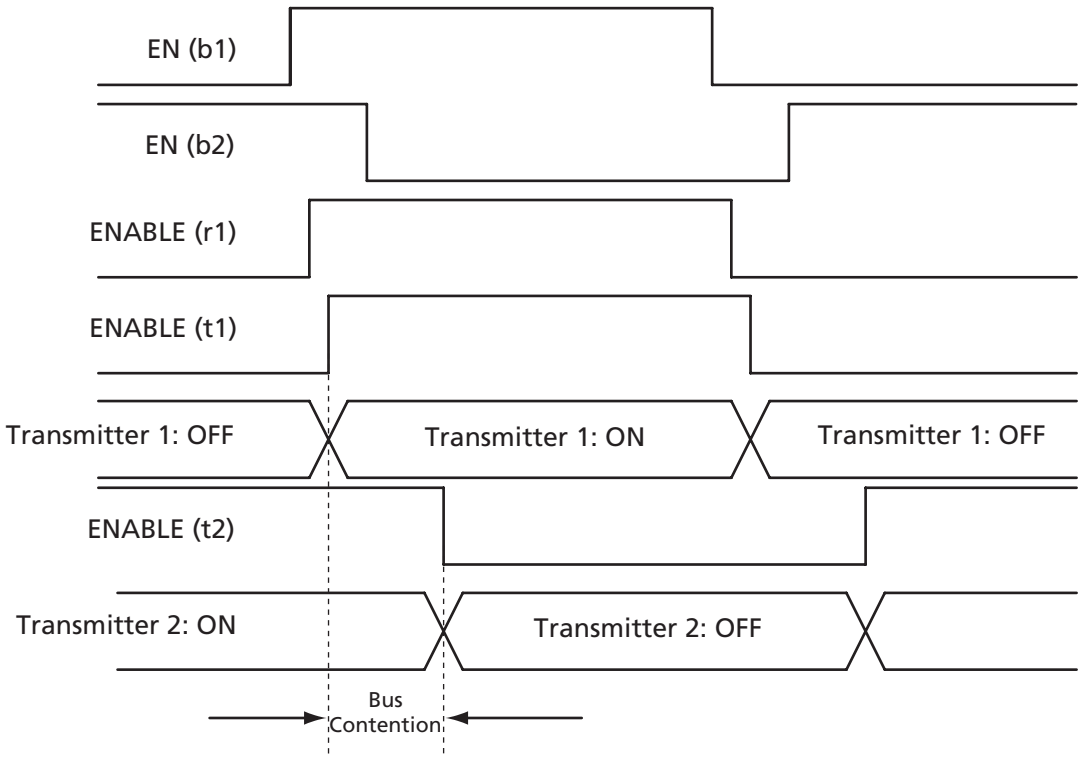

Figure 2-35 • **Timing Diagram (bypasses skew circuit)**

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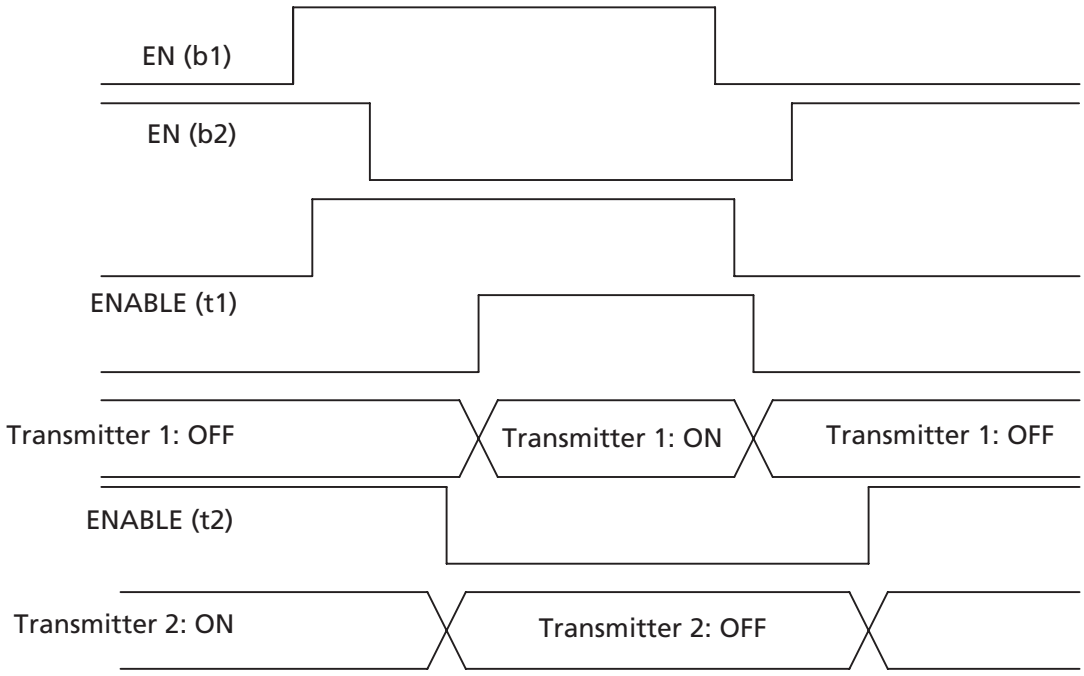

Figure 2-36 • **Timing Diagram (with skew circuit selected)**

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I/O Software Support

In the ProASIC3E development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-20 lists the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in ProASIC3E support up to five different drive strengths.

Table 2-20 • **ProASIC3E I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓	✓	✓		
PCI-X (3.3 V)	✓		✓		✓	✓	✓	✓		
GTL+ (3.3 V)			✓		✓	✓	✓	✓		✓
GTL+ (2.5 V)			✓		✓	✓	✓	✓		✓
GTL (3.3 V)			✓		✓	✓	✓	✓		✓
GTL (2.5 V)			✓		✓	✓	✓	✓		✓
HSTL Class I			✓		✓	✓	✓	✓		✓
HSTL Class II			✓		✓	✓	✓	✓		✓
SSTL2 Class I & II			✓		✓	✓	✓	✓		✓
SSTL3 Class I & II			✓		✓	✓	✓	✓		✓
LVDS, BLVDS, M-LVDS			✓			✓	✓	✓		✓
LVPECL						✓	✓	✓		✓

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Weak Pull-Up and Weak Pull-Down Resistors

ProASIC3E devices support optional weak pull-up and pull-down resistors per I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to Table 3-20 on page 3-20 for more information.

Slew Rate Control and Drive Strength

ProASIC3E devices support output slew rate control: high and low.Actel recommends the high slew rate option to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

Refer to Table 2-21 for more information about the slew rate and drive strength specification.

Table 2-21 • **ProASIC3E I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings**

I/O Standards	OUT_DRIVE (mA)							Slew	
	2	4	6	8	12	16	24		
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V/5.0 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

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Table 2-23 on page 2-49 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard.

Refer to Table 2-21 for SLEW and OUT_DRIVE settings. Table 2-22 on page 2-48 lists the I/O default attributes. Table 2-23 on page 2-49 lists the voltages for the supported I/O standards.

Table 2-22 • **ProASIC3E I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	See Table 2-21 on page 2-47	See Table 2-21 on page 2-47	Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I & II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I & II			Off	None	30 pF	–	Off	0	Off
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

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Table 2-23 • **Supported ProASIC3E I/O Standards and the Corresponding V_{REF} and V_{TT} Voltages**

I/O Standard	Input/Output Supply Voltage (VMVtyp/V_{CCI_TYP})	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_TYP})
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5/5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, DDR LVDS, BLVDS, M-LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

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User I/O Naming Convention

Due to the comprehensive and flexible nature of ProASIC3E device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-37). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-14 on page 2-16 shows the three input pins per clock source MUX at CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction

x = P (Positive) or N (Negative) for differential pairs, or R (Regular—single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–7). The bank number starts at 0 from northwest I/O bank and proceeds in a clockwise direction.

V = V_{REF}

z = V_{REF} minibank number (0–4). A given voltage-referenced signal spans 16 pins (typically) in an I/O bank. Voltage banks may have multiple V_{REF} minibanks.

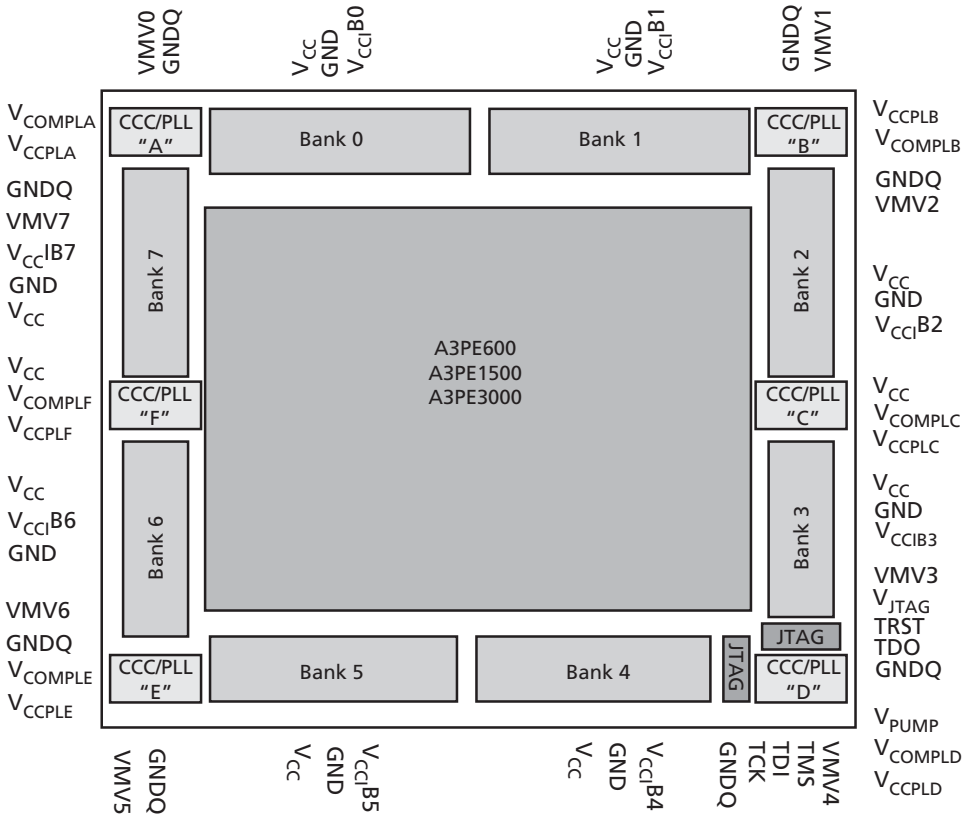

Figure 2-37 • **User I/O Naming Conventions of ProASIC3E Devices – Top View**

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Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package, and improves input signal integrity. GNDQ must always be connected to GND on the board.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. V_{CC} is required for powering the JTAG state machine in addition to V_{JTAG}. Even when a ProASIC3 device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the ProASIC3 device.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are eight I/O banks on ProASIC3E devices plus a dedicated V_{JTAG} bank. Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e., VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

$V_{CCPLA/B/C/D/E/F}$ **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V. There are six V_{CCPL} pins (PLL power) on ProASIC3E devices. Unused V_{CCPL} pins should be connected to GND.

$V_{COMPLA/B/C/D/E/F}$ **PLL Ground**

Ground to analog PLL power supplies. There are six V_{COMPL} pins (PLL ground) on ProASIC3E devices. Unused V_{COMPL} pins should be connected to GND.

V_{JTAG} **JTAG Supply Voltage**

ProASIC3E devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND. It should be noted that V_{CC} is required to be powered for JTAG operation; V_{JTAG} alone is insufficient. If a ProASIC3E device is in a JTAG chain of interconnected boards, the board containing the ProASIC3E device can be powered down, provided both V_{JTAG} and V_{CC} to the ProASIC3E part remain powered; otherwise, JTAG signals will not be able to transition the ProASIC3E device, even in bypass mode.

V_{PUMP} **Programming Supply Voltage**

ProASIC3E devices support single-voltage ISP programming of the configuration Flash and FlashROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V. Programming power supply voltage (V_{PP}) range is 3.3 V +/- 5%.

When the V_{PUMP} pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across V_{PUMP} and GND, and positioned as close to the FPGA pins as possible.

User-Defined Supply Pins

V_{REF} **I/O Voltage Reference**

Reference voltage for I/O minibanks. V_{REF} pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One V_{REF} pin can support the number of I/Os available in its minibank.

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User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI}. With V_{CCI}, VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct input into the chip level globals and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed and only one input can be used as a global input.

Refer to the "User I/O Naming Convention" section on page 2-50 for a explanation of the naming of global pins.

JTAG Pins

ProASIC3E devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both V_{JTAG} and V_{CC} to the ProASIC3E part must be supplied to allow JTAG signals to transition the ProASIC3E device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Actel recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-24 for more information.

Table 2-24 • **Recommended Tie-Off Values for the TCK and TRST Pins**

V_{JTAG}	Tie-Off Resistance
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain.*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin be pulled down.*

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 2-24 and must satisfy the parallel resistance value requirement. The values in Table 2-24 correspond to the resistor recommended when a single device is used and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases,

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Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Software Tools

Overview of Tools Flow

The ProASIC3E family of FPGAs is fully supported by both Actel Libero IDE and Designer FPGA development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE flow diagram* located on the Actel website). Libero IDE includes Synplify® AE from Synplicity,® ViewDraw® AE from Mentor Graphics,® Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD,® PALACE™ AE Physical Synthesis from Magma Design Automation,™ and Designer software from Actel.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer—a world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer—a design netlist schematic viewer
- ChipPlanner—a graphical floorplanner viewer and editor
- SmartPower—a tool that enables the designer to quickly estimate the power consumption of a design
- PinEditor—a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor—a tool that displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors such as Mentor Graphics, Synplicity, Synopsys, and Cadence.® The Designer software is available for both the Windows® and UNIX operating systems.

Programming

Programming can be performed using tools such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate STP programming files from the Designer software and use these files to program a device.

ProASIC3E devices can be programmed in system. For more information on ISP of ProASIC3E devices, refer to the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* and *Programming a ProASIC3/E Using a Microprocessor* application notes.

The ProASIC3E device can be serialized with a unique identifier stored in the FlashROM of each device. Serialization is an automatic assignment of serial numbers that are stored within the STAPL file used for programming. The area of the FlashROM used for holding such identifiers is defined using SmartGen, and the range of serial numbers to be used is defined at the time of STAPL file generation with FlashPoint. Serial number values for STAPL file generation can even be read from a file of predefined values. Serialized programming using a serialized STAPL file can be done through Actel In-House Programming (IHP), an external vendor using Silicon Sculptor software, or the ISP capabilities of the FlashPro software.

Security

ProASIC3E devices have a built-in 128-bit AES decryption core. The decryption core facilitates secure in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is

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stored in on-chip nonvolatile memory (Flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late-stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-192) block cipher is the NIST (National Institute of Standards and Technology) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in ProASIC3E devices in nonvolatile Flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of ProASIC3E devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products. See the application note *ProASIC3/E Security* for more details.

ISP

ProASIC3E devices support IEEE 1532 ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved. See the application note *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* for more details.

JTAG 1532

ProASIC3E devices support the JTAG-based IEEE 1532 standard for ISP. As part of this support, when a ProASIC3E device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. The SAMPLE/PRELOAD instruction captures the status of pads in parallel and shifts them out as new data is shifted in for loading into the Boundary Scan Register. When the ProASIC3E device is in an unprogrammed state, the SAMPLE/PRELOAD instruction has no effect on I/O status; however, it will continue to shift in new data to be loaded into the BSR. Therefore, when SAMPLE/PRELOAD is used on an unprogrammed device, the BSR will be loaded with undefined data. Refer to the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* application note for more details.

For JTAG timing information on setup, hold, and fall times, refer to the *FlashPro User's Guide*.

Boundary Scan

ProASIC3E devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic ProASIC3E boundary scan logic circuit is composed of the TAP controller, test data registers, and instruction register (Figure 2-40 on page 2-56). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-25).

Table 2-25 • **Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-52 for pull-up/down recommendations for TDO and TCK pins. Table 2-26 gives

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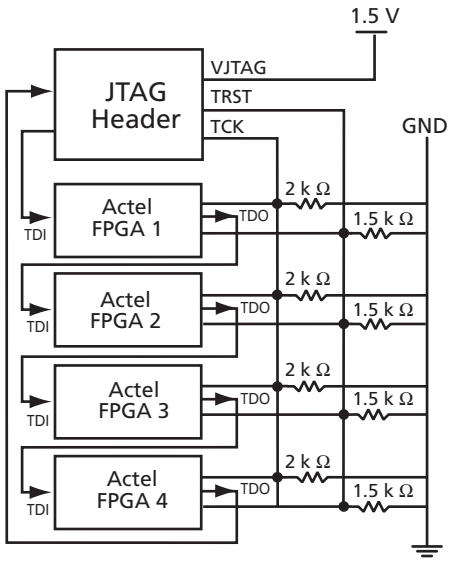
pull-down recommendations for the TRST and TCK pins.

Table 2-26 • **TRST and TCK Pull-Down Recommendations**

V_{JTAG}	Tie-Off Resistance*
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Note: **Equivalent parallel resistance if more than one device is on JTAG chain (Figure 2-38 on page 2-55).*



Note: *TCK is correctly wired with an equivalent tie-off resistance of 500 Ω, which satisfies the table for VJTAG of 1.5 V. The resistor values for TRST are not appropriate in this case, as the tie-off resistance of 375 Ω is below the recommended minimum for VJTAG = 1.5 V, but would be appropriate for a VJTAG setting of 2.5 V or 3.3 V.*

Figure 2-38 • **Parallel Resistance on JTAG Chain of Devices**

The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-39. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain HIGH for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC3E devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with serial-in, serial-out, parallel-in, and parallel-out pins.

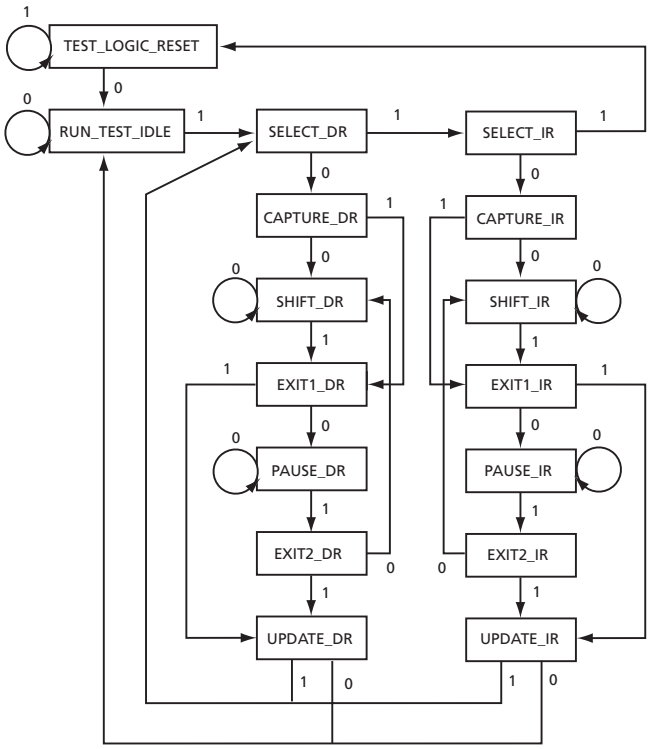


Figure 2-39 • **TAP State Machine**

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The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

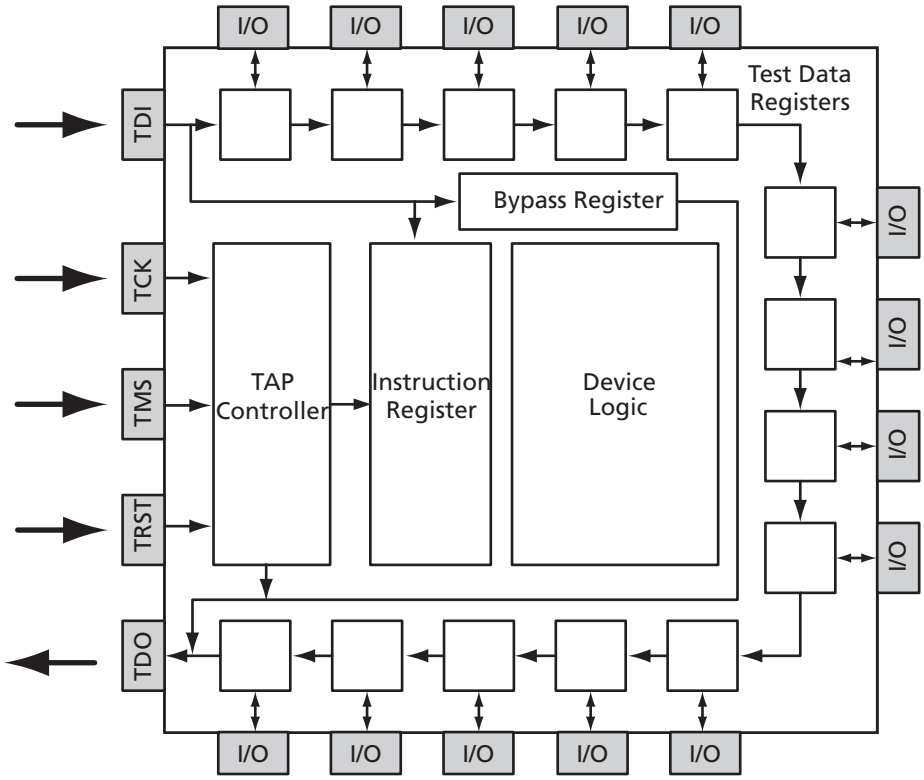

Figure 2-40 • **Boundary Scan Chain in ProASIC3E**

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DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 3-2 on page 3-2 is not implied.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-3 on page 3-2.*
2. *For Flash programming and retention maximum limits refer to Table 3-3 on page 3-2 and for recommended operating limits refer to Table 3-2 on page 3-2.*

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Table 3-2 • **Recommended Operating Conditions**

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction temperature		0 to +70	–40 to +85	°C
V_{CC}	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[3]	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)		1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS/BLVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 3-13 on page 3-15. VMV and V_{CCI} should be at the same voltage within a given I/O bank.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *V_{PUMP} can be left floating during normal operation (not programming mode).*

Table 3-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	110
Industrial	500	20 years	110	110

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 3-1 and Table 3-2 for device operating conditions and absolute limits.*

Table 3-4 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

V_{CCI} and VMV	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table refers only to overshoot/undershoot limits for simultaneous switching I/Os.*
4. *The device meets overshoot/undershoot specification requirements for PCI inputs with V_{CCI} 3.45 V at 85 °C maximum, whereas the average toggling of inputs at one-sixth of PCI frequency is considered.*

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I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1).
2. $V_{CCI} > V_{CC} – 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

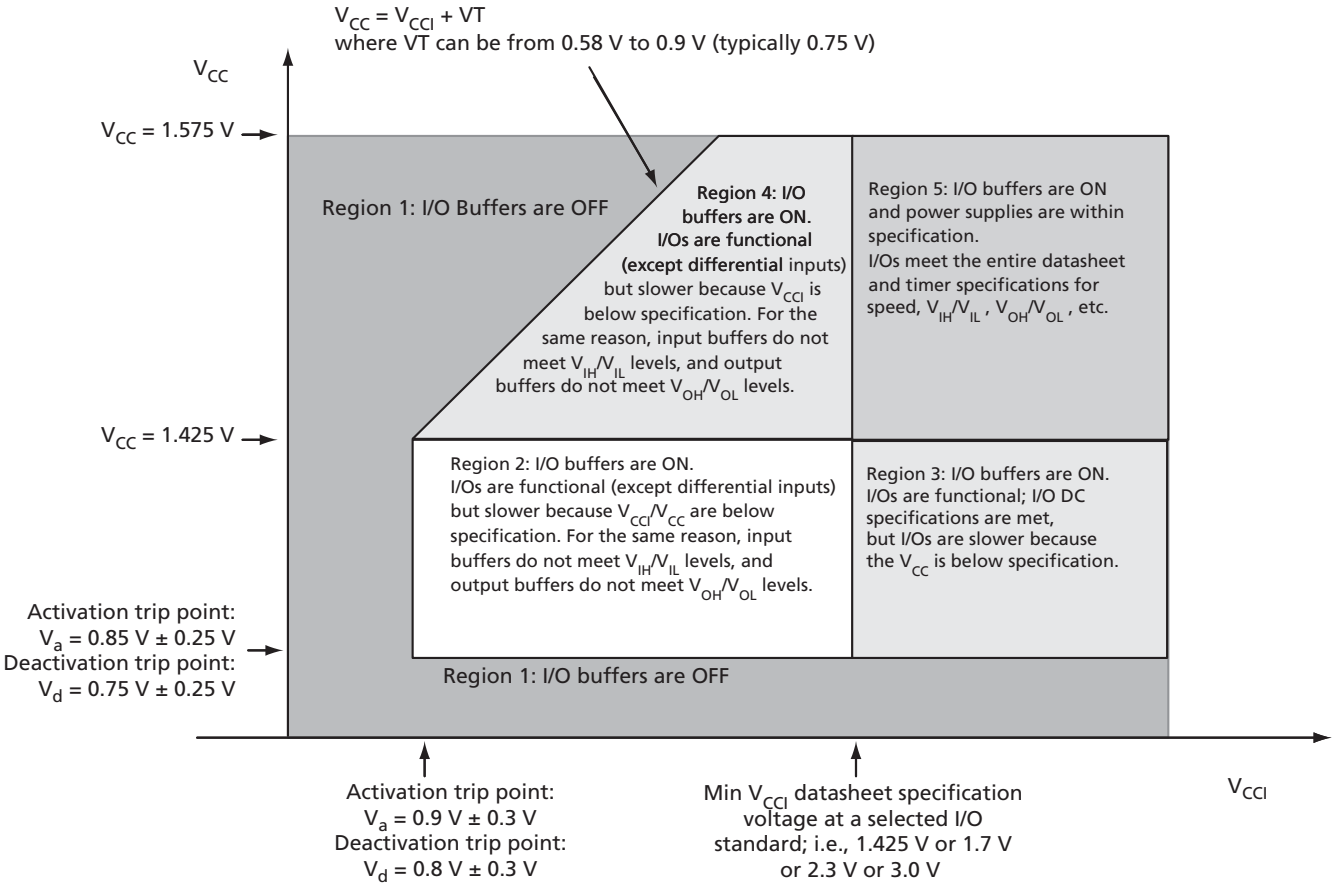

Figure 3-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

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Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 3-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 3-1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 3-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 3-2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{(°C/W)}} = \frac{110\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 5.88\ \text{W} \qquad \textit{EQ 3-2}$$

Table 3-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 3-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.425 V)**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.87	0.92	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.97	1.00
1.575	0.80	0.85	0.87	0.92	0.94	0.96

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Calculating Power Dissipation

Quiescent Supply Current

Table 3-7 • **Quiescent Supply Current Characteristics**

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. *I_{DD} Includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution, which is shown in Table 3-8 and Table 3-9 on page 3-6.*
2. *–F speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.*

Power per I/O Pin

Table 3-8 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			
LVDS/BLVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

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Table 3-9 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS/BLVDS/M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.*

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Power Consumption of Various Internal Resources

Table 3-10 • **Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices**

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)		
		A3PE600	A3PE1500	A3PE3000
P_{AC1}	Clock contribution of a Global Rib	12.77	16.21	19.7
P_{AC2}	Clock contribution of a Global Spine	1.85	3.06	4.16
P_{AC3}	Clock contribution of a VersaTile row	0.88		
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12		
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.07		
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.29		
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.29		
P_{AC8}	Average contribution of a routing net	0.70		
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 3-8 on page 3-5.		
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 3-9 on page 3-6		
P_{AC11}	Average contribution of a RAM block during a read operation	25.00		
P_{AC12}	Average contribution of a RAM block during a write operation	30.00		
P_{AC13}	Static PLL contribution	2.55 mW		
P_{AC14}	Dynamic contribution for PLL	2.60		

Note: **For a different output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero IDE software.*

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Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-11 on page 3-10.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-12 on page 3-10.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 3-12 on page 3-10. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 3-11 on page 3-10.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

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Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-10.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-12 on page 3-10.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-12 on page 3-10.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 3-12 on page 3-10.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

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Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-11 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-12 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

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User I/O Characteristics

Timing Model

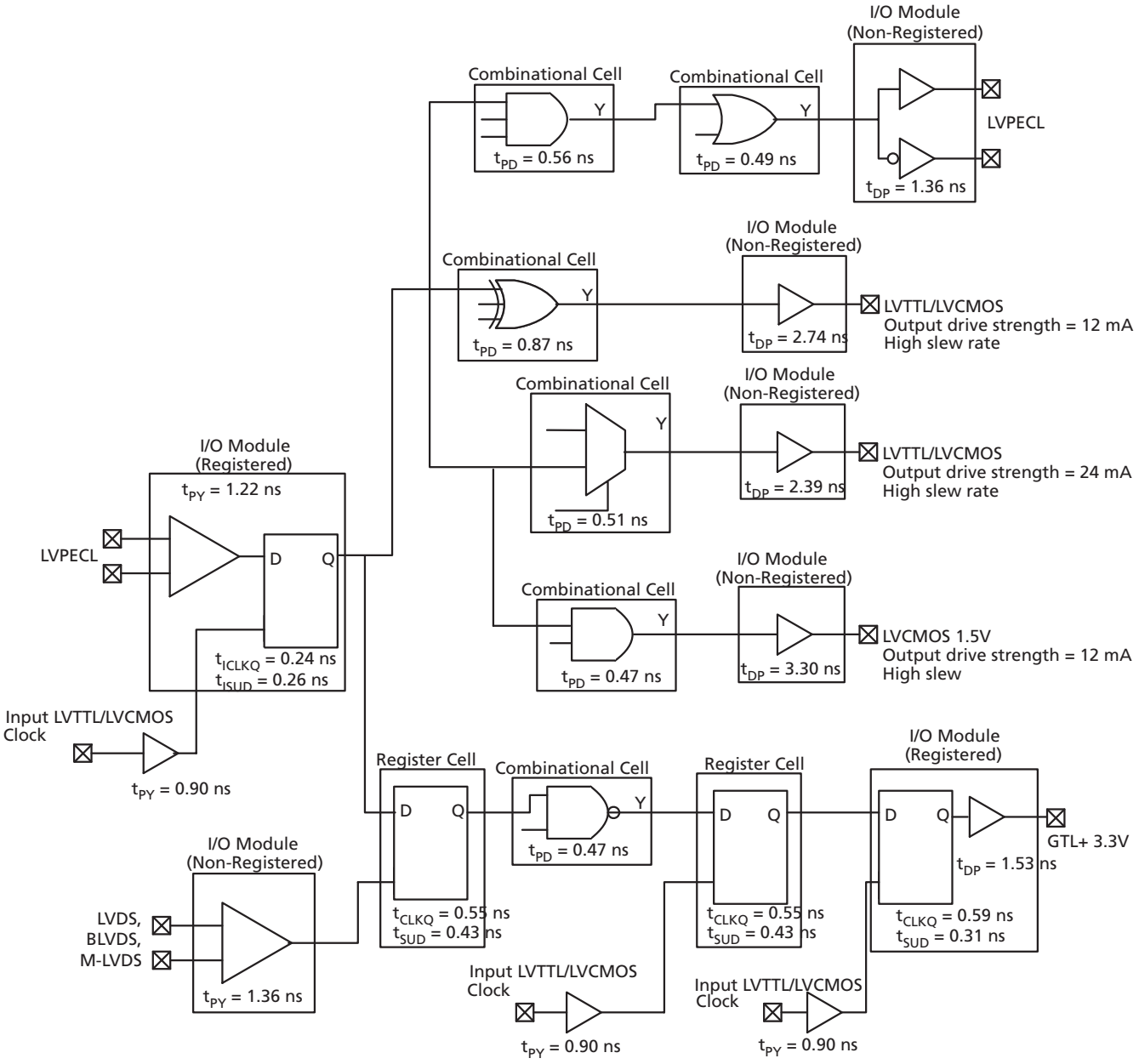

Figure 3-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case V_{CC} = 1.425 V

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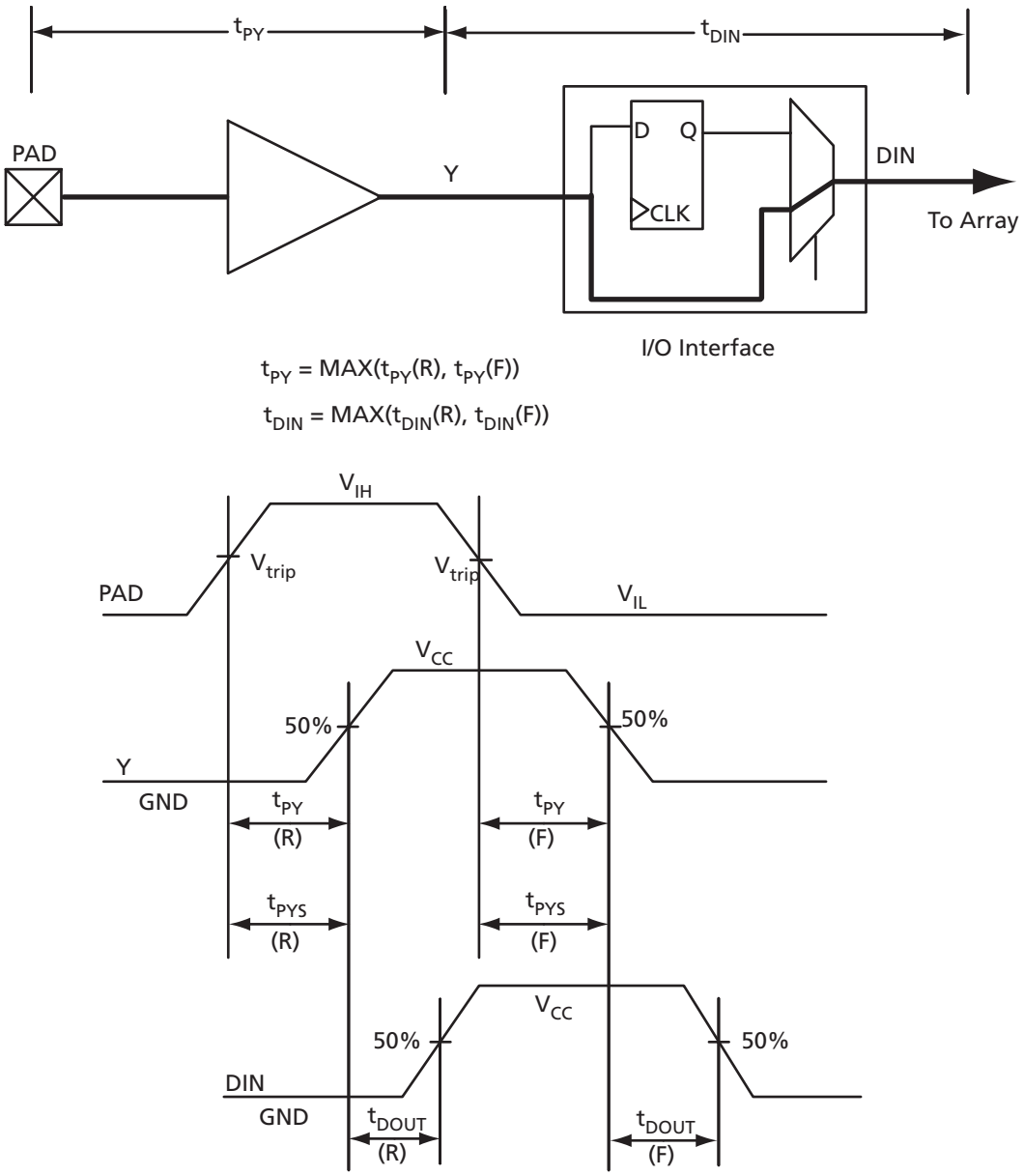

Figure 3-3 • **Input Buffer Timing Model and Delays (example)**

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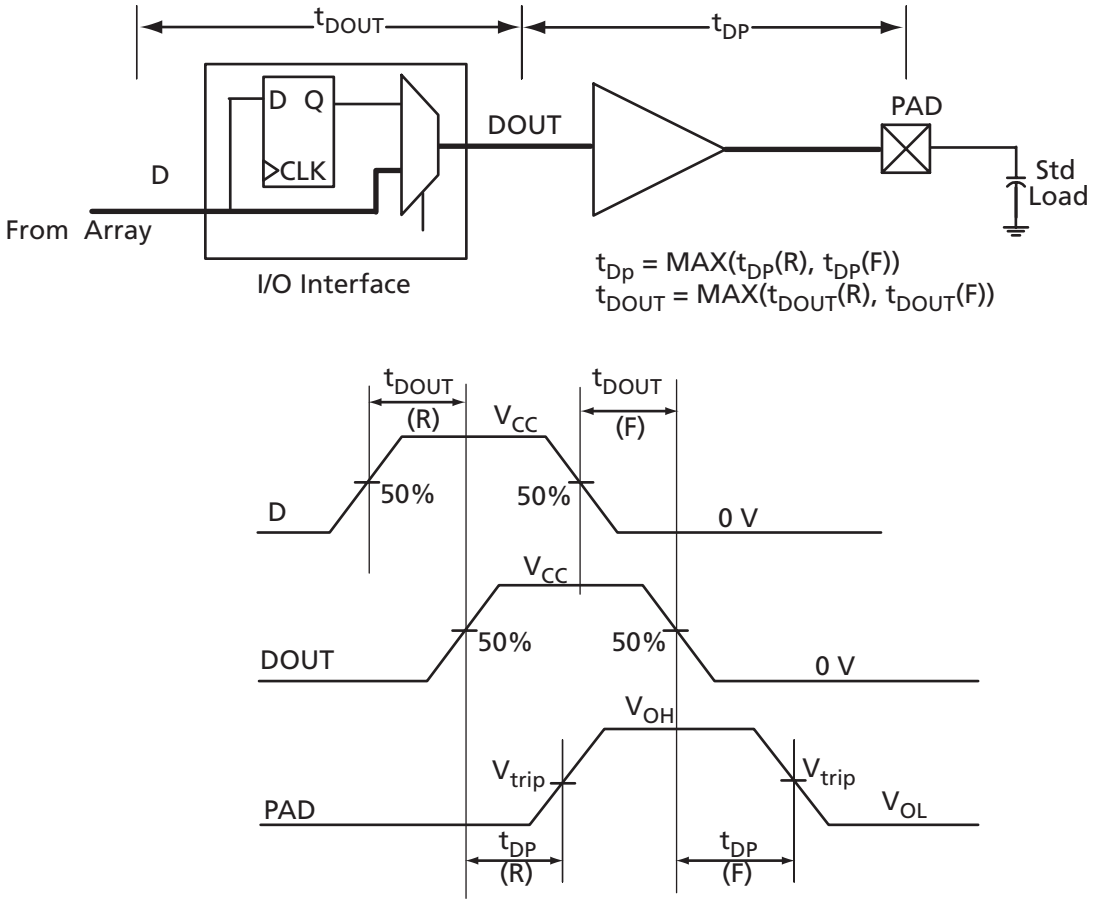

Figure 3-4 • **Output Buffer Model and Delays (example)**

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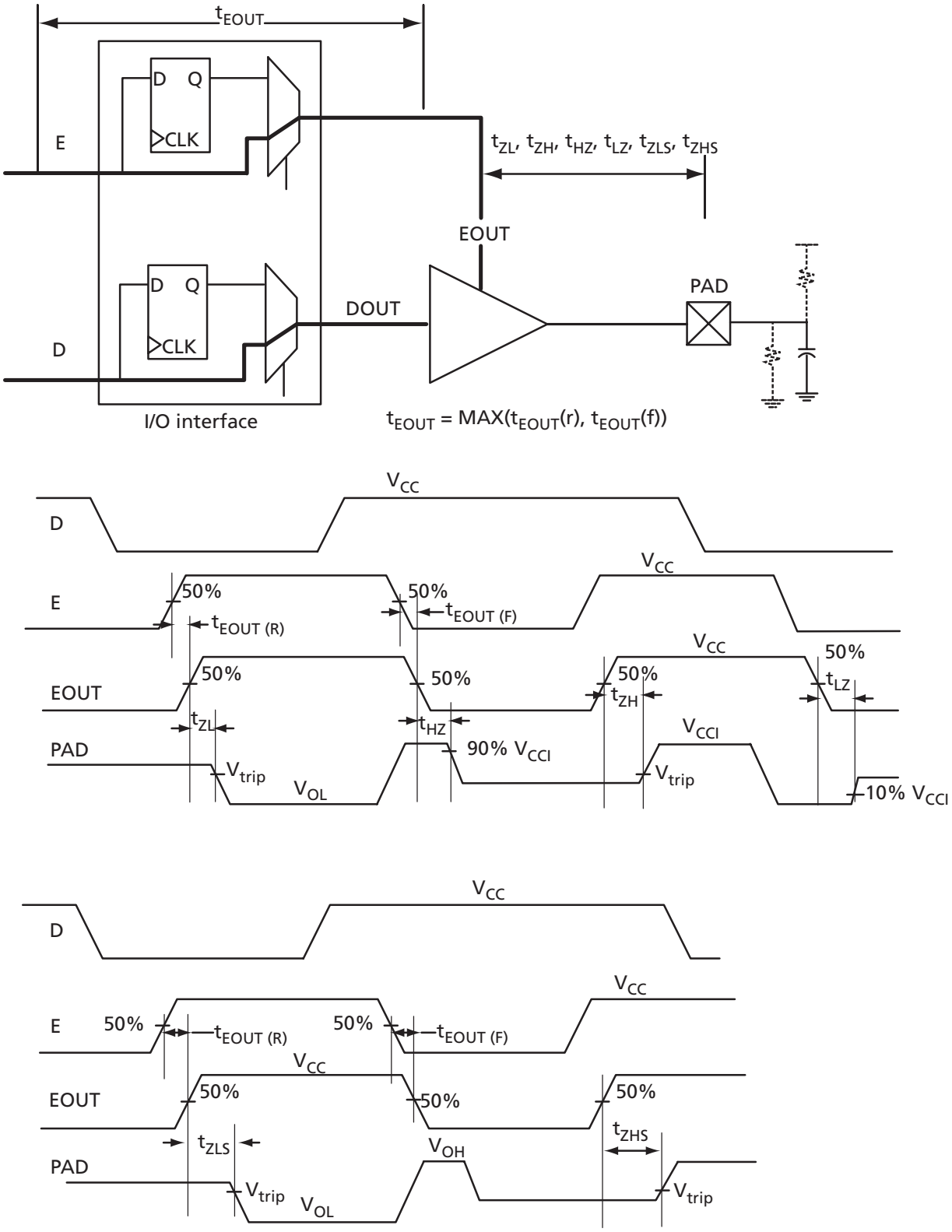

Figure 3-5 • **Tristate Output Buffer Timing Model and Delays (example)**

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Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 3-13 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	51	51
2.5 V GTL+	33 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	40	40
HSTL (I)	8 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output Slew Rates can be extracted from IBIS Models, located at http://www.actel.com/download/ibis/default.aspx.*

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Table 3-14 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 70°C)*
2. *Industrial range (–40°C < T_J < 85°C)*

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Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 3-15 • **Summary of AC Measuring Points**

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL/3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF))
3.3 V PCI-X	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 3-16 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

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Table 3-17 • **Summary of I/O Timing Characteristics—Software Default Settings –2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
2.5 V LVCMOS	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	High	10	25 2	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	High	10	25 2	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	25	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	25	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/BLVDS/ M-LVDS	24	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-35 for connectivity. This resistor is not required during normal operation.*

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Detailed I/O DC Characteristics

Table 3-18 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 3-19 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

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Table 3-19 • **I/O Output Buffer Maximum Resistances[1] (Continued)**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 3-20 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$

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Table 3-21 • **I/O Short Currents I_{OSH}/I_{OSL}**

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Note: **T_J = 100°C*

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The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 3-22 • **Short Current Event Duration before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 3-23 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 3-24 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**[1]

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: **The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

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Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 3-25 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

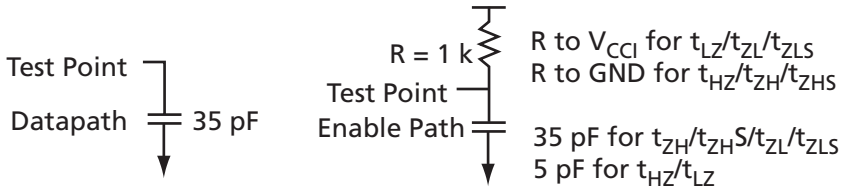

Figure 3-6 • **AC Loading**

Table 3-26 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

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Timing Characteristics

Table 3-27 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	9.47	0.05	1.44	1.88	0.51	9.64	8.05	3.23	3.11	12.33	10.74	ns
	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	–F	0.79	6.10	0.05	1.44	1.88	0.51	6.21	4.98	3.66	3.86	8.90	7.66	ns
	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	–F	0.79	4.41	0.05	1.44	1.88	0.51	4.49	3.45	3.93	4.34	7.17	6.13	ns
	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	–F	0.79	4.16	0.05	1.44	1.88	0.51	4.24	3.13	4.00	4.47	6.92	5.82	ns
	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	–F	0.79	3.85	0.05	1.44	1.88	0.51	3.92	2.59	4.07	4.96	6.61	5.28	ns
	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-28 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	13.22	0.05	1.44	1.88	0.51	13.47	10.87	3.23	2.93	16.16	13.56	ns
	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8 mA	–F	0.79	9.45	0.05	1.44	1.88	0.51	9.62	7.74	3.65	3.68	12.31	10.42	ns
	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12 mA	–F	0.79	7.24	0.05	1.44	1.88	0.51	7.37	6.03	3.93	4.17	10.06	8.72	ns
	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	–F	0.79	6.75	0.05	1.44	1.88	0.51	6.87	5.68	3.99	4.30	9.56	8.36	ns
	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	–F	0.79	6.30	0.05	1.44	1.88	0.51	6.42	5.64	4.07	4.76	9.10	8.32	ns
	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 3-29 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

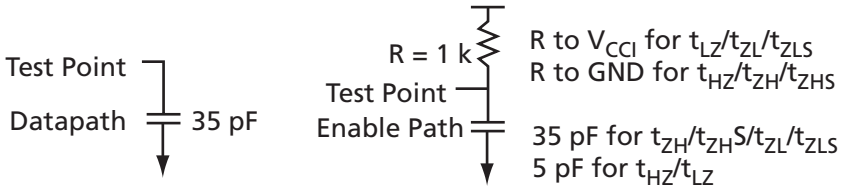

Figure 3-7 • **AC Loading**

Table 3-30 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

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Timing Characteristics

Table 3-31 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	10.59	0.05	1.82	1.99	0.51	9.77	10.59	3.26	2.75	12.45	13.28	ns
	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	–F	0.79	6.33	0.05	1.82	1.99	0.51	6.33	6.33	3.73	3.64	9.02	9.02	ns
	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	–F	0.79	4.50	0.05	1.82	1.99	0.51	4.58	4.19	4.04	4.20	7.27	6.88	ns
	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	–F	0.79	4.24	0.05	1.82	1.99	0.51	4.32	3.75	4.11	4.35	7.00	6.43	ns
	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	–F	0.79	3.92	0.05	1.82	1.99	0.51	3.99	2.98	4.20	4.93	6.68	5.67	ns
	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-32 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	14.42	0.05	1.82	1.99	0.51	14.69	13.95	3.26	2.64	17.37	16.63	ns
	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	–F	0.79	10.49	0.05	1.82	1.99	0.51	10.68	9.62	3.73	3.52	13.37	12.31	ns
	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	–F	0.79	8.14	0.05	1.82	1.99	0.51	8.29	7.34	4.04	4.08	10.97	10.02	ns
	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	–F	0.79	7.58	0.05	1.82	1.99	0.51	7.72	6.88	4.11	4.23	10.40	9.57	ns
	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	–F	0.79	7.13	0.05	1.82	1.99	0.51	7.26	6.85	4.20	4.80	9.94	9.54	ns
	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 3-33 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

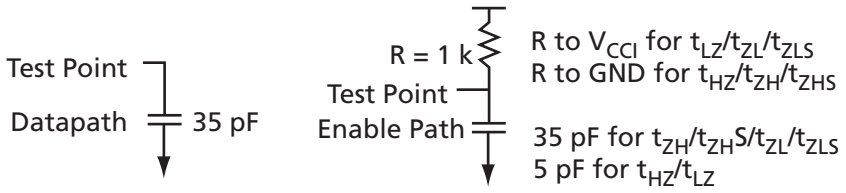

Figure 3-8 • **AC Loading**

Table 3-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

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Timing Characteristics

Table 3-35 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	14.54	0.05	1.74	2.29	0.51	11.52	14.54	3.34	1.97	14.21	17.23	ns
	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	–F	0.79	8.47	0.05	1.74	2.29	0.51	7.45	8.47	3.90	3.44	10.14	11.16	ns
	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	–F	0.79	5.43	0.05	1.74	2.29	0.51	5.36	5.43	4.29	4.17	8.05	8.12	ns
	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	–F	0.79	4.95	0.05	1.74	2.29	0.51	5.04	4.80	4.36	4.35	7.73	7.48	ns
	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-36 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	19.03	0.05	1.74	2.29	0.51	18.80	19.03	3.34	1.90	21.49	21.71	ns
	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	–F	0.79	13.68	0.05	1.74	2.29	0.51	13.94	12.92	3.91	3.33	16.62	15.61	ns
	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	–F	0.79	10.78	0.05	1.74	2.29	0.51	10.98	9.73	4.29	4.03	13.66	12.41	ns
	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	–F	0.79	10.03	0.05	1.74	2.29	0.51	10.22	9.11	4.37	4.23	12.90	11.80	ns
	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 3-37 • **Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

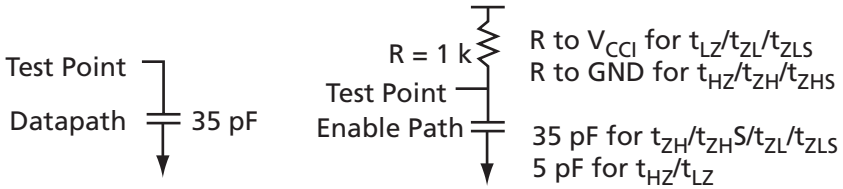

Figure 3-9 • **AC Loading**

Table 3-38 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

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Timing Characteristics

Table 3-39 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	10.25	0.05	2.04	2.58	0.51	8.72	10.25	4.08	3.35	11.41	12.94	ns
	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	–1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	–2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	–F	0.79	6.50	0.05	2.04	2.58	0.51	6.27	6.50	4.51	4.18	8.95	9.19	ns
	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	–1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	–2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	–F	0.79	5.77	0.05	2.04	2.58	0.51	5.88	5.70	4.60	4.41	8.56	8.39	ns
	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	–1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	–2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	–F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	–F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-40 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	16.95	0.05	2.04	2.58	0.51	17.26	15.78	4.09	3.22	19.95	18.47	ns
	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	–F	0.79	13.49	0.05	2.04	2.58	0.51	13.74	11.85	4.53	4.03	16.43	14.54	ns
	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	–F	0.79	12.56	0.05	2.04	2.58	0.51	12.79	11.10	4.62	4.26	15.48	13.79	ns
	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 3-41 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 3-10.

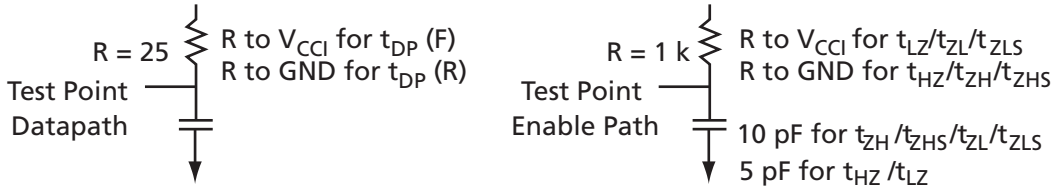

Figure 3-10 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 3-42.

Table 3-42 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	–	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-43 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.37	0.05	1.26	2.01	0.51	3.43	2.40	3.93	4.34	6.12	5.08	ns
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 3-44 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

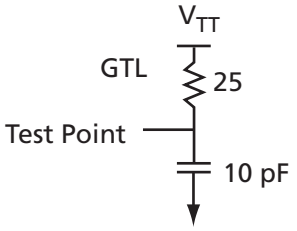

Figure 3-11 • **AC Loading**

Table 3-45 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-46 • **3.3 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.49	0.05	3.52	0.51	2.45	2.49			5.13	5.18	ns
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
–1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
–2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V

Table 3-47 • **Minimum and Maximum DC Input and Output Levels**

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

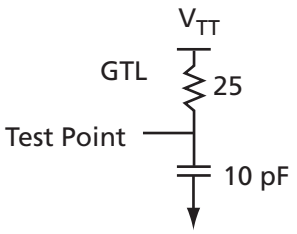

Figure 3-12 • **AC Loading**

Table 3-48 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-49 • **2.5 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.56	0.05	2.95	0.51	2.60	2.56			5.28	5.24	ns
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
–1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
–2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V

Table 3-50 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
35 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

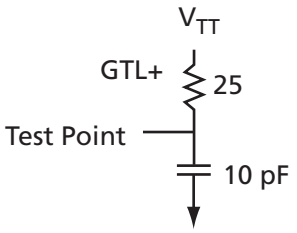

Figure 3-13 • **AC Loading**

Table 3-51 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-52 • **3.3 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.47	0.05	1.91	0.51	2.51	2.47			5.20	5.15	ns
Std.	0.60	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.51	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.45	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 3-53 • **Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
33 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

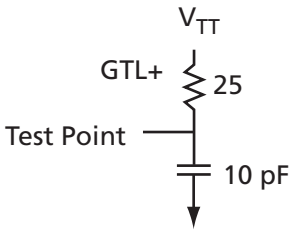

Figure 3-14 • **AC Loading**

Table 3-54 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-55 • **2.5 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.65	0.05	1.82	0.51	2.70	2.52			5.38	5.21	ns
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
–1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
–2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-56 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
8 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI}-0.4	8	8	39	32	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

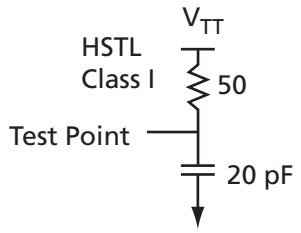

Figure 3-15 • **AC Loading**

Table 3-57 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-58 • **HSTL Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.82	0.05	2.55	0.51	3.89	3.78			6.58	6.46	ns
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-59 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
15 mA[3]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI}-0.4	15	15	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

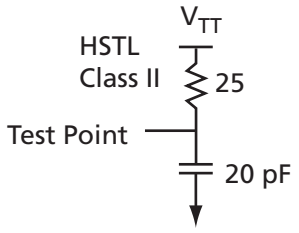

Figure 3-16 • **AC Loading**

Table 3-60 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-61 • **HSTL Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.63	0.05	2.55	0.51	3.70	3.26			6.39	5.95	ns
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-62 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
15 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} - 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

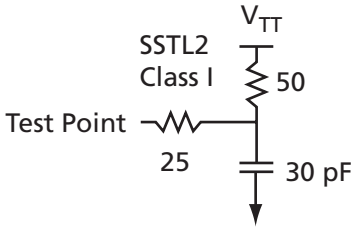

Figure 3-17 • **AC Loading**

Table 3-63 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-64 • **SSTL 2 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.56	0.05	1.60	0.51	2.60	2.22			5.29	4.90	ns
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-65 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
18 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

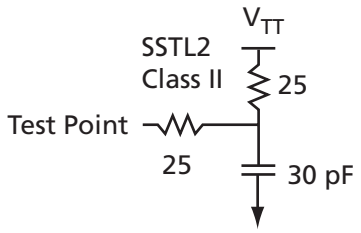

Figure 3-18 • **AC Loading**

Table 3-66 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-67 • **SSTL 2 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	0.79	2.60	0.05	1.60	0.51	2.65	2.13			5.34	ns
Std.	0.66	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	ns
–1	0.56	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	ns
–2	0.49	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-68 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	54	51	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

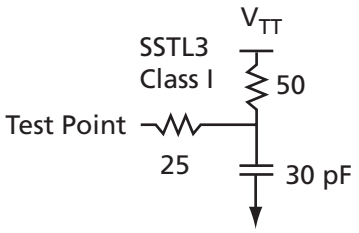

Figure 3-19 • **AC Loading**

Table 3-69 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-70 • **SSTL3 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.77	0.05	1.50	0.51	2.82	2.21			5.51	4.89	ns
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
–1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
–2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-71 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
21 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

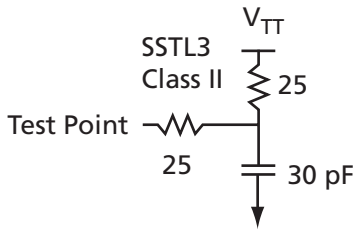

Figure 3-20 • **AC Loading**

Table 3-72 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-73 • **SSTL3 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.48	0.05	1.50	0.51	2.53	2.01			5.21	4.69	ns
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-21. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

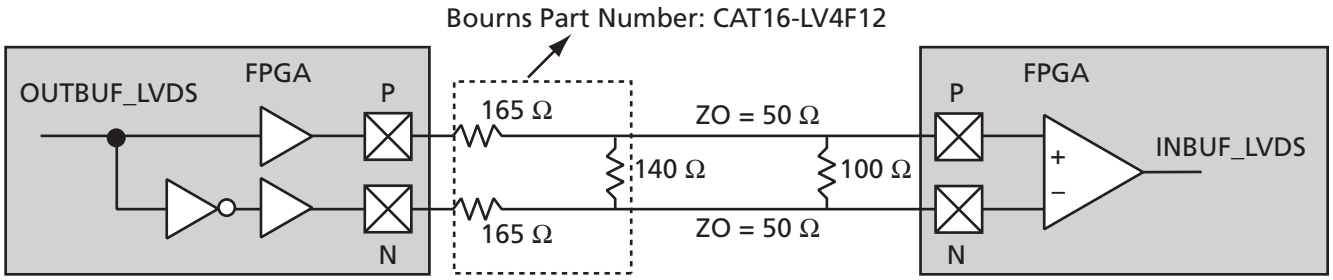

Figure 3-21 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 3-74 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output LOW Voltage	0.9	1.075	1.25	V
V_{OH}	Output HIGH Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0	–	2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common-Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350	–	mV

Notes:

1. *± 5%*
2. *Differential input voltage = ±350 mV*

Table 3-75 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

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Timing Characteristics

Table 3-76 • **LVDS**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.79	2.25	0.05	2.18	ns
Std.	0.66	1.87	0.04	1.82	ns
–1	0.56	1.59	0.04	1.55	ns
–2	0.49	1.40	0.03	1.36	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 3-22. The input and output buffer delays are available in the LVDS section in Table 3-76.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

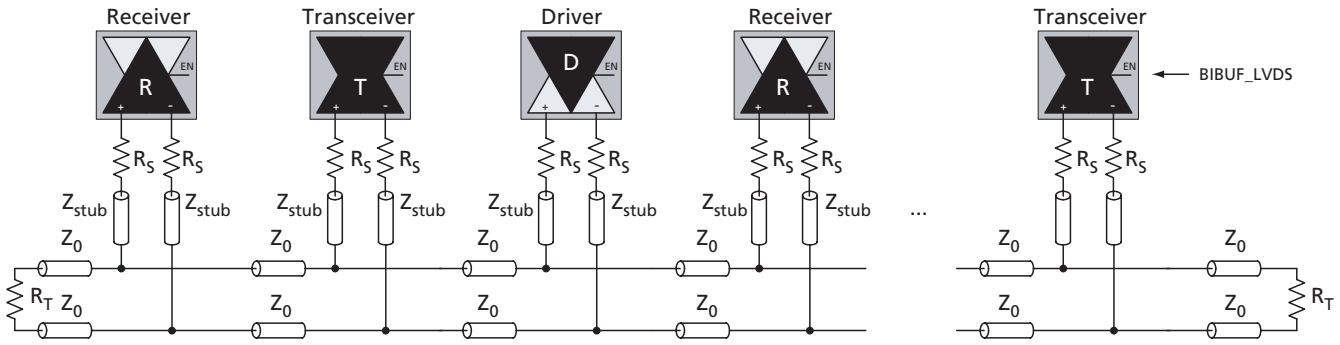

Figure 3-22 • **BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

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LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-23. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

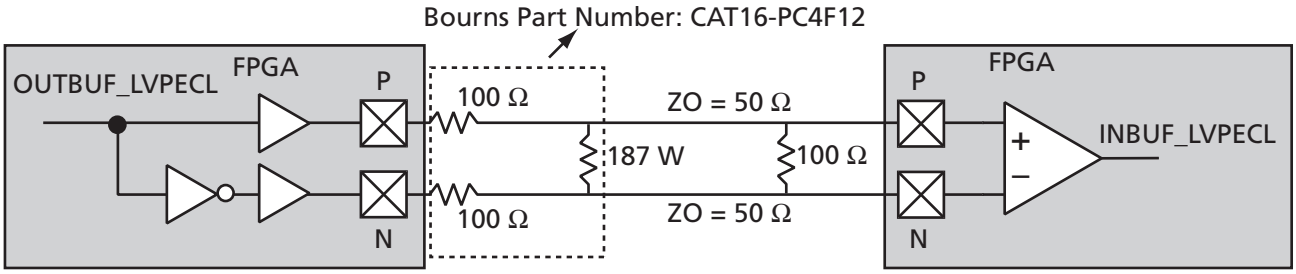

Figure 3-23 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 3-77 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 3-78 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-79 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.79	2.19	0.05	1.96	ns
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

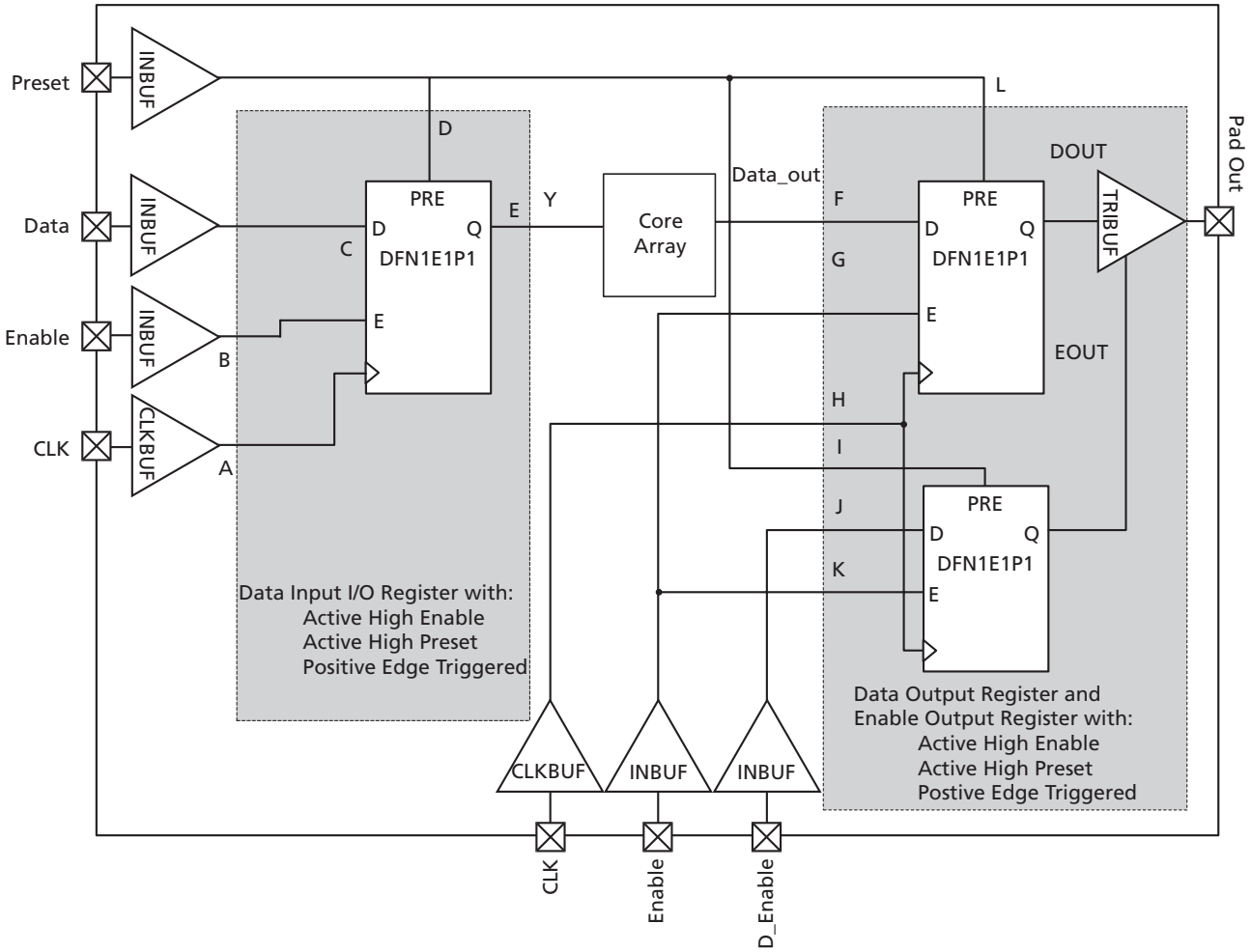

Figure 3-24 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

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Table 3-80 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: **See Figure 3-24 on page 3-49 for more information.*

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Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

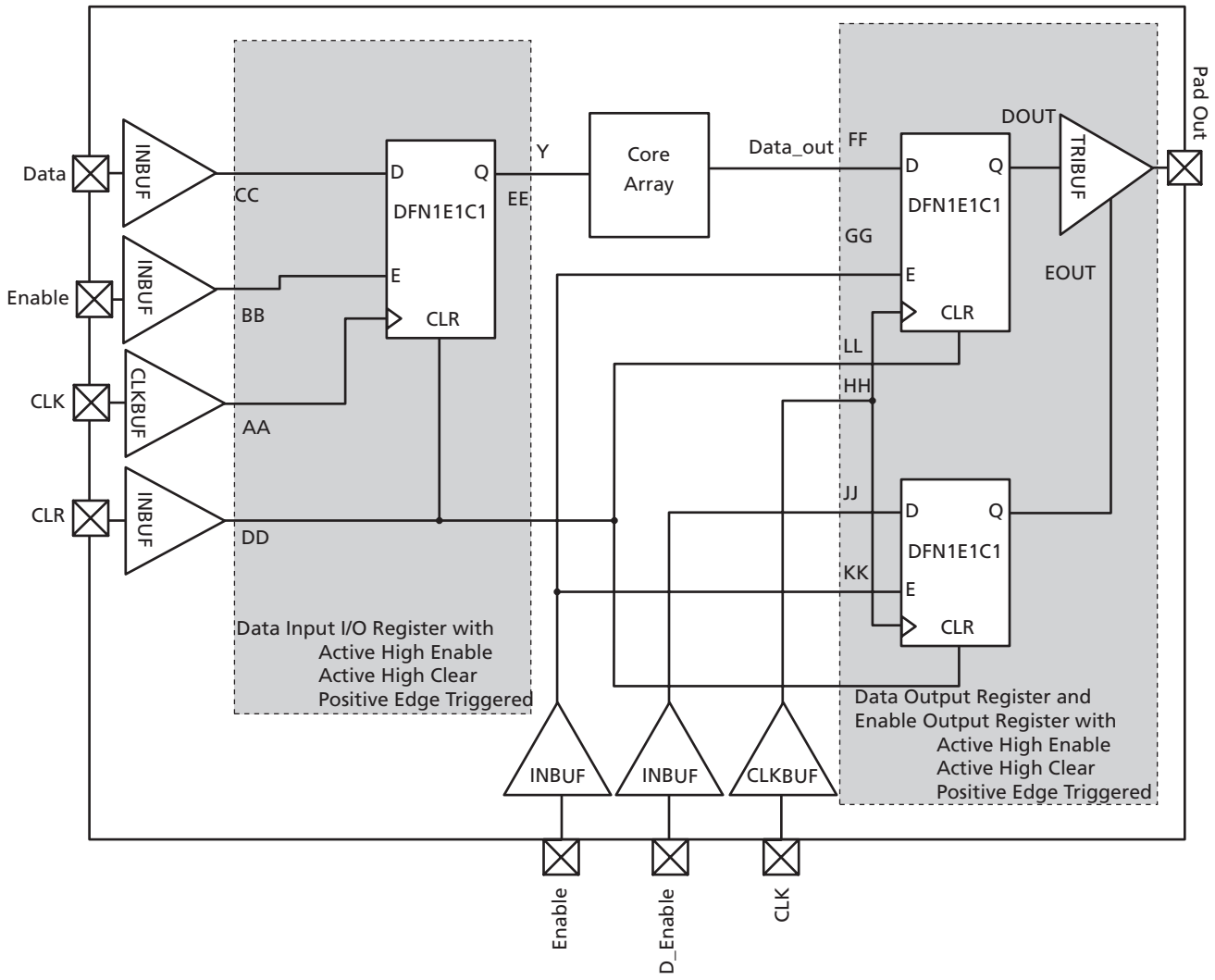

Figure 3-25 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

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Table 3-81 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: **See Figure 3-25 on page 3-51 for more information.*

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Input Register

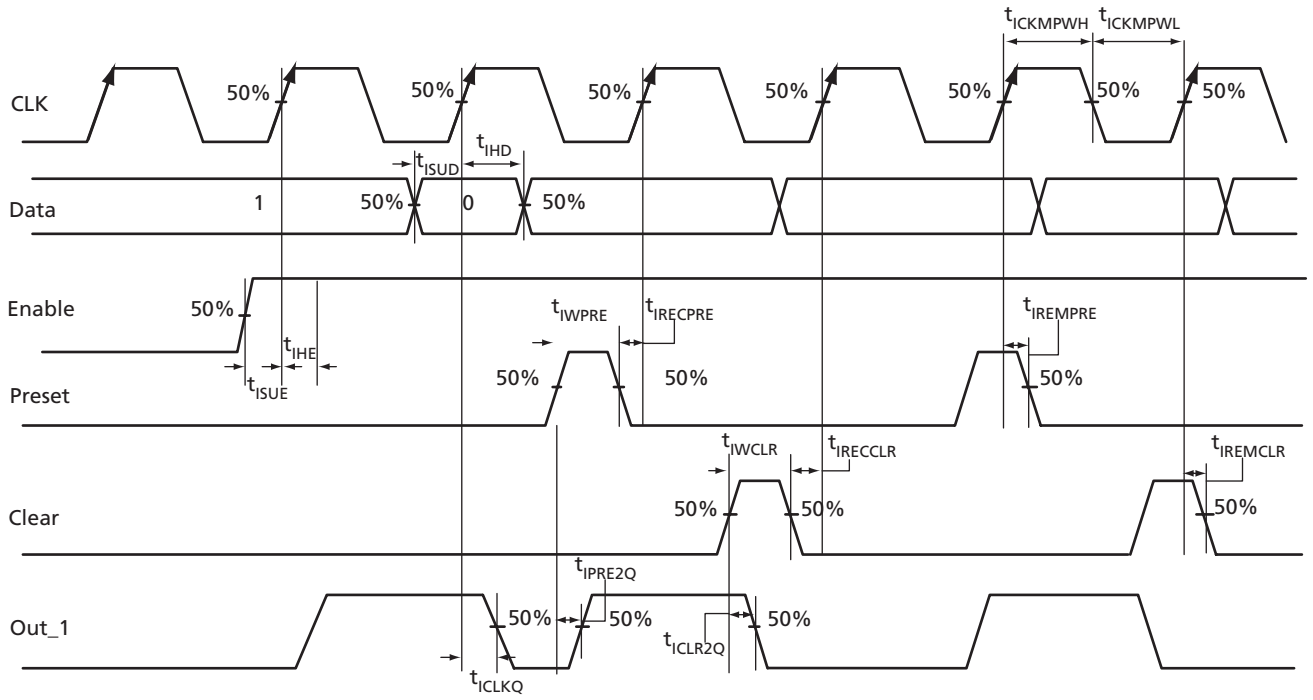

Figure 3-26 • **Input Register Timing Diagram**

Timing Characteristics

Table 3-82 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	0.38	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	0.42	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	0.60	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	0.73	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	0.73	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.36	0.41	0.48	0.57	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.32	0.37	0.43	0.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Output Register

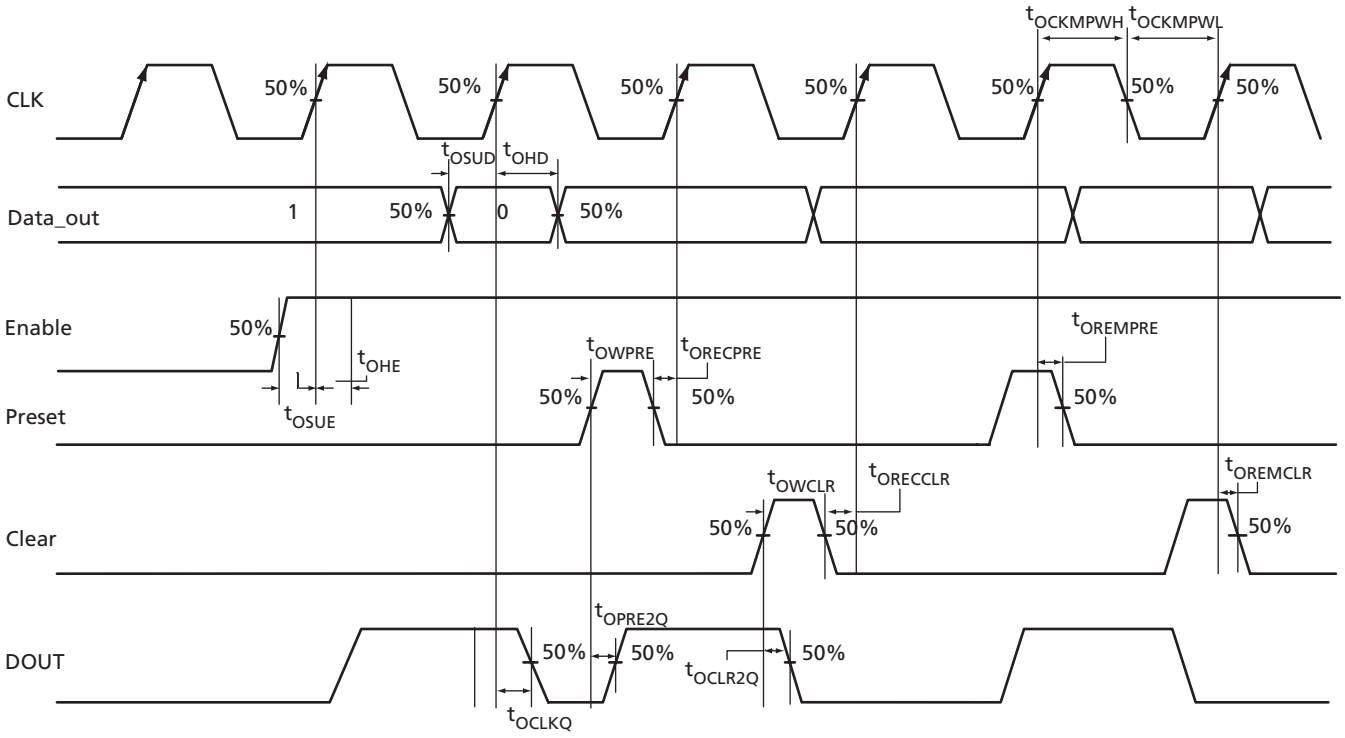

Figure 3-27 • **Output Register Timing Diagram**

Timing Characteristics

Table 3-83 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	0.95	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	0.50	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	1.29	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	1.29	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	0.36	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	0.36	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	0.36	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.36	0.41	0.48	0.57	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.32	0.37	0.43	0.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Output Enable Register

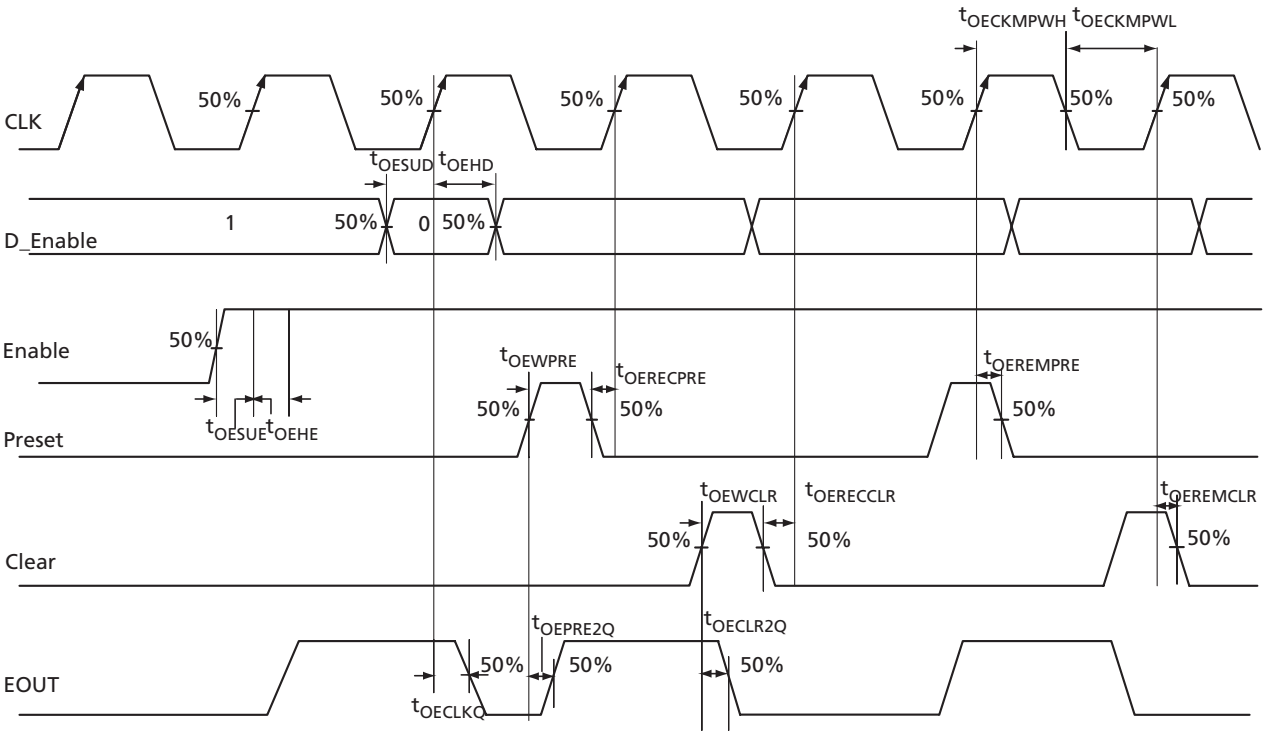

Figure 3-28 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 3-84 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	0.95	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	0.50	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	0.70	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	1.07	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	1.07	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	0.36	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.36	0.41	0.48	0.57	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.32	0.37	0.43	0.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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DDR Module Specifications

Input DDR Module

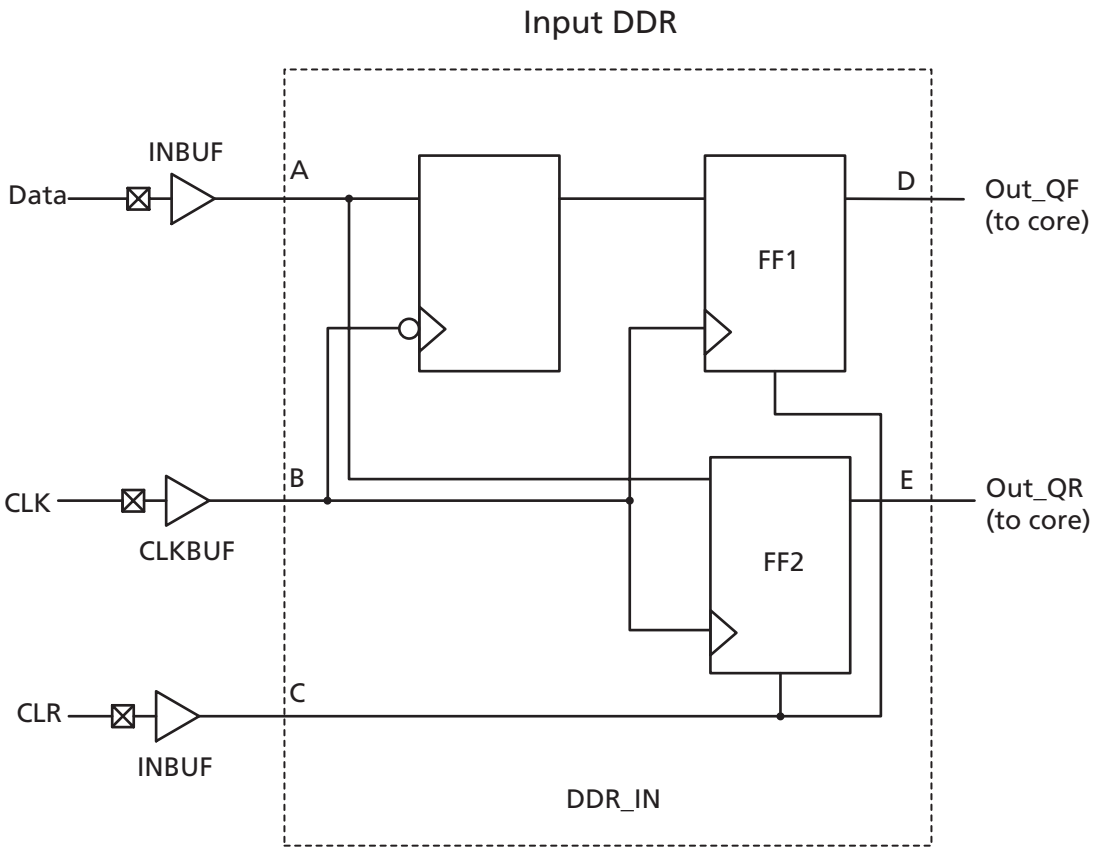

Figure 3-29 • **Input DDR Timing Model**

Table 3-85 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

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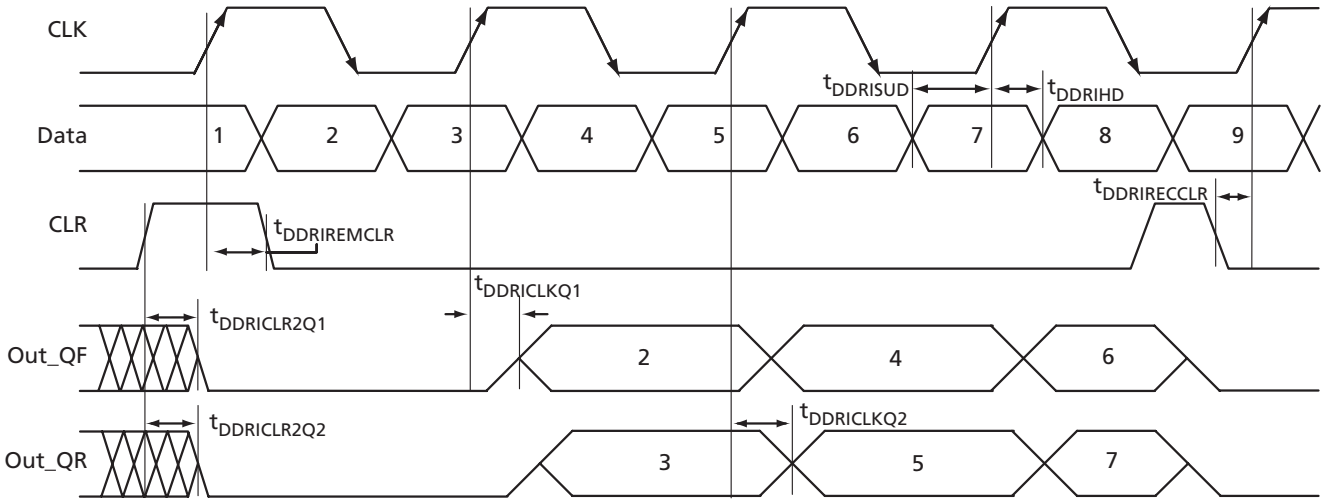

Figure 3-30 • **Input DDR Timing Diagram**

Timing Characteristics

Table 3-86 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.39	0.44	0.52	0.62	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.27	0.31	0.37	0.44	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.28	0.32	0.38	0.45	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.57	0.65	0.76	0.92	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.46	0.53	0.62	0.74	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.36	0.41	0.48	0.57	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.32	0.37	0.43	0.52	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	1404	1232	1048	871	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Output DDR Module

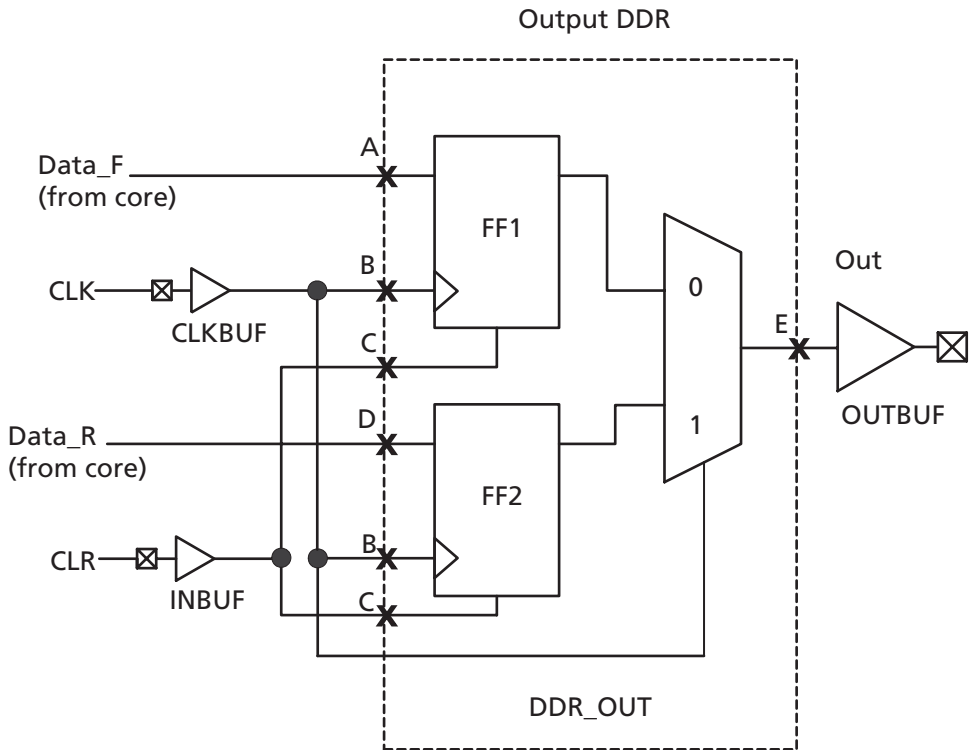

Figure 3-31 • **Output DDR Timing Model**

Table 3-87 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

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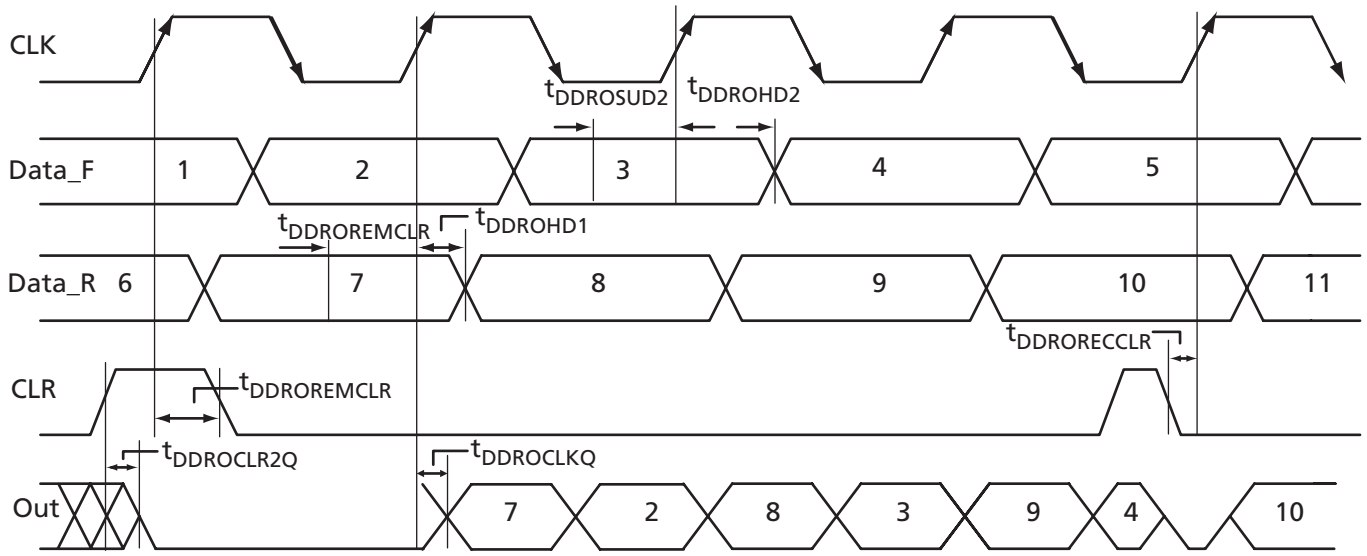

Figure 3-32 • **Output DDR Timing Diagram**

Timing Characteristics

Table 3-88 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	1.13	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	0.43	0.51	0.61	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	0.43	0.51	0.61	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	1.29	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	0.36	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	0.36	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.36	0.41	0.48	0.57	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.32	0.37	0.43	0.52	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	1404	1232	1048	871	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

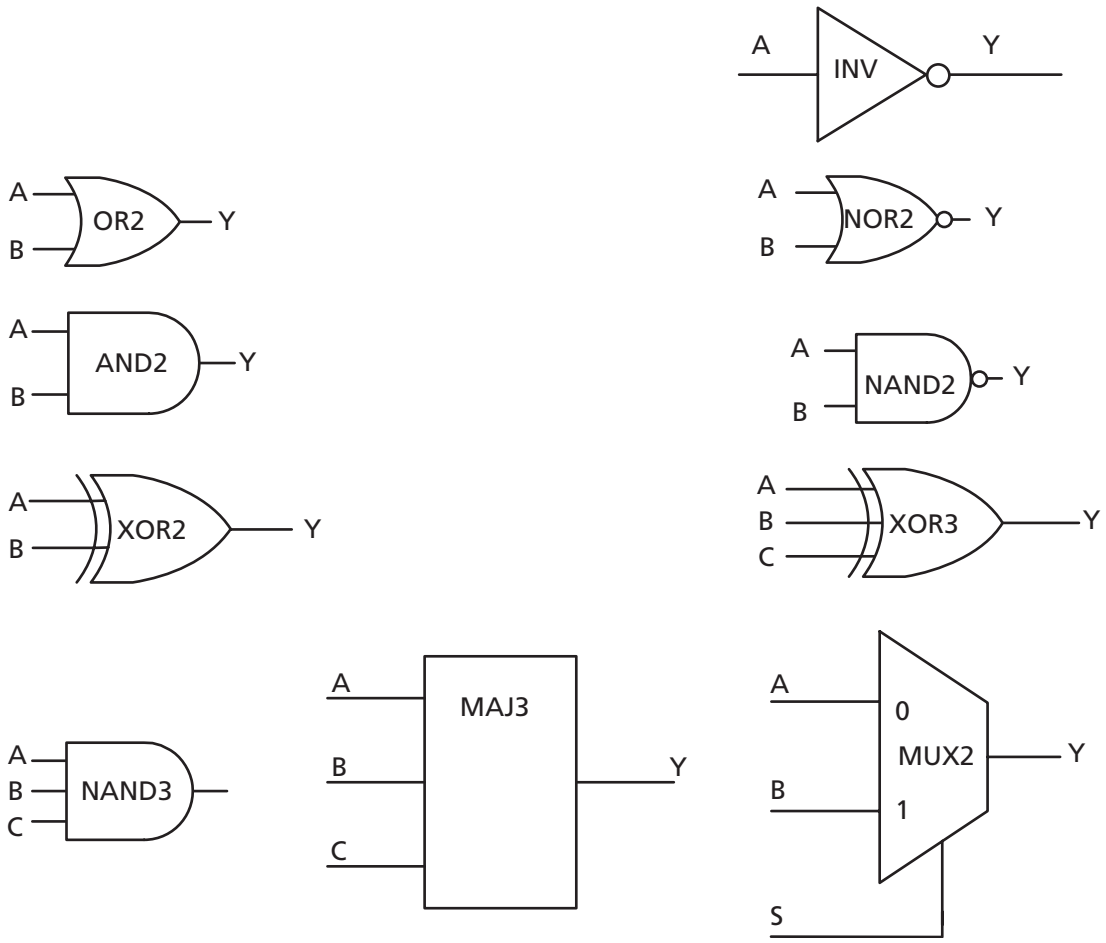

Figure 3-33 • **Sample of Combinatorial Cells**

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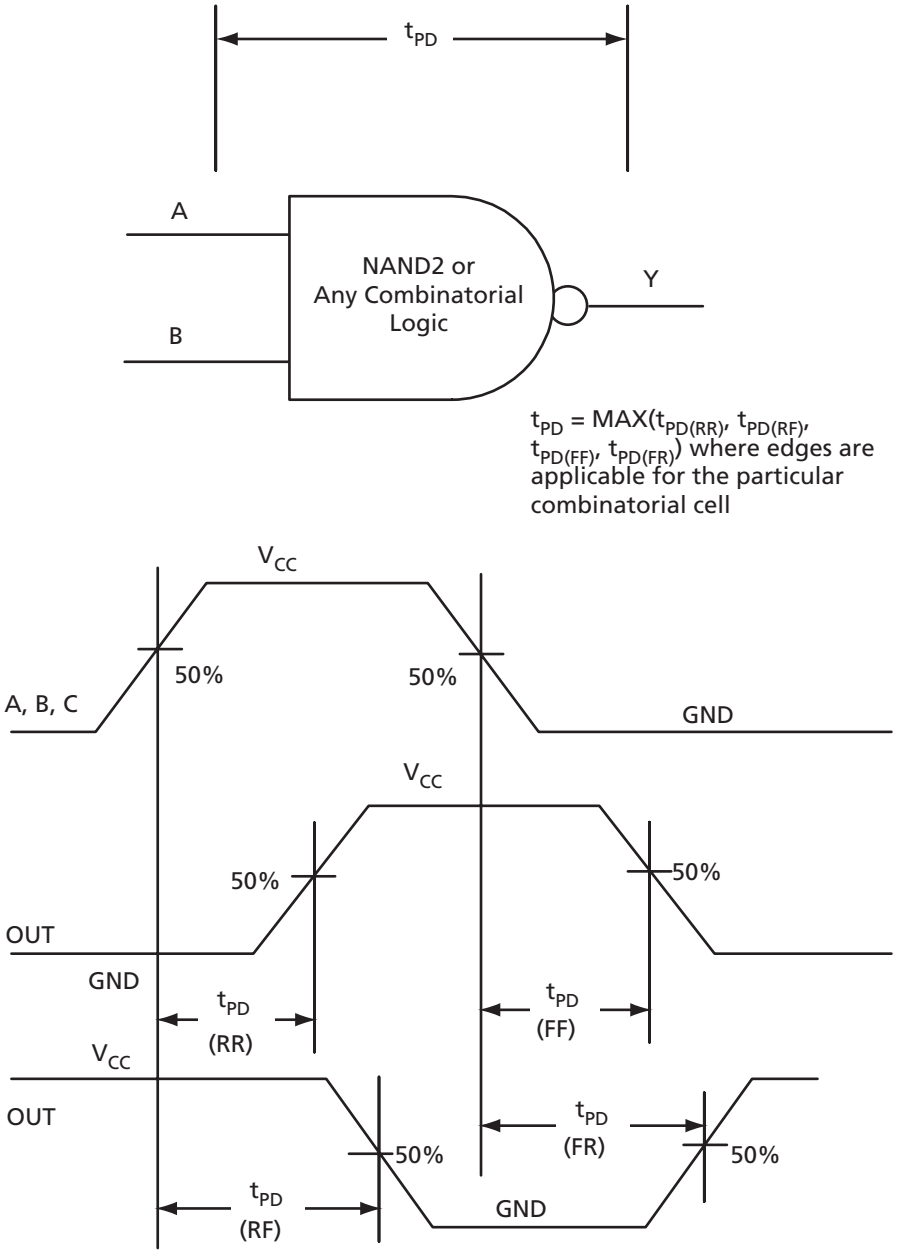

Figure 3-34 • **Timing Model and Waveforms**

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Timing Characteristics

Table 3-89 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	–F	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	0.65	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	0.76	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	0.76	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	0.78	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	0.78	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	1.19	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.70	0.79	0.93	1.12	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	1.41	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	0.81	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	0.90	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

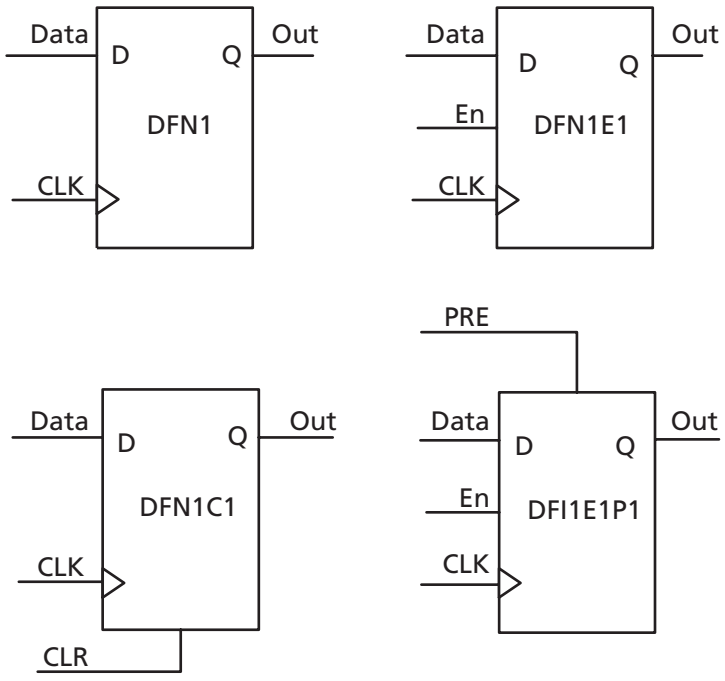

Figure 3-35 • **Sample of Sequential Cells**

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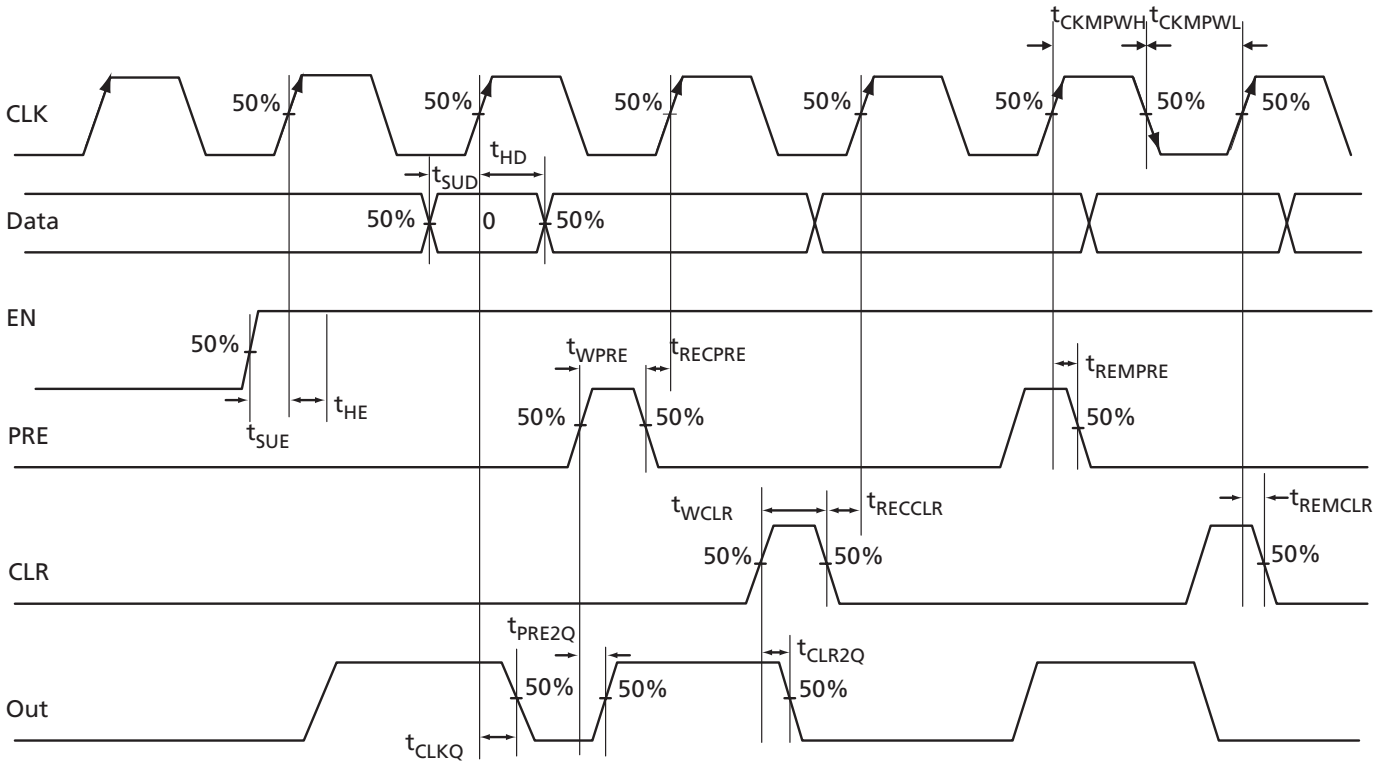

Figure 3-36 • **Timing Model and Waveforms**

Timing Characteristics

Table 3-90 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	0.69	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	0.36	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.32	0.37	0.43	0.52	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.36	0.41	0.48	0.57	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 3-37 is an example of a global tree used for clock routing. The global tree presented in Figure 3-37 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.

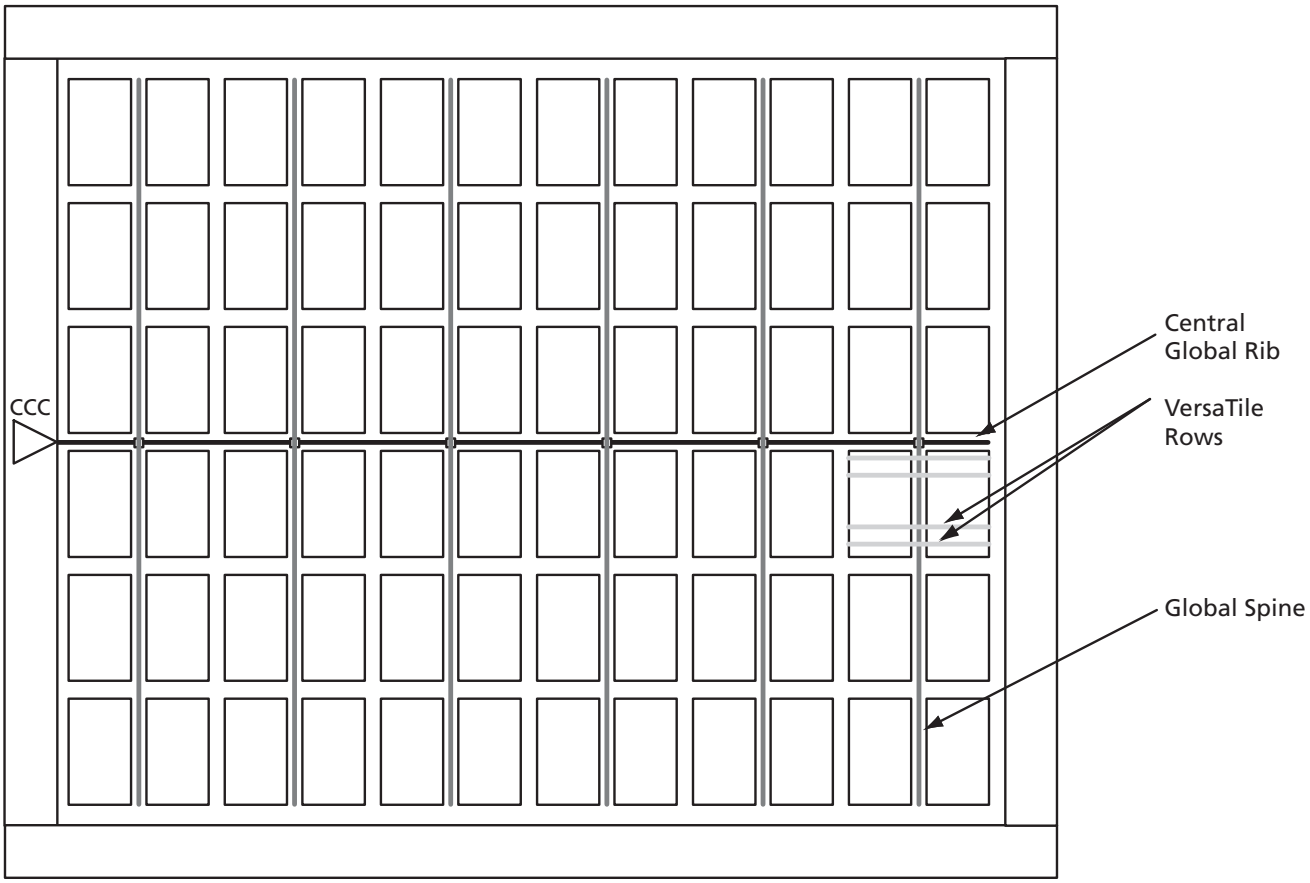

Figure 3-37 • **Example of Global Tree Use in an A3PE600 Device for Clock Routing**

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Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-13. Table 3-91, Table 3-92, and Table 3-93 on page 3-66 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 3-91 • **A3PE600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.83	1.04	0.94	1.18	1.11	1.39	1.33	1.67	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.81	1.06	0.93	1.21	1.09	1.42	1.31	1.71	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.25		0.28		0.33		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-92 • **A3PE1500 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.07	1.29	1.22	1.47	1.43	1.72	1.72	2.07	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.06	1.32	1.21	1.50	1.42	1.76	1.71	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-93 • **A3PE3000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.41	1.62	1.60	1.85	1.88	2.17	2.26	2.61	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.40	1.66	1.59	1.89	1.87	2.22	2.25	2.66	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Embedded SRAM and FIFO Characteristics

SRAM

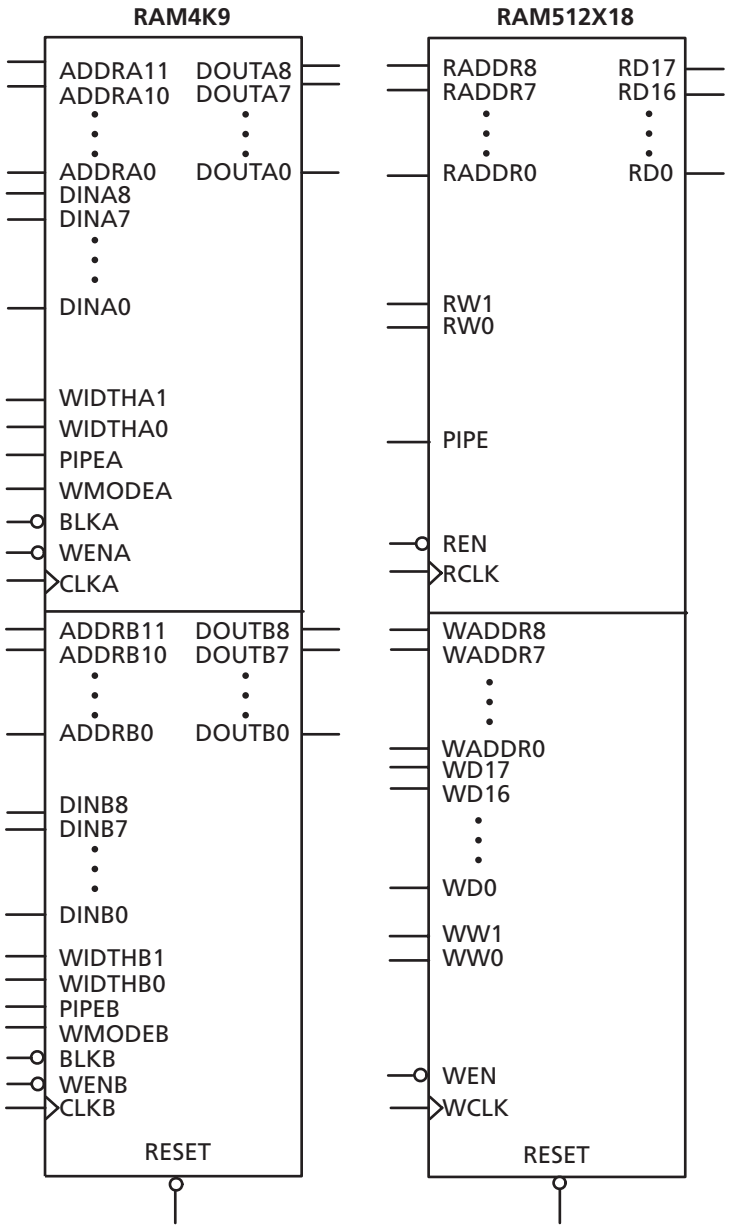

Figure 3-38 • **RAM Models**

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Timing Waveforms

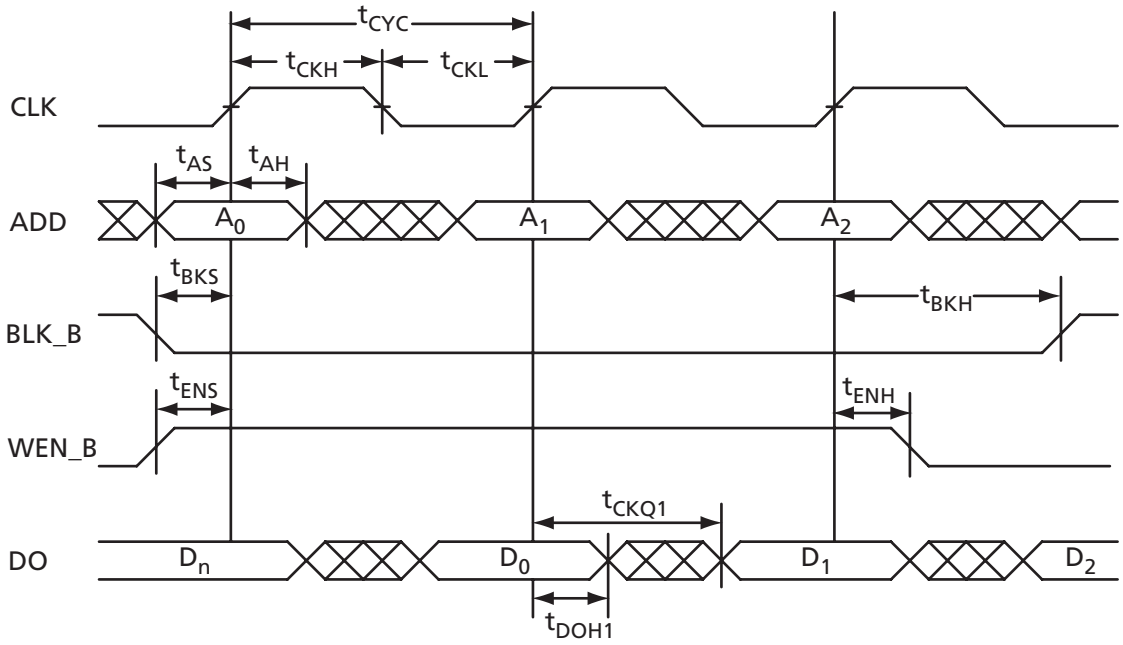

Figure 3-39 • **RAM Read for Pass-Through Output**

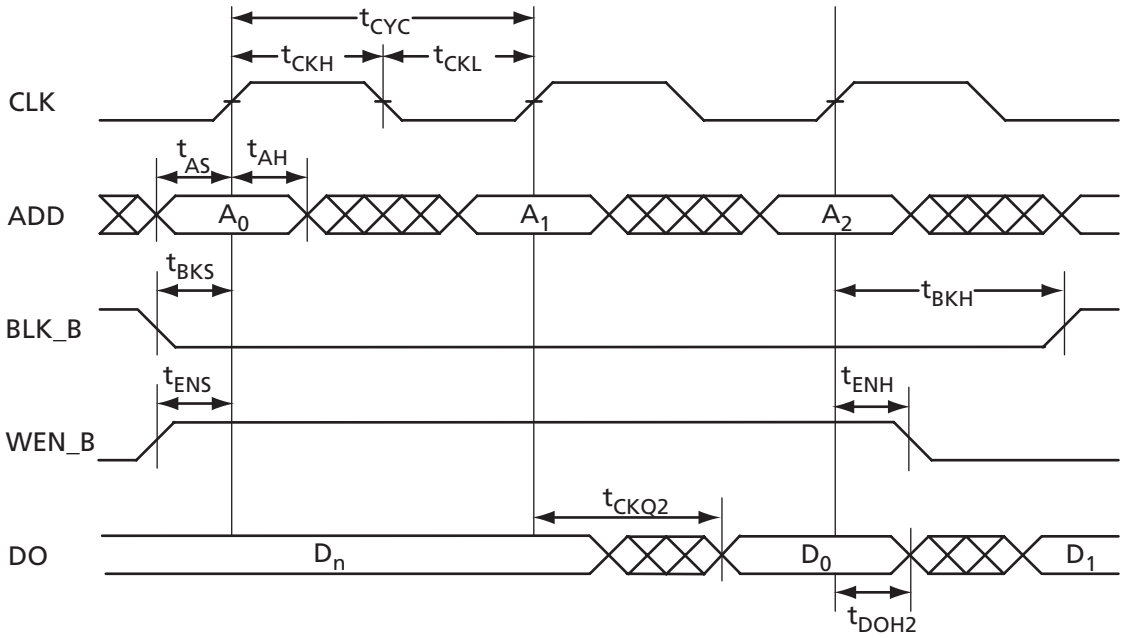

Figure 3-40 • **RAM Read for Pipelined Output**

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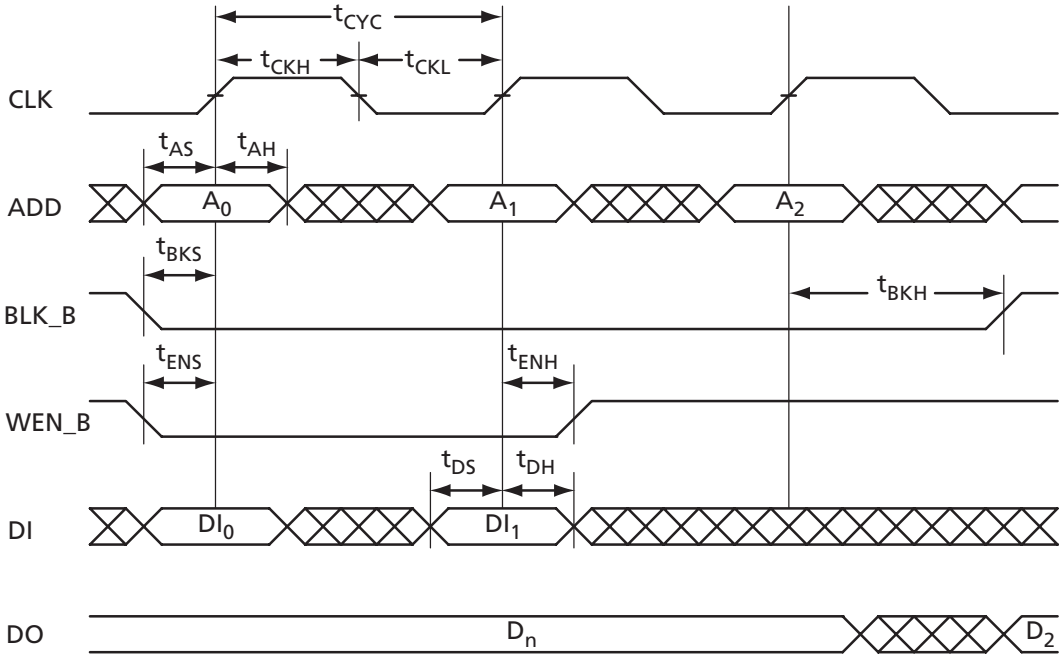

Figure 3-41 • **RAM Write, Output Retained (WMODE = 0)**

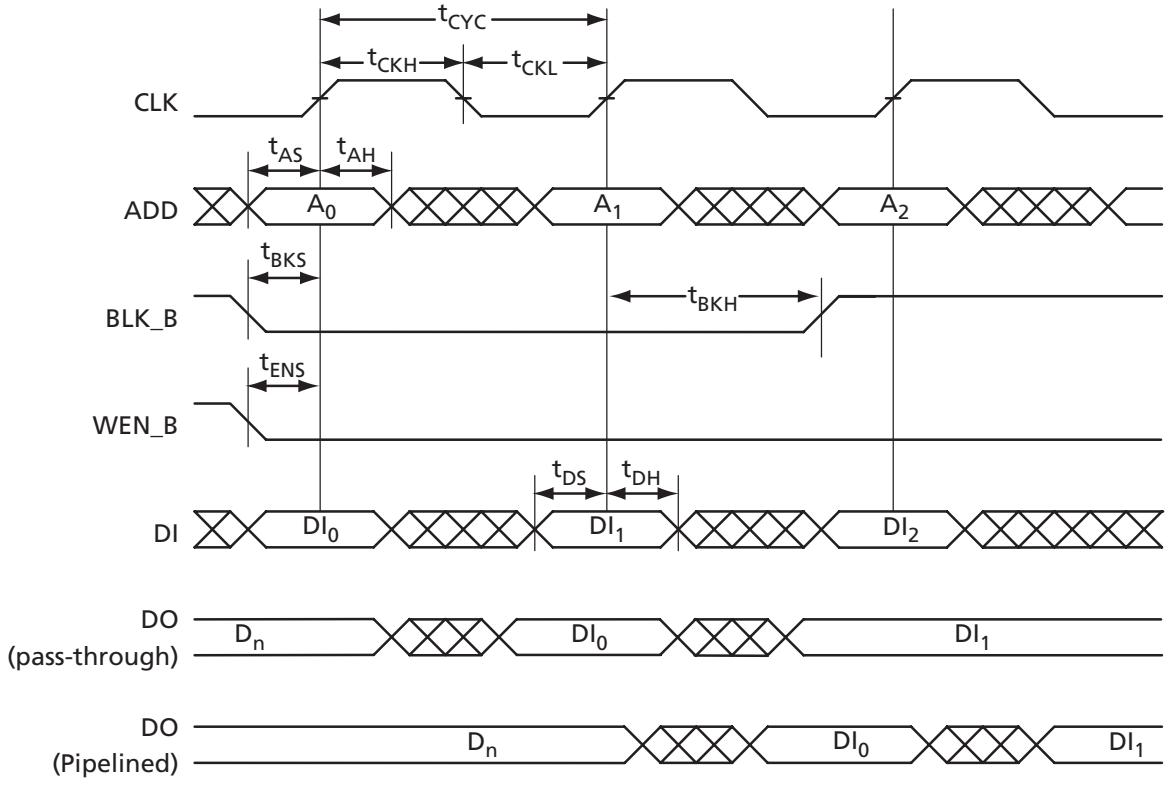

Figure 3-42 • **RAM Write, Output as Write Data (WMODE = 1)**

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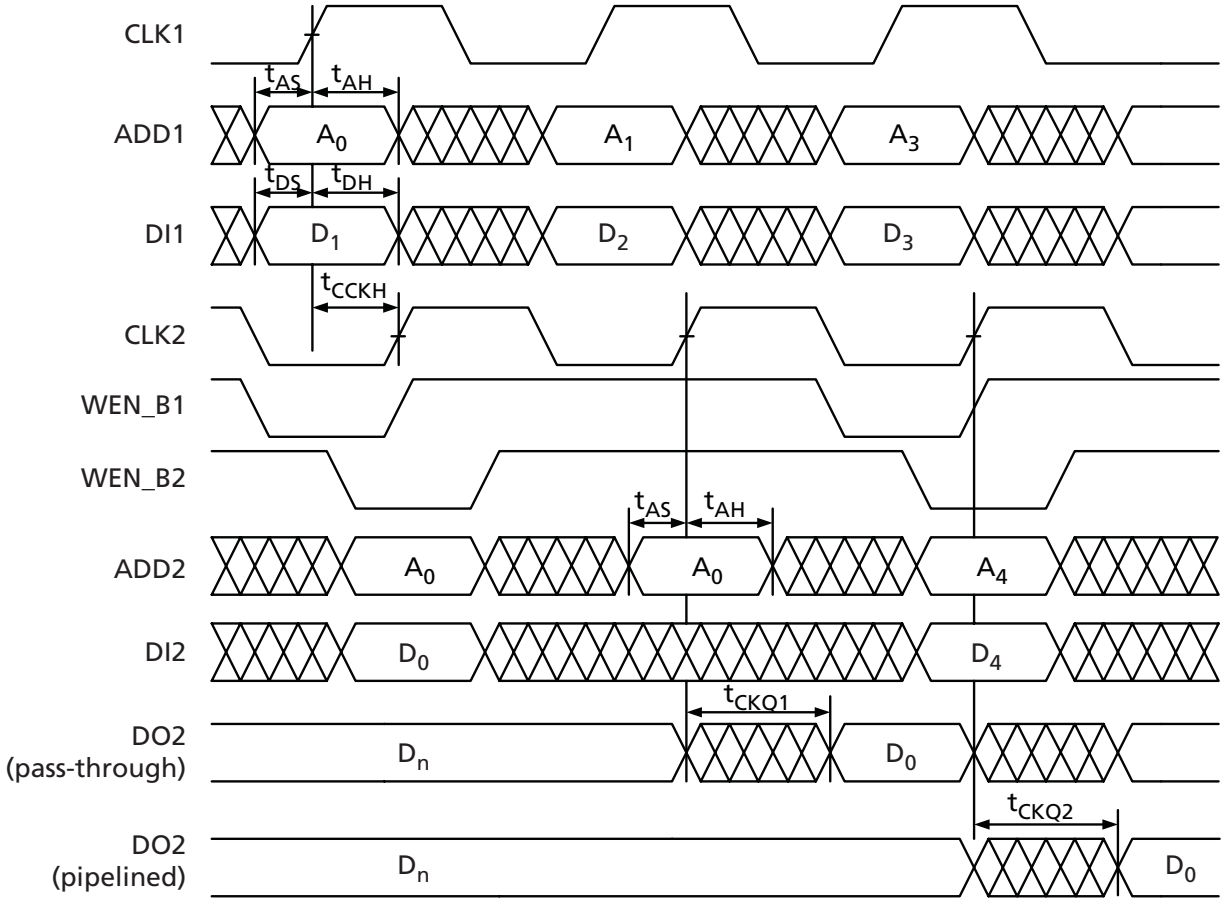

Figure 3-43 • **Write Access After Write onto Same Address**

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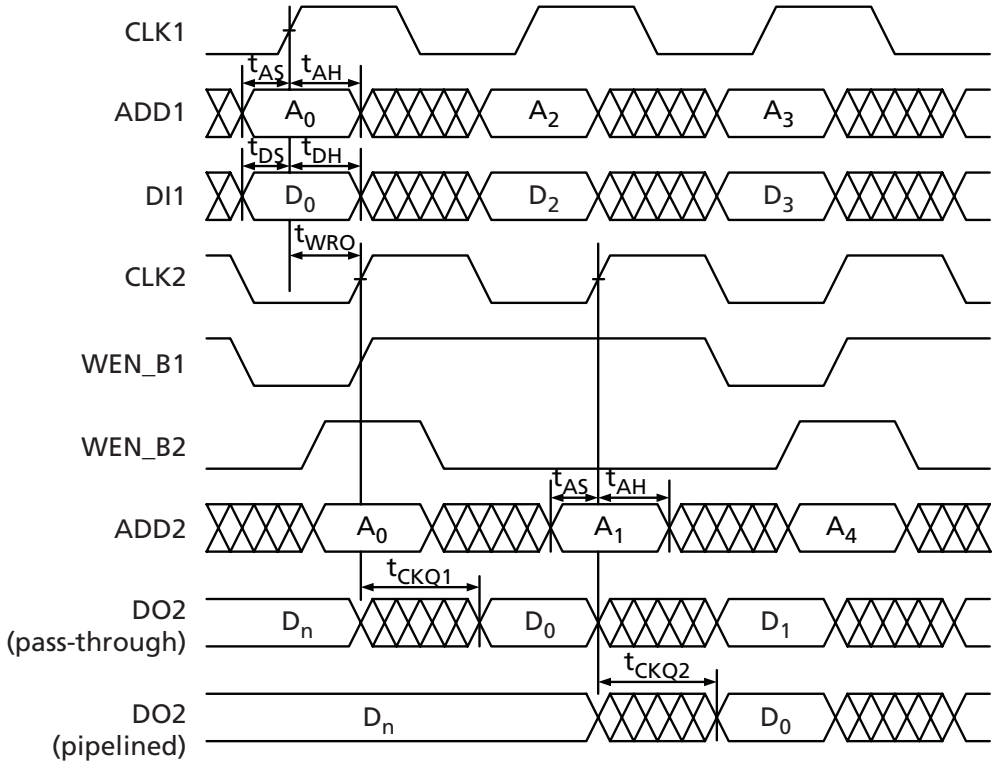

Figure 3-44 • **Read Access After Write onto Same Address**

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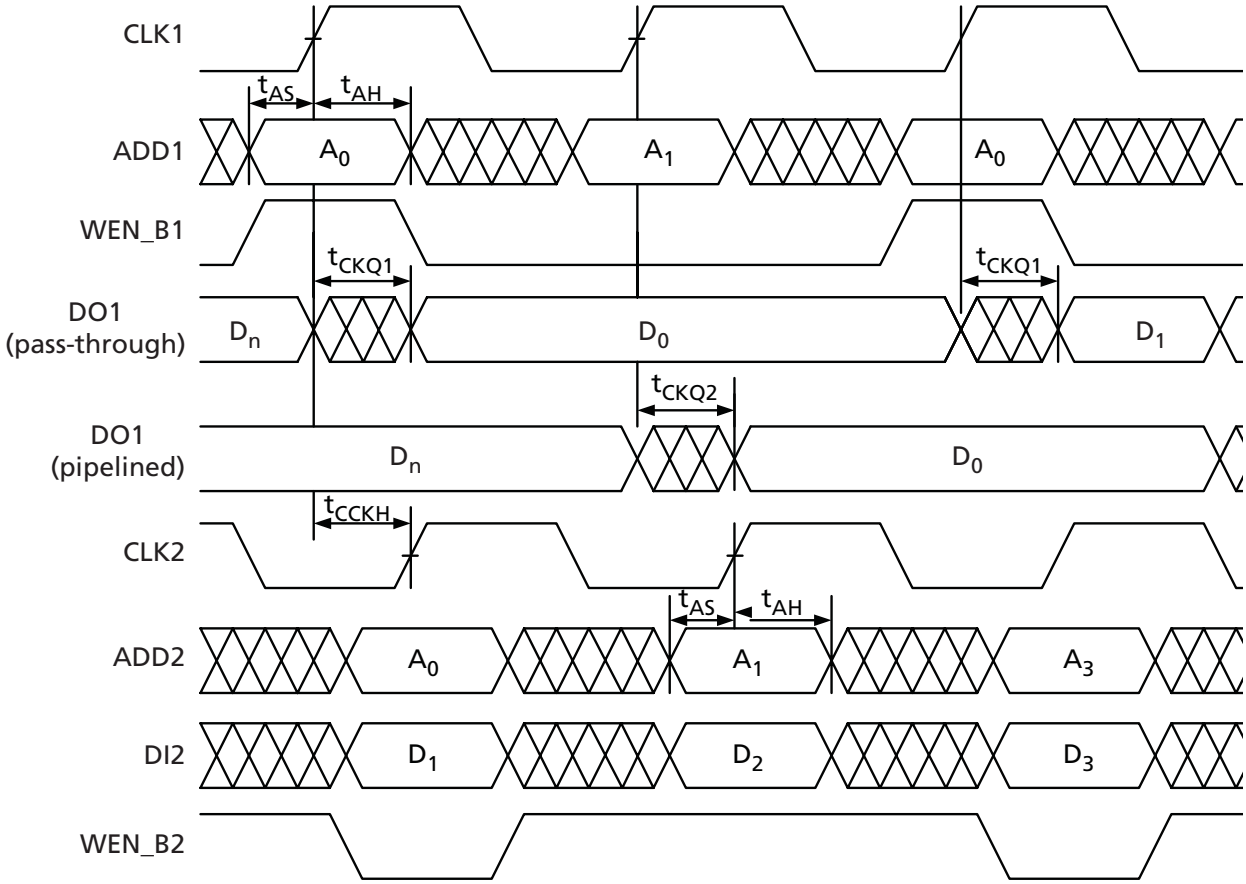

Figure 3-45 • **Write Access After Read onto Same Address**

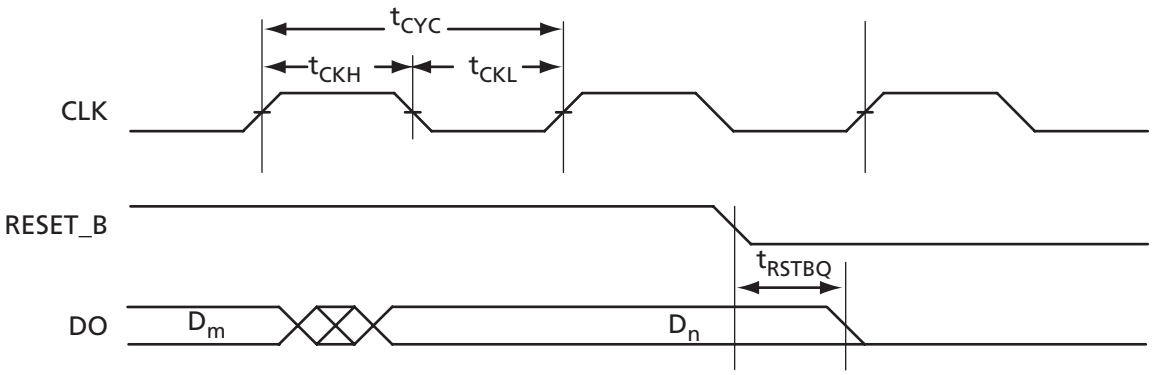

Figure 3-46 • **RAM Reset**

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Timing Characteristics

Table 3-94 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup Time	0.25	0.28	0.33	0.40	ns
t_{AH}	Address Hold Time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.14	0.16	0.19	0.23	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.10	0.11	0.13	0.16	ns
t_{BKS}	BLK_B Setup Time	0.23	0.27	0.31	0.37	ns
t_{BKH}	BLK_B Hold Time	0.02	0.02	0.02	0.03	ns
t_{DS}	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	1.79	2.03	2.39	2.87	ns
	Clock HIGH to New Data Valid on DO (pass-through, WMODE = 1)	2.36	2.68	3.15	3.79	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
$t_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F_{MAX}	Maximum Frequency	310	272	231	193	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Table 3-95 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup Time	0.25	0.28	0.33	0.40	ns
t_{AH}	Address Hold Time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.18	0.20	0.24	0.28	ns
t_{ENH}	REB_B, WEN_B Hold Time	0.06	0.07	0.08	0.09	ns
t_{DS}	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.16	2.46	2.89	3.47	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.90	1.02	1.20	1.44	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
$t_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F_{MAX}	Maximum Frequency	310	272	231	193	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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FIFO

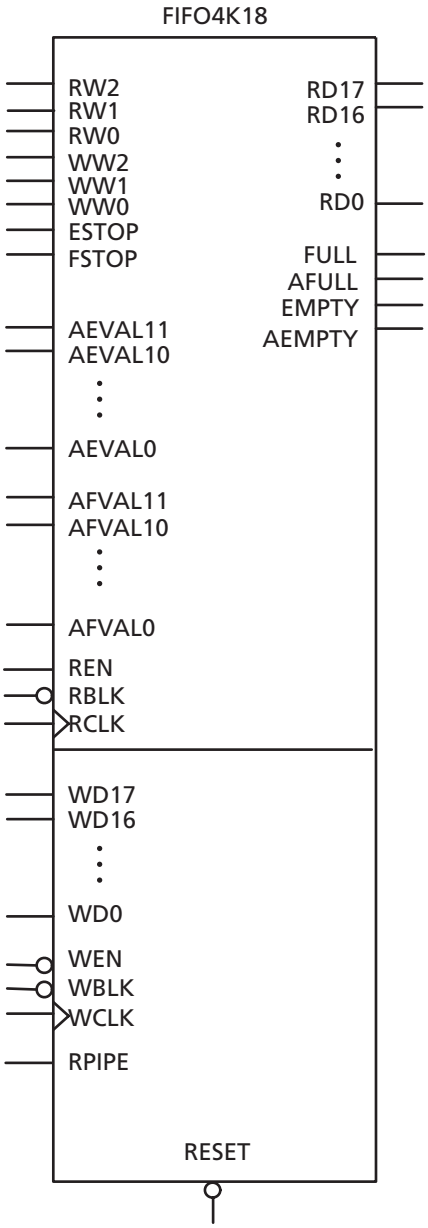

Figure 3-47 • **FIFO Model**

Timing Waveforms

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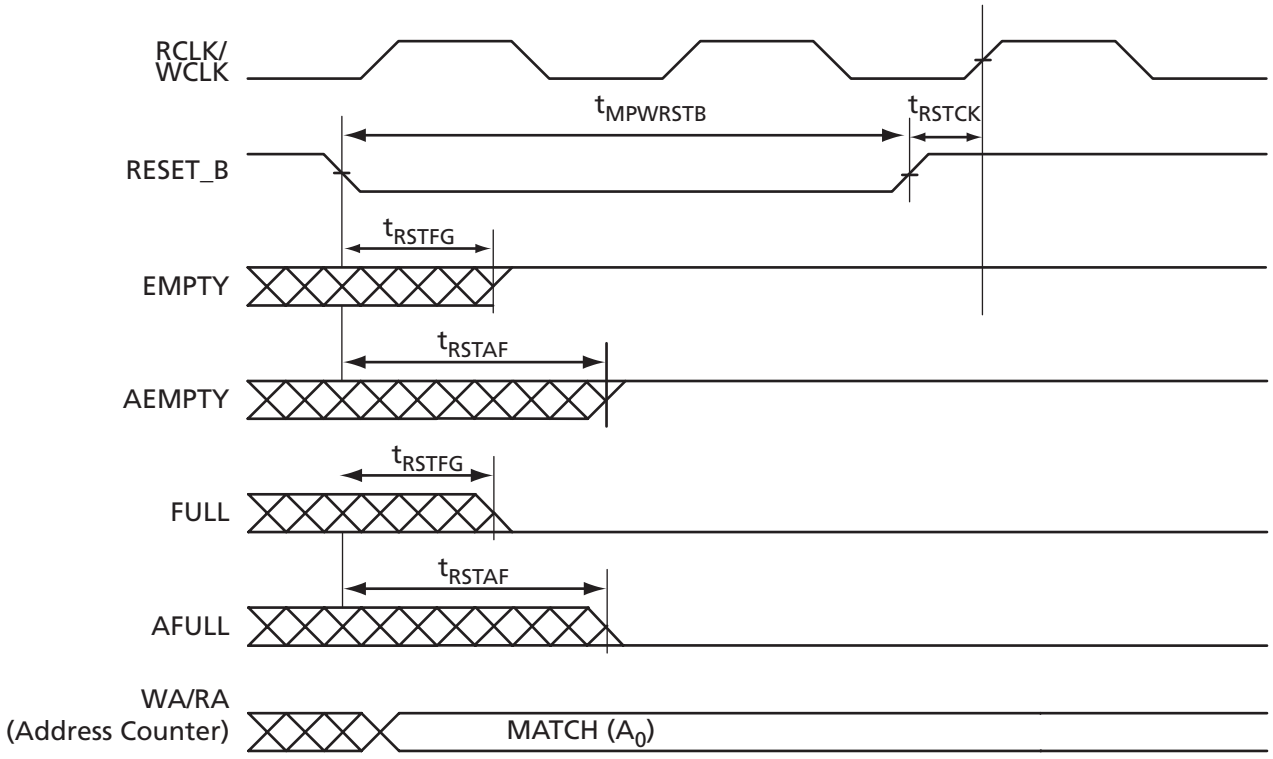

Figure 3-48 • **FIFO Reset**

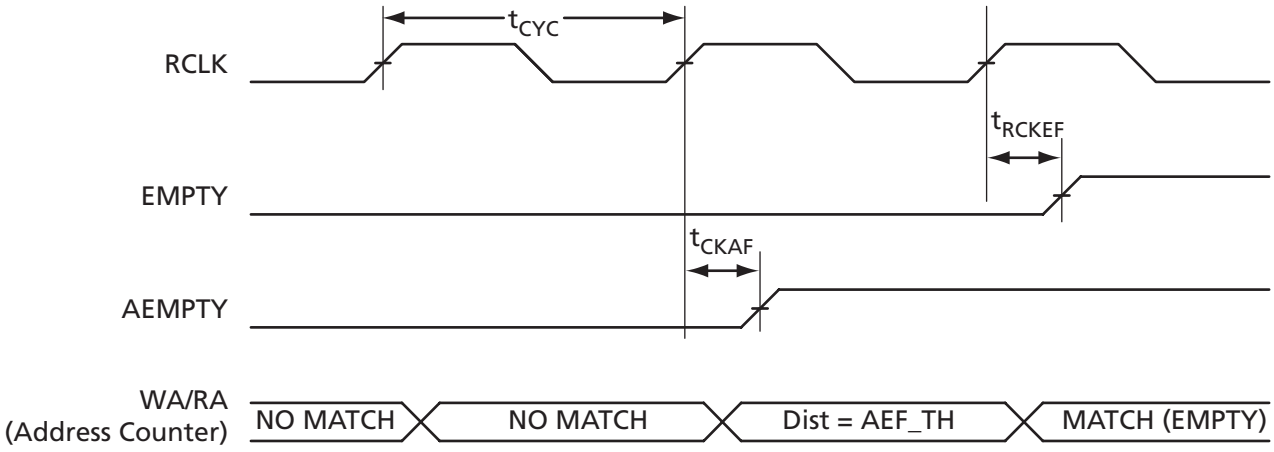

Figure 3-49 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

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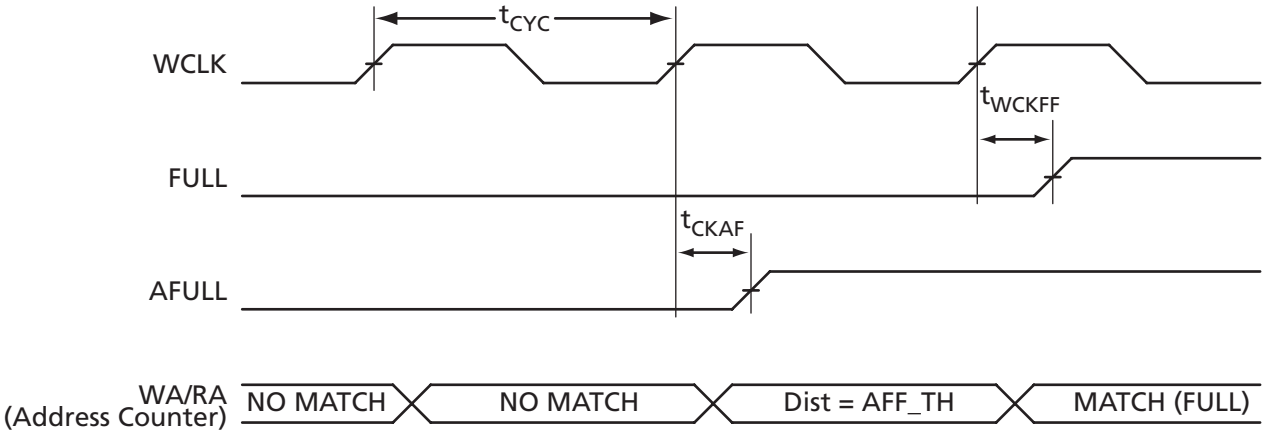

Figure 3-50 • **FIFO FULL Flag and AFULL Flag Assertion**

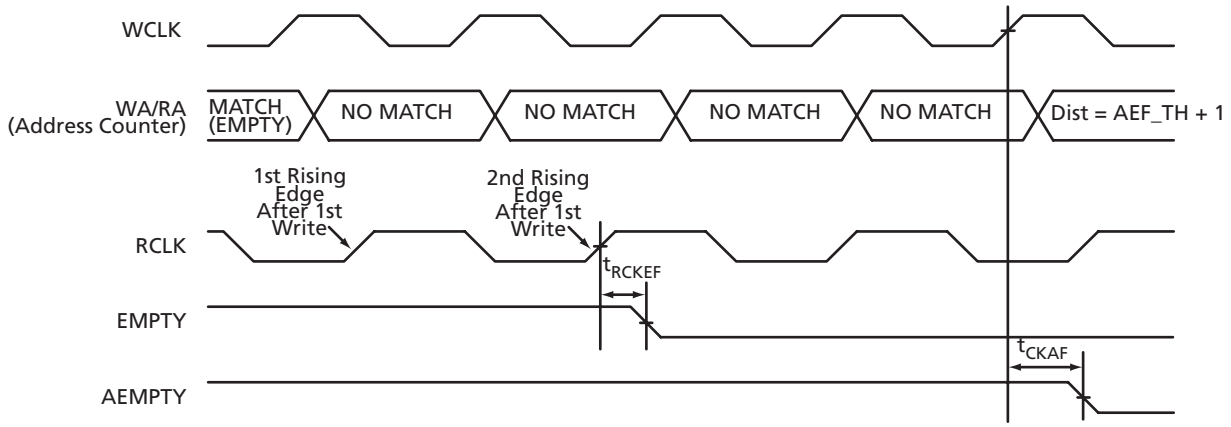

Figure 3-51 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

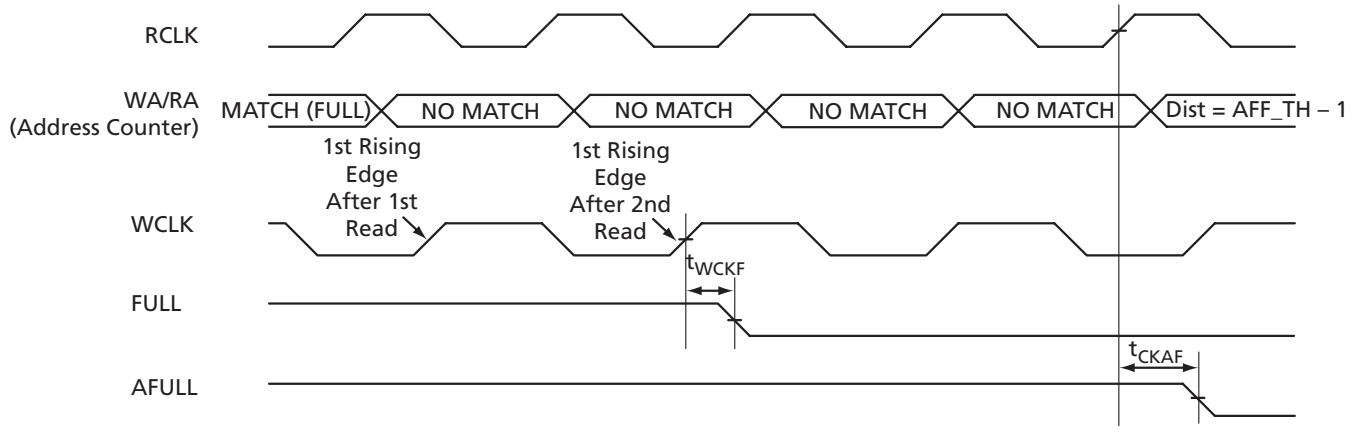

Figure 3-52 • **FIFO FULL Flag and AFULL Flag Deassertion**

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Timing Characteristics

Table 3-96 • **FIFO**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.38	1.57	1.84	2.21	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.02	0.02	0.02	0.03	ns
t_{BKS}	BLK_B Setup Time	0.19	0.22	0.26	0.31	ns
t_{BKH}	BLK_B Hold Time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (pass-through)	2.36	2.68	3.15	3.79	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	1.72	1.96	2.30	2.76	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.63	1.86	2.18	2.62	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.19	7.05	8.29	9.96	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	1.69	1.93	2.27	2.72	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	6.13	6.98	8.20	9.85	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
$t_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F_{MAX}	Maximum Frequency	310	272	231	193	HMz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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Embedded FlashROM Characteristics

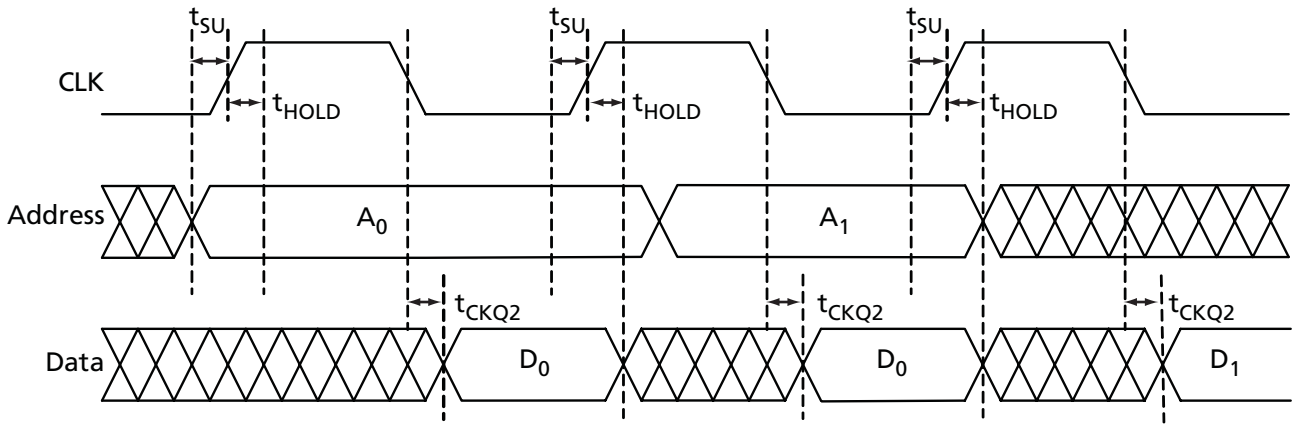

Figure 3-53 • **Timing Diagram**

Timing Characteristics

Table 3-97 • **Embedded FlashROM Access Time**

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.23	18.48	21.73	ns
F_{MAX}	Maximum Clock Frequency	15	15	15	MHz

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JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 3-11 for more details.

Timing Characteristics

Table 3-98 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (data out)				ns
t_{RSTB2Q}	Reset to Q (data out)				ns
F_{TCKMAX}	TCK Maximum Frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal Time				ns
$t_{TRSTREC}$	ResetB Recovery Time				ns
$t_{TRSTMPW}$	ResetB Minimum Pulse				ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-4 for derating values.*

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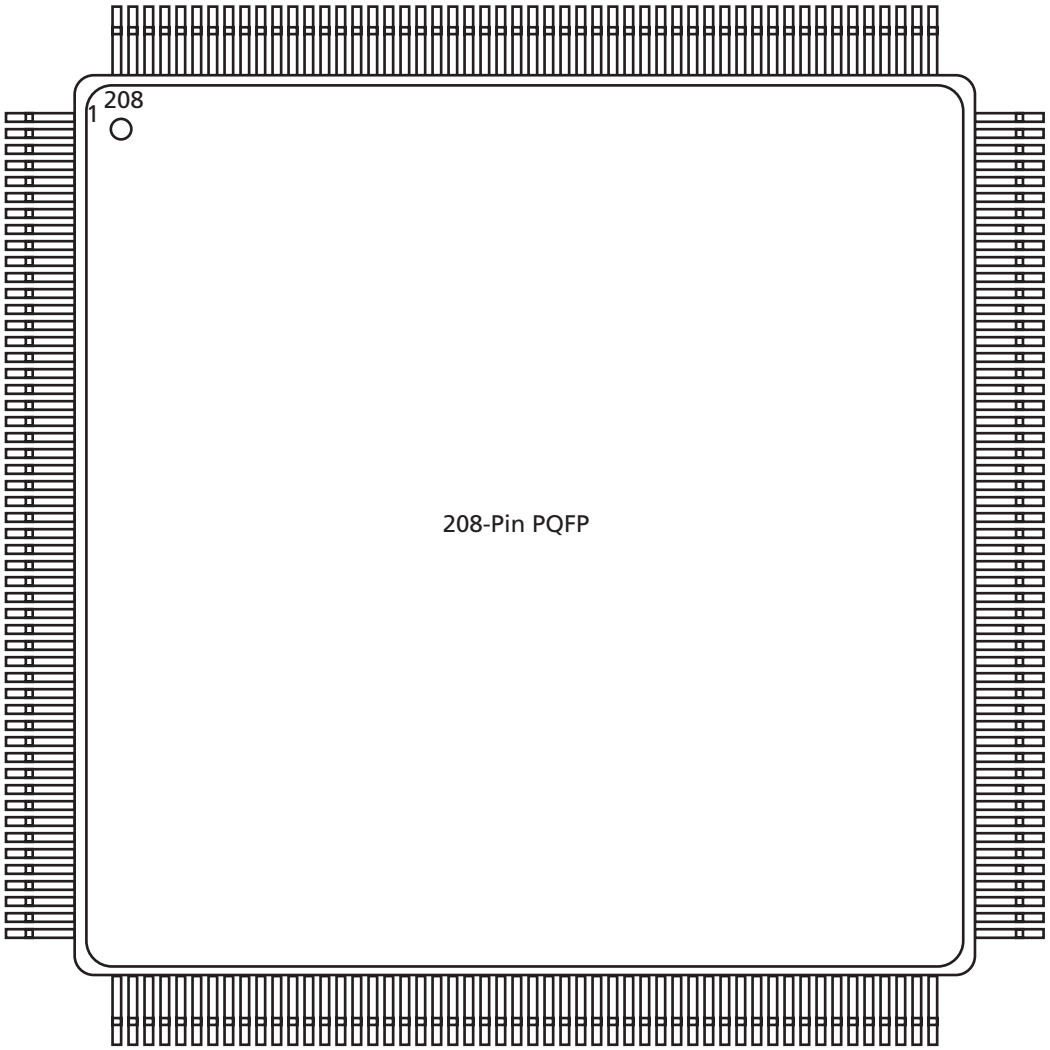
Package Pin Assignments

208-Pin PQFP



Note: *This is the top view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

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208-Pin PQFP*	
Pin Number	**A3PE600 Function**
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO133PSB7V1
5	GAA2/IO134PDB7V1
6	IO134NDB7V1
7	GAC2/IO132PDB7V1
8	IO132NDB7V1
9	IO130PDB7V1
10	IO130NDB7V1
11	IO127PDB7V1
12	IO127NDB7V1
13	IO126PDB7V0
14	IO126NDB7V0
15	IO124PSB7V0
16	V_{CC}
17	GND
18	V_{CCI}B7
19	IO122PPB7V0
20	IO121PSB7V0
21	IO122NPB7V0
22	GFC1/IO120PSB7V0
23	GFB1/IO119PDB7V0
24	GFB0/IO119NDB7V0
25	V_{COMPLF}
26	GFA0/IO118NPB6V1
27	V_{CCPLF}
28	GFA1/IO118PPB6V1
29	GND
30	GFA2/IO117PDB6V1
31	IO117NDB6V1
32	GFB2/IO116PPB6V1
33	GFC2/IO115PPB6V1
34	IO116NPB6V1
35	IO115NPB6V1
36	V_{CC}
37	IO112PDB6V1
38	IO112NDB6V1

208-Pin PQFP*	
Pin Number	**A3PE600 Function**
39	IO108PSB6V0
40	V_{CCI}B6
41	GND
42	IO106PDB6V0
43	IO106NDB6V0
44	GEC1/IO104PDB6V0
45	GEC0/IO104NDB6V0
46	GEB1/IO103PPB6V0
47	GEA1/IO102PPB6V0
48	GEB0/IO103NPB6V0
49	GEA0/IO102NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO101NDB5V2
56	GEA2/IO101PDB5V2
57	IO100NDB5V2
58	GEB2/IO100PDB5V2
59	IO99NDB5V2
60	GEC2/IO99PDB5V2
61	IO98PSB5V2
62	V_{CCI}B5
63	IO96PSB5V2
64	IO94NDB5V1
65	GND
66	IO94PDB5V1
67	IO92NDB5V1
68	IO92PDB5V1
69	IO88NDB5V0
70	IO88PDB5V0
71	V_{CC}
72	V_{CCI}B5
73	IO85NPB5V0
74	IO84NPB5V0
75	IO85PPB5V0
76	IO84PPB5V0

208-Pin PQFP*	
Pin Number	**A3PE600 Function**
77	IO83NPB5V0
78	IO82NPB5V0
79	IO83PPB5V0
80	IO82PPB5V0
81	GND
82	IO80NDB4V1
83	IO80PDB4V1
84	IO79NPB4V1
85	IO78NPB4V1
86	IO79PPB4V1
87	IO78PPB4V1
88	V_{CC}
89	V_{CCI}B4
90	IO76NDB4V1
91	IO76PDB4V1
92	IO72NDB4V0
93	IO72PDB4V0
94	IO70NDB4V0
95	GDC2/IO70PDB4V0
96	IO68NDB4V0
97	GND
98	GDA2/IO68PDB4V0
99	GDB2/IO69PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO
109	TRST
110	V_{JTAG}
111	VMV3
112	GDA0/IO67NPB3V1
113	GDB0/IO66NPB3V1
114	GDA1/IO67PPB3V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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208-Pin PQFP*	
Pin Number	**A3PE600 Function**
115	GDB1/IO66PPB3V1
116	GDC0/IO65NDB3V1
117	GDC1/IO65PDB3V1
118	IO62NDB3V1
119	IO62PDB3V1
120	IO58NDB3V0
121	IO58PDB3V0
122	GND
123	V_{CCI}B3
124	GCC2/IO55PSB3V0
125	GCB2/IO54PSB3V0
126	NC
127	IO53NDB3V0
128	GCA2/IO53PDB3V0
129	GCA1/IO52PPB3V0
130	GND
131	V_{CCPLC}
132	GCA0/IO52NPB3V0
133	V_{COMPLC}
134	GCB0/IO51NDB2V1
135	GCB1/IO51PDB2V1
136	GCC1/IO50PSB2V1
137	IO49NDB2V1
138	IO49PDB2V1
139	IO48PSB2V1
140	V_{CCI}B2
141	GND
142	V_{CC}
143	IO47NDB2V1
144	IO47PDB2V1
145	IO44NDB2V1
146	IO44PDB2V1

208-Pin PQFP*	
Pin Number	**A3PE600 Function**
147	IO43NDB2V0
148	IO43PDB2V0
149	IO40NDB2V0
150	IO40PDB2V0
151	GBC2/IO38PSB2V0
152	GBA2/IO36PSB2V0
153	GBB2/IO37PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO35PDB1V1
160	GBA0/IO35NDB1V1
161	GBB1/IO34PDB1V1
162	GND
163	GBB0/IO34NDB1V1
164	GBC1/IO33PDB1V1
165	GBC0/IO33NDB1V1
166	IO31PDB1V1
167	IO31NDB1V1
168	IO27PDB1V0
169	IO27NDB1V0
170	V_{CCI}B1
171	V_{CC}
172	IO23PPB1V0
173	IO22PSB1V0
174	IO23NPB1V0
175	IO21PDB1V0
176	IO21NDB1V0
177	IO19PPB0V2
178	GND

208-Pin PQFP*	
Pin Number	**A3PE600 Function**
179	IO18PPB0V2
180	IO19NPB0V2
181	IO18NPB0V2
182	IO17PPB0V2
183	IO16PPB0V2
184	IO17NPB0V2
185	IO16NPB0V2
186	V_{CCI}B0
187	V_{CC}
188	IO15PDB0V2
189	IO15NDB0V2
190	IO13PDB0V2
191	IO13NDB0V2
192	IO11PSB0V1
193	IO09PDB0V1
194	IO09NDB0V1
195	GND
196	IO07PDB0V1
197	IO07NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	V_{CCI}B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO220PSB7V3
5	GAA2/IO221PDB7V3
6	IO221NDB7V3
7	GAC2/IO219PDB7V3
8	IO219NDB7V3
9	IO215PDB7V3
10	IO215NDB7V3
11	IO212PDB7V2
12	IO212NDB7V2
13	IO208PDB7V2
14	IO208NDB7V2
15	IO204PSB7V1
16	V_{CC}
17	GND
18	V_{CCI}B7
19	IO200PDB7V1
20	IO200NDB7V1
21	IO196PSB7V0
22	GFC1/IO192PSB7V0
23	GFB1/IO191PDB7V0
24	GFB0/IO191NDB7V0
25	V_{COMPLF}
26	GFA0/IO190NPB6V2
27	V_{CCPLF}
28	GFA1/IO190PPB6V2
29	GND
30	GFA2/IO189PDB6V2
31	IO189NDB6V2
32	GFB2/IO188PPB6V2
33	GFC2/IO187PPB6V2
34	IO188NPB6V2
35	IO187NPB6V2
36	V_{CC}

208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
37	IO184PDB6V2
38	IO184NDB6V2
39	IO180PSB6V1
40	V_{CCI}B6
41	GND
42	IO176PDB6V1
43	IO176NDB6V1
44	GEC1/IO169PDB6V0
45	GEC0/IO169NDB6V0
46	GEB1/IO168PPB6V0
47	GEA1/IO167PPB6V0
48	GEB0/IO168NPB6V0
49	GEA0/IO167NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO166NDB5V3
56	GEA2/IO166PDB5V3
57	IO165NDB5V3
58	GEB2/IO165PDB5V3
59	IO164NDB5V3
60	GEC2/IO164PDB5V3
61	IO163PSB5V3
62	V_{CCI}B5
63	IO161PSB5V3
64	IO157NDB5V2
65	GND
66	IO157PDB5V2
67	IO153NDB5V2
68	IO153PDB5V2
69	IO149NDB5V1
70	IO149PDB5V1
71	V_{CC}
72	V_{CCI}B5

208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
73	IO145NDB5V1
74	IO145PDB5V1
75	IO143NDB5V1
76	IO143PDB5V1
77	IO137NDB5V0
78	IO137PDB5V0
79	IO135NDB5V0
80	IO135PDB5V0
81	GND
82	IO131NDB4V2
83	IO131PDB4V2
84	IO129NDB4V2
85	IO129PDB4V2
86	IO127NDB4V2
87	IO127PDB4V2
88	V_{CC}
89	V_{CCI}B4
90	IO121NDB4V1
91	IO121PDB4V1
92	IO119NDB4V1
93	IO119PDB4V1
94	IO113NDB4V0
95	GDC2/IO113PDB4V0
96	IO112NDB4V0
97	GND
98	GDB2/IO112PDB4V0
99	GDA2/IO111PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
109	TRST
110	V_{JTAG}
111	VMV3
112	GDA0/IO110NPB3V2
113	GDB0/IO109NPB3V2
114	GDA1/IO110PPB3V2
115	GDB1/IO109PPB3V2
116	GDC0/IO108NDB3V2
117	GDC1/IO108PDB3V2
118	IO105NDB3V2
119	IO105PDB3V2
120	IO101NDB3V1
121	IO101PDB3V1
122	GND
123	V_{CCI}B3
124	GCC2/IO90PSB3V0
125	GCB2/IO89PSB3V0
126	NC
127	IO88NDB3V0
128	GCA2/IO88PDB3V0
129	GCA1/IO87PPB3V0
130	GND
131	V_{CCPLC}
132	GCA0/IO87NPB3V0
133	V_{COMPLC}
134	GCB0/IO86NDB2V3
135	GCB1/IO86PDB2V3
136	GCC1/IO85PSB2V3
137	IO83NDB2V3
138	IO83PDB2V3
139	IO81PSB2V3
140	V_{CCI}B2
141	GND
142	V_{CC}

208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
143	IO73NDB2V2
144	IO73PDB2V2
145	IO71NDB2V2
146	IO71PDB2V2
147	IO67NDB2V1
148	IO67PDB2V1
149	IO65NDB2V1
150	IO65PDB2V1
151	GBC2/IO60PSB2V0
152	GBA2/IO58PSB2V0
153	GBB2/IO59PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO57PDB1V3
160	GBA0/IO57NDB1V3
161	GBB1/IO56PDB1V3
162	GND
163	GBB0/IO56NDB1V3
164	GBC1/IO55PDB1V3
165	GBC0/IO55NDB1V3
166	IO51PDB1V2
167	IO51NDB1V2
168	IO47PDB1V1
169	IO47NDB1V1
170	V_{CCI}B1
171	V_{CC}
172	IO43PSB1V1
173	IO41PDB1V1
174	IO41NDB1V1
175	IO35PDB1V0
176	IO35NDB1V0

208-Pin PQFP*	
Pin Number	**A3PE1500 Function**
177	IO31PDB0V3
178	GND
179	IO31NDB0V3
180	IO29PDB0V3
181	IO29NDB0V3
182	IO27PDB0V3
183	IO27NDB0V3
184	IO23PDB0V2
185	IO23NDB0V2
186	V_{CCI}B0
187	V_{CC}
188	IO18PDB0V2
189	IO18NDB0V2
190	IO15PDB0V1
191	IO15NDB0V1
192	IO12PSB0V1
193	IO11PDB0V1
194	IO11NDB0V1
195	GND
196	IO08PDB0V1
197	IO08NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	V_{CCI}B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO303PSB7V3
5	GAA2/IO304PDB7V3
6	IO304NDB7V3
7	GAC2/IO302PDB7V3
8	IO302NDB7V3
9	IO298PDB7V3
10	IO298NDB7V3
11	IO294PDB7V2
12	IO294NDB7V2
13	IO290PDB7V2
14	IO290NDB7V2
15	IO286PSB7V1
16	V_{CC}
17	GND
18	V_{CCI}B7
19	IO282PDB7V1
20	IO282NDB7V1
21	IO278PSB7V0
22	GFC1/IO274PSB7V0
23	GFB1/IO273PDB7V0
24	GFB0/IO273NDB7V0
25	V_{COMPLF}
26	GFA0/IO272NPB6V4
27	V_{CCPLF}
28	GFA1/IO272PPB6V4
29	GND
30	GFA2/IO271PDB6V4
31	IO271NDB6V4
32	GFB2/IO270PPB6V4
33	GFC2/IO269PPB6V4
34	IO270NPB6V4
35	IO269NPB6V4
36	V_{CC}

208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
37	IO250PDB6V2
38	IO250NDB6V2
39	IO246PSB6V1
40	V_{CCI}B6
41	GND
42	IO242PDB6V1
43	IO242NDB6V1
44	GEC1/IO234PPB6V0
45	GEB1/IO233PPB6V0
46	GEC0/IO234NPB6V0
47	GEB0/IO233NPB6V0
48	GEA1/IO232PDB6V0
49	GEA0/IO232NDB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO231NDB5V4
56	GEA2/IO231PDB5V4
57	IO230NDB5V4
58	GEB2/IO230PDB5V4
59	IO229NDB5V4
60	GEC2/IO229PDB5V4
61	IO228PSB5V4
62	V_{CCI}B5
63	IO216NDB5V3
64	IO216PDB5V3
65	GND
66	IO212PSB5V2
67	IO210NDB5V2
68	IO210PDB5V2
69	IO206NDB5V1
70	IO206PDB5V1
71	V_{CC}
72	V_{CCI}B5

208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
73	IO200NDB5V1
74	IO200PDB5V1
75	IO196NDB5V0
76	IO196PDB5V0
77	IO195NDB5V0
78	IO195PDB5V0
79	IO192NDB5V0
80	IO192PDB5V0
81	GND
82	IO182NDB4V3
83	IO182PDB4V3
84	IO178NDB4V3
85	IO178PDB4V3
86	IO174NDB4V2
87	IO174PDB4V2
88	V_{CC}
89	V_{CCI}B4
90	IO168NDB4V2
91	IO168PDB4V2
92	IO164NDB4V1
93	IO164PDB4V1
94	IO154NDB4V0
95	GDC2/IO154PDB4V0
96	IO153NDB4V0
97	GND
98	GDB2/IO153PDB4V0
99	GDA2/IO152PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
109	TRST
110	V_{JTAG}
111	VMV3
112	GDA0/IO151NPB3V4
113	GDB0/IO150NPB3V4
114	GDA1/IO151PPB3V4
115	GDB1/IO150PPB3V4
116	GDC0/IO149NDB3V4
117	GDC1/IO149PDB3V4
118	IO146NDB3V4
119	IO146PDB3V4
120	IO142NDB3V3
121	IO142PDB3V3
122	GND
123	V_{CCI}B3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	V_{CCPLC}
132	GCA0/IO114NPB3V0
133	V_{COMPLC}
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	V_{CCI}B2
141	GND
142	V_{CC}

208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	V_{CCI}B1
171	V_{CC}
172	IO67PSB1V3
173	IO66PDB1V3
174	IO66NDB1V3
175	IO63PDB1V2
176	IO63NDB1V2

208-Pin PQFP*	
Pin Number	**A3PE3000 Function**
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	V_{CCI}B0
187	V_{CC}
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	V_{CCI}B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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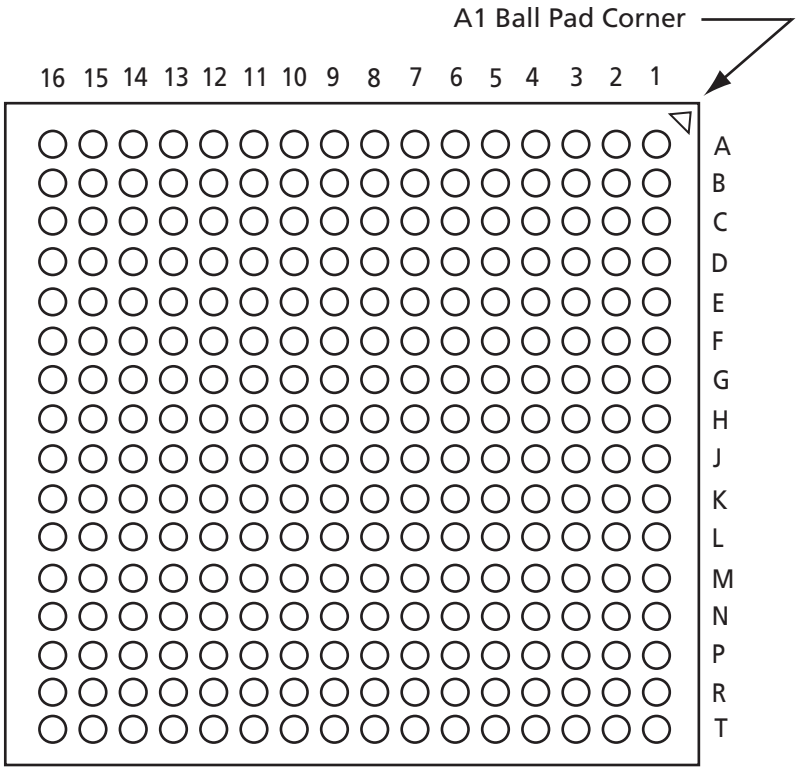
256-Pin FBGA



Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

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256-Pin FBGA*	
Pin Number	**A3PE600 Function**
A1	GND
A2	GAA0/IO00NDB0V0
A3	GAA1/IO00PDB0V0
A4	GAB0/IO01NDB0V0
A5	IO05PDB0V0
A6	IO10PDB0V1
A7	IO12PDB0V2
A8	IO16NDB0V2
A9	IO23NDB1V0
A10	IO23PDB1V0
A11	IO28NDB1V1
A12	IO28PDB1V1
A13	GBB1/IO34PDB1V1
A14	GBA0/IO35NDB1V1
A15	GBA1/IO35PDB1V1
A16	GND
B1	GAB2/IO133PDB7V1
B2	GAA2/IO134PDB7V1
B3	GNDQ
B4	GAB1/IO01PDB0V0
B5	IO05NDB0V0
B6	IO10NDB0V1
B7	IO12NDB0V2
B8	IO16PDB0V2
B9	IO20NDB1V0
B10	IO24NDB1V0
B11	IO24PDB1V0
B12	GBC1/IO33PDB1V1
B13	GBB0/IO34NDB1V1
B14	GNDQ
B15	GBA2/IO36PDB2V0
B16	IO42NDB2V0
C1	IO133NDB7V1
C2	IO134NDB7V1
C3	VMV7
C4	V_{CCPLA}
C5	GAC0/IO02NDB0V0

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
C6	GAC1/IO02PDB0V0
C7	IO15NDB0V2
C8	IO15PDB0V2
C9	IO20PDB1V0
C10	IO25NDB1V0
C11	IO27PDB1V0
C12	GBC0/IO33NDB1V1
C13	V_{CCPLB}
C14	VMV2
C15	IO36NDB2V0
C16	IO42PDB2V0
D1	IO128PDB7V1
D2	IO129PDB7V1
D3	GAC2/IO132PDB7V1
D4	V_{COMPLA}
D5	GNDQ
D6	IO09NDB0V1
D7	IO09PDB0V1
D8	IO13PDB0V2
D9	IO21PDB1V0
D10	IO25PDB1V0
D11	IO27NDB1V0
D12	GNDQ
D13	V_{COMPLB}
D14	GBB2/IO37PDB2V0
D15	IO39PDB2V0
D16	IO39NDB2V0
E1	IO128NDB7V1
E2	IO129NDB7V1
E3	IO132NDB7V1
E4	IO130PDB7V1
E5	VMV0
E6	$V_{CCI}B0$
E7	$V_{CCI}B0$
E8	IO13NDB0V2
E9	IO21NDB1V0
E10	$V_{CCI}B1$

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
E11	$V_{CCI}B1$
E12	VMV1
E13	GBC2/IO38PDB2V0
E14	IO37NDB2V0
E15	IO41NDB2V0
E16	IO41PDB2V0
F1	IO124PDB7V0
F2	IO125PDB7V0
F3	IO126PDB7V0
F4	IO130NDB7V1
F5	$V_{CCI}B7$
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	$V_{CCI}B2$
F13	IO38NDB2V0
F14	IO40NDB2V0
F15	IO40PDB2V0
F16	IO45PSB2V1
G1	IO124NDB7V0
G2	IO125NDB7V0
G3	IO126NDB7V0
G4	GFC1/IO120PPB7V0
G5	$V_{CCI}B7$
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	$V_{CCI}B2$
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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256-Pin FBGA*	
Pin Number	**A3PE600 Function**
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	V_{COMPLF}
H5	GFC0/IO120NPB7V0
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	V_{COMPLC}
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	V_{CCPLF}
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	V_{CCPLC}
J16	GCA2/IO53PSB3V0
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
K5	V_{CCI}B6
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	V_{CCI}B6
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0
M5	VMV5
M6	V_{CCI}B5
M7	V_{CCI}B5
M8	IO84NDB5V0
M9	IO84PDB5V0

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
M10	V_{CCI}B4
M11	V_{CCI}B4
M12	VMV3
M13	V_{CCPLD}
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	V_{COMPLE}
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	V_{COMPLD}
N14	V_{JTAG}
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	V_{CCPLE}
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1
P9	IO82PDB5V0
P10	IO76NDB4V1
P11	IO76PDB4V1
P12	VMV4
P13	TCK
P14	V_{PUMP}

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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256-Pin FBGA*	
Pin Number	**A3PE600 Function**
P15	TRST
P16	GDA0/IO67NDB3V1
R1	GEA1/IO102PDB6V0
R2	GEA0/IO102NDB6V0
R3	GNDQ
R4	GEC2/IO99PDB5V2
R5	IO95NPB5V1
R6	IO91NDB5V1
R7	IO91PDB5V1
R8	IO83NDB5V0
R9	IO83PDB5V0
R10	IO77NDB4V1

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
R11	IO77PDB4V1
R12	IO69NDB4V0
R13	GDB2/IO69PDB4V0
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO100NDB5V2
T3	GEB2/IO100PDB5V2
T4	IO99NDB5V2
T5	IO88NDB5V0
T6	IO88PDB5V0

256-Pin FBGA*	
Pin Number	**A3PE600 Function**
T7	IO89NSB5V0
T8	IO80NSB4V1
T9	IO81NDB4V1
T10	IO81PDB4V1
T11	IO70NDB4V0
T12	GDC2/IO70PDB4V0
T13	IO68NDB4V0
T14	GDA2/IO68PDB4V0
T15	TMS
T16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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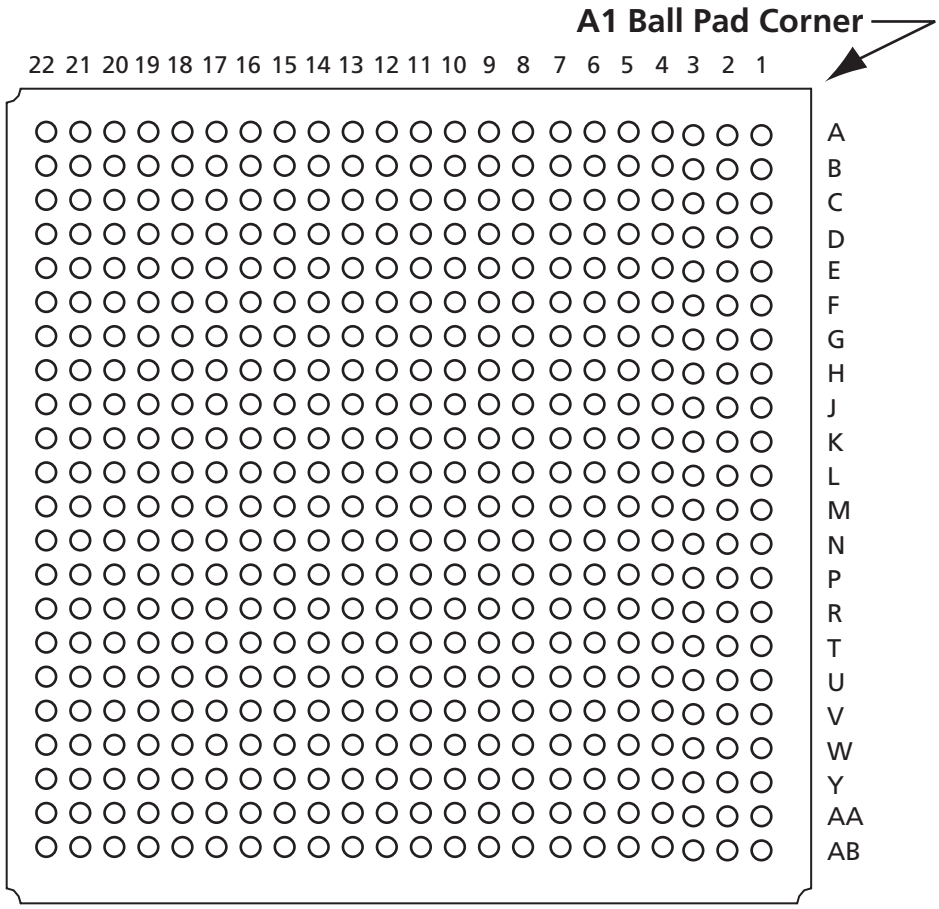
484-Pin FBGA



This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

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484-Pin FBGA*	
Pin Number	**A3PE600 Function**
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	V_{CCI}B1
A21	GND
A22	GND
B1	GND
B2	V_{CCI}B7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	V_{CCI}B2
B22	GND
C1	V_{CCI}B7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	V_{CC}
C9	V_{CC}
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	V_{CCI}B2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
D7	GAB0/IO01NDB0V0
D8	IO05PDB0V0
D9	IO10PDB0V1
D10	IO12PDB0V2
D11	IO16NDB0V2
D12	IO23NDB1V0
D13	IO23PDB1V0
D14	IO28NDB1V1
D15	IO28PDB1V1
D16	GBB1/IO34PDB1V1
D17	GBA0/IO35NDB1V1
D18	GBA1/IO35PDB1V1
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO133PDB7V1
E5	GAA2/IO134PDB7V1
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO05NDB0V0
E9	IO10NDB0V1
E10	IO12NDB0V2
E11	IO16PDB0V2
E12	IO20NDB1V0
E13	IO24NDB1V0
E14	IO24PDB1V0
E15	GBC1/IO33PDB1V1
E16	GBB0/IO34NDB1V1
E17	GNDQ
E18	GBA2/IO36PDB2V0
E19	IO42NDB2V0
E20	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE600 Function**
E21	NC
E22	NC
F1	NC
F2	IO131NDB7V1
F3	IO131PDB7V1
F4	IO133NDB7V1
F5	IO134NDB7V1
F6	VMV7
F7	V_{CCPLA}
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO15NDB0V2
F11	IO15PDB0V2
F12	IO20PDB1V0
F13	IO25NDB1V0
F14	IO27PDB1V0
F15	GBC0/IO33NDB1V1
F16	V_{CCPLB}
F17	VMV2
F18	IO36NDB2V0
F19	IO42PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO127NDB7V1
G2	IO127PDB7V1
G3	NC
G4	IO128PDB7V1
G5	IO129PDB7V1
G6	GAC2/IO132PDB7V1
G7	V_{COMPLA}
G8	GNDQ
G9	IO09NDB0V1
G10	IO09PDB0V1
G11	IO13PDB0V2
G12	IO21PDB1V0

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
G13	IO25PDB1V0
G14	IO27NDB1V0
G15	GNDQ
G16	V_{COMPLB}
G17	GBB2/IO37PDB2V0
G18	IO39PDB2V0
G19	IO39NDB2V0
G20	IO43PDB2V0
G21	IO43NDB2V0
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO128NDB7V1
H5	IO129NDB7V1
H6	IO132NDB7V1
H7	IO130PDB7V1
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO13NDB0V2
H12	IO21NDB1V0
H13	V_{CCI}B1
H14	V_{CCI}B1
H15	VMV1
H16	GBC2/IO38PDB2V0
H17	IO37NDB2V0
H18	IO41NDB2V0
H19	IO41PDB2V0
H20	V_{CC}
H21	NC
H22	NC
J1	IO123NDB7V0
J2	IO123PDB7V0
J3	NC
J4	IO124PDB7V0

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
J5	IO125PDB7V0
J6	IO126PDB7V0
J7	IO130NDB7V1
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO38NDB2V0
J17	IO40NDB2V0
J18	IO40PDB2V0
J19	IO45PDB2V1
J20	NC
J21	IO48PDB2V1
J22	IO46PDB2V1
K1	IO121NDB7V0
K2	IO121PDB7V0
K3	NC
K4	IO124NDB7V0
K5	IO125NDB7V0
K6	IO126NDB7V0
K7	GFC1/IO120PPB7V0
K8	V_{CCI}B7
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO50PPB2V1
K17	IO44NDB2V1
K18	IO44PDB2V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE600 Function**
K19	IO49NPB2V1
K20	IO45NDB2V1
K21	IO48NDB2V1
K22	IO46NDB2V1
L1	NC
L2	IO122PDB7V0
L3	IO122NDB7V0
L4	GFB0/IO119NPB7V0
L5	GFA0/IO118NDB6V1
L6	GFB1/IO119PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO120NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO50NPB2V1
L16	GCB1/IO51PPB2V1
L17	GCA0/IO52NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO51NPB2V1
L20	IO49PPB2V1
L21	IO47NDB2V1
L22	IO47PDB2V1
M1	NC
M2	IO114NDB6V1
M3	IO117NDB6V1
M4	GFA2/IO117PDB6V1
M5	GFA1/IO118PDB6V1
M6	V_{CCPLF}
M7	IO116NDB6V1
M8	GFB2/IO116PDB6V1
M9	V_{CC}
M10	GND

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO54PPB3V0
M16	GCA1/IO52PPB3V0
M17	GCC2/IO55PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO53PDB3V0
M20	IO53NDB3V0
M21	IO56PDB3V0
M22	NC
N1	IO114PDB6V1
N2	IO111NDB6V1
N3	NC
N4	GFC2/IO115PDB6V1
N5	IO113PPB6V1
N6	IO112PDB6V1
N7	IO112NDB6V1
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO54NPB3V0
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
P3	IO115NDB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	V_{CCI}B6
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	V_{CC}
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	V_{CCI}B5
R10	V_{CCI}B5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	V_{CCI}B4
R14	V_{CCI}B4
R15	VMV3
R16	V_{CCPLD}

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE600 Function**
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	V_{CC}
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO101NPB5V2

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	V_{CC}
Y9	V_{CC}
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	V_{CC}

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE600 Function**
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B3
AA1	GND
AA2	V_{CCI}B6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B3
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1

484-Pin FBGA*	
Pin Number	**A3PE600 Function**
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	V_{CCI}B4
AB21	GND
AB22	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO05NDB0V0
A5	IO05PDB0V0
A6	IO11NDB0V1
A7	IO11PDB0V1
A8	IO15PDB0V1
A9	IO17PDB0V2
A10	IO27NDB0V3
A11	IO27PDB0V3
A12	IO32PDB1V0
A13	IO43PDB1V1
A14	IO47NDB1V1
A15	IO47PDB1V1
A16	IO51NDB1V2
A17	IO51PDB1V2
A18	IO54NDB1V3
A19	NC
A20	V_{CCI}B1
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B6
AA3	NC
AA4	IO161PDB5V3
AA5	IO155NDB5V2
AA6	IO155PDB5V2
AA7	IO154NDB5V2
AA8	IO154PDB5V2
AA9	IO143PDB5V1
AA10	IO143NDB5V1
AA11	IO131PPB4V2
AA12	IO129NDB4V2
AA13	IO129PDB4V2
AA14	NC

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AA15	NC
AA16	IO117NDB4V0
AA17	IO117PDB4V0
AA18	IO115NDB4V0
AA19	IO115PDB4V0
AA20	NC
AA21	V_{CCI}B3
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B5
AB4	IO159NDB5V3
AB5	IO159PDB5V3
AB6	IO149NDB5V1
AB7	IO149PDB5V1
AB8	IO138NDB5V0
AB9	IO138PDB5V0
AB10	NC
AB11	NC
AB12	IO127NDB4V2
AB13	IO127PDB4V2
AB14	IO125NDB4V1
AB15	IO125PDB4V1
AB16	IO122NDB4V1
AB17	IO122PDB4V1
AB18	NC
AB19	NC
AB20	V_{CCI}B4
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO10NDB0V1

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
B7	IO10PDB0V1
B8	IO15NDB0V1
B9	IO17NDB0V2
B10	IO20PDB0V2
B11	IO29PDB0V3
B12	IO32NDB1V0
B13	IO43NDB1V1
B14	NC
B15	NC
B16	IO53NDB1V2
B17	IO53PDB1V2
B18	IO54PDB1V3
B19	NC
B20	NC
B21	V_{CCI}B2
B22	GND
C1	V_{CCI}B7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO07NDB0V0
C7	IO07PDB0V0
C8	V_{CC}
C9	V_{CC}
C10	IO20NDB0V2
C11	IO29NDB0V3
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
C21	NC
C22	V_{CCI}B2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO09PDB0V1
D9	IO13PDB0V1
D10	IO21PDB0V2
D11	IO31NDB0V3
D12	IO37NDB1V0
D13	IO37PDB1V0
D14	IO49NDB1V2
D15	IO49PDB1V2
D16	GBB1/IO56PDB1V3
D17	GBA0/IO57NDB1V3
D18	GBA1/IO57PDB1V3
D19	GND
D20	NC
D21	IO69PDB2V1
D22	NC
E1	NC
E2	IO218PPB7V3
E3	GND
E4	GAB2/IO220PDB7V3
E5	GAA2/IO221PDB7V3
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO09NDB0V1
E9	IO13NDB0V1
E10	IO21NDB0V2
E11	IO31PDB0V3
E12	IO35NDB1V0

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
E13	IO41NDB1V1
E14	IO41PDB1V1
E15	GBC1/IO55PDB1V3
E16	GBB0/IO56NDB1V3
E17	GNDQ
E18	GBA2/IO58PDB2V0
E19	IO63NDB2V0
E20	GND
E21	IO69NDB2V1
E22	NC
F1	IO218NPB7V3
F2	IO216NDB7V3
F3	IO216PDB7V3
F4	IO220NDB7V3
F5	IO221NDB7V3
F6	VMV7
F7	V_{CCPLA}
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO23NDB0V2
F11	IO23PDB0V2
F12	IO35PDB1V0
F13	IO39NDB1V0
F14	IO45PDB1V1
F15	GBC0/IO55NDB1V3
F16	V_{CCPLB}
F17	VMV2
F18	IO58NDB2V0
F19	IO63PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO211NDB7V2
G2	IO211PDB7V2
G3	NC
G4	IO214PDB7V3

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
G5	IO217PDB7V3
G6	GAC2/IO219PDB7V3
G7	V_{COMPLA}
G8	GNDQ
G9	IO19NDB0V2
G10	IO19PDB0V2
G11	IO25PDB0V3
G12	IO33PDB1V0
G13	IO39PDB1V0
G14	IO45NDB1V1
G15	GNDQ
G16	V_{COMPLB}
G17	GBB2/IO59PDB2V0
G18	IO62PDB2V0
G19	IO62NDB2V0
G20	IO71PDB2V2
G21	IO71NDB2V2
G22	NC
H1	IO209PSB7V2
H2	NC
H3	V_{CC}
H4	IO214NDB7V3
H5	IO217NDB7V3
H6	IO219NDB7V3
H7	IO215PDB7V3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO25NDB0V3
H12	IO33NDB1V0
H13	V_{CCI}B1
H14	V_{CCI}B1
H15	VMV1
H16	GBC2/IO60PDB2V0
H17	IO59NDB2V0
H18	IO67NDB2V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
H19	IO67PDB2V1
H20	V_{CC}
H21	VMV2
H22	IO74PSB2V2
J1	IO212NDB7V2
J2	IO212PDB7V2
J3	VMV7
J4	IO206PDB7V1
J5	IO204PDB7V1
J6	IO210PDB7V2
J7	IO215NDB7V3
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO60NDB2V0
J17	IO65NDB2V1
J18	IO65PDB2V1
J19	IO75PPB2V2
J20	GNDQ
J21	IO77PDB2V2
J22	IO79PDB2V3
K1	IO200NDB7V1
K2	IO200PDB7V1
K3	GNDQ
K4	IO206NDB7V1
K5	IO204NDB7V1
K6	IO210NDB7V2
K7	GFC1/IO192PPB7V0
K8	V_{CCI}B7
K9	V_{CC}
K10	GND

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO85PPB2V3
K17	IO73NDB2V2
K18	IO73PDB2V2
K19	IO81NPB2V3
K20	IO75NPB2V2
K21	IO77NDB2V2
K22	IO79NDB2V3
L1	NC
L2	IO196PDB7V0
L3	IO196NDB7V0
L4	GFB0/IO191NPB7V0
L5	GFA0/IO190NDB6V2
L6	GFB1/IO191PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO192NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO85NPB2V3
L16	GCB1/IO86PPB2V3
L17	GCA0/IO87NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO86NPB2V3
L20	IO81PPB2V3
L21	IO83NDB2V3
L22	IO83PDB2V3
M1	GNDQ
M2	IO185NPB6V2

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
M3	IO189NDB6V2
M4	GFA2/IO189PDB6V2
M5	GFA1/IO190PDB6V2
M6	V_{CCPLF}
M7	IO188NDB6V2
M8	GFB2/IO188PDB6V2
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO89PPB3V0
M16	GCA1/IO87PPB3V0
M17	GCC2/IO90PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO88PDB3V0
M20	IO88NDB3V0
M21	IO93PDB3V0
M22	NC
N1	IO185PPB6V2
N2	IO183NDB6V2
N3	VMV6
N4	GFC2/IO187PPB6V2
N5	IO184PPB6V2
N6	IO186PDB6V2
N7	IO186NDB6V2
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO89NPB3V0

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
N17	IO91NPB3V0
N18	IO90NPB3V0
N19	IO91PPB3V0
N20	GNDQ
N21	IO93NDB3V0
N22	IO95PDB3V1
P1	NC
P2	IO183PDB6V2
P3	IO187NPB6V2
P4	IO184NPB6V2
P5	IO176PPB6V1
P6	IO182PDB6V1
P7	IO182NDB6V1
P8	V_{CCI}B6
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B3
P16	GDB0/IO109NPB3V2
P17	IO97NDB3V1
P18	IO97PDB3V1
P19	IO99PDB3V1
P20	VMV3
P21	IO98PDB3V1
P22	IO95NDB3V1
R1	NC
R2	IO177PDB6V1
R3	V_{CC}
R4	IO176NPB6V1
R5	IO174NDB6V0
R6	IO174PDB6V0
R7	GEC0/IO169NPB6V0
R8	VMV5

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
R9	V_{CCI}B5
R10	V_{CCI}B5
R11	IO135NDB5V0
R12	IO135PDB5V0
R13	V_{CCI}B4
R14	V_{CCI}B4
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO109PPB3V2
R18	GDC1/IO108PDB3V2
R19	IO99NDB3V1
R20	V_{CC}
R21	IO98NDB3V1
R22	IO101PDB3V1
T1	NC
T2	IO177NDB6V1
T3	NC
T4	IO171PDB6V0
T5	IO171NDB6V0
T6	GEC1/IO169PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO166PPB5V3
T10	IO145NDB5V1
T11	IO141NDB5V0
T12	IO139NDB5V0
T13	IO119NDB4V1
T14	IO119PDB4V1
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO108NDB3V2
T19	GDA1/IO110PDB3V2
T20	NC
T21	IO103PDB3V2
T22	IO101NDB3V1

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
U1	IO175PPB6V1
U2	IO173PDB6V0
U3	IO173NDB6V0
U4	GEB1/IO168PDB6V0
U5	GEB0/IO168NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO166NPB5V3
U9	IO157PPB5V2
U10	IO145PDB5V1
U11	IO141PDB5V0
U12	IO139PDB5V0
U13	IO121NDB4V1
U14	IO121PDB4V1
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO110NDB3V2
U20	NC
U21	IO103NDB3V2
U22	IO105PDB3V2
V1	NC
V2	IO175NPB6V1
V3	GND
V4	GEA1/IO167PDB6V0
V5	GEA0/IO167NDB6V0
V6	GNDQ
V7	GEC2/IO164PDB5V3
V8	IO157NPB5V2
V9	IO151NDB5V2
V10	IO151PDB5V2
V11	IO137NDB5V0
V12	IO137PDB5V0
V13	IO123NDB4V1
V14	IO123PDB4V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
V15	IO112NDB4V0
V16	GDB2/IO112PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO105NDB3V2
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO165NDB5V3
W6	GEB2/IO165PDB5V3
W7	IO164NDB5V3
W8	IO153NDB5V2
W9	IO153PDB5V2
W10	IO147NDB5V1

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
W11	IO133NDB4V2
W12	IO130NDB4V2
W13	IO130PDB4V2
W14	IO113NDB4V0
W15	GDC2/IO113PDB4V0
W16	IO111NDB4V0
W17	GDA2/IO111PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B6
Y2	NC
Y3	NC
Y4	IO161NDB5V3
Y5	GND
Y6	IO163NDB5V3

484-Pin FBGA*	
Pin Number	**A3PE1500 Function**
Y7	IO163PDB5V3
Y8	V_{CC}
Y9	V_{CC}
Y10	IO147PDB5V1
Y11	IO133PDB4V2
Y12	IO131NPB4V2
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B3

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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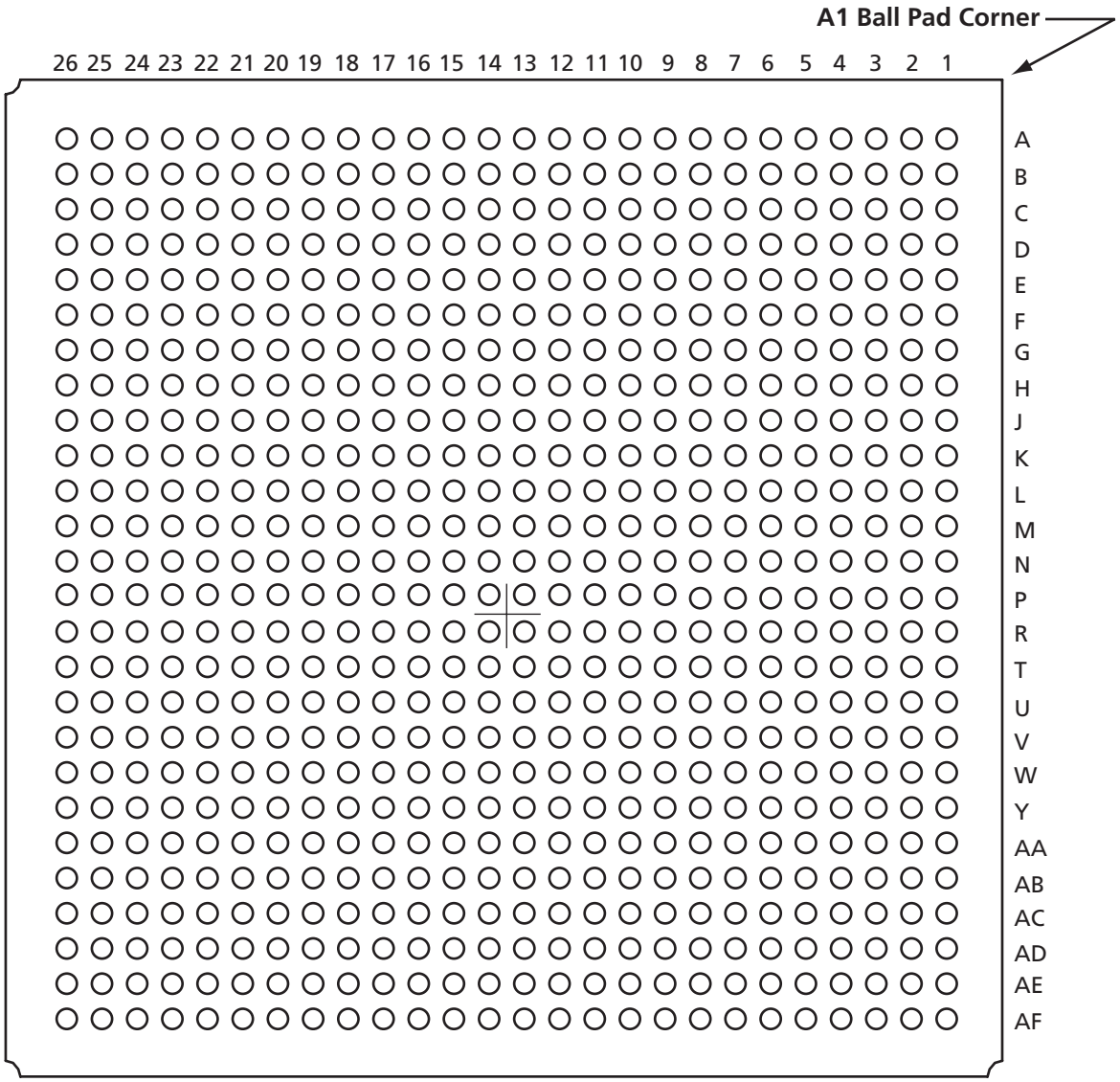
676-Pin FBGA



Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
A1	GND
A2	GND
A3	GAA0/IO00NDB0V0
A4	GAA1/IO00PDB0V0
A5	IO06NDB0V0
A6	IO09NDB0V1
A7	IO09PDB0V1
A8	IO14NDB0V1
A9	IO14PDB0V1
A10	IO22NDB0V2
A11	IO22PDB0V2
A12	IO26NDB0V3
A13	IO26PDB0V3
A14	IO30NDB0V3
A15	IO30PDB0V3
A16	IO34NDB1V0
A17	IO34PDB1V0
A18	IO38NDB1V0
A19	IO38PDB1V0
A20	IO41PDB1V1
A21	IO44PDB1V1
A22	IO49PDB1V2
A23	IO50PDB1V2
A24	GBC1/IO55PDB1V3
A25	GND
A26	GND
AA1	IO174PDB6V0
AA2	IO171PDB6V0
AA3	GEA1/IO167PPB6V0
AA4	GEC0/IO169NPB6V0
AA5	V_{COMPLE}
AA6	GND
AA7	IO165NDB5V3
AA8	GEB2/IO165PDB5V3
AA9	IO163PDB5V3
AA10	IO159NDB5V3

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AA11	IO153NDB5V2
AA12	IO147NDB5V1
AA13	IO139NDB5V0
AA14	IO137NDB5V0
AA15	IO123NDB4V1
AA16	IO123PDB4V1
AA17	IO117NDB4V0
AA18	IO117PDB4V0
AA19	GDB2/IO112PDB4V0
AA20	GNDQ
AA21	TDO
AA22	GND
AA23	GND
AA24	IO102NDB3V1
AA25	IO102PDB3V1
AA26	IO98NDB3V1
AB1	IO174NDB6V0
AB2	IO171NDB6V0
AB3	GEB1/IO168PPB6V0
AB4	GEA0/IO167NPB6V0
AB5	V_{CCPLE}
AB6	GND
AB7	GND
AB8	IO156NDB5V2
AB9	IO156PDB5V2
AB10	IO150PDB5V1
AB11	IO155PDB5V2
AB12	IO142PDB5V0
AB13	IO135NDB5V0
AB14	IO135PDB5V0
AB15	IO132PDB4V2
AB16	IO129PDB4V2
AB17	IO121PDB4V1
AB18	IO119NDB4V1
AB19	IO112NDB4V0
AB20	VMV4

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AB21	TCK
AB22	TRST
AB23	GDC0/IO108NDB3V2
AB24	GDC1/IO108PDB3V2
AB25	IO104NDB3V2
AB26	IO104PDB3V2
AC1	IO170PDB6V0
AC2	GEB0/IO168NPB6V0
AC3	IO166NPB5V3
AC4	GNDQ
AC5	GND
AC6	IO160PDB5V3
AC7	IO161PDB5V3
AC8	IO154PDB5V2
AC9	GND
AC10	IO150NDB5V1
AC11	IO155NDB5V2
AC12	IO142NDB5V0
AC13	IO138NDB5V0
AC14	IO138PDB5V0
AC15	IO132NDB4V2
AC16	IO129NDB4V2
AC17	IO121NDB4V1
AC18	IO119PDB4V1
AC19	IO118NDB4V0
AC20	IO118PDB4V0
AC21	IO114PPB4V0
AC22	TMS
AC23	V_{JTAG}
AC24	VMV3
AC25	IO106NDB3V2
AC26	IO106PDB3V2
AD1	IO170NDB6V0
AD2	GEA2/IO166PPB5V3
AD3	VMV5
AD4	GEC2/IO164PDB5V3

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AD5	IO162PDB5V3
AD6	IO160NDB5V3
AD7	IO161NDB5V3
AD8	IO154NDB5V2
AD9	IO148PDB5V1
AD10	IO151PDB5V2
AD11	IO144PDB5V1
AD12	IO140PDB5V0
AD13	IO143PDB5V1
AD14	IO141PDB5V0
AD15	IO134PDB4V2
AD16	IO133PDB4V2
AD17	IO127PDB4V2
AD18	IO130PDB4V2
AD19	IO126PDB4V1
AD20	IO124PDB4V1
AD21	IO120PDB4V1
AD22	IO114NPB4V0
AD23	TDI
AD24	GNDQ
AD25	GDA0/IO110NDB3V2
AD26	GDA1/IO110PDB3V2
AE1	GND
AE2	GND
AE3	GND
AE4	IO164NDB5V3
AE5	IO162NDB5V3
AE6	IO158PPB5V2
AE7	IO157PPB5V2
AE8	IO152PPB5V2
AE9	IO148NDB5V1
AE10	IO151NDB5V2
AE11	IO144NDB5V1
AE12	IO140NDB5V0
AE13	IO143NDB5V1
AE14	IO141NDB5V0

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AE15	IO134NDB4V2
AE16	IO133NDB4V2
AE17	IO127NDB4V2
AE18	IO130NDB4V2
AE19	IO126NDB4V1
AE20	IO124NDB4V1
AE21	IO120NDB4V1
AE22	IO116PDB4V0
AE23	GDC2/IO113PDB4V0
AE24	GDA2/IO111PDB4V0
AE25	GND
AE26	GND
AF1	GND
AF2	GND
AF3	GND
AF4	GND
AF5	IO158NPB5V2
AF6	IO157NPB5V2
AF7	IO152NPB5V2
AF8	IO146NDB5V1
AF9	IO146PDB5V1
AF10	IO149NDB5V1
AF11	IO149PDB5V1
AF12	IO145NDB5V1
AF13	IO145PDB5V1
AF14	IO136NDB5V0
AF15	IO136PDB5V0
AF16	IO131NDB4V2
AF17	IO131PDB4V2
AF18	IO128NDB4V2
AF19	IO128PDB4V2
AF20	IO122NDB4V1
AF21	IO122PDB4V1
AF22	IO116NDB4V0
AF23	IO113NDB4V0
AF24	IO111NDB4V0

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
AF25	GND
AF26	GND
B1	GND
B2	GND
B3	GND
B4	GND
B5	IO06PDB0V0
B6	IO04NDB0V0
B7	IO07NDB0V0
B8	IO11NDB0V1
B9	IO10NDB0V1
B10	IO16NDB0V2
B11	IO20NDB0V2
B12	IO24NDB0V3
B13	IO23NDB0V2
B14	IO28NDB0V3
B15	IO31NDB0V3
B16	IO32PDB1V0
B17	IO36PDB1V0
B18	IO37PDB1V0
B19	IO42NPB1V1
B20	IO41NDB1V1
B21	IO44NDB1V1
B22	IO49NDB1V2
B23	IO50NDB1V2
B24	GBC0/IO55NDB1V3
B25	GND
B26	GND
C1	GND
C2	GND
C3	GND
C4	GND
C5	GAA2/IO221PDB7V3
C6	IO04PDB0V0
C7	IO07PDB0V0
C8	IO11PDB0V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
C9	IO10PDB0V1
C10	IO16PDB0V2
C11	IO20PDB0V2
C12	IO24PDB0V3
C13	IO23PDB0V2
C14	IO28PDB0V3
C15	IO31PDB0V3
C16	IO32NDB1V0
C17	IO36NDB1V0
C18	IO37NDB1V0
C19	IO45NDB1V1
C20	IO42PPB1V1
C21	IO46NPB1V1
C22	IO48NPB1V2
C23	GBB0/IO56NPB1V3
C24	VMV1
C25	GBC2/IO60PDB2V0
C26	IO60NDB2V0
D1	IO218NDB7V3
D2	IO218PDB7V3
D3	GND
D4	VMV7
D5	IO221NDB7V3
D6	GAC0/IO02NDB0V0
D7	GAC1/IO02PDB0V0
D8	IO05NDB0V0
D9	IO08PDB0V1
D10	IO12NDB0V1
D11	IO18NDB0V2
D12	IO17NDB0V2
D13	IO25NDB0V3
D14	IO29NDB0V3
D15	IO33NDB1V0
D16	IO40PDB1V1
D17	IO43NDB1V1
D18	IO47PDB1V1

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
D19	IO45PDB1V1
D20	IO46PPB1V1
D21	IO48PPB1V2
D22	GBA0/IO57NPB1V3
D23	GNDQ
D24	GBB1/IO56PPB1V3
D25	GBB2/IO59PDB2V0
D26	IO59NDB2V0
E1	IO212PDB7V2
E2	IO211NDB7V2
E3	IO211PDB7V2
E4	IO220NPB7V3
E5	GNDQ
E6	GAB2/IO220PPB7V3
E7	GAB1/IO01PDB0V0
E8	IO05PDB0V0
E9	IO08NDB0V1
E10	IO12PDB0V1
E11	IO18PDB0V2
E12	IO17PDB0V2
E13	IO25PDB0V3
E14	IO29PDB0V3
E15	IO33PDB1V0
E16	IO40NDB1V1
E17	IO43PDB1V1
E18	IO47NDB1V1
E19	IO54NDB1V3
E20	IO52NDB1V2
E21	IO52PDB1V2
E22	V_{CCPLB}
E23	GBA1/IO57PPB1V3
E24	IO63PDB2V0
E25	IO63NDB2V0
E26	IO68PDB2V1
F1	IO212NDB7V2
F2	IO203PPB7V1

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
F3	IO213NDB7V2
F4	IO213PDB7V2
F5	GND
F6	V_{CCPLA}
F7	GAB0/IO01NDB0V0
F8	GNDQ
F9	IO03PDB0V0
F10	IO13PDB0V1
F11	IO15PDB0V1
F12	IO19PDB0V2
F13	IO21PDB0V2
F14	IO27NDB0V3
F15	IO35PDB1V0
F16	IO39NDB1V0
F17	IO51PDB1V2
F18	IO53PDB1V2
F19	IO54PDB1V3
F20	VMV2
F21	V_{COMPLB}
F22	IO61PDB2V0
F23	IO61NDB2V0
F24	IO66PDB2V1
F25	IO66NDB2V1
F26	IO68NDB2V1
G1	IO203NPB7V1
G2	IO207NDB7V2
G3	IO207PDB7V2
G4	IO216NDB7V3
G5	IO216PDB7V3
G6	V_{COMPLA}
G7	VMV0
G8	V_{CC}
G9	IO03NDB0V0
G10	IO13NDB0V1
G11	IO15NDB0V1
G12	IO19NDB0V2

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	V_{CCI}B1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	V_{CCI}B7
H8	V_{CC}
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	V_{CCI}B0
H12	V_{CCI}B0
H13	V_{CCI}B0
H14	V_{CCI}B1
H15	V_{CCI}B1
H16	V_{CCI}B1
H17	V_{CCI}B1
H18	V_{CCI}B1
H19	V_{CC}
H20	V_{CC}
H21	IO58NPB2V0
H22	IO70PDB2V1

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	V_{CCI}B7
J9	V_{CC}
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	V_{CC}
J15	V_{CC}
J16	V_{CC}
J17	V_{CC}
J18	V_{CC}
J19	V_{CCI}B2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
K7	IO217NDB7V3
K8	V_{CCI}B7
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	V_{CC}
K19	V_{CCI}B2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	V_{CCI}B7
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
L17	GND
L18	V_{CC}
L19	V_{CCI}B2
L20	IO67PDB2V1
L21	IO67NDB2V1
L22	IO71PDB2V2
L23	IO71NDB2V2
L24	GNDQ
L25	IO82PDB2V3
L26	IO84NDB2V3
M1	IO198NPB7V0
M2	IO202PDB7V1
M3	IO202NDB7V1
M4	IO206NDB7V1
M5	IO206PDB7V1
M6	IO204NDB7V1
M7	IO204PDB7V1
M8	V_{CCI}B7
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	V_{CC}
M19	V_{CCI}B2
M20	IO73NDB2V2
M21	IO73PDB2V2
M22	IO81PPB2V3
M23	IO77PDB2V2
M24	IO77NDB2V2
M25	IO82NDB2V3
M26	IO83PDB2V3

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
N1	GFB0/IO191NPB7V0
N2	V_{COMPLF}
N3	GFB1/IO191PPB7V0
N4	IO196PDB7V0
N5	GFA0/IO190NDB6V2
N6	IO200PDB7V1
N7	IO200NDB7V1
N8	V_{CCI}B7
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	V_{CC}
N19	V_{CCI}B2
N20	IO79PDB2V3
N21	IO79NDB2V3
N22	GCA2/IO88PPB3V0
N23	IO81NPB2V3
N24	GCA0/IO87NDB3V0
N25	GCB0/IO86NPB2V3
N26	IO83NDB2V3
P1	GFA2/IO189PDB6V2
P2	V_{CCPLF}
P3	IO193PPB7V0
P4	IO196NDB7V0
P5	GFA1/IO190PDB6V2
P6	IO194PDB7V0
P7	IO194NDB7V0
P8	V_{CCI}B6
P9	V_{CC}
P10	GND

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	V_{CC}
P19	V_{CCI}B3
P20	GCC0/IO85NDB2V3
P21	GCC1/IO85PDB2V3
P22	GCB1/IO86PPB2V3
P23	IO88NPB3V0
P24	GCA1/IO87PDB3V0
P25	V_{CCPLC}
P26	V_{COMPLC}
R1	IO189NDB6V2
R2	IO185PDB6V2
R3	IO187NPB6V2
R4	IO193NPB7V0
R5	GFC2/IO187PPB6V2
R6	GFC1/IO192PDB7V0
R7	GFC0/IO192NDB7V0
R8	V_{CCI}B6
R9	V_{CC}
R10	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	V_{CC}
R19	V_{CCI}B3
R20	NC

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
R21	IO89NDB3V0
R22	GCB2/IO89PDB3V0
R23	IO90NDB3V0
R24	GCC2/IO90PDB3V0
R25	IO91PDB3V0
R26	IO91NDB3V0
T1	IO186PDB6V2
T2	IO185NDB6V2
T3	GNDQ
T4	IO180PDB6V1
T5	IO180NDB6V1
T6	IO188NDB6V2
T7	GFB2/IO188PDB6V2
T8	V_{CCI}B6
T9	V_{CC}
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	V_{CC}
T19	V_{CCI}B3
T20	IO99PDB3V1
T21	IO99NDB3V1
T22	IO97PDB3V1
T23	IO97NDB3V1
T24	GNDQ
T25	IO93PPB3V0
T26	NC
U1	IO186NDB6V2
U2	IO184NDB6V2
U3	IO184PDB6V2
U4	IO182NDB6V1

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
U5	IO182PDB6V1
U6	IO178PDB6V1
U7	IO178NDB6V1
U8	V_{CCI}B6
U9	V_{CC}
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	V_{CC}
U19	V_{CCI}B3
U20	NC
U21	IO101NDB3V1
U22	IO101PDB3V1
U23	IO92NDB3V0
U24	IO92PDB3V0
U25	IO95PDB3V1
U26	IO93NPB3V0
V1	IO183PDB6V2
V2	IO183NDB6V2
V3	VMV6
V4	IO181PDB6V1
V5	IO181NDB6V1
V6	IO176PDB6V1
V7	IO176NDB6V1
V8	V_{CCI}B6
V9	V_{CC}
V10	V_{CC}
V11	V_{CC}
V12	V_{CC}
V13	V_{CC}
V14	V_{CC}

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
V15	V_{CC}
V16	V_{CC}
V17	V_{CC}
V18	V_{CC}
V19	V_{CCI}B3
V20	IO107PDB3V2
V21	IO107NDB3V2
V22	IO103NDB3V2
V23	IO103PDB3V2
V24	VMV3
V25	IO95NDB3V1
V26	IO94PDB3V0
W1	IO179NDB6V1
W2	IO179PDB6V1
W3	IO177NDB6V1
W4	IO177PDB6V1
W5	IO172PDB6V0
W6	IO172NDB6V0
W7	V_{CC}
W8	V_{CC}
W9	V_{CCI}B5
W10	V_{CCI}B5
W11	V_{CCI}B5
W12	V_{CCI}B5
W13	V_{CCI}B5
W14	V_{CCI}B4
W15	V_{CCI}B4
W16	V_{CCI}B4
W17	V_{CCI}B4
W18	V_{CCI}B4
W19	V_{CC}
W20	V_{CCI}B3
W21	GDB0/IO109NDB3V2
W22	GDB1/IO109PDB3V2
W23	IO105NDB3V2
W24	IO105PDB3V2

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
W25	IO96PDB3V1
W26	IO94NDB3V0
Y1	IO175NDB6V1
Y2	IO175PDB6V1
Y3	IO173NDB6V0
Y4	IO173PDB6V0
Y5	GEC1/IO169PPB6V0
Y6	GNDQ
Y7	VMV6
Y8	V_{CCI}B5

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
Y9	IO163NDB5V3
Y10	IO159PDB5V3
Y11	IO153PDB5V2
Y12	IO147PDB5V1
Y13	IO139PDB5V0
Y14	IO137PDB5V0
Y15	IO125NDB4V1
Y16	IO125PDB4V1
Y17	IO115NDB4V0
Y18	IO115PDB4V0

676-Pin FBGA*	
Pin Number	**A3PE1500 Function**
Y19	V_{CC}
Y20	V_{PUMP}
Y21	V_{COMPLD}
Y22	V_{CCPLD}
Y23	IO100NDB3V1
Y24	IO100PDB3V1
Y25	IO96NDB3V1
Y26	IO98PDB3V1

Note: **Refer to the "User I/O Naming Convention" section on page 2-50.*

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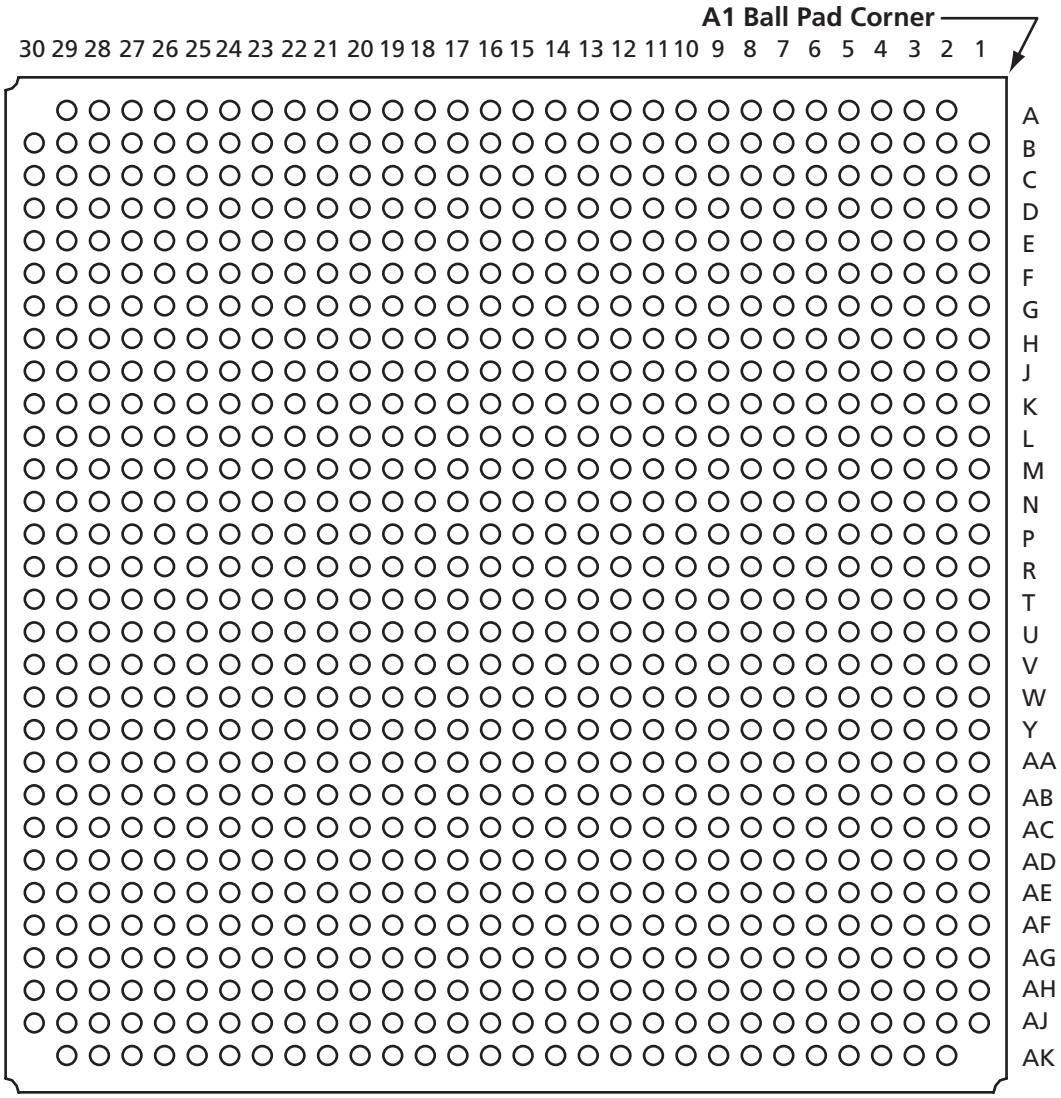
896-Pin FBGA



This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

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Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.0)	Page
Advanced v0.6 (January 2007)	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	i
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
	In the "ProASIC3E Ordering Information", Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iv
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-4 • ProASIC3E CCC/PLL Specification was updated.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	Figure 2-18 • Peak-to-Peak Jitter Definition is new.	2-18
	The "RESET" section was updated with read and write information.	2-24
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Pro I/Os" section was updated to include information on input and output buffers being disabled.	2-27
	PCI-X 3.3 V was added to Table 2-12 • VCCI Voltages and Compatible ProASIC3E Standards.	2-29
	In the Table 2-17 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-36
	Table 2-18 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-37
	Notes 3, 4, and 5 were added to Table 2-19 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-41
	The "VCCPLA/B/C/D/E/F PLL Supply Voltage" section was updated.	2-51
	The "VPUMP Programming Supply Voltage" section was updated.	2-51
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-52
	V_{JTAG} was deleted from the "TCK Test Clock" section.	2-52
	In Table 2-24 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-52
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2

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Previous Version	Changes in Current Version (v2.0)	Page
Advanced v0.6 (continued)	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1.	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed from 5.88 to	3-4
	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-4
	Table 3-5 • Package Thermal Resistivities was updated.	3-4
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-7
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-73 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was updated.	3-22
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-70 to 3-72
	Figure 3-53 • Timing Diagram was updated.	3-79
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP*" table is new.	4-4
	The A3PE1500 "484-Pin FBGA*" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advanced v0.5 (April 2006)	In the "I/Os Per Package1" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	iii
Advanced v0.4 (October 2005)	BLVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	The "Pro I/Os with Advanced I/O Standards" section was updated to include I/O bank information.	1-5
	Figure 2-7 • Very-Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-16 • CCC/PLL Macro were updated.	2-17
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-13 • ProASIC3E CCC Options were updated.	2-14
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-24
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-26
	The "Introduction" of the "Pro I/Os" section was updated.	2-27

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Previous Version	Changes in Current Version (v2.0)	Page
Advanced v0.4 (continued)	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-12 • VCCI Voltages and Compatible ProASIC3E Standards	2-29
	Table 2-15 • ProASIC3E I/O Features was updated.	2-31
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-34
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-37
	The notes in Table 2-18 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices were updated.	2-37
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-42
	A footnote was added to Table 2-16 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected).	2-32
	Table 2-20 • ProASIC3E I/O Attributes vs. I/O Standard Applications	2-46
	Table 2-21 • ProASIC3E I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings	2-47
	The "x" was updated in the "User I/O Naming Convention" section.	2-50
	The "VCC Core Supply Voltage" pin description was updated.	2-51
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-51
	EXTFB was removed from Figure 2-13 • ProASIC3E CCC Options.	2-14
	The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-4 • ProASIC3E CCC/PLL Specification.	2-18
	The LVPECL specification in Table 2-18 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-37
	Table 2-17 • Levels of Hot-Swap Support was updated.	2-36
	The "Cold-Sparing Support" section was updated.	2-37
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-37
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-51

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Previous Version	Changes in Current Version (v2.0)	Page
Advanced v0.3	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-51
	The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-51
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-52
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-52
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54
	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-4
	In Table 3-10 PAC4 was updated.	3-7
	Table 3-19 was updated.	3-19
	The note in Table 3-24 was updated.	3-22
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-25 to 3-63
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-73 to 3-78
	F_{TCKMAX} was updated in Table 3-98.	3-80
Advanced v0.2	The "ProASIC3E Ordering Information" table was updated.	iii
	The "Live at Power-Up" section is new.	1-2
	Figure 2-4 was updated.	2-4
	The "Clock Resources (VersaNets)" section was updated.	2-8
	The "VersaNet Global Networks and Spine Access" section was updated.	2-10
	The "PLL Macro" section was updated.	2-15
	Figure 2-16 was updated.	2-17
	Figure 2-19 was updated.	2-19
	Table 2-6 was updated.	2-24
	Table 2-7 was updated.	2-24
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-14 was updated.	2-30
	Figure 2-24 was updated.	2-33
	The "Cold-Sparing Support" section is new.	2-37
	Table 2-18 was updated.	2-37
	Table 2-20 was updated.	2-46
	Pin descriptions in the "JTAG Pins" section were updated.	2-52
	The "User I/O Naming Convention" section was updated.	2-50
	Table 3-7 was updated.	3-5
	The "Methodology" section was updated.	3-8
	The A3PE3000 "208-Pin PQFP*" pin table was updated.	4-6

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Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a advanced datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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