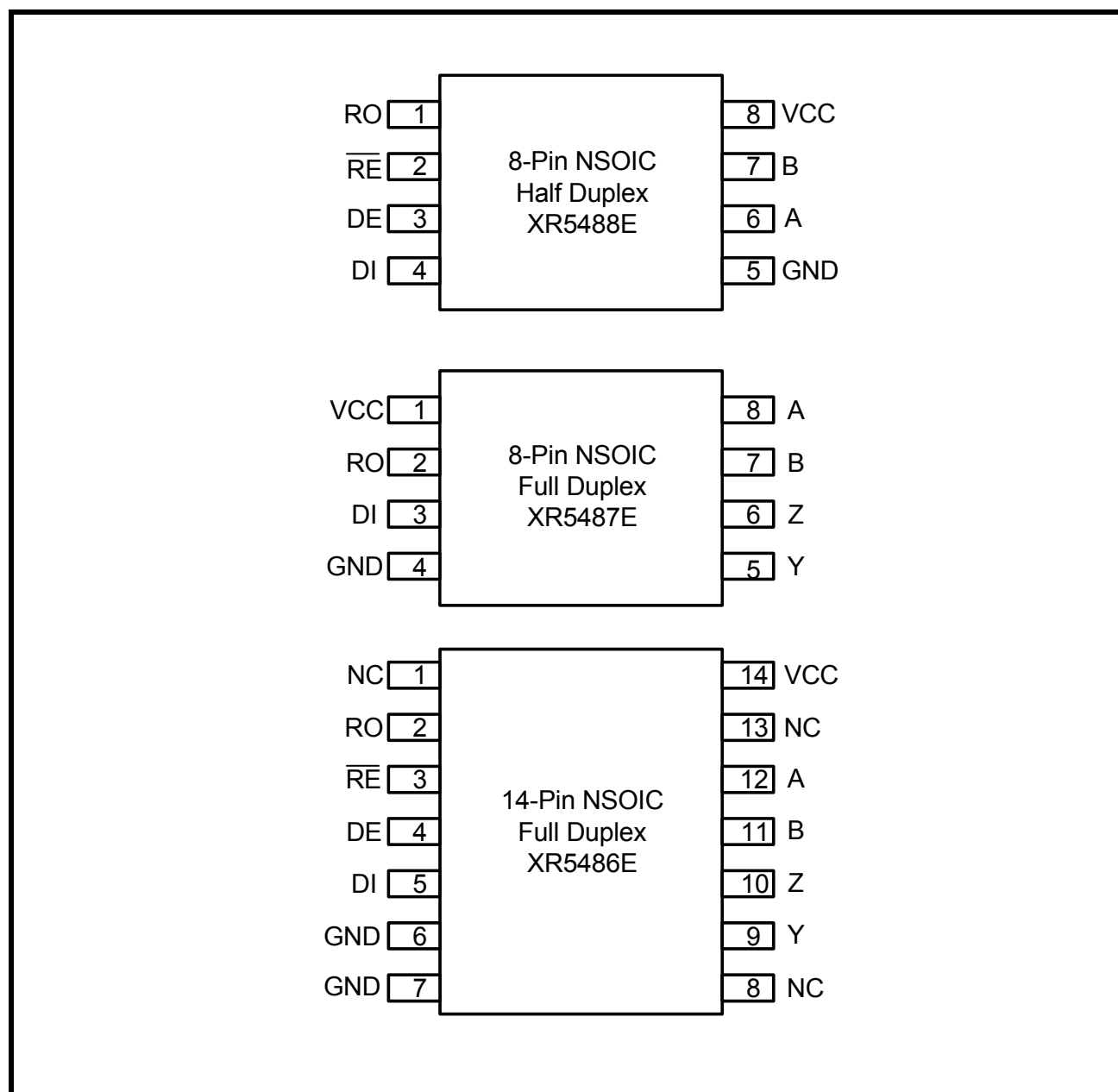


FIGURE 2. PIN OUT ASSIGNMENT

**ORDERING INFORMATION**

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR5486EID-F	14-pin Narrow SOIC	-40°C to +85°C	Active
XR5487EID-F	8-pin Narrow SOIC	-40°C to +85°C	Active
XR5488EID-F	8-pin Narrow SOIC	-40°C to +85°C	Active

Note: To order Tape and Reel option include "/TR" in ordering part number. All packages are Pb-free/ RoHS compliant.

PIN DESCRIPTIONS

Pin Assignments

PIN NUMBER			PIN NAME	TYPE	DESCRIPTION
HALF DUPLEX	FULL DUPLEX				
XR5488E	XR5487E	XR5486E			
1	2	2	RO	O	Receiver Output. When $\overline{RE}$ is low and if (A-B) $\geq$ -50mV, RO is High. If (A-B) $\leq$ -200mV, RO is Low.
2	-	3	$\overline{RE}$	I	Receiver Output Enable. When $\overline{RE}$ is Low, RO is enabled. When $\overline{RE}$ is High, RO is high impedance. $\overline{RE}$ should be High and $\overline{DE}$ should be low to enter shutdown mode. $\overline{RE}$ is a hot-swap input.
3	-	4	DE	I	Driver Output Enable. When DE is High, outputs are enabled. When DE is low, outputs are high impedance. DE should be low and $\overline{RE}$ should be High to enter shutdown mode. DE is a hot-swap input.
4	3	5	DI	I	Driver Input. With DE high, a low level on DI forces Non-Inverting output low and inverting output high. Similarly, a high level on DI forces Non-Inverting output High and Inverting output Low.
5	4	6, 7	GND	Pwr	Ground.
6	-	-	A	O	Non-Inverting Receiver Input and Non-Inverting Driver Output.
7	-	-	B	O	Inverting Receiver Input and Inverting Driver Output.
8	1	14	Vcc	Pwr	+5.0V power supply input. Bypass with 0.1uF capacitor.
-	8	12	A	I	Non-Inverting Receiver Input.
-	7	11	B	I	Inverting Receiver Input.
-	5	9	Y	O	Non-Inverting Driver Output.
-	6	10	Z	O	Inverting Driver Output.
-	-	1, 8, 13	NC	-	No Connect, not internally connected.

Pin type: I=Input, O=Output.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}	$V_{CC} \leq +7.0V$
Input voltage at control pins ($\overline{RE}$, DE)	-0.3V to ($V_{CC} + 0.3V$)
Driver input voltage (DI)	-0.3V to ($V_{CC} + 0.3V$)
Receiver output voltage (RO)	-0.3V to ($V_{CC} + 0.3V$)
Driver output voltage (A, B, Y and Z)	-8V to +13V
Receiver input voltage (A, B)	-8V to +13V
Voltage input range, transient pulse, A, B, Y and Z, through 100 Ω , see Figure 19.	+/-65.0V
Storage temperature range	-65°C to + 150°C
Lead temperature	+300°C
Power Dissipation Maximum Junction Temperature 150°C 8-Pin SO $\theta_{JA} = 128.4^{\circ}C/W$ 14-Pin SO $\theta_{JA} = 86^{\circ}C/W$	

CAUTION:

ESD (Electrostatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: $V_{CC} = +5.0V \pm 0.25V$ WITH T_A FROM -40°C TO +85°C. TYPICAL VALUES ARE AT $V_{CC} = +5.0V$ AND 25°C.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
DRIVER DC CHARACTERISTICS						
V_{OD}	Differential Driver Output			V_{CC}	V	No Load
		2.8				$R_L = 100\Omega$ (RS-422), Figure 3
		2.4				$R_L = 54\Omega$ (RS-485), Figure 3
		2.4				$V_{CM} = -7V$, Figure 4
		2.4				$V_{CM} = +12V$, Figure 4
ΔV_{OD}	Change in Magnitude of Differential Output	-0.20		0.20	V	$R_L = 100\Omega$ (RS-422), Figure 3, See note 1
		-0.20		0.20		$R_L = 54\Omega$ (RS-485), Figure 3, See note 1
		-0.20		0.20		$V_{CM} = -7V$, Figure 4, See note 1
		-0.20		0.20		$V_{CM} = +12V$, Figure 4, See note 1

UNLESS OTHERWISE NOTED: $V_{CC} = +5.0V \pm 0.25V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +5.0V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OC}	Driver Common Mode Output Voltage steady state			3.0	V	Figure 3
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	-0.2		0.2	V	Figure 3, See note 1
I_{OSD}	Driver Short Circuit Current Limit	-250		250	mA	$-7V \leq V_{OUT} \leq +12V$, Figure 5
I_{OL}	Output Leakage Current (Full-Duplex versions, Y and Z pins)	-75		125	μA	$DE = 0V, \overline{RE} = 0V, V_{CC} = 0V$ or $5V, -7V \leq V_{OUT} \leq +12V$
V_{IH}	Logic Input Thresholds (DI, DE, $\overline{RE}$)	2.0			V	Logic Input High
V_{IL}				0.8	V	Logic Input Low
V_{HYS}	Driver Input Hysteresis		100		mV	$T_A = 25^{\circ}C$
I_{IN}	Logic Input Current (DI, DE and $\overline{RE}$)	-1		1	μA	$0V \leq I_N \leq +V_{CC}$, after first transition
DRIVER AC CHARACTERISTICS						
freq	Data Signaling Rate	52			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%, Figure 4, $C_L = 50pF, R_L = 54\Omega$.
t_{PLH}	Driver Propagation Delay (Low to High)	4		25	ns	$C_L = 50pF, R_L = 54\Omega$, Figures 6 and 7
t_{PHL}	Driver Propagation Delay (High to Low)	4		25	ns	$C_L = 50pF, R_L = 54\Omega$, Figures 6 and 7
t_R	Driver Rise Time		2	8	ns	$C_L = 50pF, R_L = 54\Omega$, Figures 6 and 7
t_F	Driver Fall time		2	8	ns	$C_L = 50pF, R_L = 54\Omega$, Figures 6 and 7
$ t_{PLH} - t_{PHL} $	Differential Pulse Skew			+/-3	ns	Figures 6 and 7
t_{ZH}	Driver Enable to Output High			60	ns	$C_L = 50pF, R_L = 500\Omega$, Figures 8 and 9
t_{ZL}	Driver Enable to Output Low			60	ns	$C_L = 50pF, R_L = 500\Omega$, Figures 10 and 11
t_{HZ}	Driver Disable from Output High			60	ns	$C_L = 50pF, R_L = 500\Omega$, Figures 8 and 9
t_{LZ}	Driver Disable from Output Low			60	ns	$C_L = 50pF, R_L = 500\Omega$, Figures 10 and 11
t_{ZV}	Shutdown to Driver Output Valid			1	μs	$C_L = 50pF, R_L = 500\Omega$
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 2, 3 and 4

UNLESS OTHERWISE NOTED: $V_{CC} = +5.0V \pm 0.25V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +5.0V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
RECEIVER DC CHARACTERISTICS						
I_{IN}	Input Current (A, B pins)	-75		125	μA	DE = 0, $V_{CC} = 0$ or 3.3V V_A or $V_B = 12V$, other input 0V V_A or $V_B = -7V$, other input 0V
V_{IH}	Receiver Differential Thresholds ($V_A - V_B$)			-50	mV	$-7V \leq V_{CM} \leq +12V$, rising
V_{IL}		-200			mV	$-7V \leq V_{CM} \leq +12V$, falling
	Receiver Input Hysteresis		25		mV	$V_{CM} = 0V$
V_{OH}	Receiver Output Voltage High	$V_{CC} - 1.2$			V	$I_{OUT} = -8mA$, $V_{ID} = -50mV$
V_{OL}	Receiver Output Voltage Low			0.4	V	$I_{OUT} = 8mA$, $V_{ID} = -200mV$
I_{OZ}	High-Z Receiver Output Current			+/-1	μA	$\overline{RE} = V_{CC}$, $0.40 \leq V_{OUT} \leq +2.4V$
I_{OSS}	Receiver Output Short Circuit Current			+/-125	mA	$0 \leq V_{RO} \leq V_{CC}$
R_{IN}	Receiver Input Resistance	96			K Ω	$-7V \leq V_{CM} \leq +12V$
RECEIVER AC CHARACTERISTICS						
freq	Data Signaling Rate	52			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%, $C_L = 15pF$
t_{PLH}	Receiver Propagation Delay (Low to High)		20	30	ns	$V_{ID} = +/-2V$, $C_L = 15pF$, Figures 12 and 13
t_{PHL}	Receiver Propagation Delay (High to Low)		20	30	ns	$V_{ID} = +/-2V$, $C_L = 15pF$, Figures 12 and 13
skew	Receiver Propagation Delay Skew			+/-3	ns	$V_{ID} = +/-2V$, $C_L = 15pF$, Figures 12 and 13 $skew = t_{PLH} - t_{PHL} $
t_R	Receiver Output Rise Time		2	4	ns	$C_L = 15pF$
t_F	Receiver Output Fall Time		2	4	ns	$C_L = 15pF$
t_{ZH}	Receiver Enable to Output High			40	ns	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 15
t_{ZL}	Receiver Enable to Output Low			40	ns	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 16
t_{HZ}	Receiver Disable from Output High			40	ns	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 17
t_{LZ}	Receiver Disable from Output Low			40	ns	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 18
$t_{ZH(SHDN)}$	Shutdown to Receiver Output Valid High			1	μs	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 15

UNLESS OTHERWISE NOTED: $V_{CC} = +5.0V \pm 0.25V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +5.0V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{ZL(SHDN)}$	Shutdown to Receiver Output Valid Low			1	μs	$C_L = 15pF$, $R_L = 1k\Omega$, Figures 14 and 16
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 2, 3 and 4
POWER REQUIREMENTS AND RECOMMENDED OPERATING CONDITIONS						
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
I_{CC1}	Supply Current - Active Mode		800	1500	μA	No Load, $DE = \overline{RE} = V_{CC}$ or 0V, $DI = 0V$ or V_{CC}
I_{CC2}	Supply Current - Shutdown Mode			1	μA	$DE = 0V$, $\overline{RE} = V_{CC}$, $DI = V_{CC}$ or 0V
T_{SD}	Thermal Shutdown Temperature		165		$^{\circ}C$	
	Thermal Shutdown Hysteresis		20		$^{\circ}C$	
	ESD Protection at Pins A, B, Y and Z pins		+/-15		kV	Human Body Model
			+/-15		kV	IEC-61000-4-2 Air Discharge
			+/-8		kV	IEC-61000-4-2 Contact Discharge
	ESD Protection for RO, DI, DE and RE pins		+/-2		kV	Human Body Model
			+/-200		V	Machine Model

NOTE:

1. Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.
2. The transceivers are put into shutdown by bringing $\overline{RE}$ High and DE Low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. Note that the receiver and driver enable times increase during shutdown.
3. Guaranteed by design and bench characterization.
4. Except devices which do not have DE or $\overline{RE}$ inputs.

FIGURE 3. DRIVER DC TEST CIRCUIT

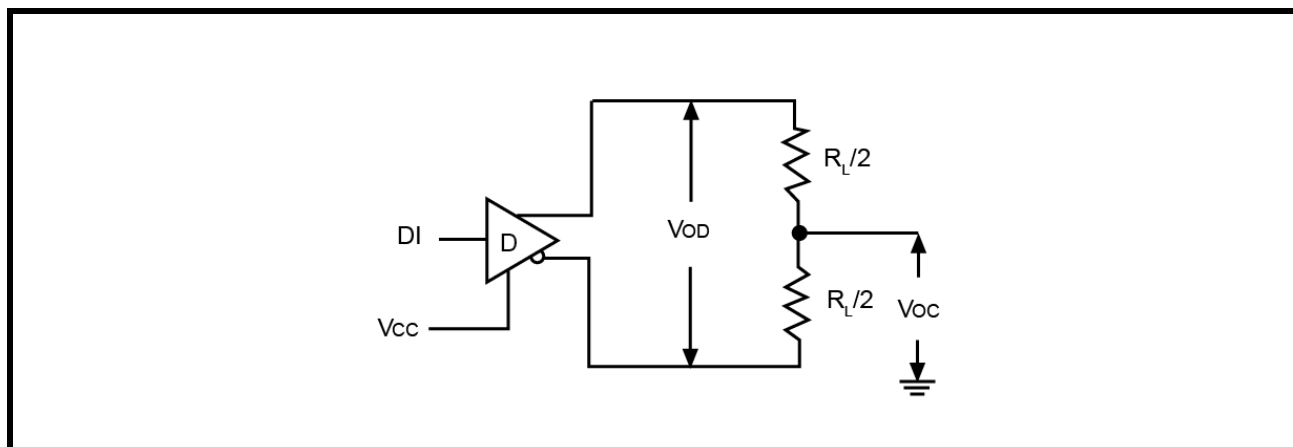


FIGURE 4. DRIVER COMMON MODE LOAD TEST

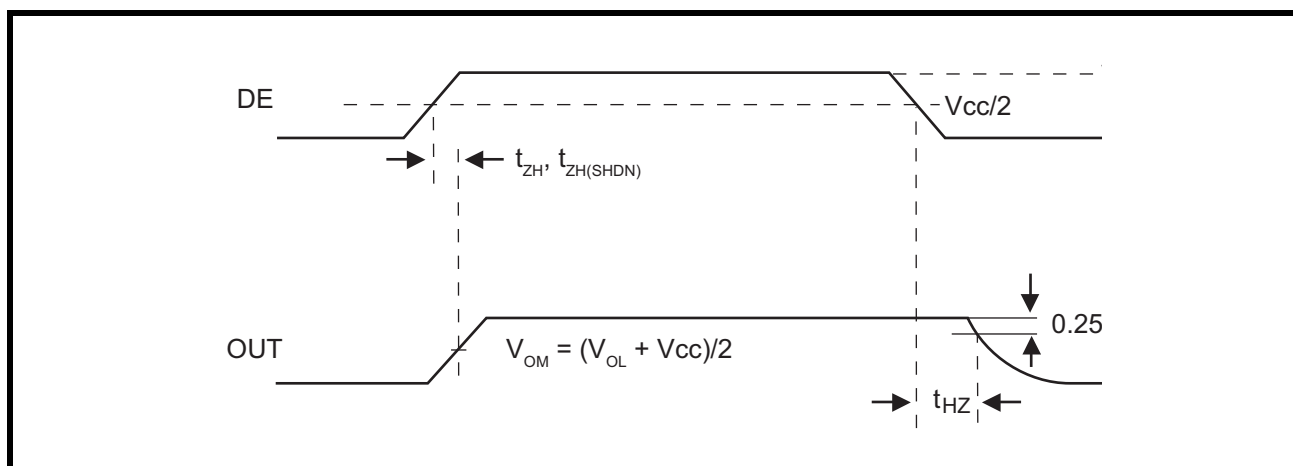


FIGURE 5. DRIVER SHORT CIRCUIT CURRENT LIMIT TEST

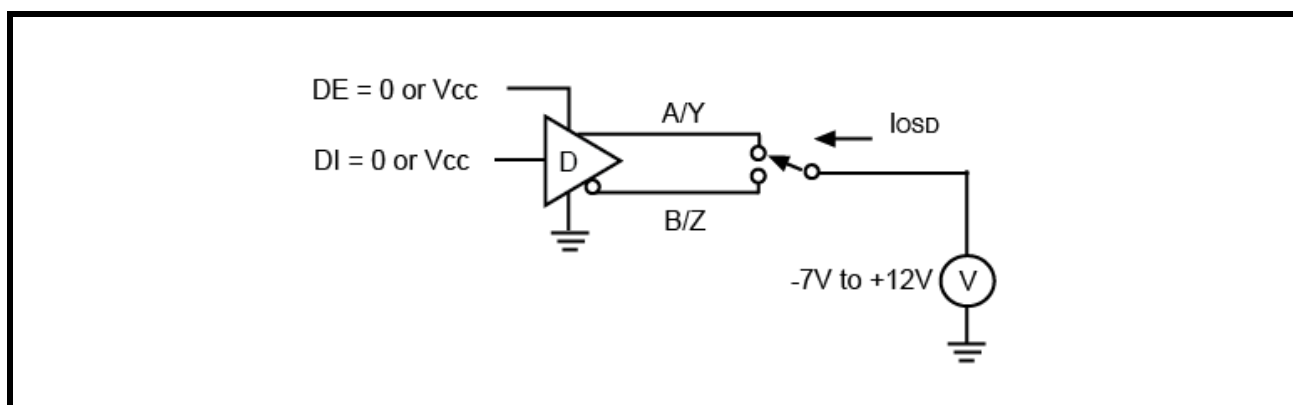


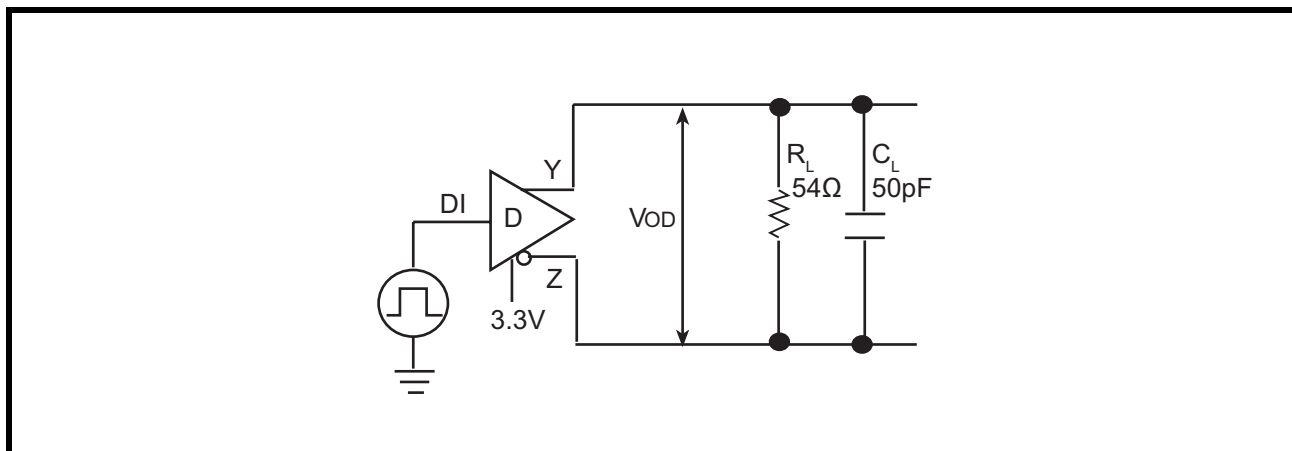
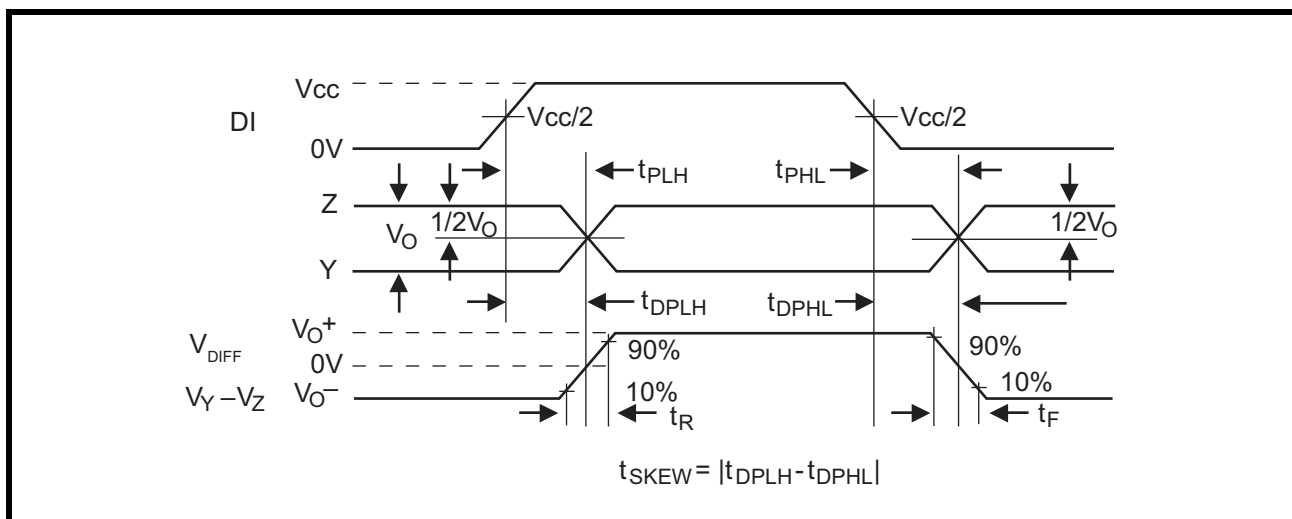
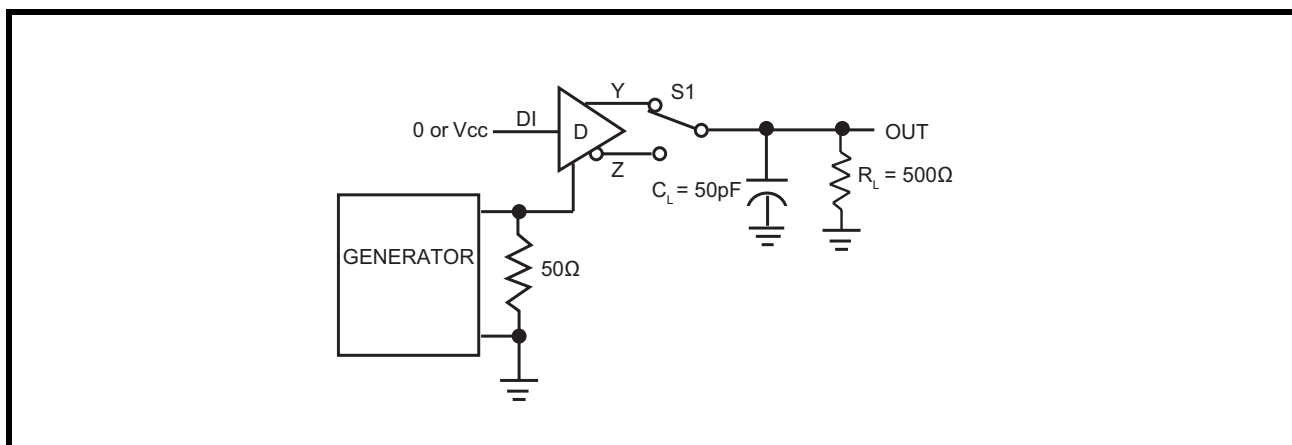
FIGURE 6. DRIVER PROPAGATION DELAY TEST CIRCUIT

FIGURE 7. DRIVER PROPAGATION DELAY TIMING DIAGRAM

FIGURE 8. DRIVER ENABLE AND DISABLE TIME TEST CIRCUIT 1


FIGURE 9. DRIVER ENABLE DISABLE TIMING DIAGRAM 1

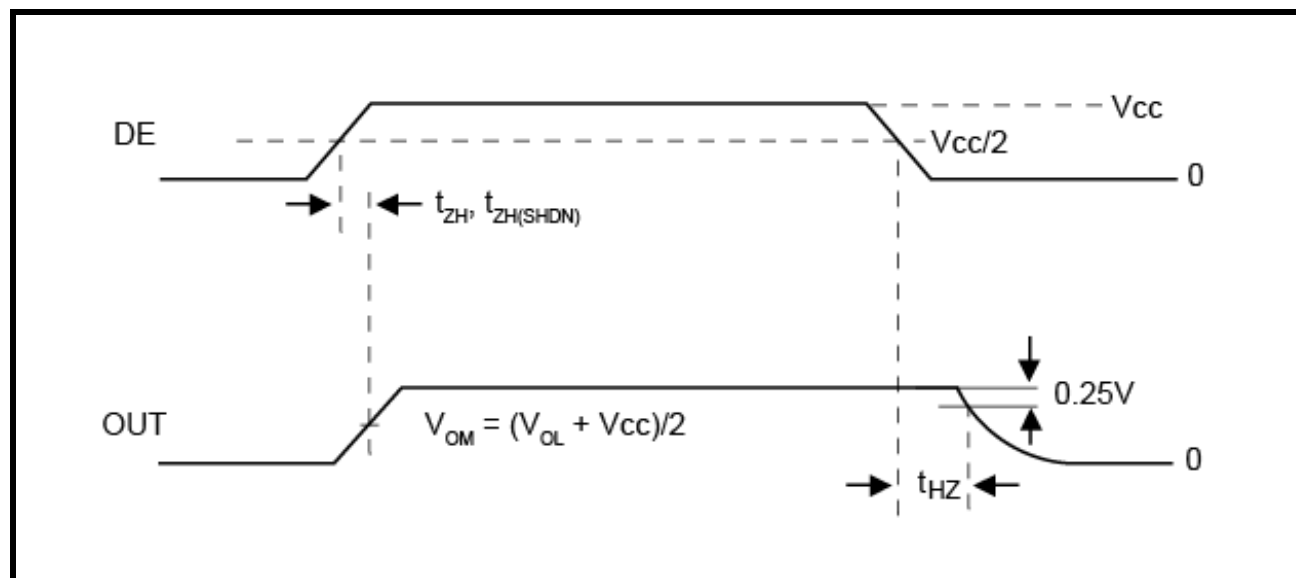


FIGURE 10. DRIVER ENABLE AND DISABLE TIME TEST CIRCUIT 2

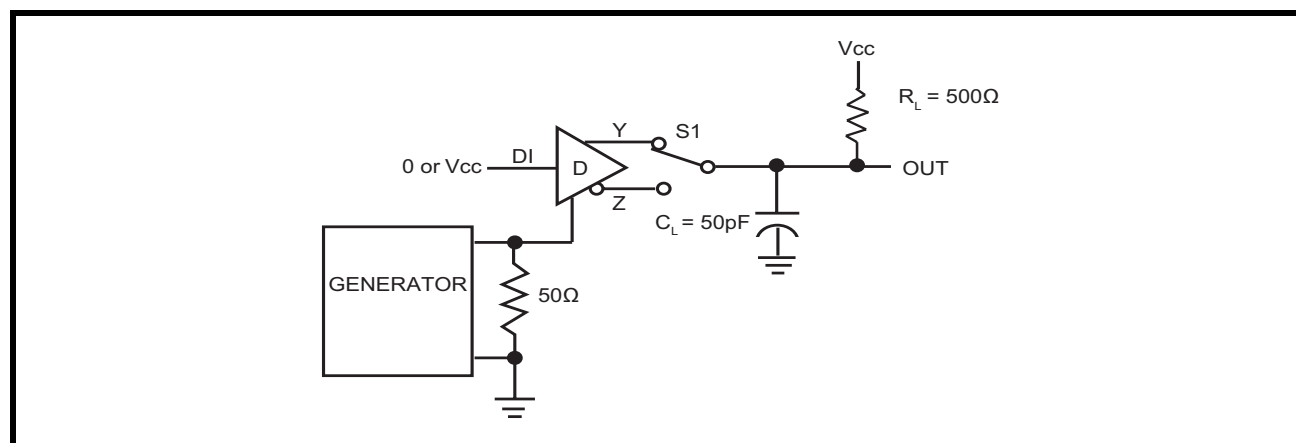


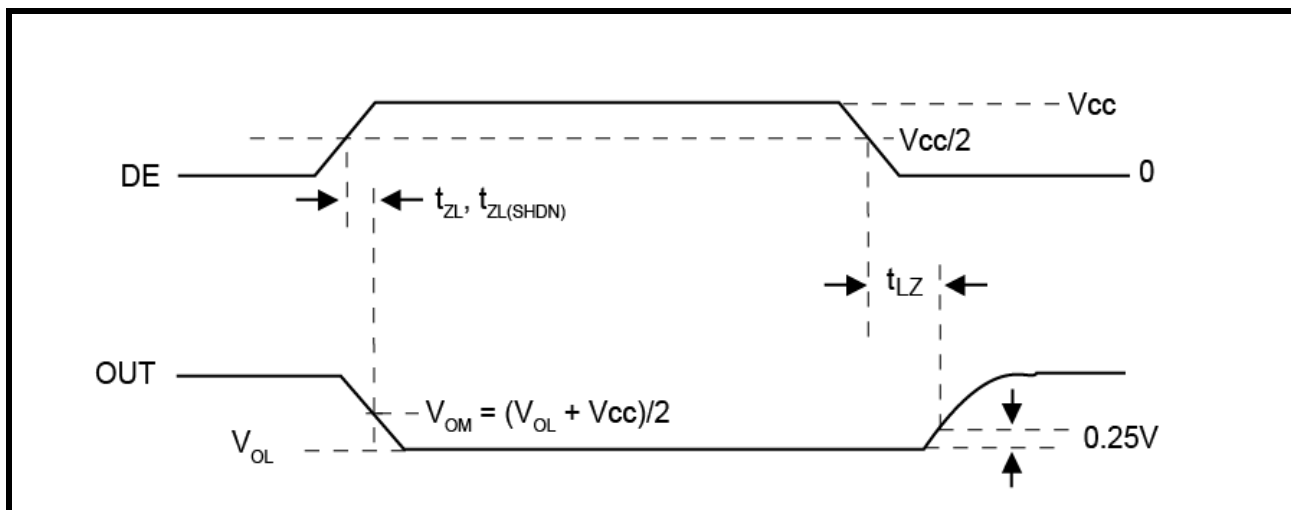
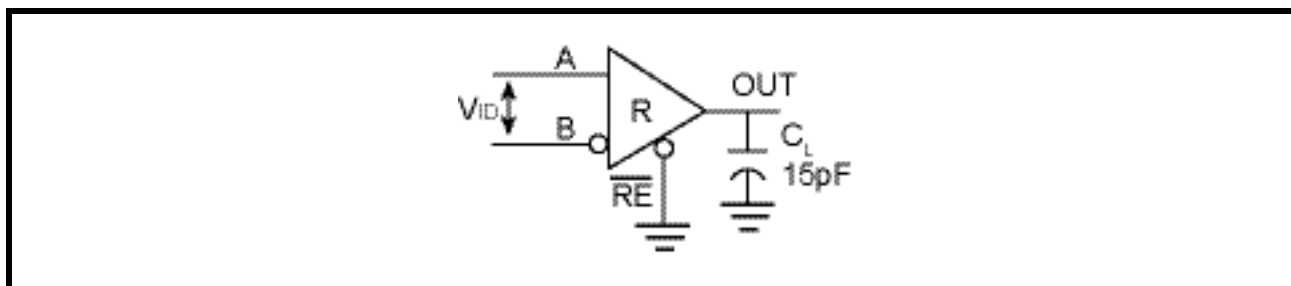
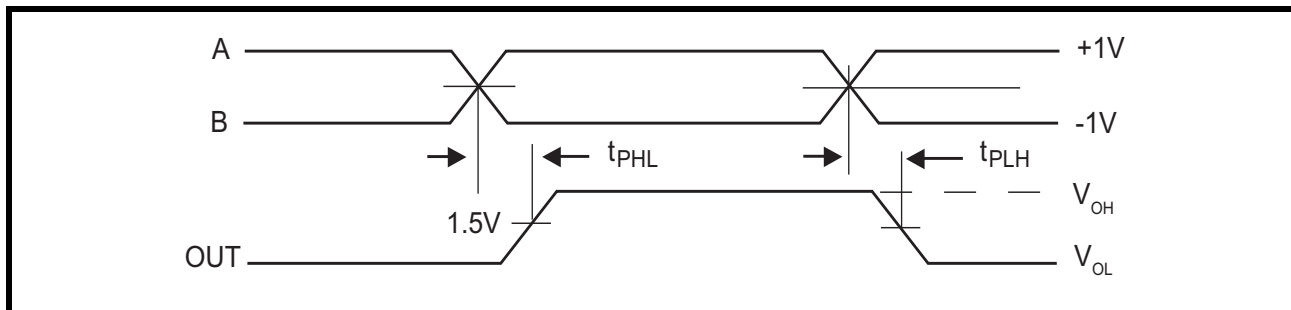
FIGURE 11. DRIVER ENABLE AND DISABLE TIMING DIAGRAM 2

FIGURE 12. RECEIVER PROPAGATION DELAY TEST CIRCUIT

FIGURE 13. RECEIVER PROPAGATION DELAY TIMING DIAGRAM


FIGURE 14. RECEIVER ENABLE AND DISABLE TIMES TEST CIRCUIT

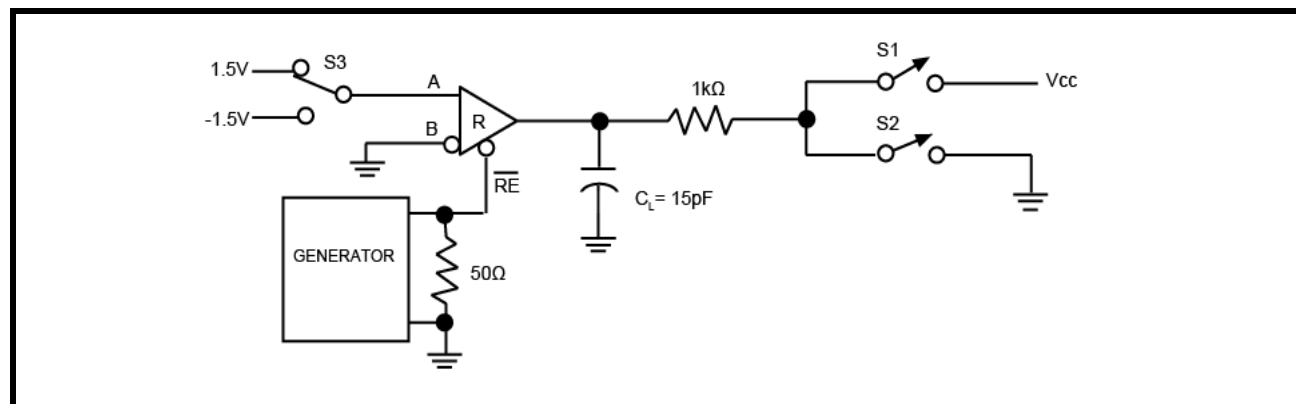


FIGURE 15. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 1

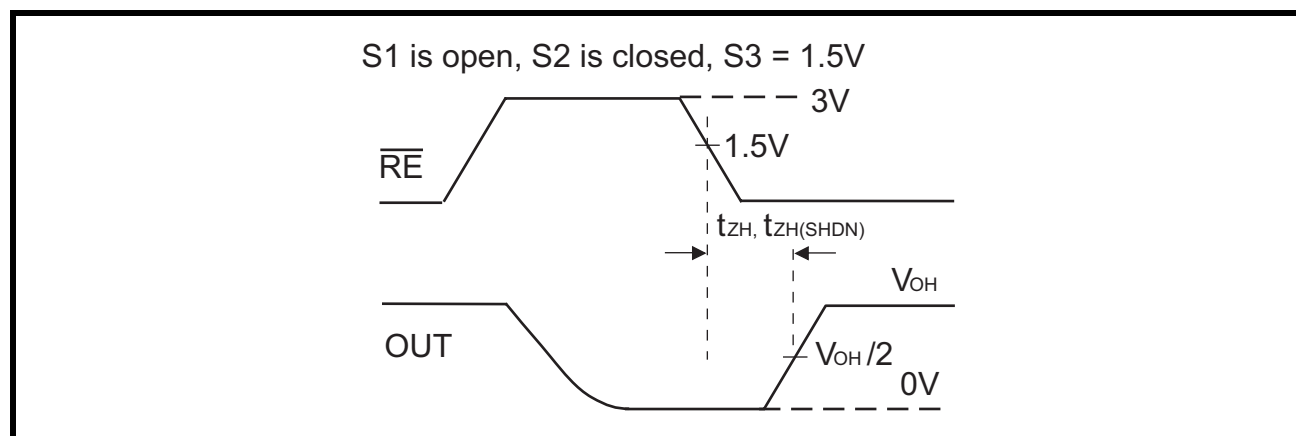


FIGURE 16. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 2

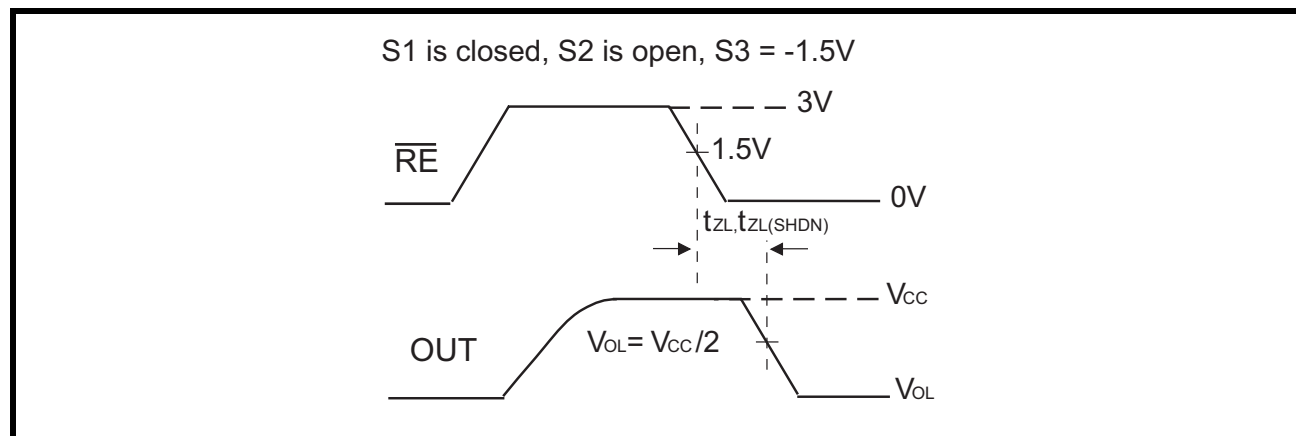
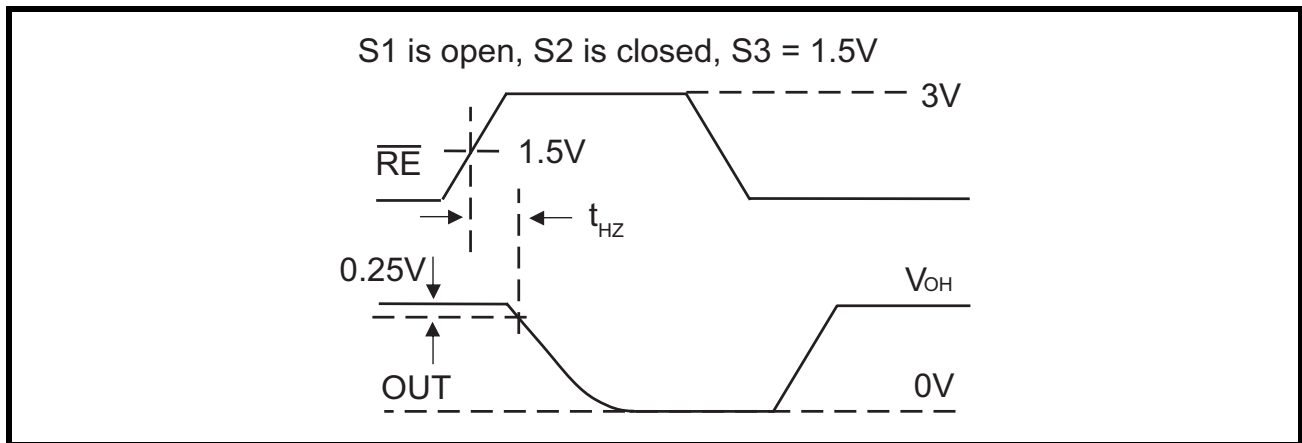
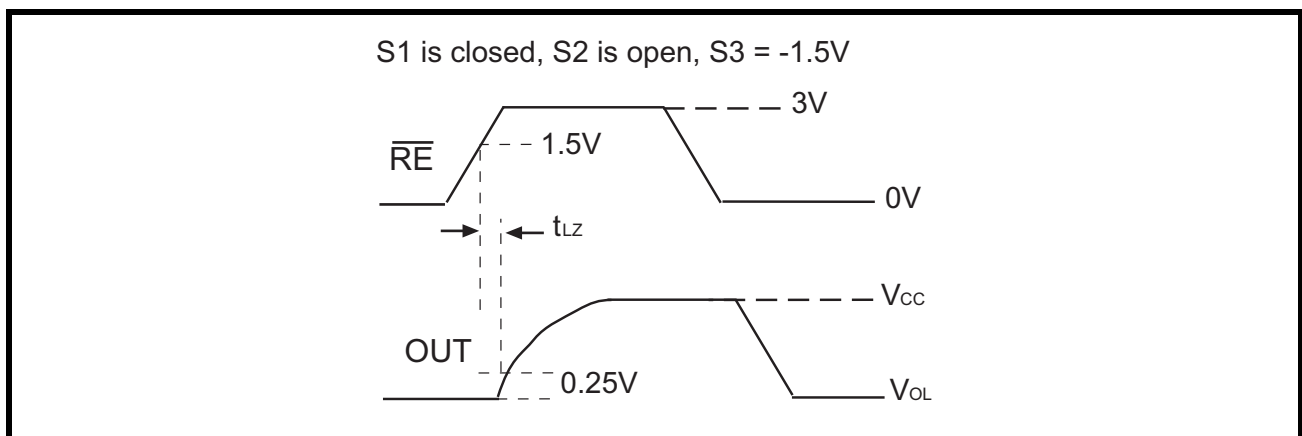
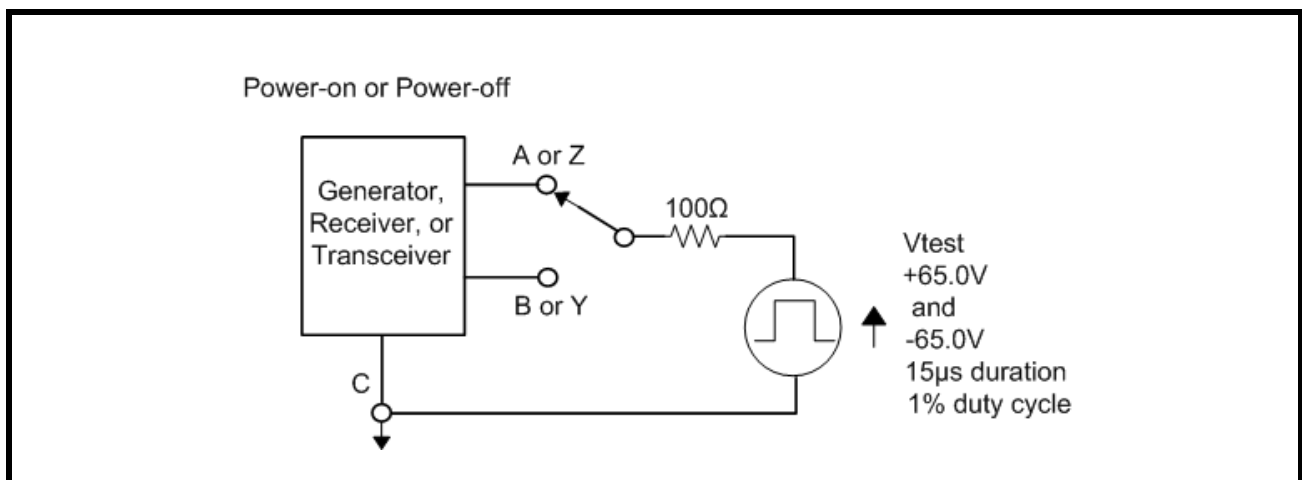


FIGURE 17. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 3

FIGURE 18. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 4

FIGURE 19. TRANSIENT OVER VOLTAGE TOLERANCE TEST CIRCUIT 1


1.0 PRODUCT DESCRIPTION

XR5486E-XR5488E is a family of advanced RS-485/RS-422 transceivers. Each contain one driver and one receiver. The XR5488E is a half-duplex design while the XR5486E and XR5487E are full-duplex designs. All devices operate from a single 5.0V power supply. These devices feature failsafe circuitry that guarantees a logic-high receiver output when the inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. The control pins $\overline{RE}$ and $\overline{DE}$ feature a hotswap capability allowing live insertion without spurious data transfer. The drivers are not slew rate limited making transmit speeds up to 52Mbps possible. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry forces the driver output into a high-impedance state.

ADVANCED FAILSAFE

Ordinary RS-485 differential receivers will be in an indeterminate state whenever the data bus is not being actively driven. The Advanced Failsafe feature of the XR5486E-XR5488E family guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. In a terminated bus with all transmitters disabled, the receivers' differential input voltage is pulled to 0V by the termination. The XR5486E-XR5488E family interprets 0V differential as a logic high with a minimum 50mV noise margin while maintaining compliance with the EIA/TIA-485 standard of +/-200mV.

HOT-SWAP CAPABILITY

When a micro-processor or other logic device undergoes its power-up sequence, its logic-outputs are typically at high impedance. In this state they are unable to drive the $\overline{DE}$ and $\overline{RE}$ signals to a defined logic level. During this period, noise, parasitic coupling or leakage from other devices could cause standard CMOS enable inputs to drift to an incorrect logic level.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may suddenly be applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

The XR5486E-XR5488E family contains a special power-on-reset circuit that holds the driver enable and receiver enable inactive for approximately 10 microseconds. After this initial power-up sequence the hot-swap circuit becomes transparent and driver enable and receiver enable resume their normal un-skewed functions and timings.

+/-15kV ESD PROTECTION

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the XR5486E-XR5488E family have extra protection against static electricity. Exar uses state of the art structures to protect these pins against ESD of +/-15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown and powered down. After an ESD event, the XR5486E-XR5488E family keep operating without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the XR5486E-XR5488E family are characterized for protection to the following limits:

- +/-15kV using the Human Body Model
- +/-8kV using the Contact Discharge Model
- +/-15kV using the Airgap Discharge Model

ESD TEST CONDITIONS

ESD performance depends on a variety of conditions. Contact Exar for a reliability report that documents test setup, methodology and results.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The XR5486E-XR5488E family helps you design equipment to meet IEC 61000-4-2, without sacrificing board-space and cost for external ESD-protection components.

The major differences between tests done using the Human body model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that of human body model.

The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

MACHINE MODEL

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12k Ohms (1 unit load). A standard driver can drive up to 32 unit loads. The XR5486E-XR5488E family of transceivers have only a 1/8th unit load receiver input impedance of 96k Ohms, thereby allowing eight times as many, up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown devices draw only 50nA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ apply when the parts are shutdown. The drivers and receivers take longer to become enabled from low-power shutdown $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver / receiver disable mode (t_{ZH} and t_{ZL}).

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

LINE LENGTH

The RS-485/RS-422 standard covers line lengths up to 4000ft. Maximum achievable line length is a function of signal attenuation and noise. Termination prevents signal reflections by eliminating the impedance mismatches on a transmission line. Line termination is generally used if rise and fall times are shorter than the round-trip signal propagation time.

2.0 FUNCTION TABLES

TABLE 1: FULL DUPLEX 14 PIN XR5486E

TRANSMITTING				
Inputs			Outputs	
$\overline{\text{RE}}$	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

TABLE 2: FULL DUPLEX 8 PIN XR5487E

TRANSMITTING		
Input	Outputs	
DI	Y	Z
1	1	0
0	0	1

TABLE 3: HALF DUPLEX XR5488E

TRANSMITTING				
Inputs			Outputs	
$\overline{\text{RE}}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

TABLE 4: FULL DUPLEX 14 PIN XR5486E

RECEIVING			
Inputs			Ouptut
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	$\geq -50\text{mV}$	1
0	X	$\leq -200\text{mV}$	0
0	X	Open/Shorted	1
1	1	X	High-Z
1	0	X	Shutdown

TABLE 5: FULL DUPLEX 8 PIN XR5487E

RECEIVING	
Inputs	Output
$V_A - V_B$	RO
$\geq -50\text{mV}$	1
$\leq -200\text{mV}$	0
Open/Shorted	1

TABLE 6: HALF DUPLEX XR5488E

RECEIVING			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	$\geq -50\text{mV}$	1
0	X	$\leq -200\text{mV}$	0
0	X	Open/Shorted	1
1	1	X	High-Z
1	0	X	Shutdown

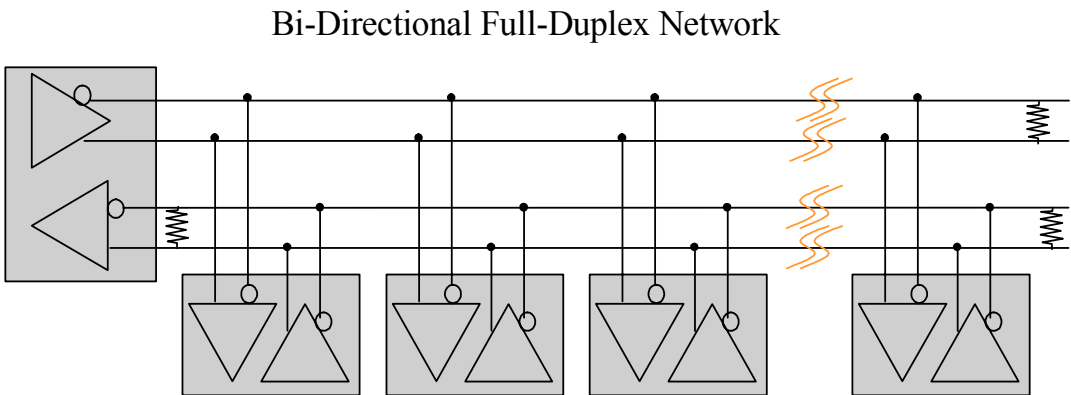
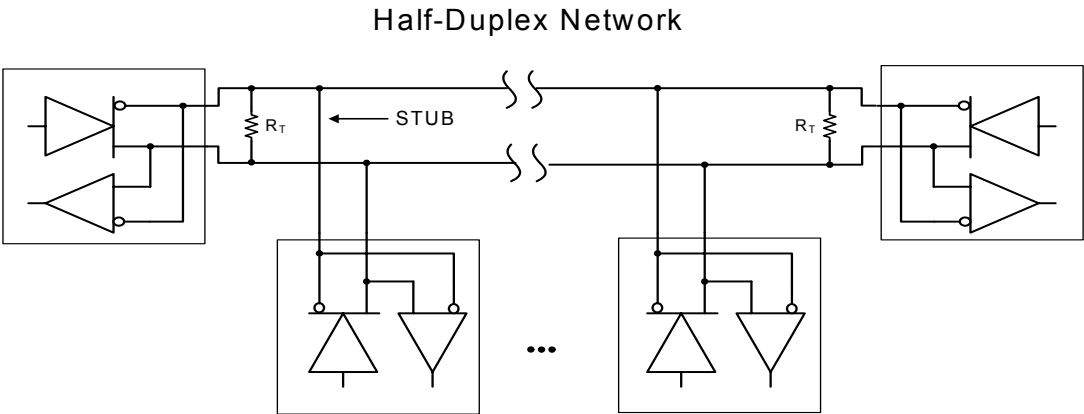
Note: Receiver inputs $-200\text{mV} < V_A - V_B < -50\text{mV}$ should be considered indeterminate.

3.0 PRODUCT SELECTOR GUIDE

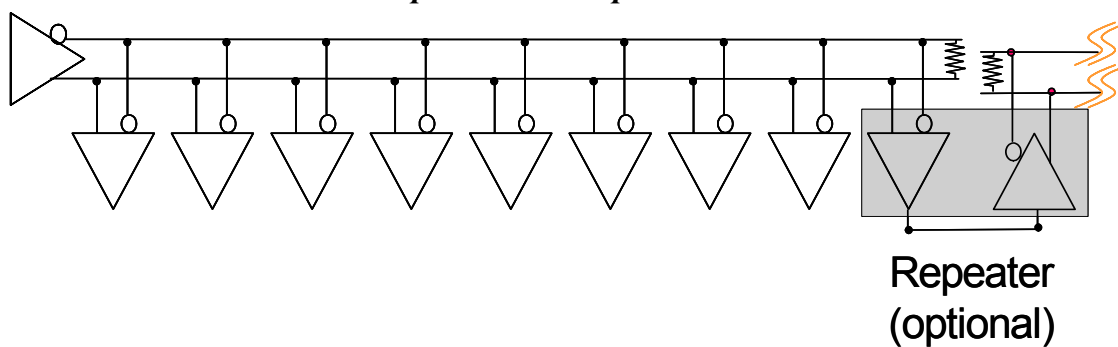
TABLE 7: SELECTION GUIDE

PART NUMBER	DUPLEX	DATA RATE MBPS	SHUTDOWN	RECEIVER AND DRIVER ENABLE	TRANS ON BUS	FOOT-PRINT
XR5486E	Full	52	Yes	Yes	256	SN75180
XR5487E	Full	52	No	No	256	SN75179
XR5488E	Half	52	Yes	Yes	256	SN75176

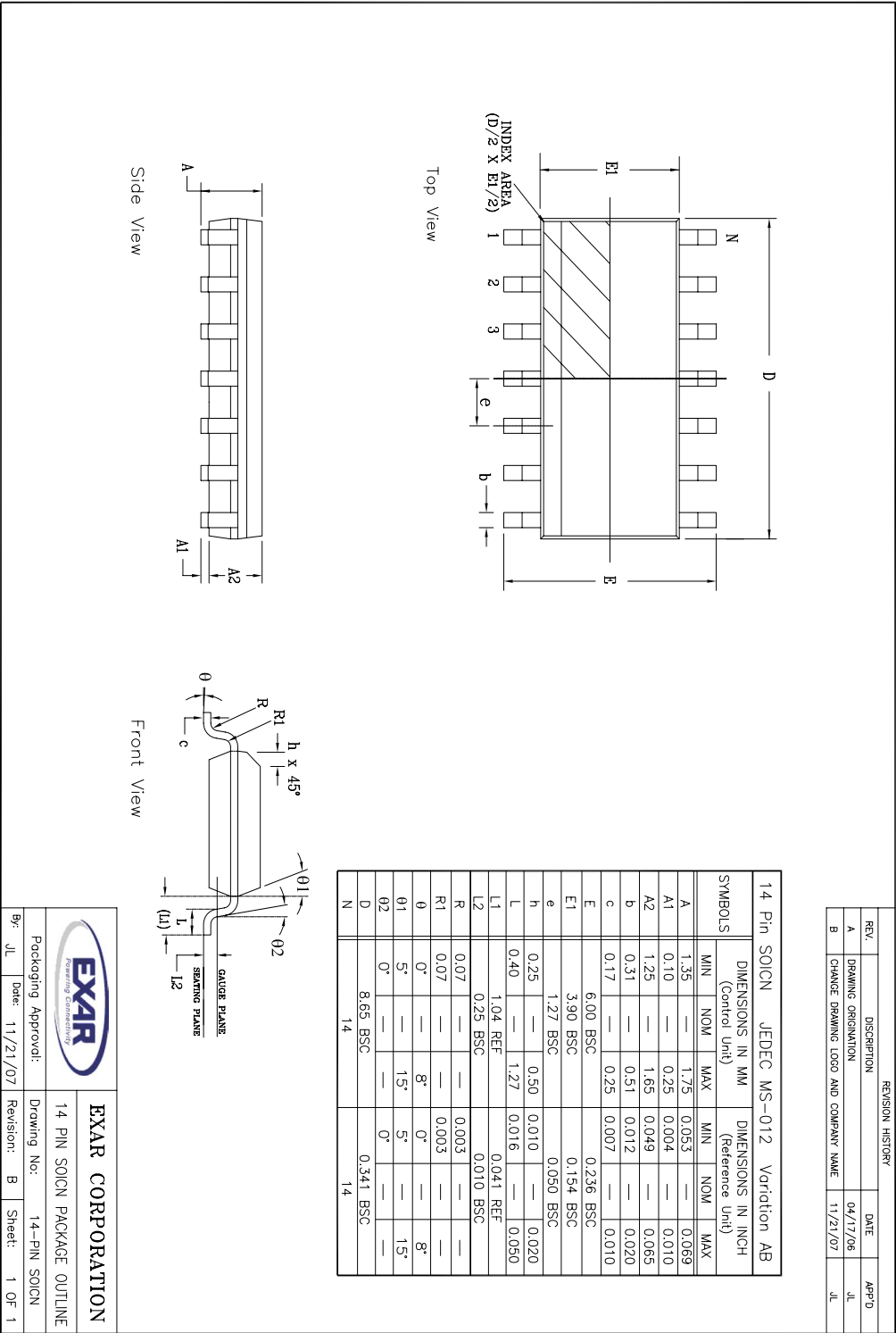
4.0 TYPICAL APPLICATIONS:



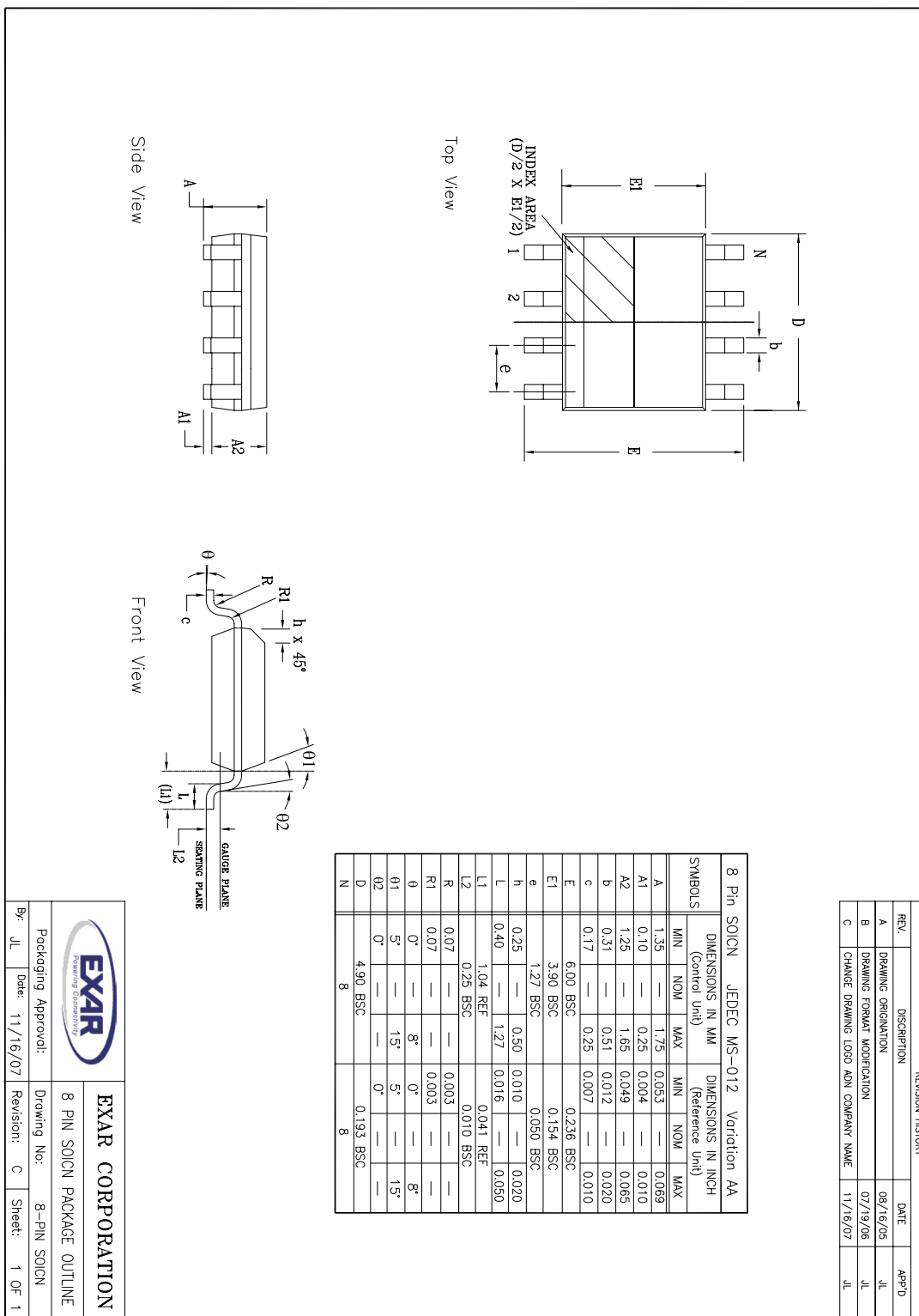
Point to Multi-point with Repeater



PACKAGE DIMENSIONS (14 PIN NSOIC)



PACKAGE DIMENSIONS (8 PIN NSOIC)



REVISION HISTORY

DATE	REVISION	DESCRIPTION
November 2009	Rev 1.0.0	Released datasheet.
October 2010	1.0.1	Add PROFIBUS logo to front page
August 2011	1.0.2	Change driver rise and fall time from 2ns minimum to 2ns typical. Add +/-65V Transient over voltage tolerance to ABS Max Ratings and add Figure 19 Transient test circuit.

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