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1 Block diagram and pin description

Figure 1. Block diagram

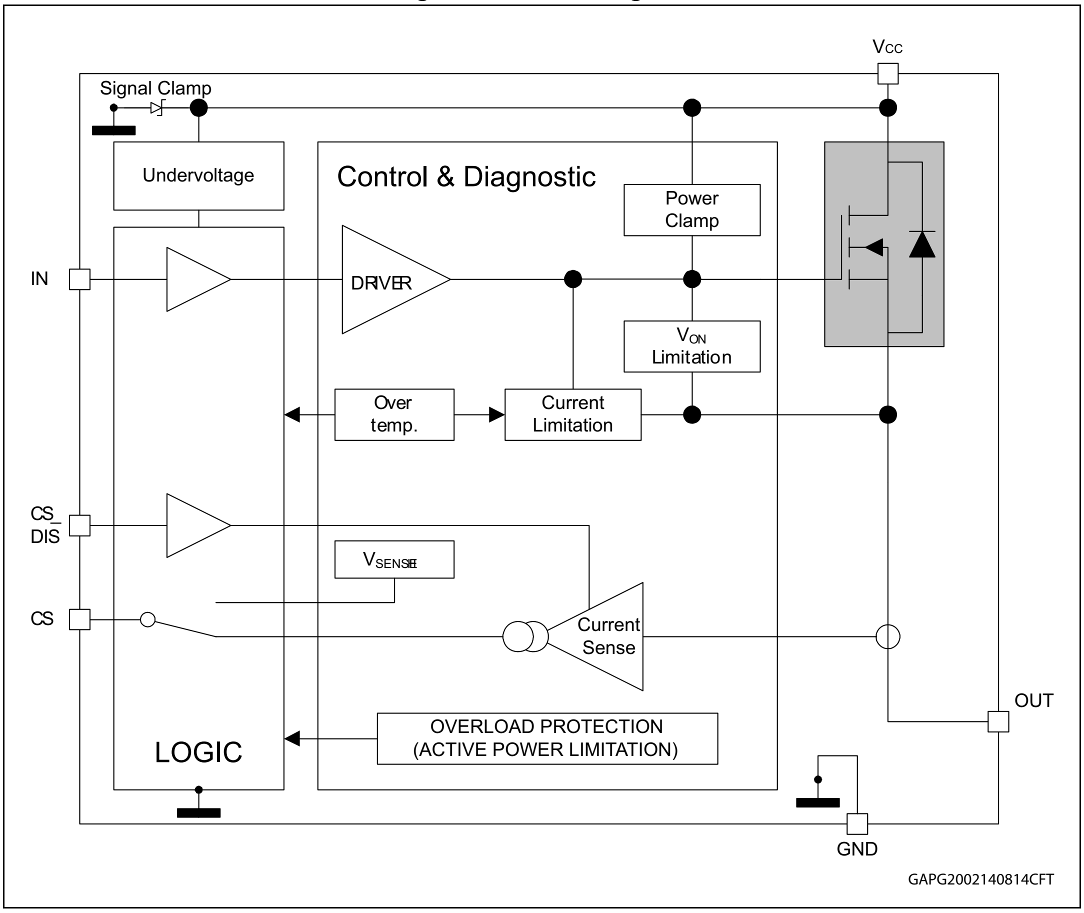


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection
OUTPUT	Power output (1)
GND	Ground connection
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

1. Pins 1 and 7 must be externally tied together.

Figure 2. Configuration diagram (top view) not in scale

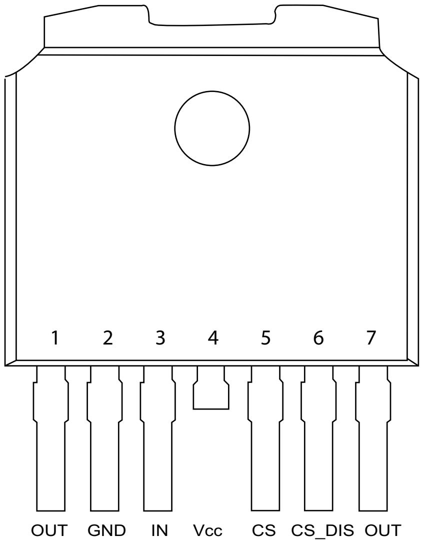
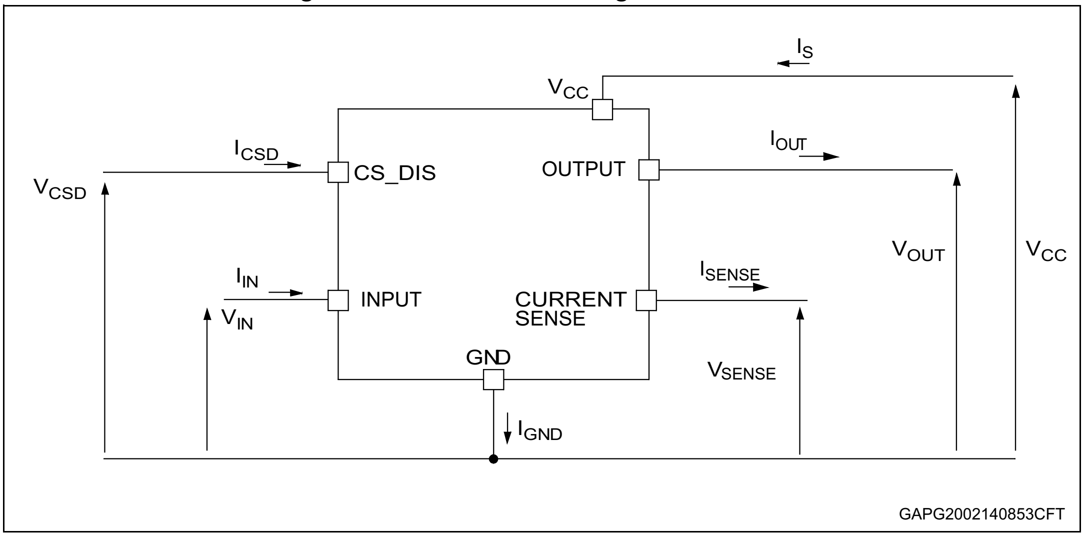


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	Output	Input	CS_DIS
Floating	Not allowed	X	X	X
To ground	Through 1 kΩ resistor	Through 22 kΩ resistor	Through 10 kΩ resistor	Through 10 kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
I_{GND}	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage ($V_{CC} > 0$)	V_{CC}-41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 1.55$ mH; $R_L = 0\ \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}$(Typ.))	350	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.63	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	69.3	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V, -40 °C < T_j < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 5 A; T_j = 25 °C			16	mΩ
		I_{OUT} = 5 A; T_j = 150 °C			32	mΩ
		I_{OUT} = 5 A; V_{CC} = 5 V; T_j = 25 °C			20	mΩ
V_F	Output - V_{CC} diode voltage	-I_{OUT} = 5 A; T_j = 150 °C			0.7	V
V_{clamp}	Clamp voltage	I_{CC} = 20 mA; I_{OUT} = 0 A	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2	5	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		1.5	3	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	µA

Table 6. Switching (V_{CC} = 13 V, T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.6 Ω (see *Figure 5*)	—	15	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.6 Ω (see *Figure 5*)	—	45	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.6 Ω	—	0.2	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.6 Ω	—	0.2	—	V/µs
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 2.6 Ω (see *Figure 5*)	—	1.4	—	mJ
W_{OFF}	Switching energy losses at turn-off (t_{won})	R_L = 2.6 Ω (see *Figure 5*)	—	0.8	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Table 8. Protection and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	V_{CC} = 13 V	54	73	108	A
		5 V < V_{CC} < 28 V			108	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		18		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC} -41	V_{CC} -46	V_{CC} -52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5 A; T_j = -40 °C to 150 °C		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; T_j = -40 °C to 150 °C	2836	6200	10444	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 5 A; V_{SENSE} = 0.5 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	 4306 4358	 5200 5200	 7004 6106	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 5 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	- 11		+ 11	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	 4608 4501	 5040 5040	 5926 5502	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} =10 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	- 8		+ 8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	 4612 4566	 4930 4930	 5367 5168	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j= -40 °C to 150 °C	- 4		+ 4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40 °C to 150 °C	0		1	µA
		V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40 °C to 150 °C	0		2	µA
		I_{OUT} = 2 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; T_j = -40 °C to 150 °C			1	µA
I_{OL}	Openload ON-state current detection threshold	V_{IN} = 5 V; I_{SENSE} = 5 µA	5		70	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} =18 A; R_{SENSE} = 3.9 KΩ	5			V
V_{SENSEH} (2)	Analog sense output voltage in fault condition	V_{CC} = 13V; R_{SENSE} = 3.9 KΩ		8		V
I_{SENSEH} (2)	Analog sense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		270	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V; I_{SENSE} = 90 % of $I_{SENSEMAX}$; I_{OUT} = 90 % of I_{OUTMAX}; I_{OUTMAX} = 3 A (see *Figure 7*)			280	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design, it is not tested.
2. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

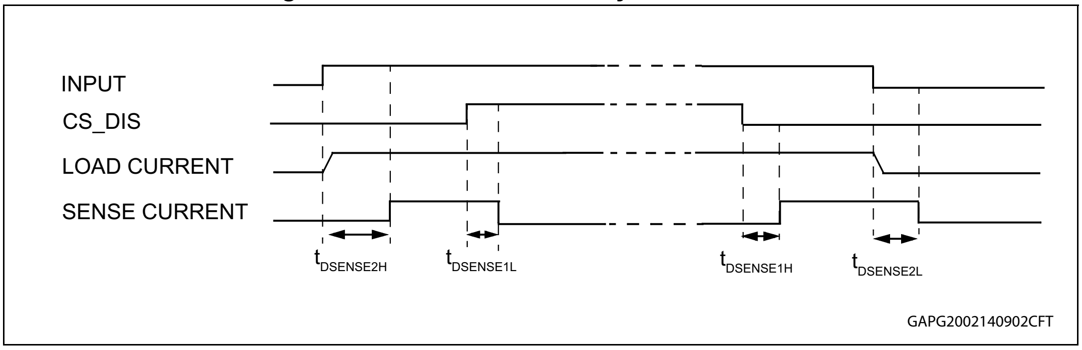


Figure 5. Switching characteristics

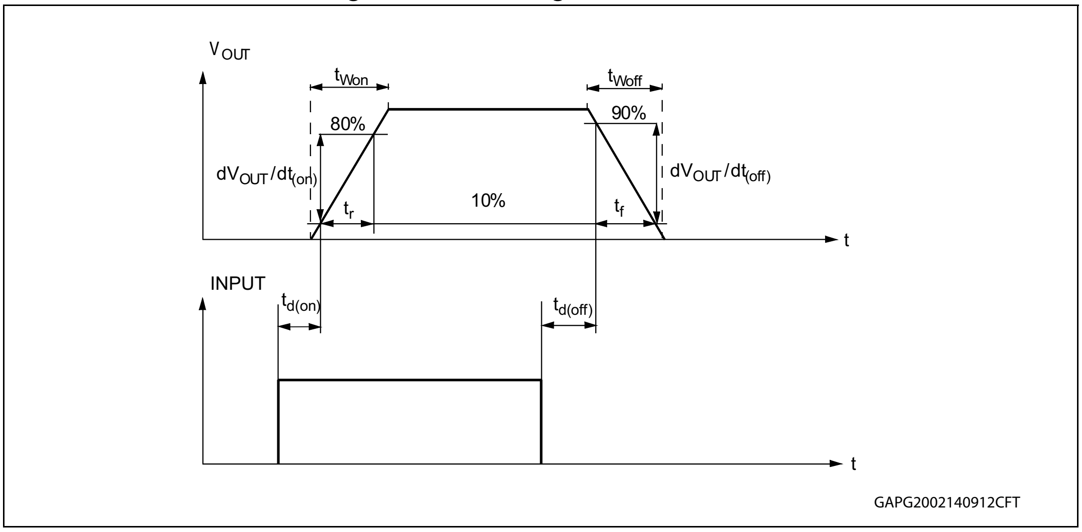


Figure 6. Output voltage drop limitation

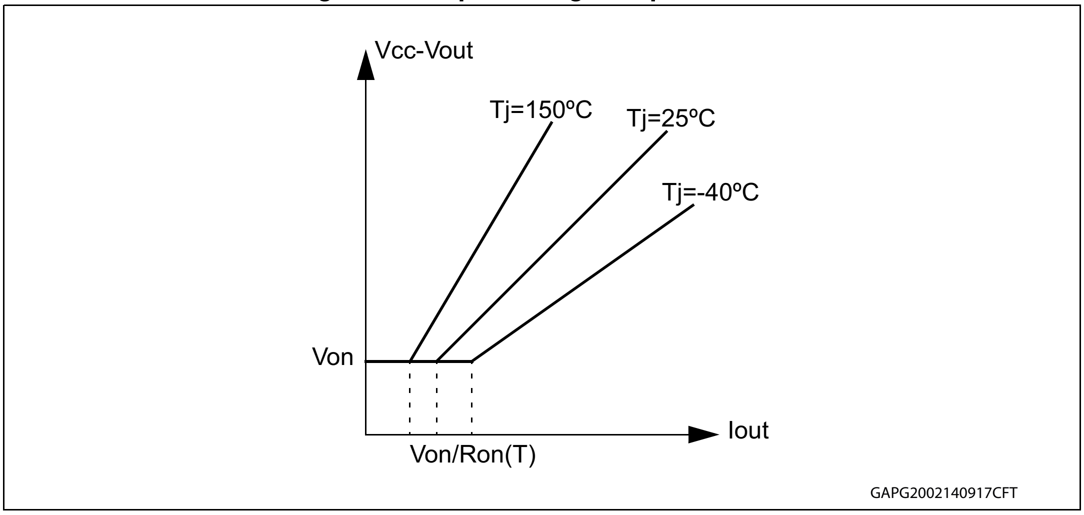


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

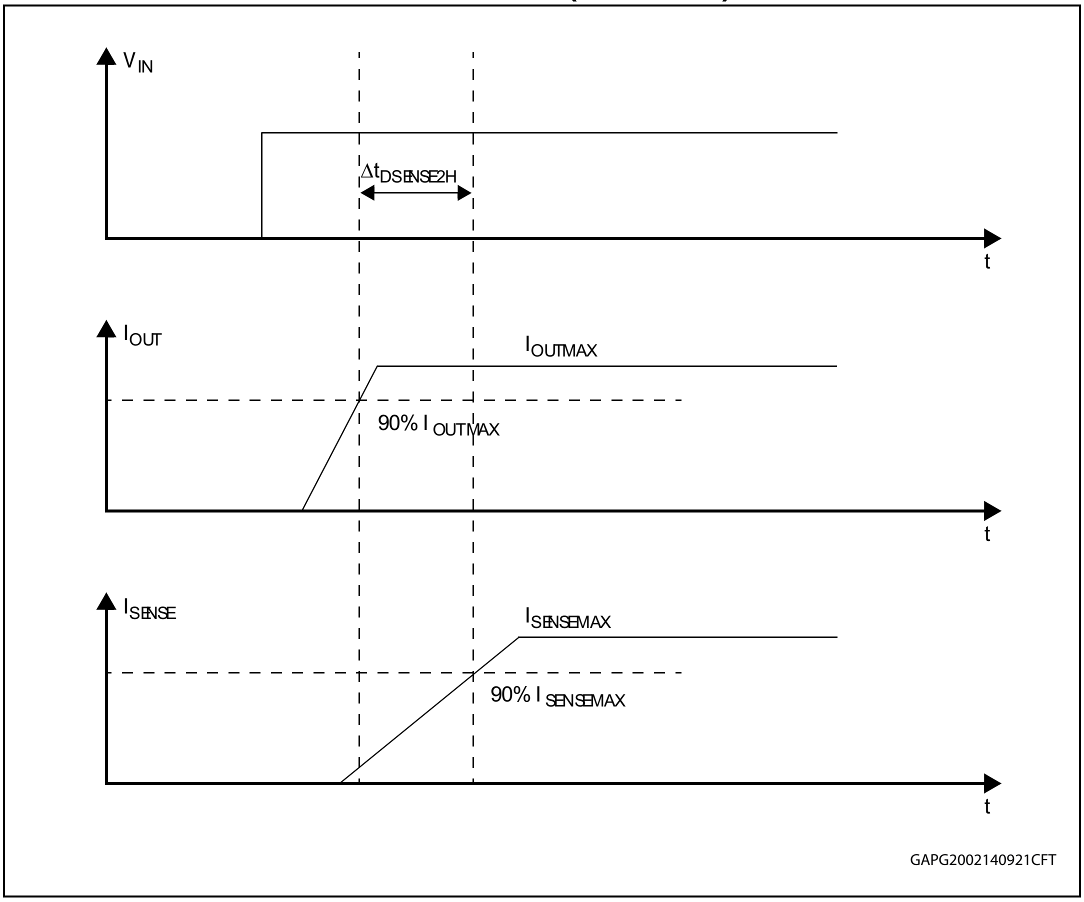


Figure 8. I_{OUT}/I_{SENSE} vs I_{OUT}

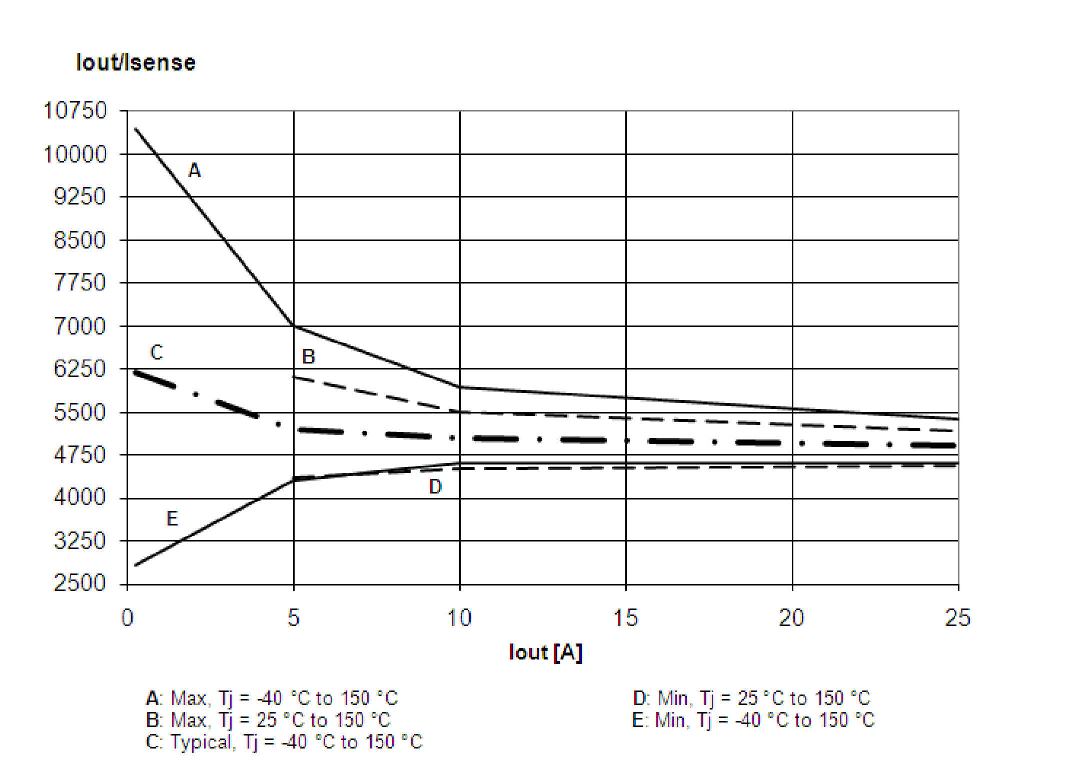
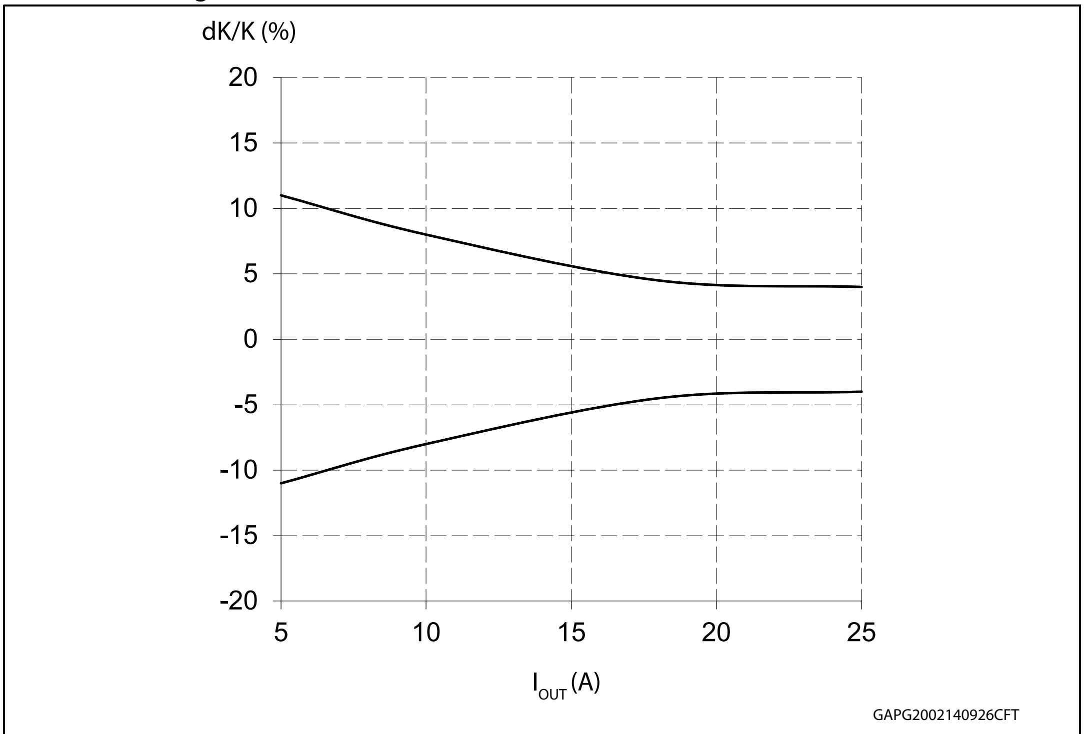


Figure 9. Maximum current sense ratio drift vs load current



1. Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01Ω
5b(1)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

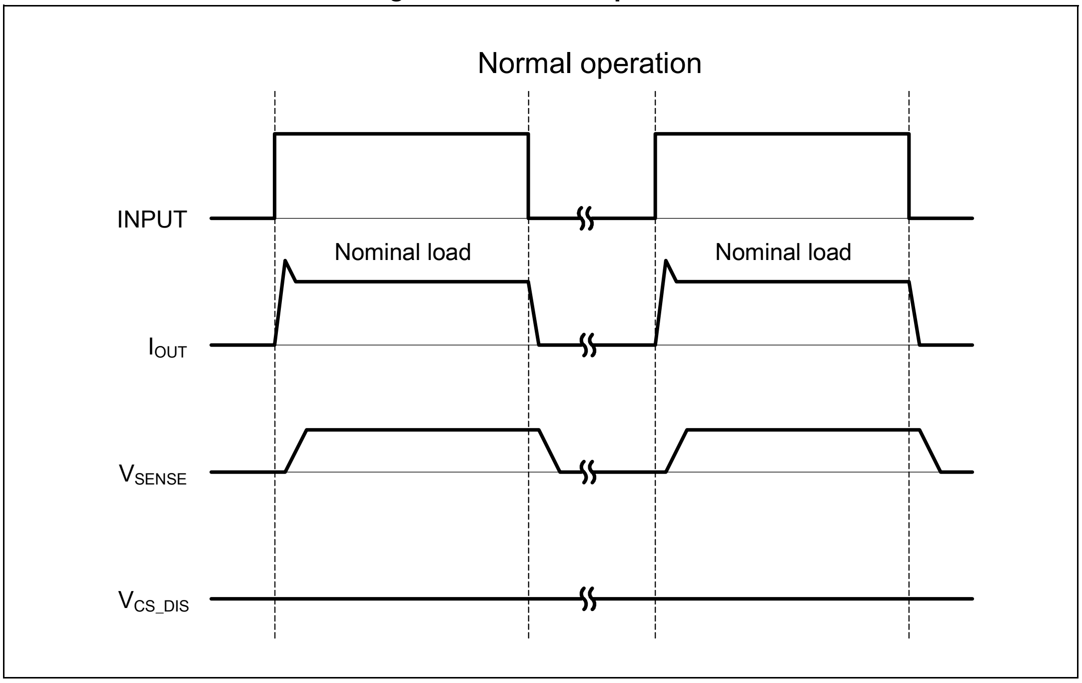


Figure 11. Overload or short to GND

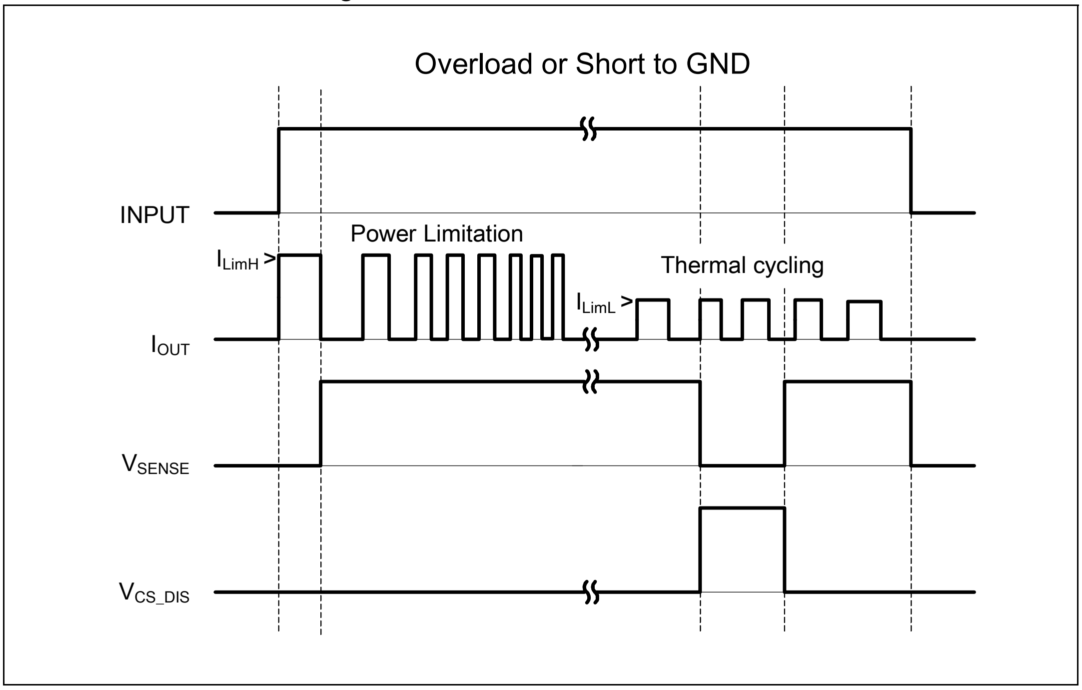


Figure 12. Intermittent overload

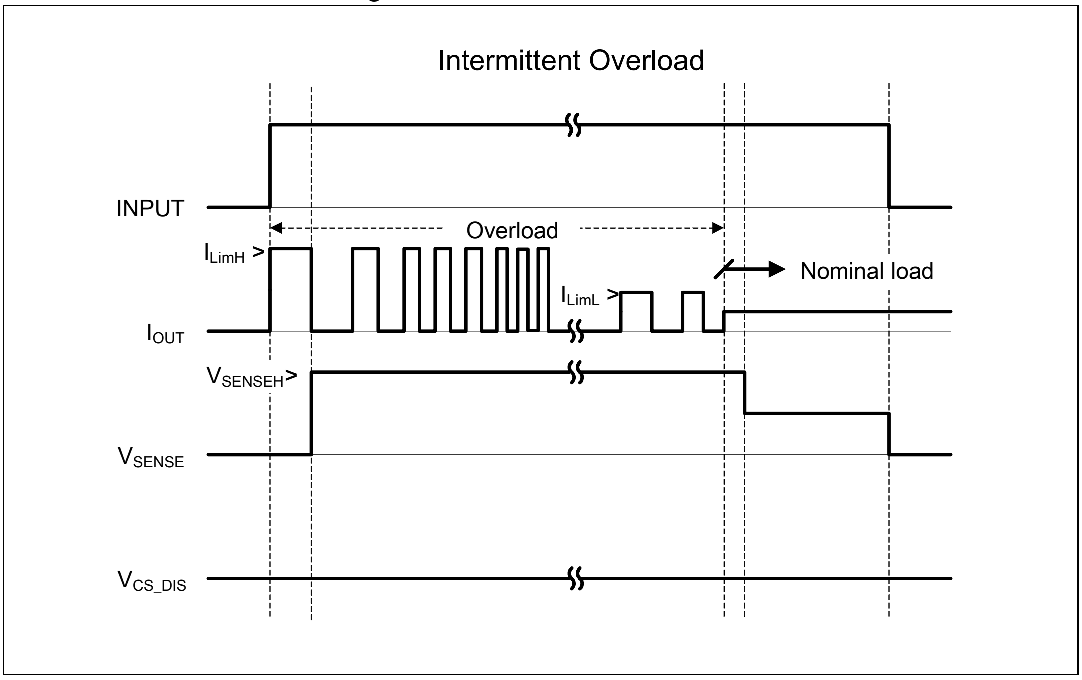
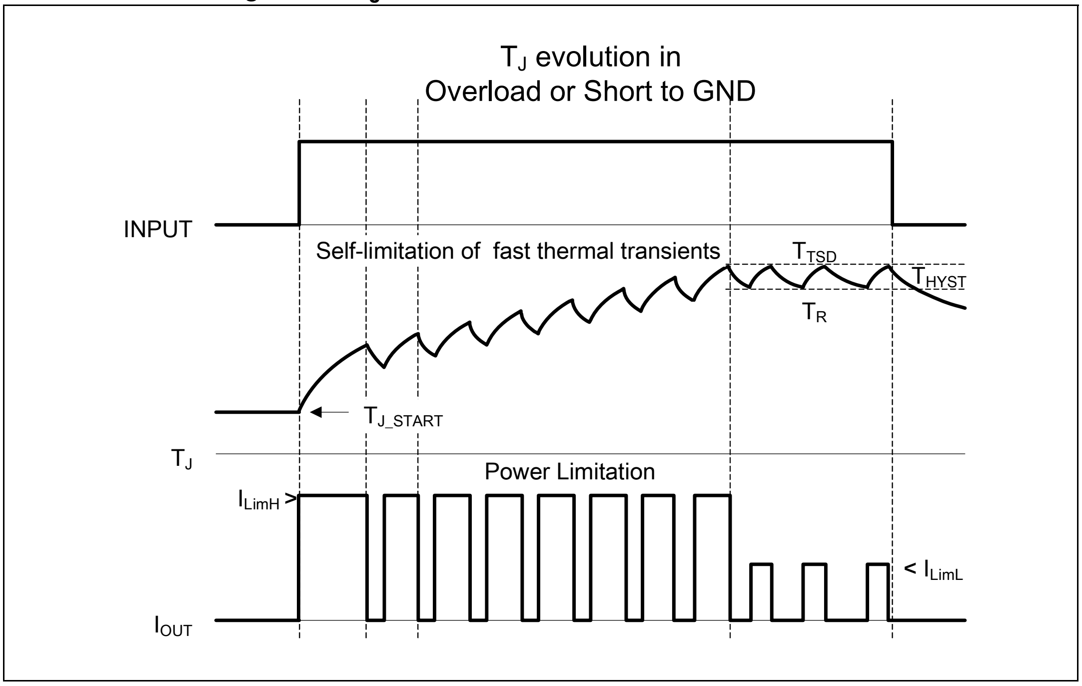


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

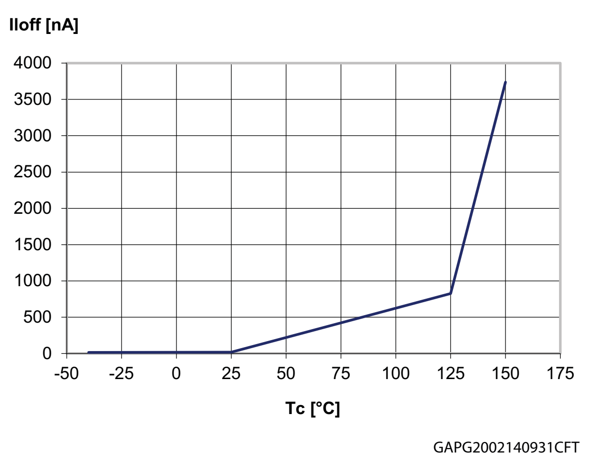


Figure 15. High level input current

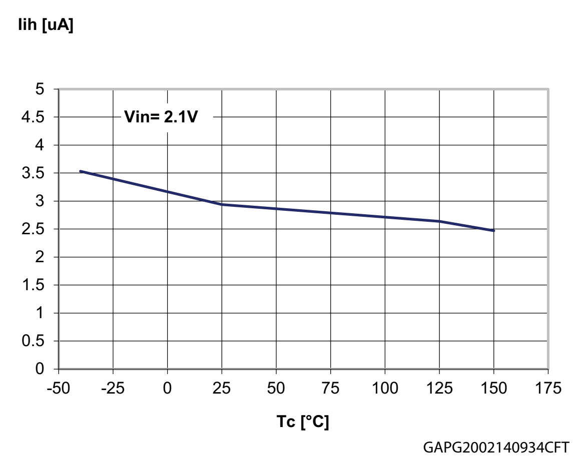


Figure 16. Input clamp level

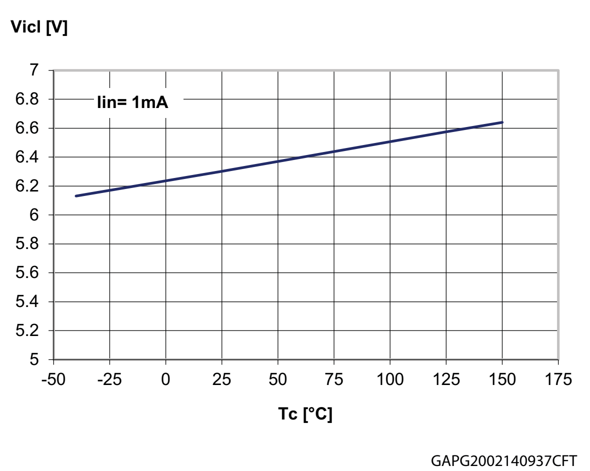


Figure 17. Input low level

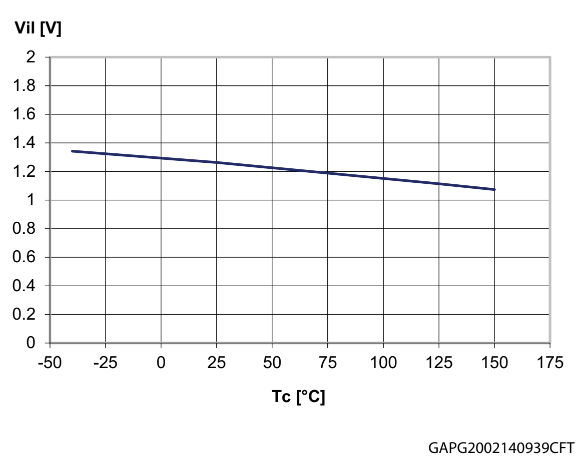


Figure 18. Input high level

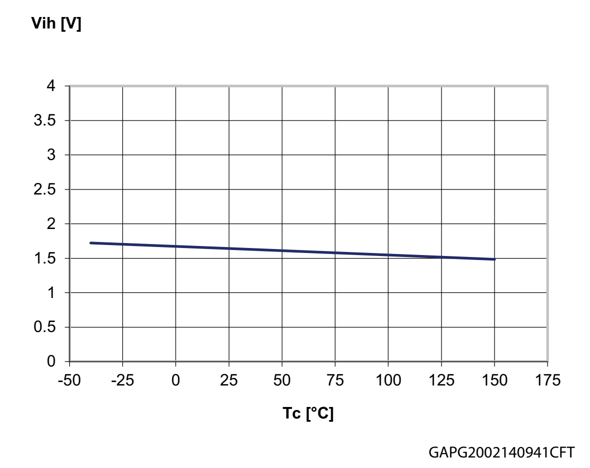


Figure 19. Input hysteresis voltage

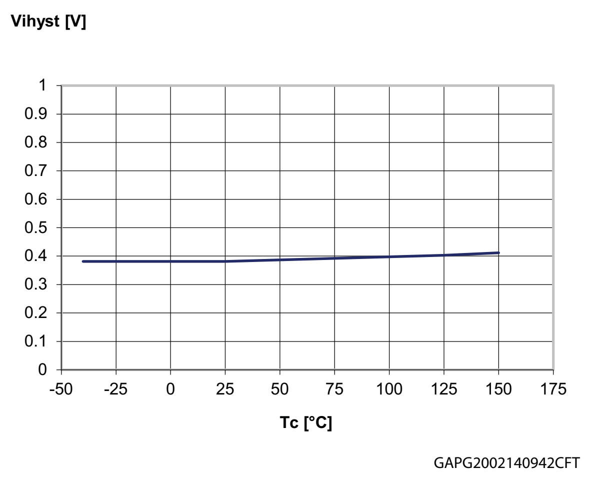


Figure 20. On-state resistance vs T_{case}

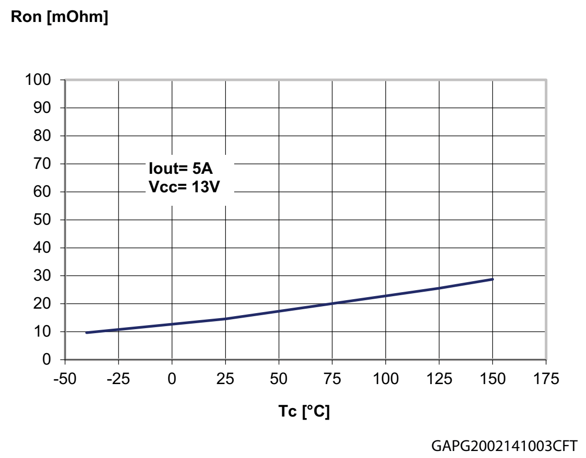


Figure 21. On-state resistance vs V_{CC}

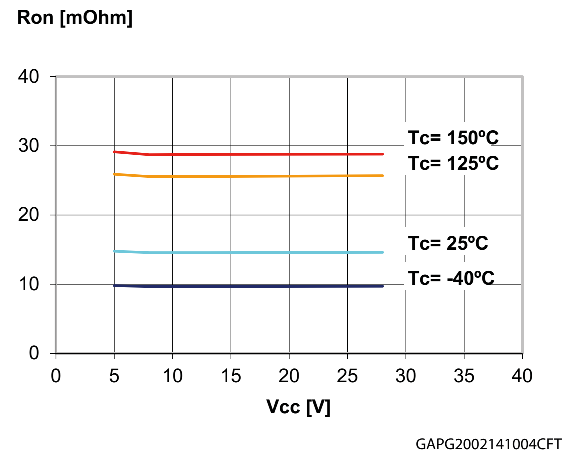


Figure 22. Undervoltage shutdown

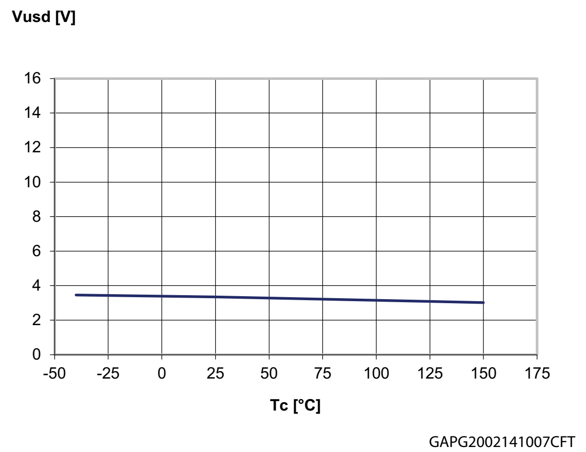


Figure 23. Turn-on voltage slope

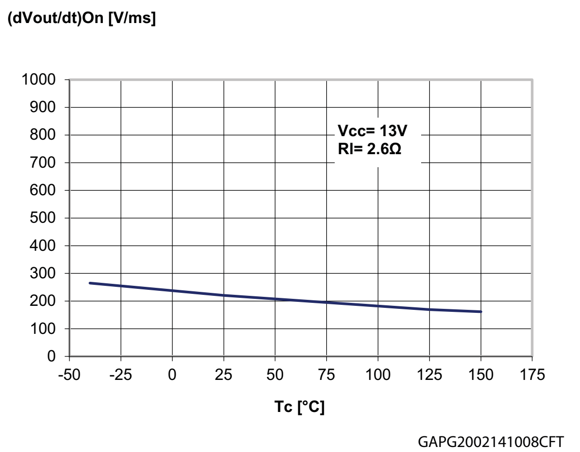


Figure 24. I_{LIMH} vs T_{case}

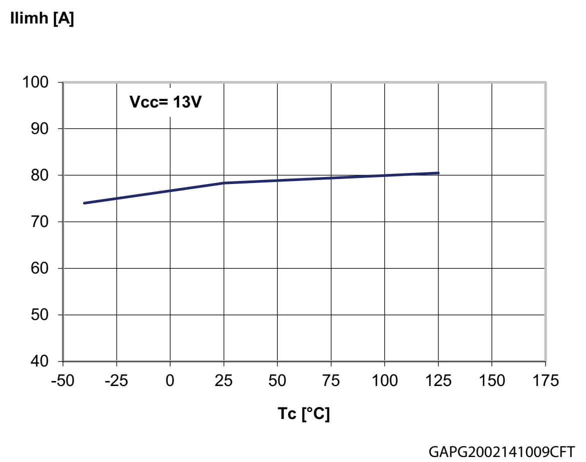


Figure 25. Turn-off voltage slope

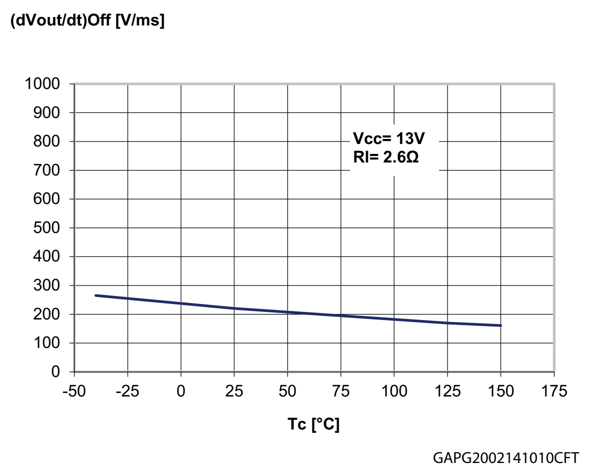


Figure 26. CS_DIS high level voltage

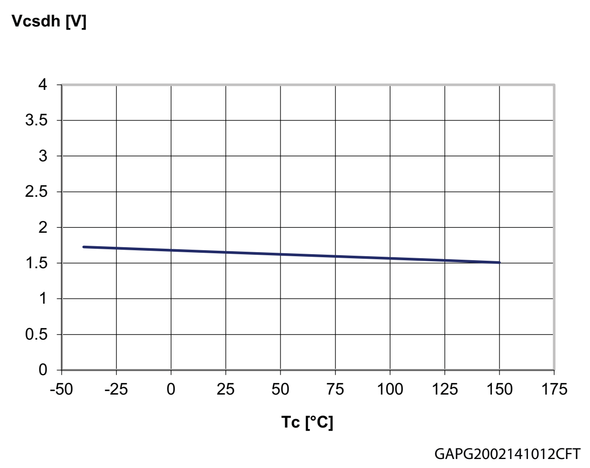


Figure 27. CS_DIS clamp voltage

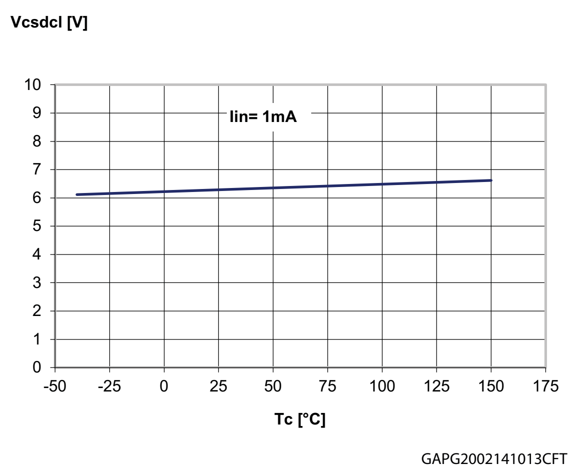
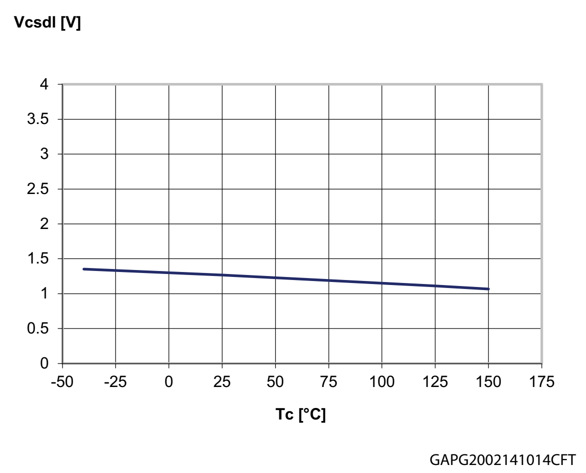
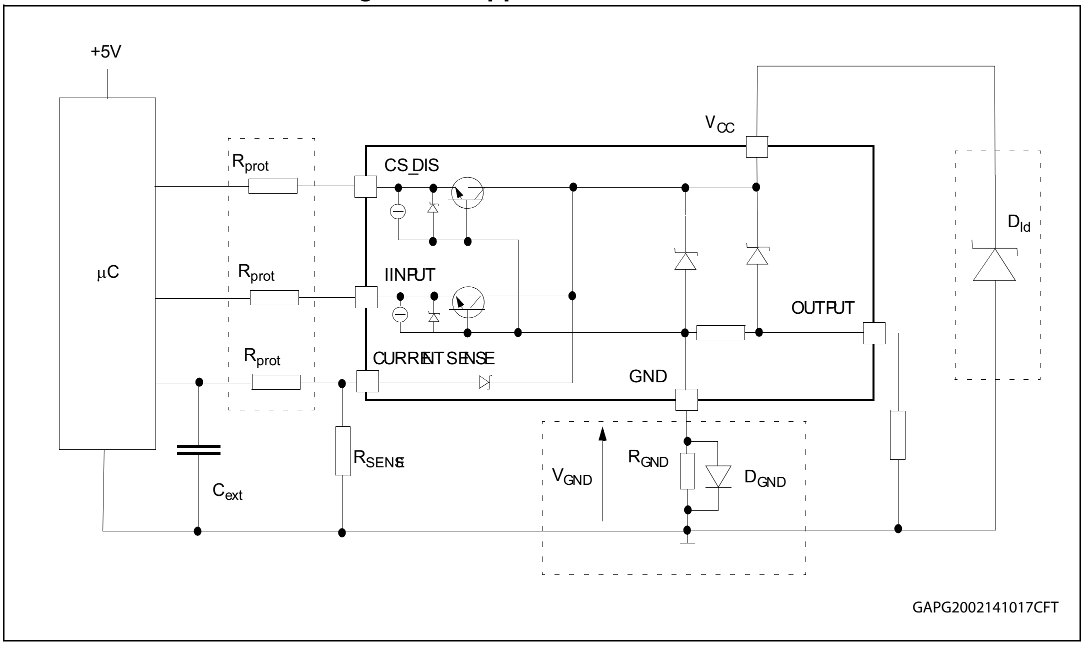


Figure 28. CS_DIS low level voltage



3 Application information

Figure 29. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to set the dimension of R_{GND} resistor.

1) $R_{GND} \leq 600\ mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2/R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

Equation 2

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended values: R_{prot} =10 kΩ, C_{EXT}=10 nF.

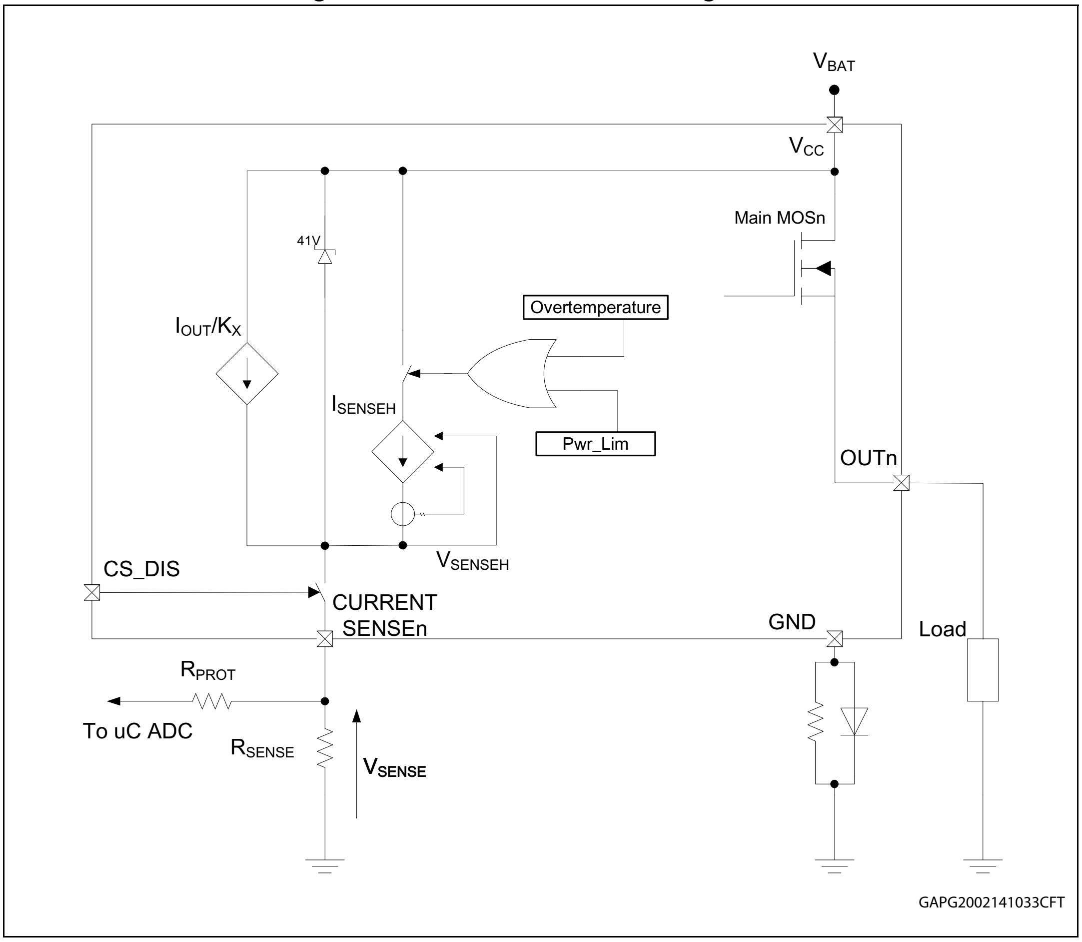
3.4 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 30: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load according to a known ratio K_X.
  The current I_{SENSE} can be easily converted into a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < VCC < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < VCC < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 10*):
  - Power limitation activation
  - Overtemperature

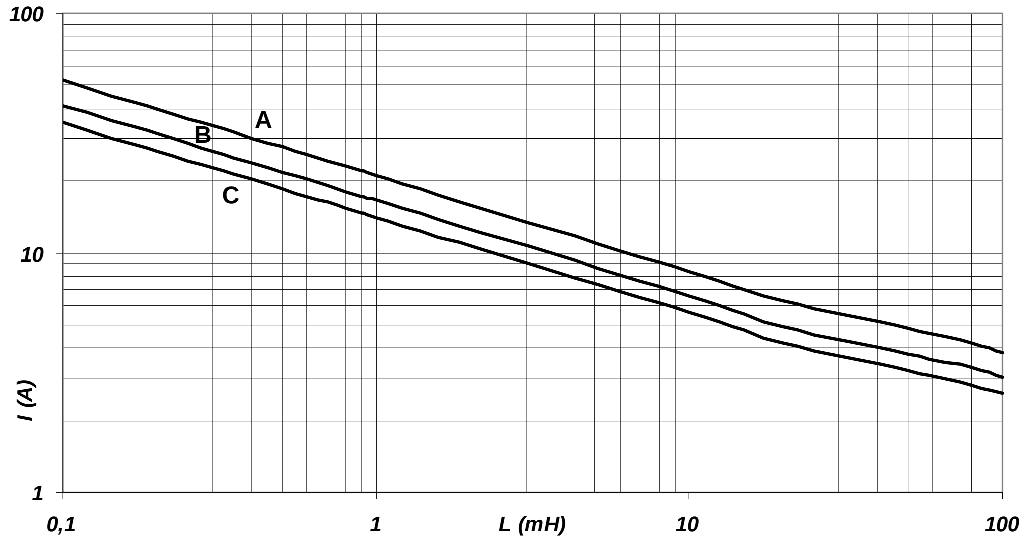
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.5 Maximum demagnetization energy (V_{CC} = 13.5 V)

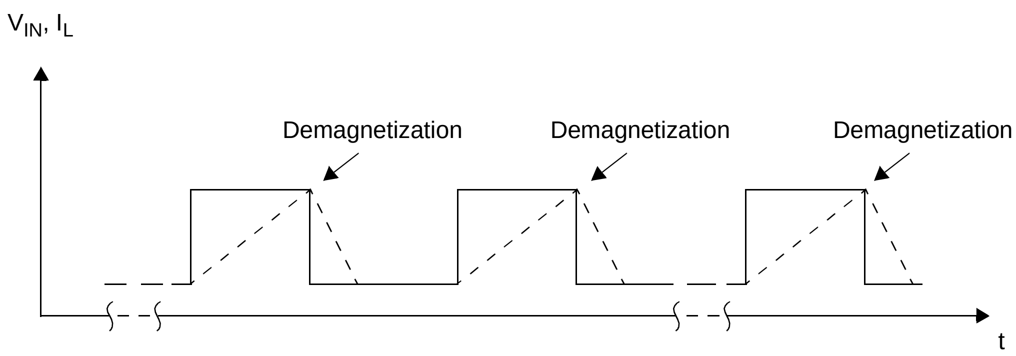
Figure 31. Maximum turn-off current versus inductance



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse

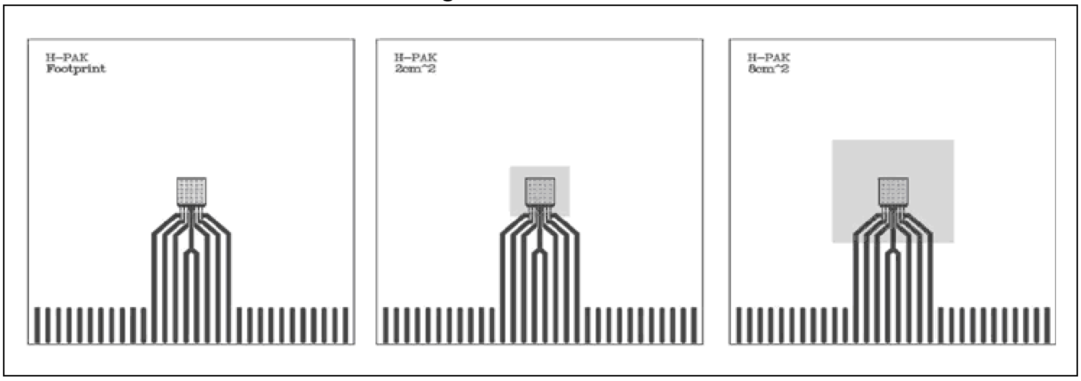


1. Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 HPak thermal data

Figure 32. PC board



1. Layout condition of Rth and Zth measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 1.8 mm, Cu thickness = 70 µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 33. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

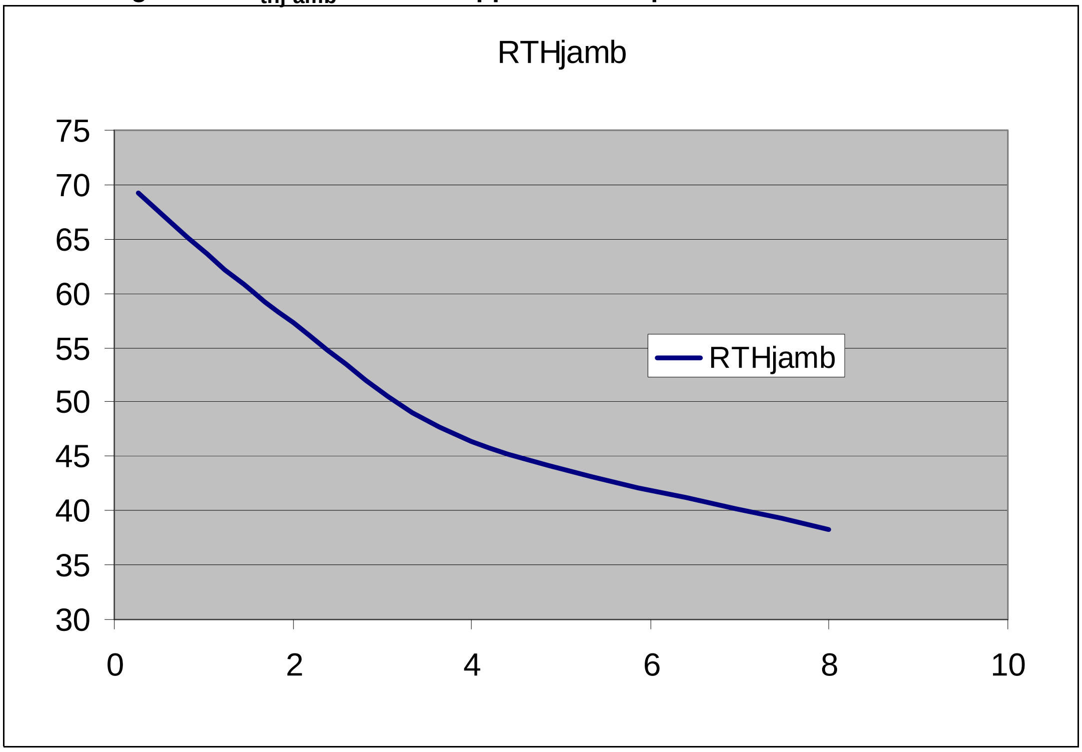
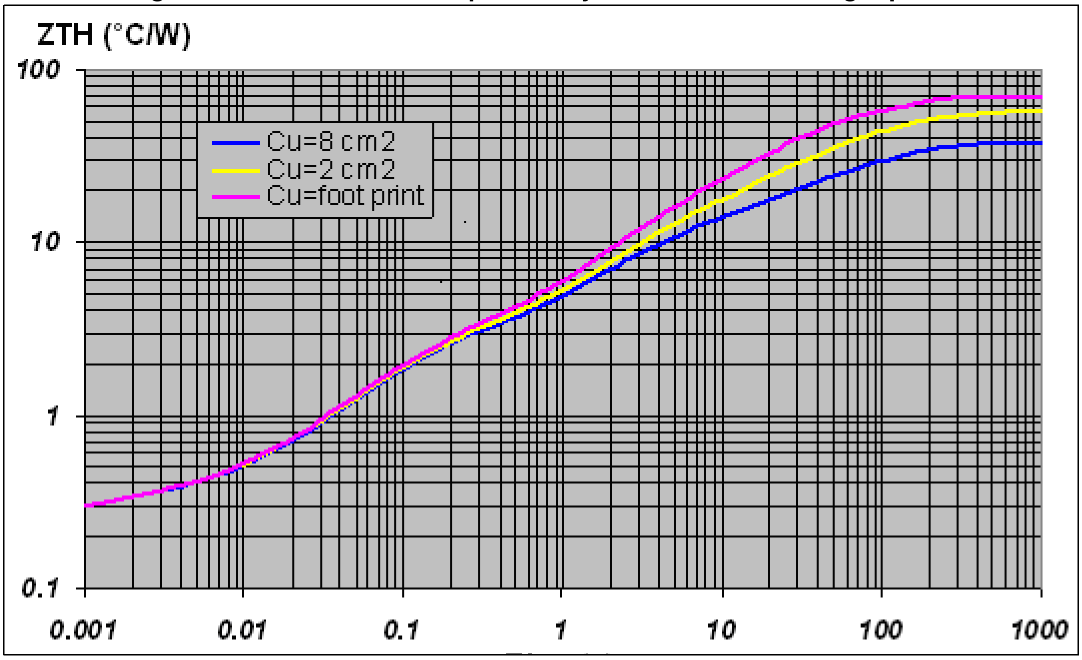


Figure 34. HPak thermal impedance junction ambient single pulse

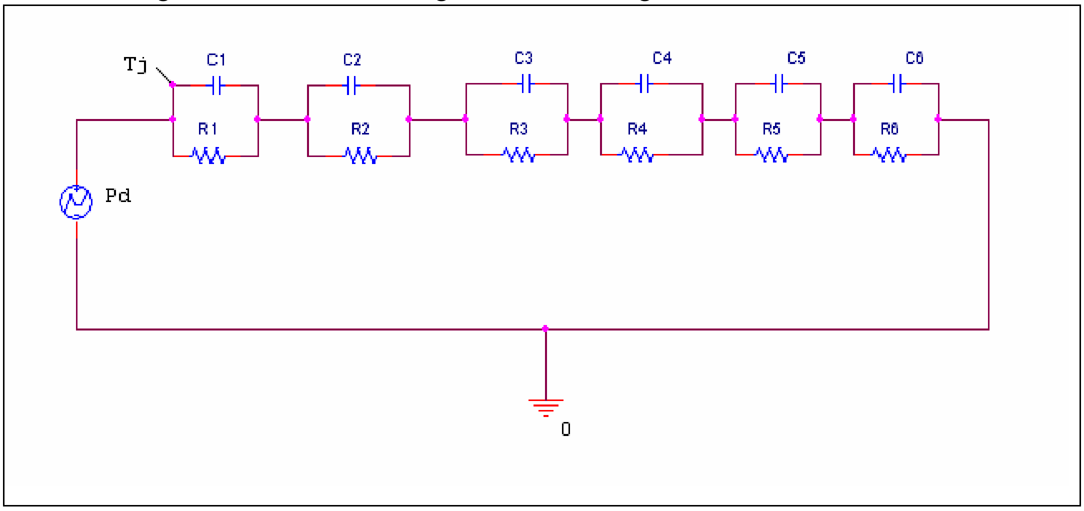


Equation 3: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 35. Thermal fitting model of a single channel HSD in HPak



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. Thermal parameter

Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	0.1	-	-
R2 (°C/W)	0.2	-	-
R3 (°C/W)	2	-	-
R4 (°C/W)	8	-	-
R5 (°C/W)	28	22	12
R6 (°C/W)	31	25	16
C1 (W.s/°C)	0.0001	-	-
C2 (W.s/°C)	0.002	-	-
C3 (W.s/°C)	0.05	-	-
C4 (W.s/°C)	0.4	-	-
C5 (W.s/°C)	0.8	1.4	3
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 HPak mechanical data

Figure 36. KPak package dimension

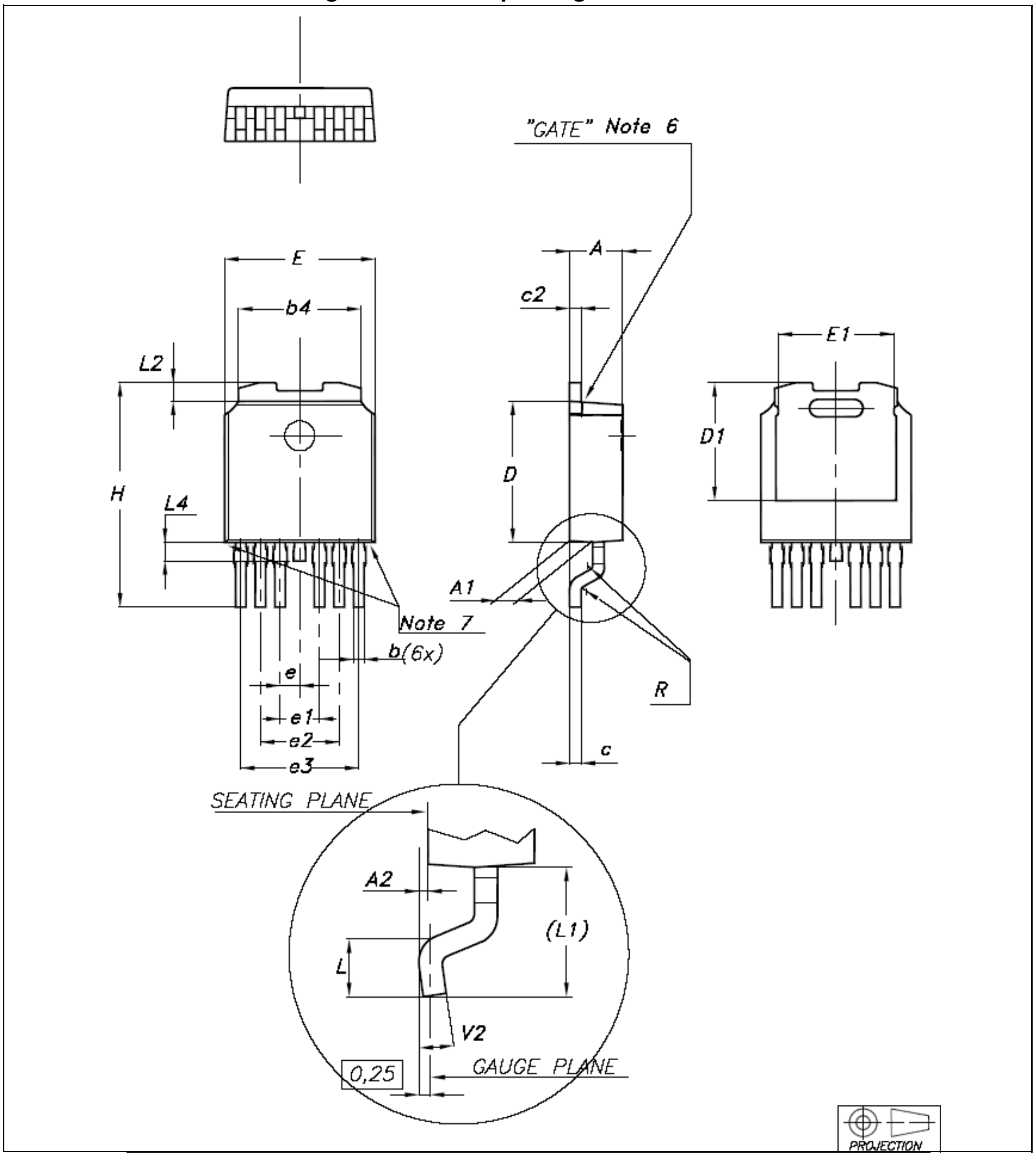


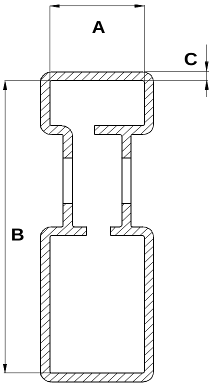
Table 15. HPak mechanical data

Ref. dim	Data book mm		
	Nom.	Min.	Max.
A		2.20	2.40
A1		0.90	1.10
A2		0.03	0.23
b		0.45	0.60
b4		5.20	5.40
c		0.45	0.60
c2		0.48	0.60
D		6.00	6.20
D1	5.10		
E		6.40	6.60
E1	5.20		
e	0.85		
e1		1.60	1.80
e2		3.30	3.50
e3		5.00	5.20
H		9.35	10.10
L		1	
(L1)	2.80		
L2	0.80		
L4		0.60	1.00
R	0.20		
V2		0°	8°

5.3 HPak packing information

The devices can be packed in tube or tape and reel shipments (see *Table 16: Device summary*).

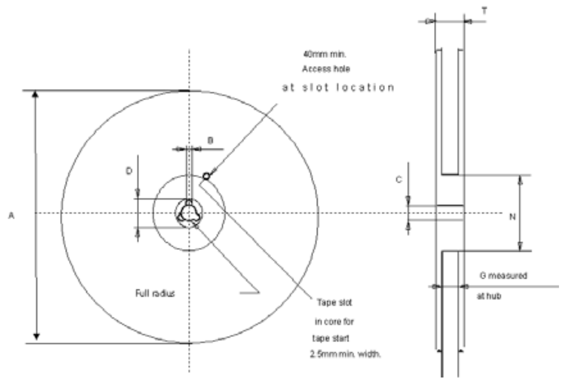
Figure 37. HPak tube shipment (no suffix)



Base q.ty	75
Bulk q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

Figure 38. HPak tape and reel (suffix "TR")



REEL DIMENSIONS

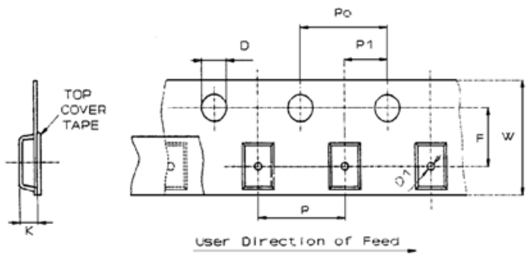
All dimensions are in mm.

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

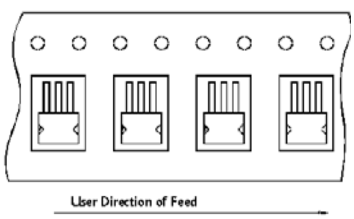
TAPE DIMENSIONS

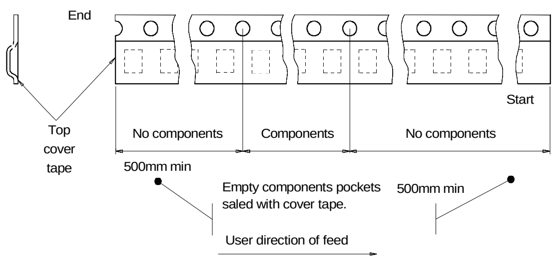
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (+ 0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	7.5
Compartment depth	**K (max)**	2.75
Hole spacing	**P1 (± 0.1)**	2



All dimensions are in mm.





6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
7 pins H-pack	Root part number 1	VN5E016MHTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
29-Jun-2010	1	Initial release.
30-Jun-2010	2	Changed status from target specification to preliminary data.
29-Jul-2010	3	*Table 9: Current sense (8 V < VCC < 18 V)*: – Updated K1 maximun value for T_j = 25 °C...150 °C
04-Aug-2010	4	*Table 9: Current sense (8 V < VCC < 18 V)*: – Updated K1, K2 and K3 typical values for T_j = -40 °C...150 °C – Updated dK_1/K_1 test conditions Updated *Figure 8: IOUT/ISENSE vs IOUT*.
19-Feb-2014	5	Changed document status from “Preliminary data” to “Production data”
07-May-2014	6	Updated *Figure 2: Configuration diagram (top view) not in scale*