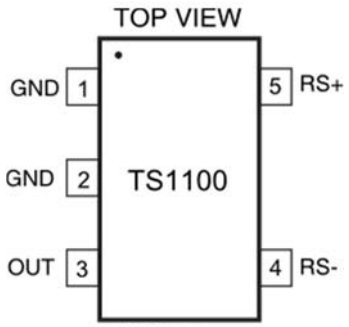
ABSOLUTE MAXIMUM RATINGS

RS+, RS- to GND .....-0.3V to +27V
OUT to GND.....-0.3V to +6V
RS+ to RS-..... ±28V
Short-Circuit Duration: OUT to GND ..... Continuous
Continuous Input Current (Any Pin) ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (Derate at 3.9mW/°C above +70°C).. 312mW

Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C
Soldering Temperature (Reflow) ..... +260°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



SOT23-5
G5 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS1100-25EG5	TADJ	Tape & Reel	-----
TS1100-25EG5T		Tape & Reel	3000
TS1100-50EG5	TADK	Tape & Reel	-----
TS1100-50EG5T		Tape & Reel	3000
TS1100-100EG5	TADL	Tape & Reel	-----
TS1100-100EG5T		Tape & Reel	3000
TS1100-200EG5	TADM	Tape & Reel	-----
TS1100-200EG5T		Tape & Reel	3000

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{RS+} = V_{RS-} = 3.6V; V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V; C_{OUT} = 47nF; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See Note 1

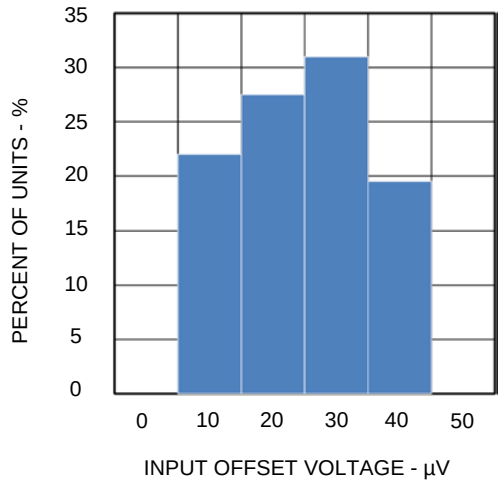
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (Note 2)	I_{CC}	T_A = +25°C			0.68	0.85	µA
						1.0	
		V_{RS+} = 25V	T_A = +25°C			1.0	
						1.2	
Common-Mode Input Range	V_{CM}	Guaranteed by CMRR		2		27	V
Common-Mode Rejection Ratio	CMRR	2V < V_{RS+} < 27V		120	150		dB
Input Offset Voltage (Note 3)	V_{OS}	T_A = +25°C			±30	±100	µV
						±200	
Gain	G	TS1100-25			25		V/V
		TS1100-50			50		
		TS1100-100			100		
		TS1100-200			200		
Gain Error (Note 4)	GE	T_A = +25°C			±0.1	±0.5	%
						±0.6	
Output Resistance (Note 5)	R_{OUT}		TS1100-25/50/100	7.0	10	13.2	kΩ
			TS1100-200	14.0	20	26.4	
OUT Low Voltage	V_{OL}	Gain = 25				5	mV
		Gain = 50				10	
		Gain = 100				20	
		Gain = 200				40	
OUT High Voltage (Note 6)	V_{OH}	V_{OH} = V_{RS-} - V_{OUT}			0.05	0.2	V
Output Settling Time	t_S	TS1100-25/50/100	1% final value, V_{SENSE} = 50mV		2.2		ms
		TS1100-200			4.3		ms

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by product characterization.
Note 2: Extrapolated to V_{OUT} = 0. I_{CC} is the total current into the RS+ and the RS- pins.
Note 3: Input offset voltage V_{OS} is extrapolated from V_{OUT} with V_{SENSE} set to 1mV.
Note 4: Gain error is calculated by applying two values for V_{SENSE} and then calculating the error of the actual slope vs. the ideal transfer characteristic:
For GAIN = 25, the applied V_{SENSE} is 20mV and 120mV.
For GAIN = 50, the applied V_{SENSE} is 10mV and 60mV.
For GAIN = 100, the applied V_{SENSE} is 5mV and 30mV.
For GAIN = 200, the applied V_{SENSE} is 2.5mV and 15mV.
Note 5: The device is stable for any capacitive load at V_{OUT}.
Note 6: V_{OH} is the voltage from V_{RS-} to V_{OUT} with V_{SENSE} = 3.6V/GAIN.

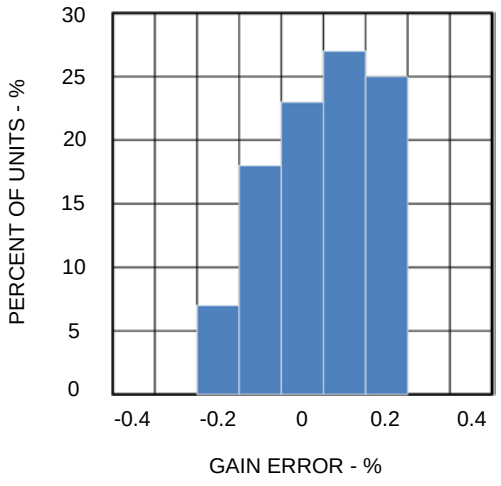
TYPICAL PERFORMANCE CHARACTERISTICS

V_{RS+} = V_{RS-} = 3.6V; T_A = +25°C, unless otherwise noted.

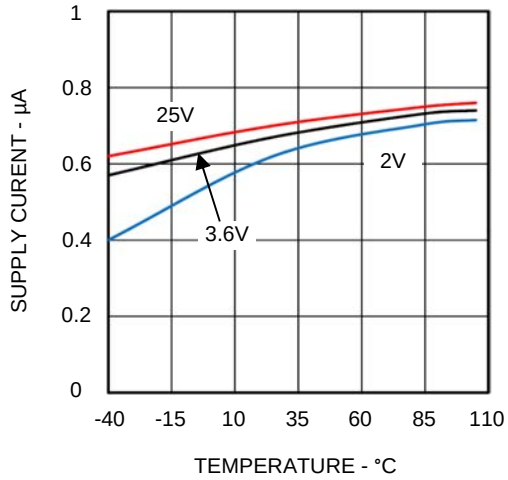
Input Offset Voltage Histogram



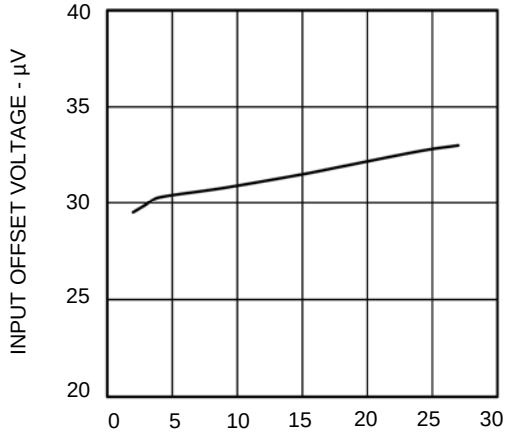
Gain Error Histogram



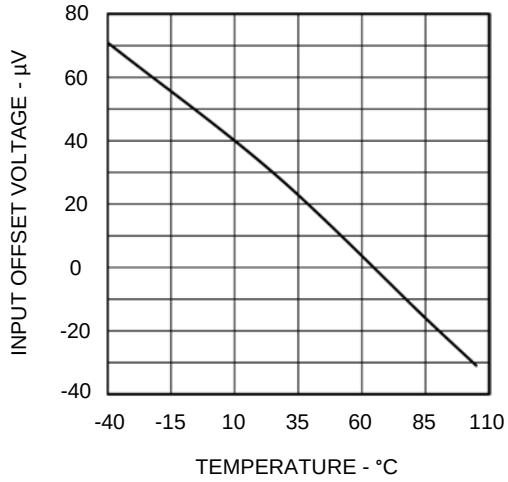
Supply Current vs Temperature



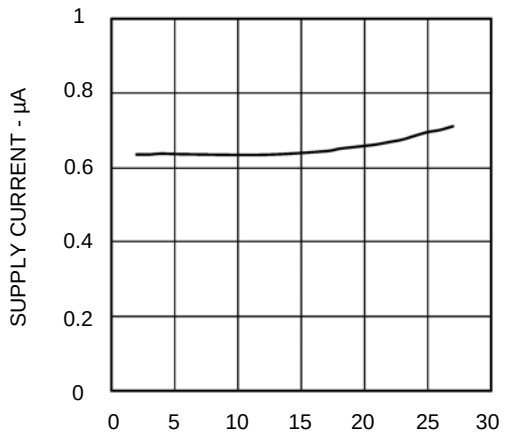
Input Offset Voltage vs Common-Mode Voltage



Input Offset Voltage vs Temperature



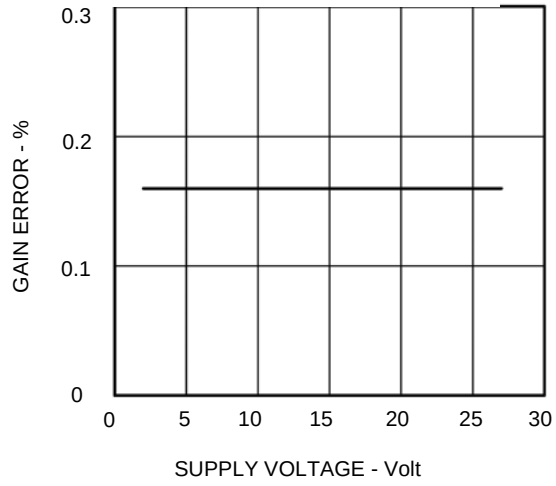
Supply Current vs Common-Mode Voltage



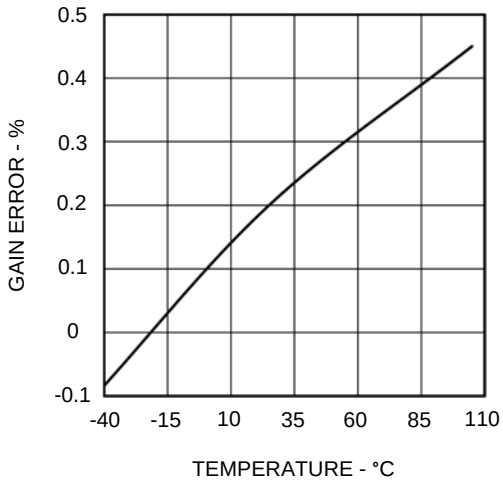
TYPICAL PERFORMANCE CHARACTERISTICS

V_{RS+} = V_{RS-} = 3.6V; T_A = +25°C, unless otherwise noted.

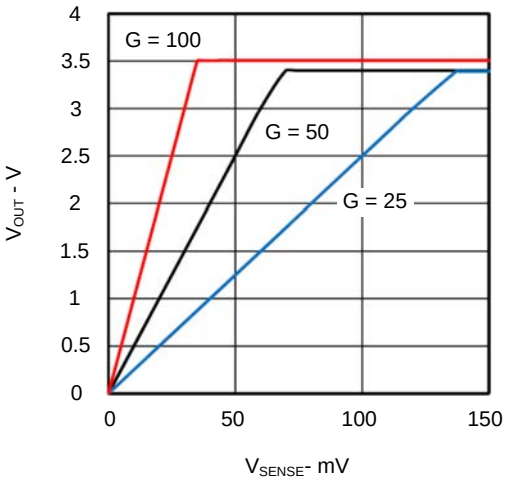
Gain Error vs Common-Mode Voltage



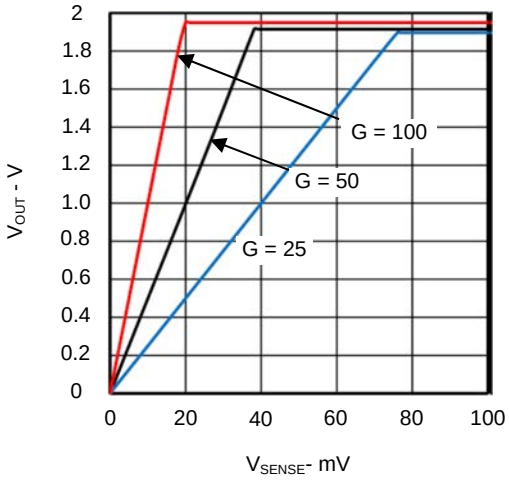
Gain Error vs. Temperature



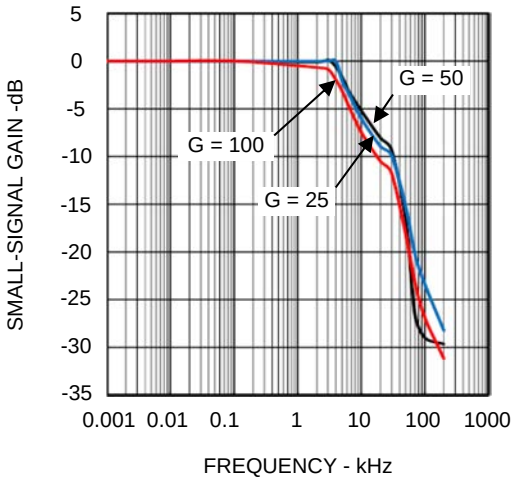
V_{OUT} vs V_{SENSE} @ Supply = 3.6V



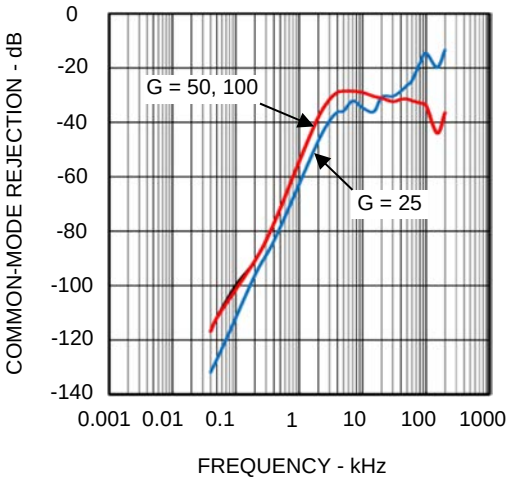
V_{OUT} vs V_{SENSE} @ Supply = 2V



Small-Signal Gain vs Frequency



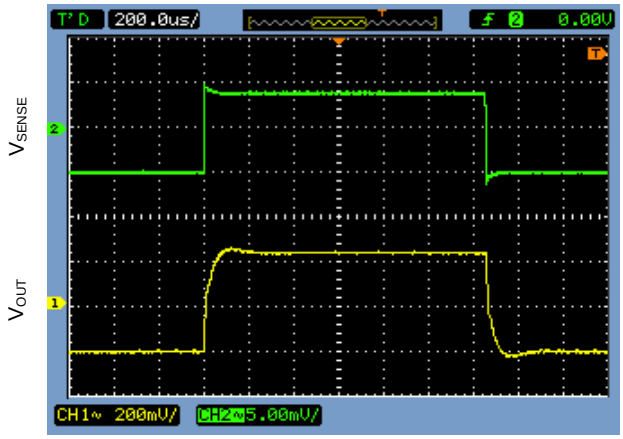
Common-Mode Rejection vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

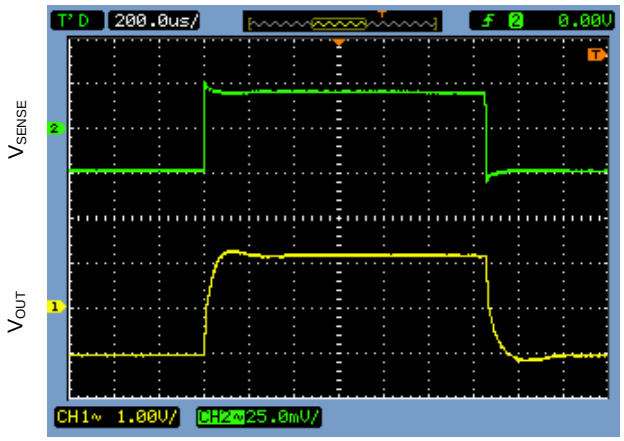
V_{RS+} = V_{RS-} = 3.6V; T_A = +25°C, unless otherwise noted.

Small-Signal Pulse Response, Gain = 50



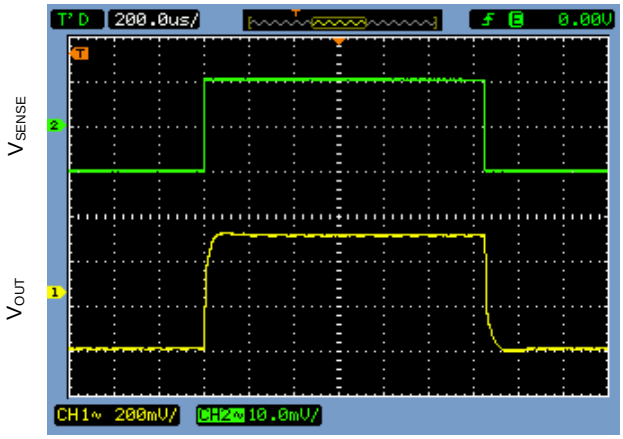
200µs/DIV

Large-Signal Pulse Response, Gain = 50



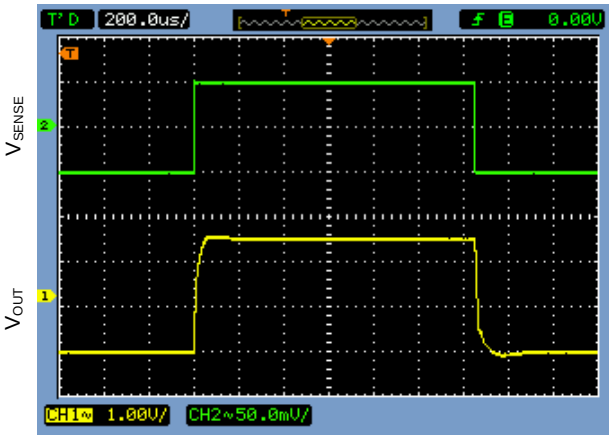
200µs/DIV

Small-Signal Pulse Response, Gain = 25



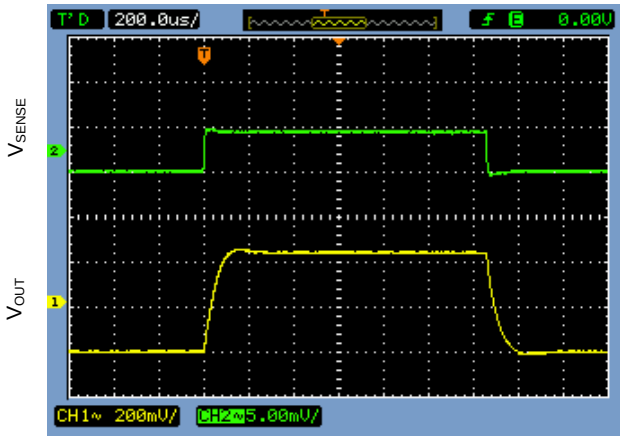
200µs/DIV

Large-Signal Pulse Response, Gain = 25



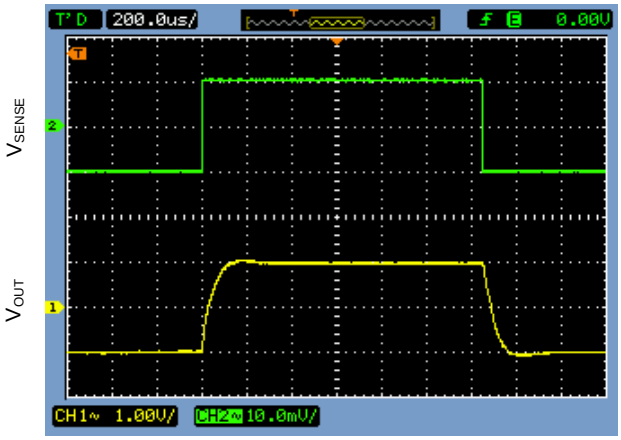
200µs/DIV

Small-Signal Pulse Response, Gain = 100



200µs/DIV

Large-Signal Pulse Response, Gain = 100

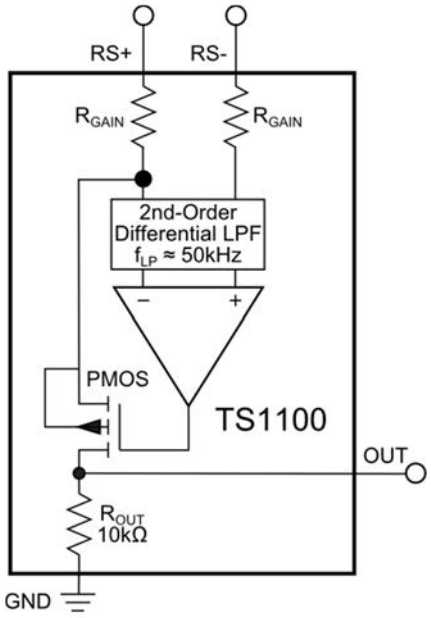


200µs/DIV

PIN FUNCTIONS

PIN SOT23	LABEL	FUNCTION
5	RS+	External Sense Resistor Power-Side Connection
4	RS-	External Sense Resistor Load-Side Connection
1, 2	GND	Ground. Connect these pins to analog ground.
3	OUT	Output Voltage. V_{OUT} is proportional to $V_{SENSE} = V_{RS+} - V_{RS-}$

BLOCK DIAGRAM



DESCRIPTION OF OPERATION

The internal configuration of the TS1100 – a unidirectional high-side, current-sense amplifier - is based on a commonly-used operational amplifier (op amp) circuit for measuring load currents (in one direction) in the presence of high-common-mode voltages. In the general case, a current-sense amplifier monitors the voltage caused by a load current through an external sense resistor and generates an output voltage as a function of that load current. Referring to the typical application circuit on Page 1, the inputs of the op-amp-based circuit are connected across an external RSENSE resistor that is used to measure load current. At the non-inverting input of the TS1100 (the RS+ terminal), the applied voltage is I_{LOAD} x RSENSE. Since the RS- terminal is the non-inverting input of the internal op amp, op-amp feedback action forces the inverting input of the internal op amp to the same potential (I_{LOAD} x RSENSE). Therefore, the voltage drop across RSENSE (V_{SENSE}) and the voltage drop across R_{GAIN} (at the RS+ terminal) are equal. To minimize any additional error because of op-amp input bias current mismatch, both R_{GAIN}s are the same value.

Since the internal p-channel FET's source is connected to the inverting input of the internal op amp and since the voltage drop across R_{GAIN} is the same as the external V_{SENSE}, op amp feedback action drives the gate of the FET such that the FET's drain-source current is equal to:

$$I_{DS} = \frac{V_{SENSE}}{R_{GAIN}}$$

or

$$I_{DS} = \frac{I_{LOAD} \times R_{SENSE}}{R_{GAIN}}$$

Since the FET's drain terminal is connected to R_{OUT}, the output voltage of the TS1100 at the OUT terminal is, therefore;

$$V_{OUT} = I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAIN}}$$

The current-sense amplifier's gain accuracy is therefore the ratio match of R_{OUT} to R_{GAIN}. For each of the four gain options available, Table 1 lists the values for R_{OUT} and R_{GAIN}. The TS1100's output stage is protected against input overdrive by use of an output current-limiting circuit of 3mA (typical) and a 7V internal clamp protection circuit.

Table 1: Internal Gain Setting Resistors (Typical Values)

GAIN (V/V)	R_{GAIN} (Ω)	R_{OUT} (Ω)	Part Number
25	400	10k	TS1100-25
50	200	10k	TS1100-50
100	100	10k	TS1100-100
200	100	20k	TS1100-200

To achieve its very-low input offset voltage performance over temperature, VSENSE voltage, and power supply voltage, the design of the TS1100's amplifier is chopper-stabilized, a commonly-used technique to reduce significantly the input offset voltage of amplifiers. This method, however, does employ the use of sampling techniques and therefore residue of the TS1100's 10kHz internal clock is contained in the TS1100's output voltage spectrum.

APPLICATIONS INFORMATION

Choosing the Sense Resistor

Selecting the optimal value for the external RSENSE is based on the following criteria and for each commentary follows:

1) RSENSE Voltage Loss
2) V_{OUT} Swing vs. Applied Input Voltage at V_{RS+} and Desired V_{SENSE}
3) Total I_{LOAD} Accuracy
4) Circuit Efficiency and Power Dissipation
5) RSENSE Kelvin Connections
6) Sense Resistor Composition

1) RSENSE Voltage Loss

For lowest IR voltage loss in RSENSE, the smallest usable value for RSENSE should be selected.

2) V_{OUT} Swing vs. Applied Input Voltage at V_{RS+} and Desired V_{SENSE}

As there is no separate power supply pin for the TS1100, the circuit draws its power from the applied voltage at both its RS+ and RS- terminals. Therefore, the signal voltage at the OUT terminal is bounded by the minimum supply voltage applied to the TS1100.

Therefore,

$$V_{OUT(max)} = V_{RS+(min)} - V_{SENSE(max)} - V_{OH(max)}$$

and

$$R_{SENSE} = \frac{V_{OUT}(max)}{GAIN \times I_{LOAD}(max)}$$

where the full-scale V_{SENSE} should be less than $V_{OUT(MAX)}$/GAIN at the application's minimum RS+ terminal voltage. For best performance with a 3.6V power supply, RSENSE should be chosen to generate a V_{SENSE} of: a) 120mV (for the 25V/V GAIN option), b) 60mV (for the 50V/V GAIN option), c) 30mV (for the 100V/V GAIN option), or d) 15mV (for the 200V/V GAIN option) at the full-scale $I_{LOAD(MAX)}$ current in each application. For the case where the minimum power supply voltage is higher than 3.6V, each of the four full-scale V_{SENSE}s above can be increased.

3) Total I_{LOAD} Accuracy

In the TS1100's linear region where $V_{OUT} < V_{OUT(MAX)}$, there are two specifications related to the circuit's accuracy: a) the TS1100's input offset voltage (V_{OS} = 100µV, max) and b) its gain error (GE(max) = 0.5%).

An expression for the TS1100's total output voltage (+ error) is given by:

$$V_{OUT} = [GAIN \times (1 \pm GE) \times V_{SENSE}] \pm (GAIN \times V_{OS})$$

A large value for RSENSE permits the use of smaller load currents to be measured more accurately because the effects of offset voltages are less significant when compared to larger VSENSE voltages. Due care though should be exercised as previously mentioned with large values of RSENSE.

4) Circuit Efficiency and Power Dissipation

IR losses in RSENSE can be large especially at high load currents. It is important to select the smallest, usable RSENSE value to minimize power dissipation and to keep the physical size of RSENSE small. If the external RSENSE is allowed to dissipate significant power, then its inherent temperature coefficient may alter its design center value, thereby reducing load current measurement accuracy. Precisely because the TS1100's input stage was designed to exhibit a very low input offset voltage, small RSENSE values can be used to reduce power dissipation and minimize local hot spots on the pcb.

5) RSENSE Kelvin Connections

For optimal V_{SENSE} accuracy in the presence of large load currents, parasitic pcb track resistance should be minimized. Kelvin-sense pcb connections

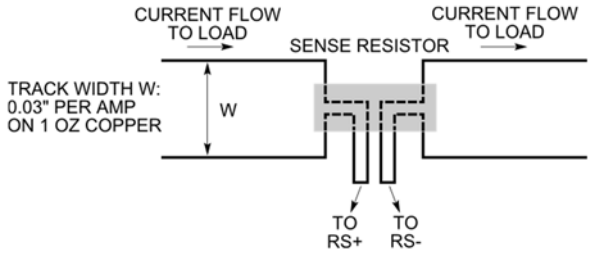


Figure 1: Making PCB Connections to the Sense Resistor.

between RSENSE and the TS1100's RS+ and RS- terminals are strongly recommended. The drawing in Figure 1 illustrates the connections between the current-sense amplifier and the current-sense resistor. The pcb layout should be balanced and symmetrical to minimize wiring-induced errors. In addition, the pcb layout for RSENSE should include good thermal management techniques for optimal RSENSE power dissipation.

6) RSENSE Composition

Current-shunt resistors are made available in metal film, metal strip, and wire-wound constructions. Wire-wound current-shunt resistors are constructed with wire spirally wound onto a core. As a result, these types of current shunt resistors exhibit the largest self inductance. In applications where the load current contains high-frequency transients, metal film or metal strip current sense resistors are recommended.

Internal Noise Filter

In power management and motor control applications, current-sense amplifiers are required to measure load currents accurately in the presence of both externally-generated differential and common-mode noise. An example of differential-mode noise that can appear at the inputs of a current-sense amplifier is high-frequency ripple. High-frequency ripple – whether injected into the circuit inductively or capacitively - can produce a differential-mode voltage drop across the external current-shunt resistor (RSENSE). An example of externally-generated, common-mode noise is the high-frequency output ripple of a switching regulator that can result in common-mode noise injection into both inputs of a current-sense amplifier.

Even though the load current signal bandwidth is DC, the input stage of any current-sense amplifier can rectify unwanted, out-of-band noise that can result in an apparent error voltage at its output. This rectification of noise signals occurs because all amplifier input stages are constructed with transistors that can behave as high-frequency signal detectors in the same way pn-junction diodes were used as RF envelope detectors in early radio designs. Against common-mode injected noise, the amplifier's internal common-mode rejection is usually sufficient.

To counter the effects of externally-injected noise, it has always been good engineering practice to add external low-pass filters in series with the inputs of a current-sense amplifier. In the design of discrete current-sense amplifiers, resistors used in the external low-pass filters were incorporated into the circuit's overall design so errors because of any input-bias current-generated offset voltage errors and gain errors were compensated.

With the advent of monolithic current-sense amplifiers, like the TS1100, the addition of external

low-pass filters in series with the current-sense amplifier's inputs only introduces additional offset voltage and gain errors. To minimize or eliminate altogether the need for external low-pass filters and to maintain low input offset voltage and gain errors, the TS1100 incorporates a 50-kHz (typ), 2nd-order differential low-pass filter as shown in the TS1100's Block Diagram.

Optional Output Filter Capacitor

If the TS1100 is part of a signal acquisition system where its OUT terminal is connected to the input of an ADC with an internal, switched-capacitor track-and-hold circuit, the internal track-and-hold's sampling capacitor can cause voltage droop at V_{OUT}. A 22nF to 100nF good-quality ceramic capacitor from the OUT terminal to GND forms a low-pass filters with the TS1100's R_{OUT} and should be used to minimize voltage droop (holding V_{OUT} constant during the sample interval. Using a capacitor on the OUT terminal will also reduce the TS1100's small-signal bandwidth as well as band-limiting amplifier noise.

PC Board Layout and Power-Supply Bypassing

For optimal circuit performance, the TS1100 should be in very close proximity to the external current-sense resistor and the pcb tracks from RSENSE to the RS+ and the RS- input terminals of the TS1100 should be short and symmetric. Also recommended are a ground plane and surface mount resistors and capacitors.

Using the TS1100 in Bidirectional Load Current Applications

In many battery-powered systems, it is oftentimes necessary to monitor a battery's discharge and charge currents. To perform this function, a bidirectional current-sense amplifier is required. The circuit illustrated in Figure 2 shows how two TS1100s can be configured as a bidirectional current-sense amplifier. As shown in the figure, the RS+/RS- input pair of TS1100 #2 is wired opposite in polarity with respect to the RS+/RS- connections of TS1100 #1. Current-sense amplifier #1 therefore measures the discharge current and current-sense amplifier #2 measures the charge current. Note that both output voltages are measured with respect to GND. When the discharge current is being measured, V_{OUT1} is active and V_{OUT2} is zero; for the case where charge current is being measured, V_{OUT1} is zero, and V_{OUT2} is active.

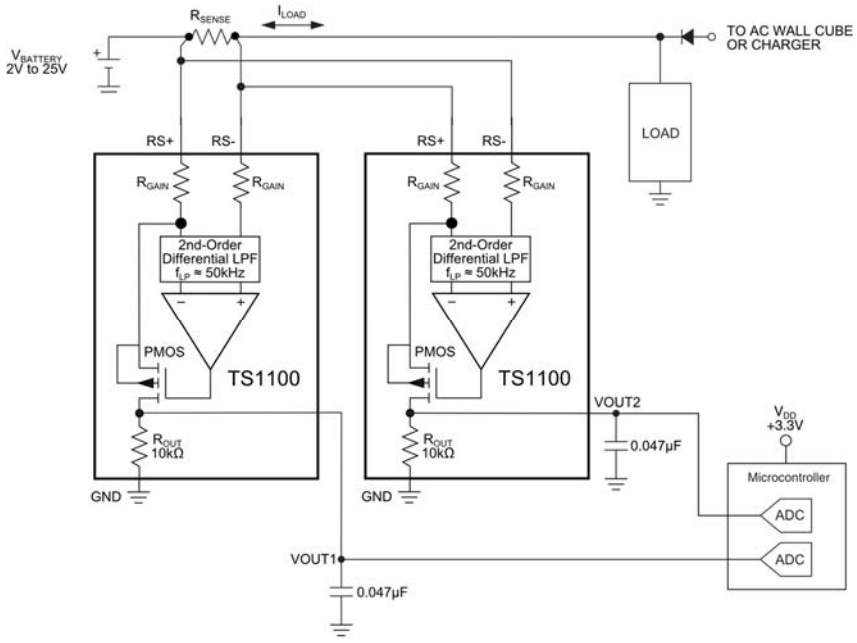
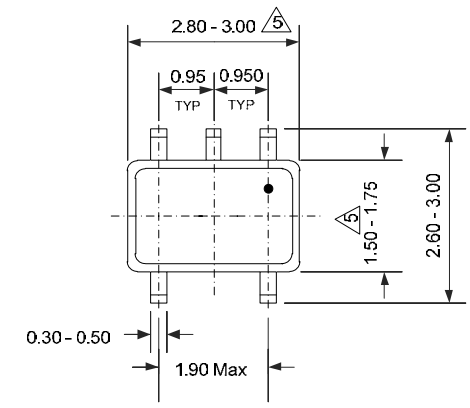


Figure 2: Using Two TS1100s for Bidirectional Load Current Detection

PACKAGE OUTLINE DRAWING

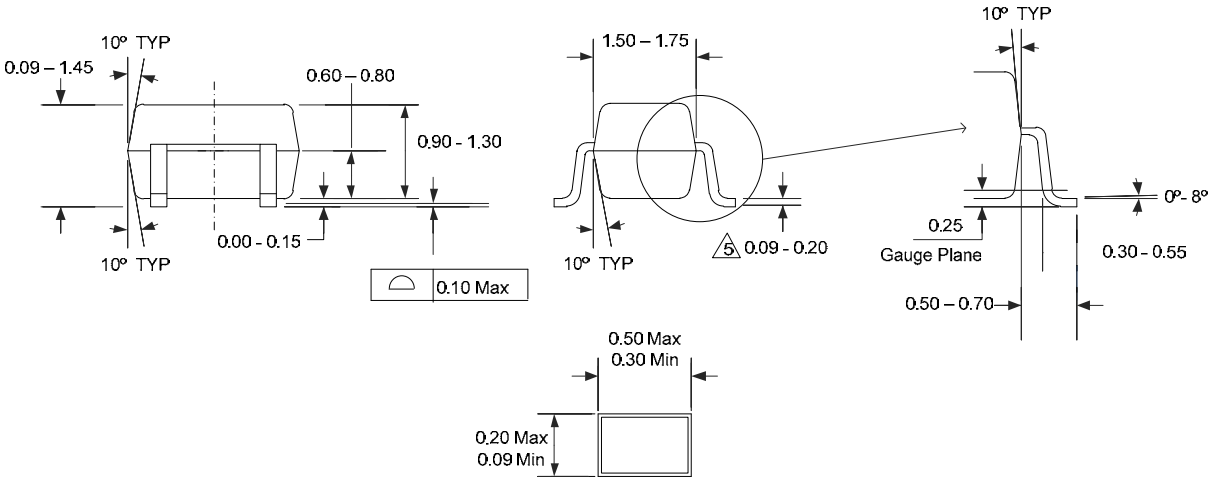
5-Pin SOT23 Package Outline Drawing

(N.B., Drawings are not to scale)



NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up mold and facing down for trim/form, ie, reverse trim/form.
4. The foot length measuring is based on the gauge plane method.
5. Dimensions are exclusive of mold flash and gate burr.
6. Dimensions are exclusive of solder plating.
7. All dimensions are in mm.
8. This part is compliant with EIAJ spec. and JEDEC MO-178 AA
9. Lead span/stand off height/coplanarity are considered as special characteristic.



Patent Notice

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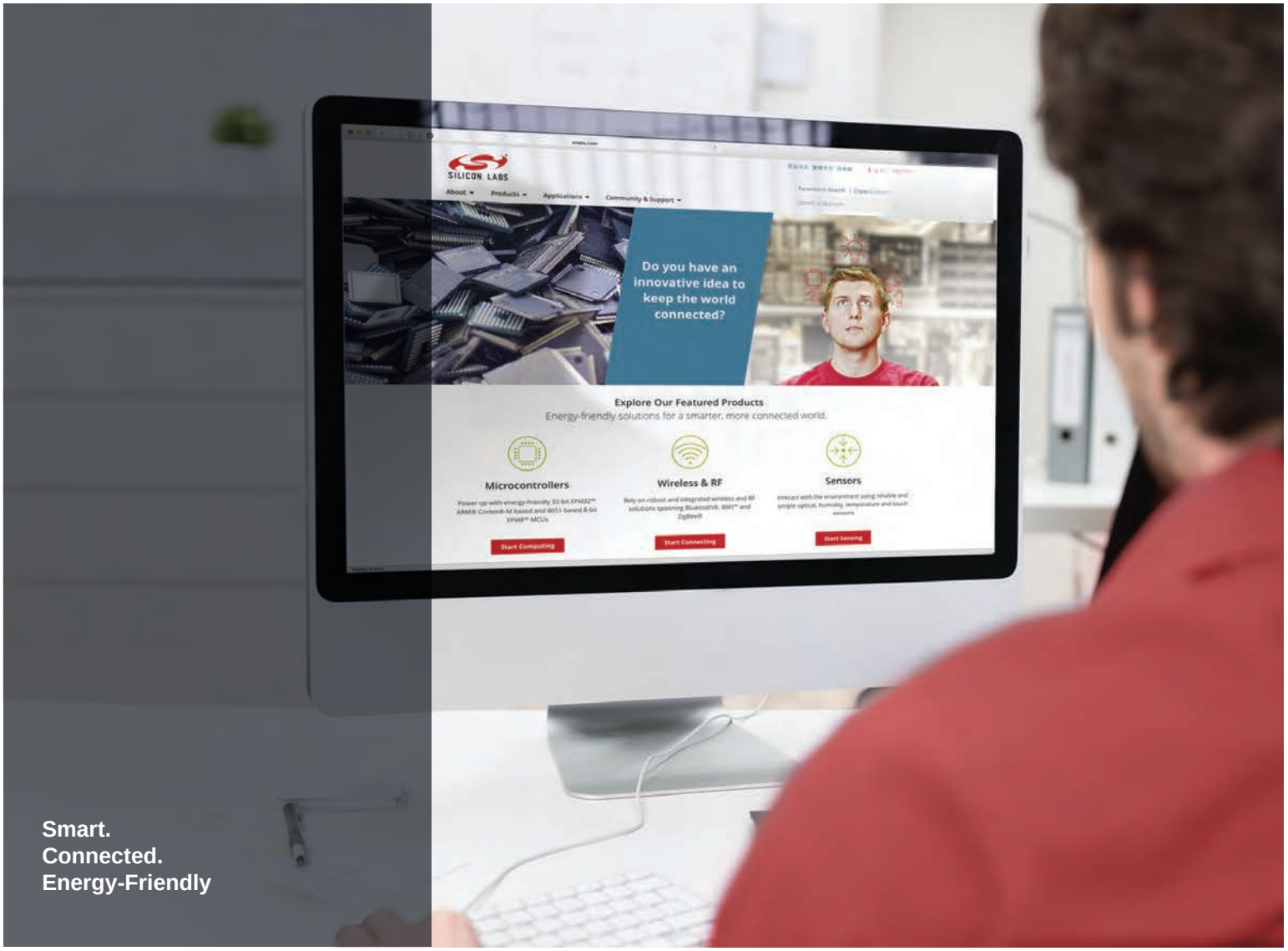

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