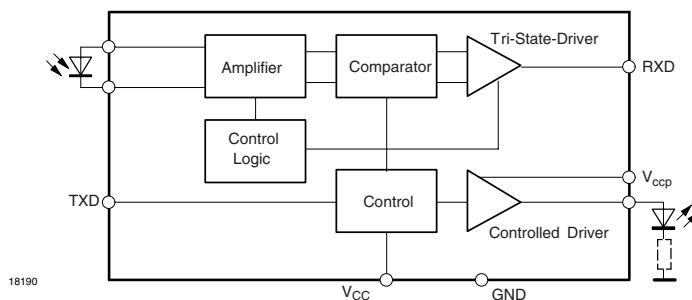


Functional Block Diagram



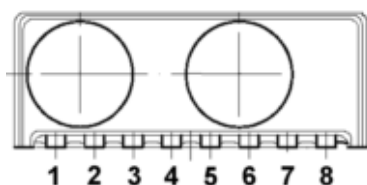
Pin Description

Pin Number	Function	Description	I/O	Active
1	IREG GND	IREG cathode, ground		
2	IREG GND	IREG cathode, ground		
3	RXD	Output, received data, push-pull output	O	low
4	V _{CCP}	IREG supply voltage		
5	GND	Ground		
6	GND	Ground		
7	TXD	Input, transmit data	I	high
8	V _{CC}	Power supply voltage	I	high

Pinout

TFDU4202

weight 100 mg



Absolute Maximum Ratings

Reference Point Pin 8, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range		V _{CC}	- 0.5		6	V
	2.4 V ≤ V _{CC} ≤ 6 V	V _{CCP}	- 0.5		6	V
Input current	all pins				10	mA
Output sink current					25	mA
Power dissipation		P _{tot}			200	mW
Junction temperature		T _J			125	°C
Ambient temperature range (operating)		T _{amb}	- 25		85	°C
Storage temperature range		T _{stg}	- 40		100	°C
Soldering temperature	see the chapter "Soldering conditions" for lead-bearing and Pb-free processing				260	°C
Average IRED current		I _{IRED(DC)}			125	mA
Repetitive pulsed IRED current	< 90μs, t _{on} < 20 %	I _{IRED(RP)}			500	mA
Transmitter data input voltage		V _{TXD}	- 0.5		6	V
Receiver data output voltage		V _{RXD}	- 0.5		6	V

Eye safety information

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Virtual source size	Method: (1 - 1/e) encircled energy	d		2		mm

Compatible to Class 1 operation of IEC 60825 or EN60825 with worst case IrDA SIR pulse pattern, 115.2 kbit/s

Electrical Characteristics

Transceiver

Tested for the following parameters ($V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, $-25^\circ\text{C to } +85^\circ\text{C}$, unless otherwise stated).

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supported data rates	base band		9.6		115.2	kbit/s
Supply voltage range	operational down to 2.0 V	V_{CC}	2.4		5.5	V
Supply current	$V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, $E_e = 0$, receive mode, full temperature range	I_S		65	100	μA
	$V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, 10 klx sunlight, receive mode, full temperature range, no signal	I_S		70	100	μA
	$V_{CC} = 2.7 \text{ V}$, $V_{CCP} = 2.7 \text{ V}$, 115.2 kbit/s transmission, receive mode, nose to nose operation	I_S		1		mA
Supply current at V_{CCP}	shutdown mode, entire temperature range 20°C	$I_{Sshdown}$		0.02	1	μA
IRE peak current transmitting	$I_e = 40 \text{ mW/sr}$, no external resistor, $V_{CCP} = 2.7 \text{ V}$, SIR standard	I_{Str}			360	mA
Transceiver 'power on' settling time	time from switching on V_{CC} to established specified operation				1	ms

Optoelectronic Characteristics

Receiver

Tested for the following parameters ($V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, $-25^\circ\text{C to } +85^\circ\text{C}$, unless otherwise stated).

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance (logic high receiver input irradiance)	$ \alpha \leq \pm 15^\circ$, $V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$	$E_{e, \min}$		25 (2.5)	50 (5)	mW/m^2 ($\mu\text{W/cm}^2$)
	2.0 V, 25°C tested	$E_{e, \min}$		50	100	mW/m^2
Maximum detection threshold irradiance	$ \alpha \leq \pm 90^\circ$, $V_{CC} = 5 \text{ V}$	$E_{e, \max}$	3300 (330)	5000 (500)		W/m^2 (mW/cm^2)
	$ \alpha \leq \pm 90^\circ$, $V_{CC} = 3 \text{ V}$	$E_{e, \max}$	8000 (800)	15000 (1500)		W/m^2 (mW/cm^2)
Logic low receiver input irradiance		$E_{e, \max, \text{low}}$			4 (0.4)	mW/m^2 ($\mu\text{W/cm}^2$)
		$E_{e, \max, \text{low}}$				$\mu\text{W/m}^2$
Output voltage RXD	active, $C = 15 \text{ pF}$	V_{OL}	0		0.5	V
	non active, $C = 15 \text{ pF}$	V_{OH}	$V_{CC} - 0.5$			V
Output current RXD	$V_{OL} < 0.5 \text{ V}$				4	mA
Rise time at load	$C = 15 \text{ pF}$, $R = 2.2 \text{ k}\Omega$	t_r	20		70	ns

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Fall time at load	$C = 15 \text{ pF}$, $R = 2.2 \text{ k}\Omega$	t_f	20		70	ns
RXD signal electrical output pulse width	2.4 kbit/s, input pulse width 1.41 μs to 3/16 of bit duration	t_p	1.41		20	μs
	115.2 kbit/s, input pulse width 1.41 μs to 3/16 of bit duration	t_p	1.41		4.5	μs
Output delay time (RXD), leading edge optical input to electrical output	output level = $0.5 \times V_{CC}$ at 40 mW/m ²	t_{dl}		1	2	μs
Jitter, leading edge of output signal	over a period of 10 bit, 115.2 kbit/s	t_j			400	ns
Output delay time (RXD), trailing edge optical input to electrical output	output level = $0.5 \times V_{CC}$ at 40 mW/m ²	t_{dt}			6.5	μs
Power on time, SD recovery time				0.1	1	ms
Latency		t_L		100	200	μs

Transmitter

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Logic low transmitter input voltage		$V_{IL(TXD)}$	- 0.5		$0.15 \times V_{CC}$	V
Logic high transmitter input voltage		$V_{IH(TXD)}$	$0.8 \times V_{CC}$		6	V
Output radiant intensity	$I_{F1} = 320 \text{ mA}$, $ \alpha \leq \pm 15^\circ$, current controlled by external resistor, voltage range 2.7 V to 5.5 V	I_e	45			mW/sr
Peak emission wavelength		λ_p	850		900	nm
Spectral emission bandwidth				60		nm
Optical rise/fall time	115.2 kHz square wave signal (duty cycle 1 : 1)				200	ns
Optical output pulse duration	input pulse duration 1.6 μs		1.5	1.6	1.7	μs
	input pulse duration > 25 μs , safety protection				25	μs
Output radiant intensity	logic low level				0.04	$\mu\text{W/sr}$
Overshoot, optical					25	%
Rising edge peak to peak jitter	over a period of 10 bits, independent of information content	t_j			0.2	μs

Truth table

Inputs			Outputs	
V_{CC}	TXD	Optical input Irradiance mW/m ²	RXD	Transmitter
low	x	x	low	0
high	high	x	high	I_e
	high $\geq 25 \mu\text{s}$	x	high	0
	low	< 4	high	0
	low	> Min. detection threshold irradiance < Max. detection threshold irradiance	x	0
	low	> Max. detection threshold irradiance	undefined	0

Application Hints

The TFDU4202 does not need any external component when operated with a "clean" power supply. In a more noisy ambient it is recommended to add a capacitor C1 and a resistor R1 for noise suppression. A combination of a tantalum with a ceramics capacitor will be efficient to attenuate both, RF and LF. The power supply V_{CCP} must be able to source up to 550 mA current with a fast rise time. If that cannot be guaranteed an additional capacitor near pin 4 (V_{CCP}) should be included. The value is depending on the power supply quality. A good choice is between 4.7 μ F and 10 μ F.

Latency

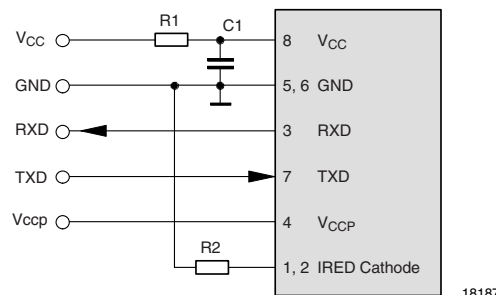
The receiver is in specified conditions after the defined latency.

In a UART related application after that time after the last transmitted signal (IrDA specifies 500 μ s maximum for low power applications and 10 ms maximum for standard) the receiver buffer of the UART must be

cleared. Therefore the transceiver has to wait at least the specified latency after receiving the last bit before starting the transmission to be sure that the corresponding receiver is in a defined state.

For more application circuits, see IrDC Design Guide and TOIM4232 data sheet.

Recommended Circuit Diagram



Table

Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1	4.7 μ F, 16 V	293D 475X9 016B 2T
R1	5 Ω (2 Ω to 47 Ω)	

This is a recommendation for a combination to start with to exclude power supply effects.

Optimum, from a costs point of view, to work without both.

Temperature Derating Diagram

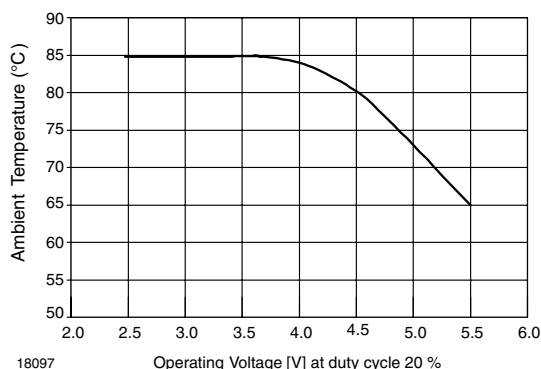


Figure 1. Temperature Derating Diagram

The temperature derating diagram shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to Ground for supply voltages above 4 V. In that case the device can be operated up to 85 °C, too.

Recommended Solder Profiles

Solder Profile for Sn/Pb Soldering

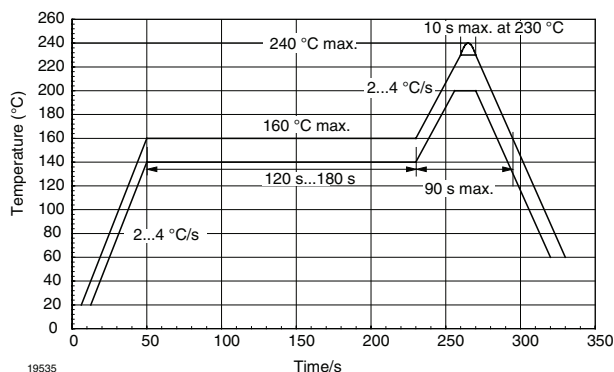


Figure 2. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFDU4202 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn (3.0 - 4.0) Ag (0.5 - 0.9) Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 3 and 4 are VISHAY's recommended profiles for use with the TFDU4202 transceivers. For more details please refer to the application note "SMD Assembly Instructions" (<http://www.vishay.com/docs/82602/82602.pdf>).

A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing" (<http://www.vishay.com/docs/82601/82601.pdf>).

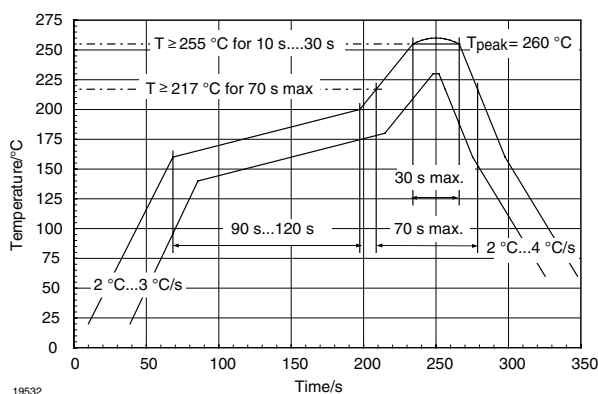


Figure 3. Solder Profile, RSS Recommendation

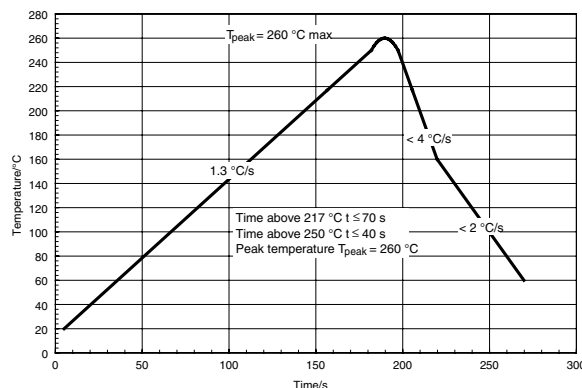
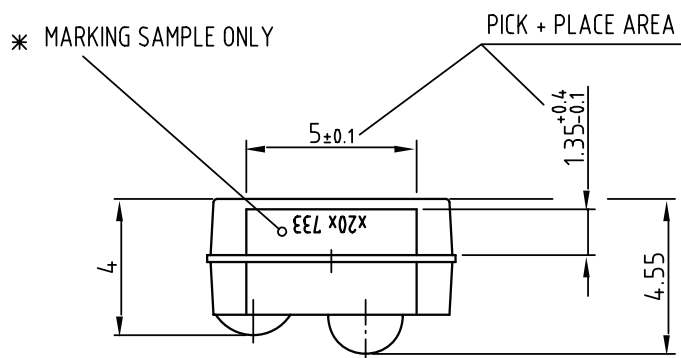
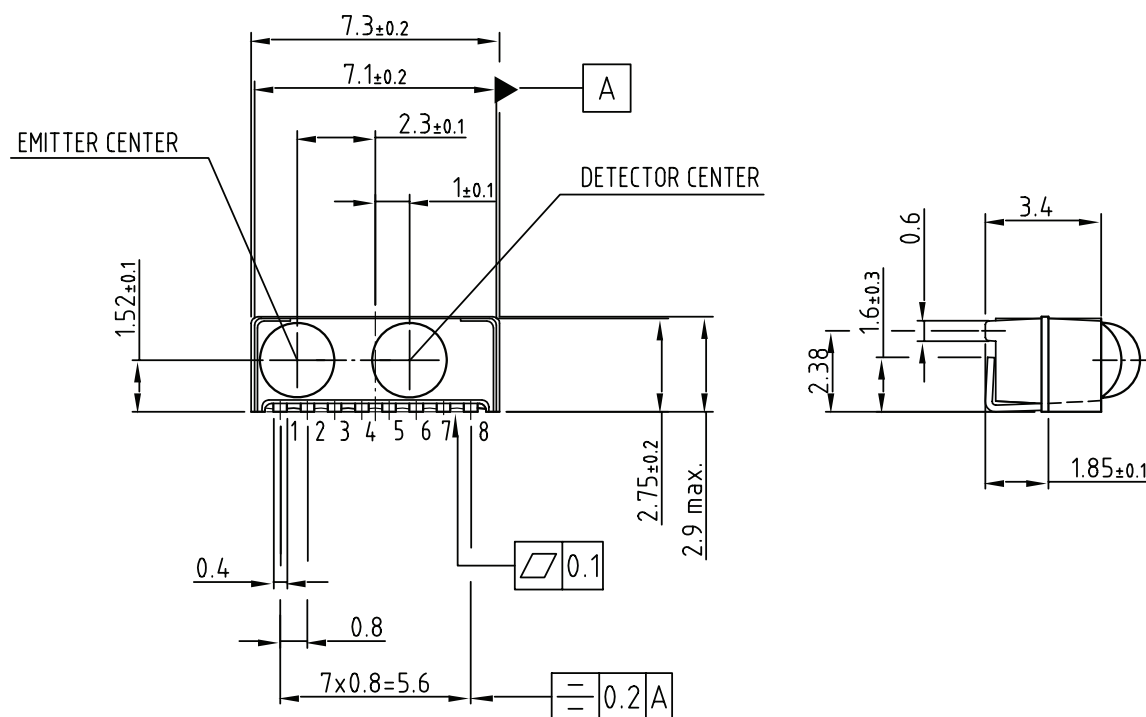
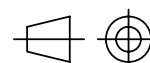


Figure 4. RTS Recommendation

Package Dimensions



All dimensions in mm



technical drawings
according to DIN
specifications

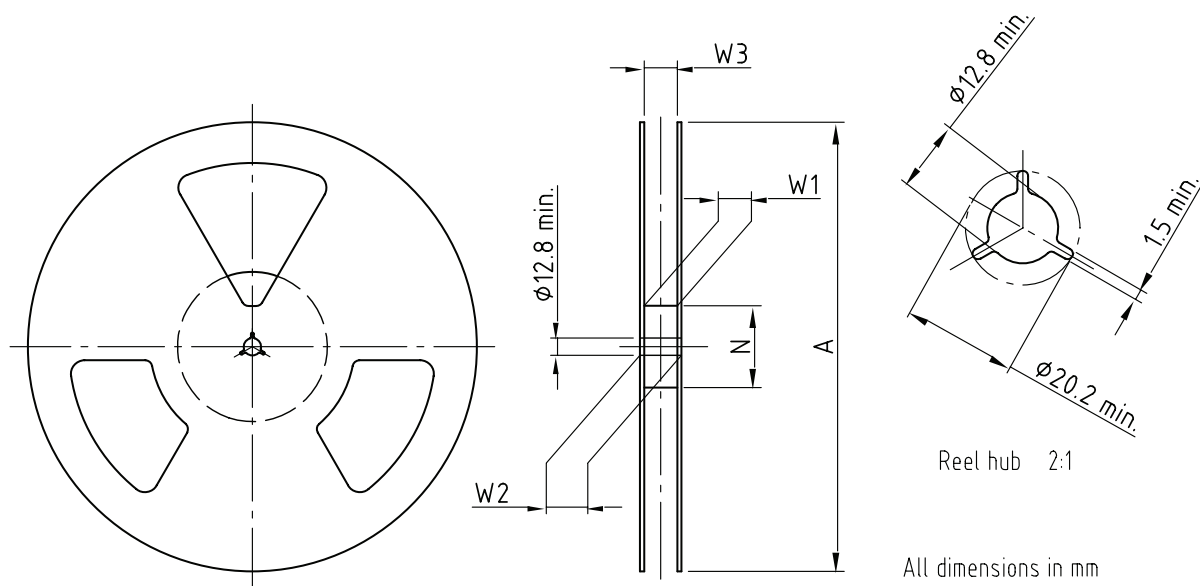
19821

* MARKING ORIENTATION
180 DEGREES ALLOWED

Drawing-No.: 6.550-5185.01-4
Issue: 5; 02.09.05

Figure 5. Package drawing, TFDU4202

Reel Dimensions



Reel hub 2:1

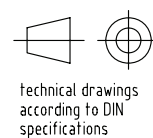
All dimensions in mm

Drawing-No.: 9.800-5090.01-4
Issue: 1; 29.11.05

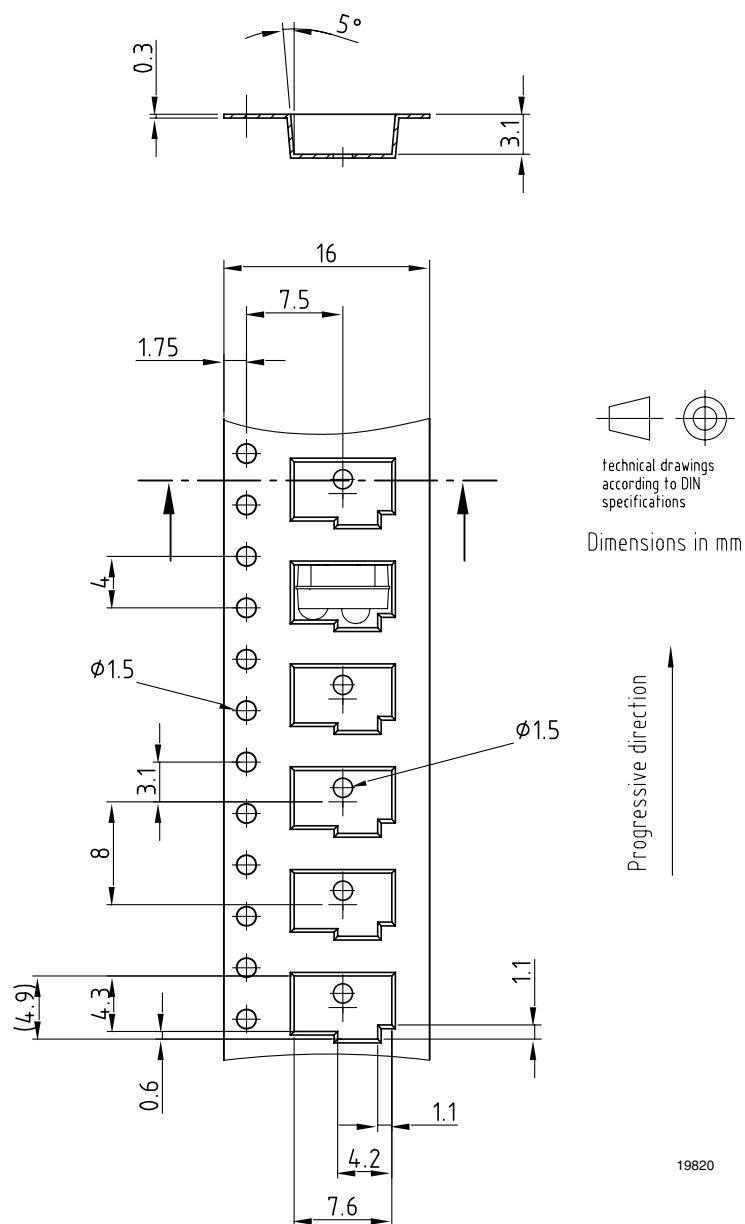
14017

Form of the leave open
of the wheel is supplier specific.

Dimension acc. to IEC EN 60 286-3



mm	mm	mm	mm	mm	mm	mm
Tape Width	A max.	N	$W_1 \text{ min.}$	$W_2 \text{ max.}$	$W_3 \text{ min.}$	$W_3 \text{ max.}$
16	180	60	16.4	22.4	15.9	19.4
16	330	50	16.4	22.4	15.9	19.4

Tape Dimensions


Drawing-No.: 9.700-5227.01-4
Issue: 3; 03.09.99

Figure 6. Tape drawing, TFDU4202 for side view mounting



Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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