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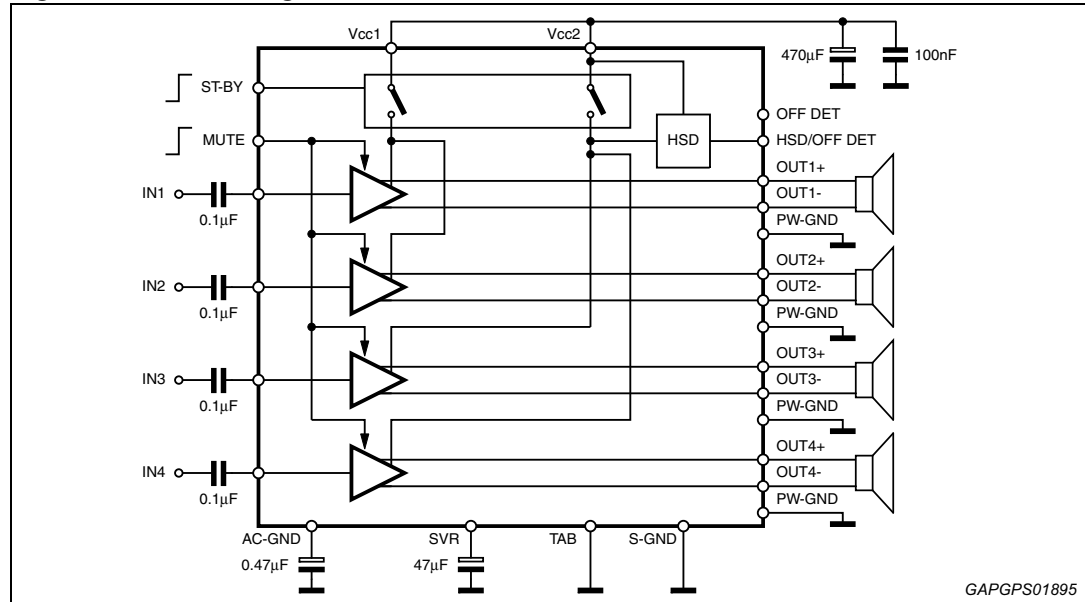
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1 Block diagram and application circuit

1.1 Block diagram

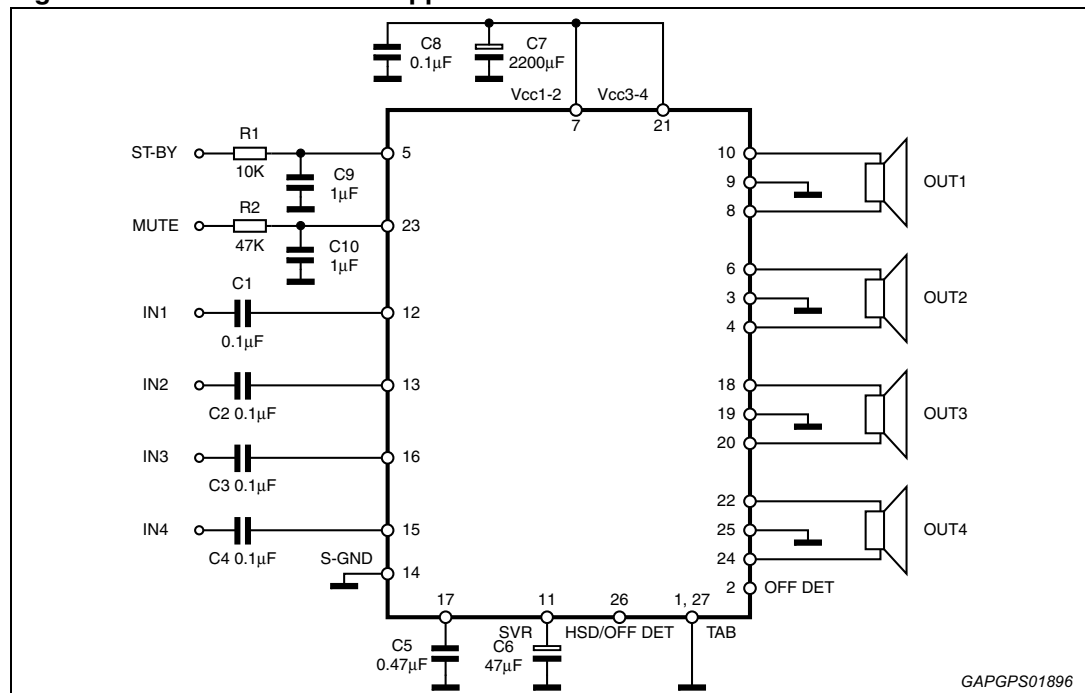
Figure 1. Block diagram



GAPGPS01895

1.2 Standard test and application circuit

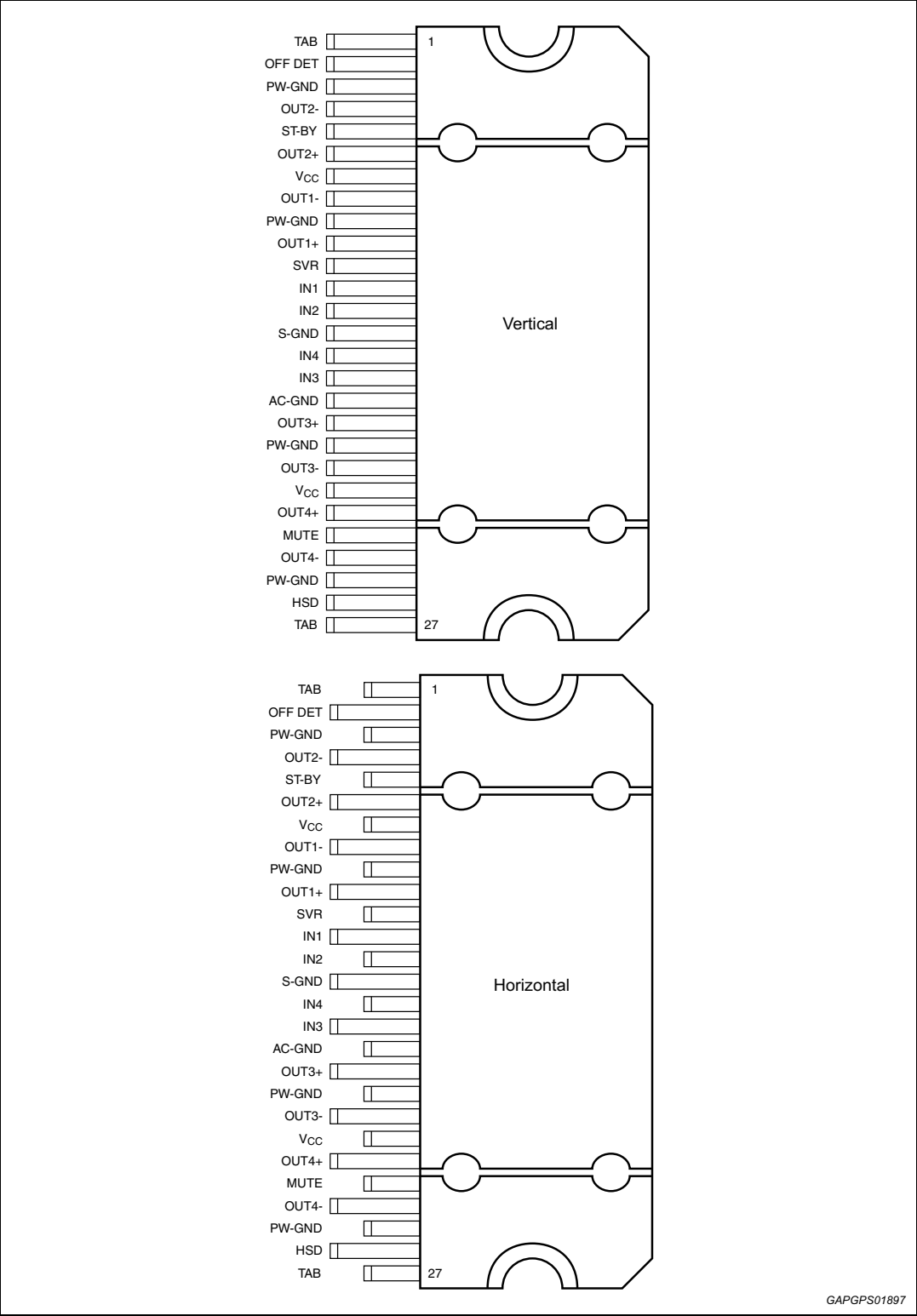
Figure 2. Standard test and application circuit



GAPGPS01896

2 Pin description

Figure 3. Pin connections (top view)



GAPGPS01897

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	18	V
$V_{S(DC)}$	DC supply voltage	28	V
$V_{S(pk)}$	Peak supply voltage (for $t = 50$ ms)	50	V
I_O	Output peak current repetitive (duty cycle 10 % at $f = 10$ Hz) non repetitive ($t = 100$ μ s)	9	A
		10	A
P_{tot}	Power dissipation $T_{case} = 70$ °C	80	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal resistance junction-to-case Max.	1	°C/W

3.3 Electrical characteristics

Refer to the test and application diagram, $V_S = 14.4$ V; $R_L = 4$ Ω ; $R_g = 600$ Ω ; $f = 1$ kHz;
 $T_{amb} = 25$ °C; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{q1}	Quiescent current	$R_L = \infty$	100	180	280	mA
V_{OS}	Output offset voltage	Play mode - Mute mode	-	-	± 50	mV
dV_{OS}	During mute ON/OFF output offset voltage	ITU R-ARM weighted see Figure 18	-10	-	+10	mV
	During St-By ON/OFF output offset voltage		-10	-	+10	mV
G_v	Voltage gain	-	25	26	27	dB
dG_v	Channel gain unbalance	-	-	-	± 1	dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P _O	Output power	V _S = 13.2 V; THD = 10 %	23	25	-	W
		V _S = 13.2 V; THD = 1 %	16	19		
		V _S = 14.4 V; THD = 10 %	28	30		
		V _S = 14.4 V; THD = 1 %	20	23		
		V _S = 14.4 V; THD = 10 %, 2 Ω	50	55		W
P _{O max.}	Max. output power ⁽¹⁾	V _S = 14.4 V; R _L = 4 Ω V _S = 14.4 V; R _L = 2 Ω	-	50 85	-	W
THD	Distortion	P _O = 4 W P _O = 15 W; R _L = 2 Ω	-	0.006 0.015	0.02 0.03	%
e _{No}	Output noise	"A" Weighted Bw = 20 Hz to 20 kHz	-	35 50	50 70	μV
SVR	Supply voltage rejection	f = 100 Hz; V _r = 1 Vrms	50	75	-	dB
f _{ch}	High cut-off frequency	P _O = 0.5 W	100	300	-	KHz
R _i	Input impedance		80	100	120	KΩ
C _T	Cross talk	f = 1 kHz; P _O = 4 W	60	70	-	dB
		f = 10 kHz; P _O = 4 W	-	60	-	
I _{SB}	Standby current consumption	V _{ST-BY} = 1.5 V	-	-	20	μA
		V _{ST-BY} = 0V	-	-	10	
I _{pin5}	Standby pin current	V _{ST-BY} = 1.5V to 3.5V	-	-	±1	μA
V _{SB out}	Standby out threshold voltage	(Amp: ON)	2.75	-	-	V
V _{SB in}	Standby in threshold voltage	(Amp: OFF)	-	-	1.5	V
A _M	Mute attenuation	P _{Oref} = 4W	80	90	-	dB
V _{M out}	Mute out threshold voltage	(Amp: Play)	3.5	-	-	V
V _{M in}	Mute in threshold voltage	(Amp: Mute)	-	-	1.5	V
V _{AM in}	V _S automute threshold	(Amp: Mute) Att ≥ 80 dB; P _{Oref} = 4 W	6.5	7		V
		(Amp: Play) Att < 0.1 dB; P _O = 0.5 W		7.5	8	
I _{pin23}	Muting pin current	V _{MUTE} = 1.5 V (Sourced Current)	7	12	18	μA
		V _{MUTE} = 3.5 V	-5	-	18	μA
HSD section						
V _{dropout}	Dropout voltage	I _O = 0.35 A; V _S = 9 to 16 V	-	0.25	0.6	V
I _{prot}	Current limits	-	400	-	800	mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Offset detector (Pin 26)						
V_{M_ON}	Mute voltage for DC offset detection enabled	$V_{ST-BY} = 5\text{ V}$	8	-	-	V
V_{M_OFF}			-	-	6	V
V_{OFF}	Detected differential output offset	$V_{ST-BY} = 5\text{ V}; V_{mute} = 8\text{ V}$	± 2	± 3	± 4	V
V_{26_T}	Pin 26 voltage for detection = TRUE	$V_{ST-BY} = 5\text{ V}; V_{mute} = 8\text{ V}$ $V_{OFF} > \pm 4\text{ V}$	0	-	1.5	V
V_{26_F}	Pin 26 voltage for detection = FALSE	$V_{ST-BY} = 5\text{ V}; V_{mute} = 8\text{ V}$ $V_{OFF} > \pm 2\text{ V}$	12	-	-	V

1. Saturated square wave output.

3.4 Electrical characteristic curves

Figure 4. Quiescent current vs. supply voltage

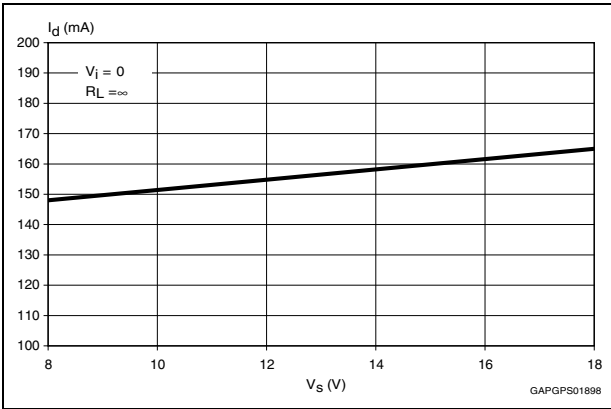


Figure 5. Output power vs. supply voltage ($R_L = 4\ \Omega$)

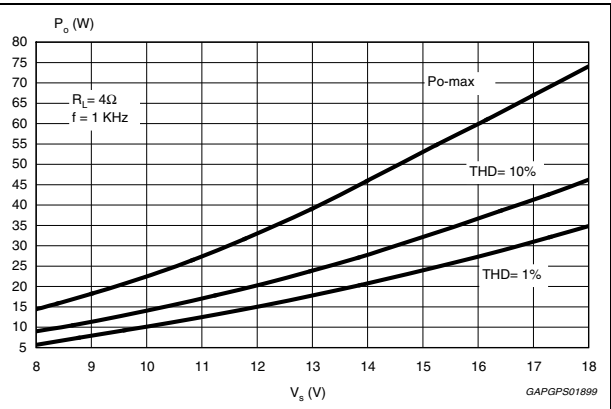


Figure 6. Output power vs. supply voltage ($R_L = 2\ \Omega$)

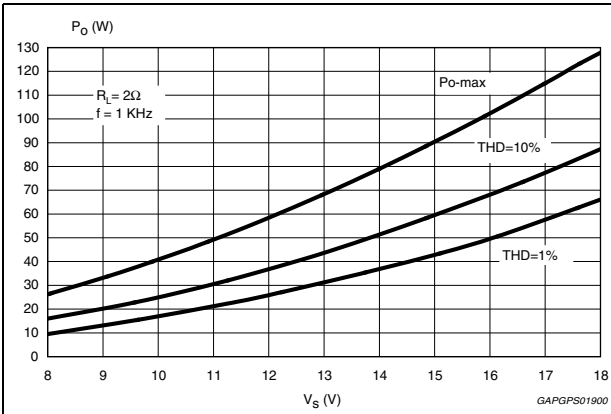


Figure 7. Distortion vs. output power ($R_L = 4\ \Omega$)

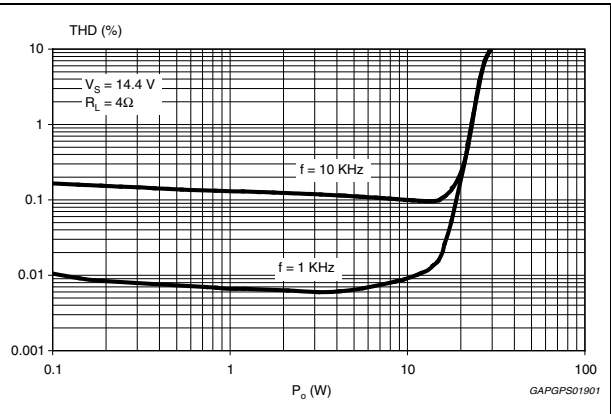


Figure 8. Distortion vs. output power
($R_L = 2\ \Omega$)

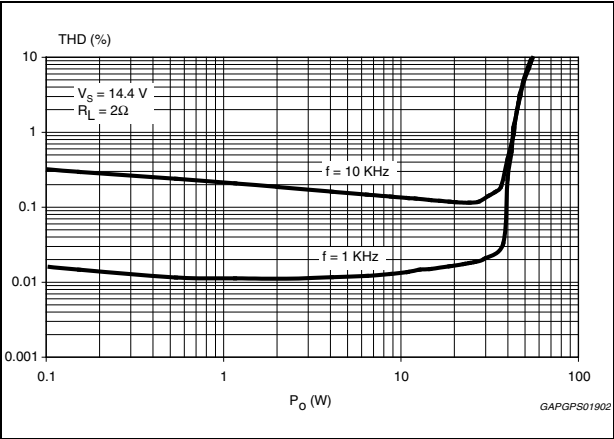


Figure 9. Distortion vs. frequency
($R_L = 4\ \Omega$)

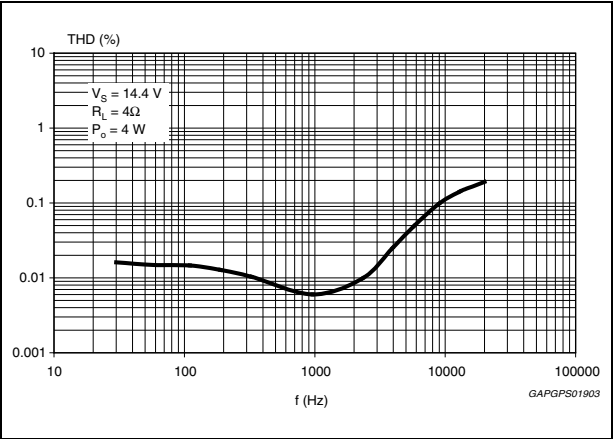


Figure 10. Distortion vs. frequency
($R_L = 2\ \Omega$)

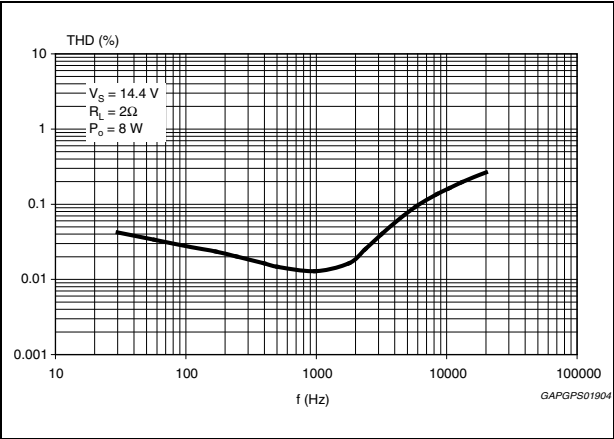


Figure 11. Crosstalk vs. frequency

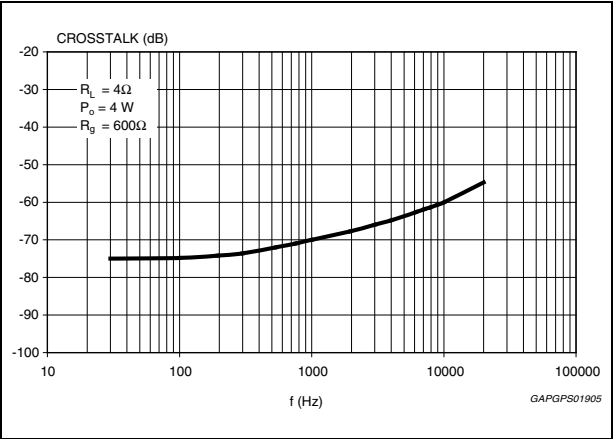


Figure 12. Supply voltage rejection vs. frequency

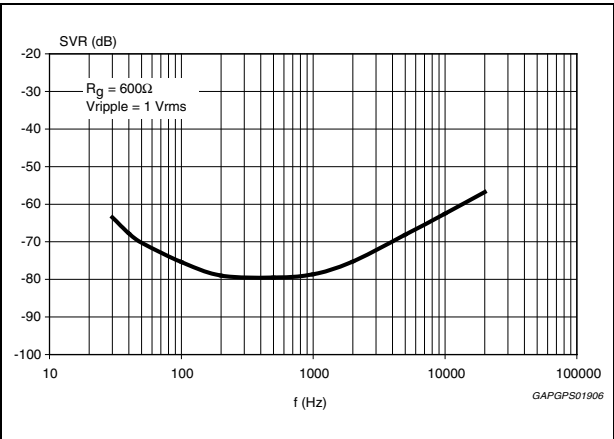


Figure 13. Output attenuation vs. supply voltage

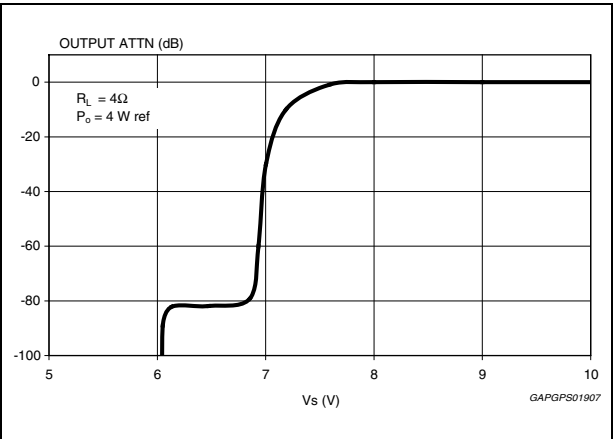


Figure 14. Power dissipation and efficiency vs. output power ($R_L = 4 \Omega$, SINE)

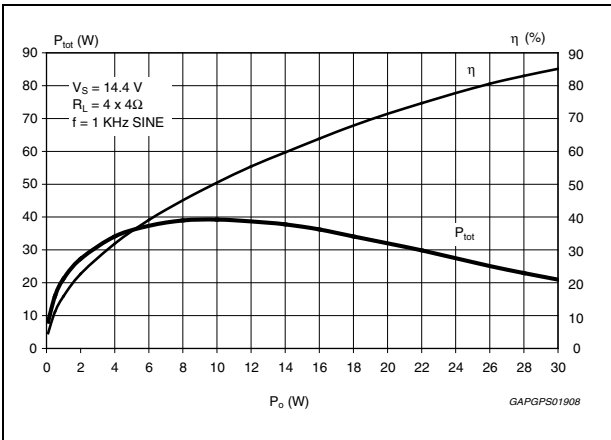


Figure 15. Power dissipation and efficiency vs. output power ($R_L = 2 \Omega$, SINE)

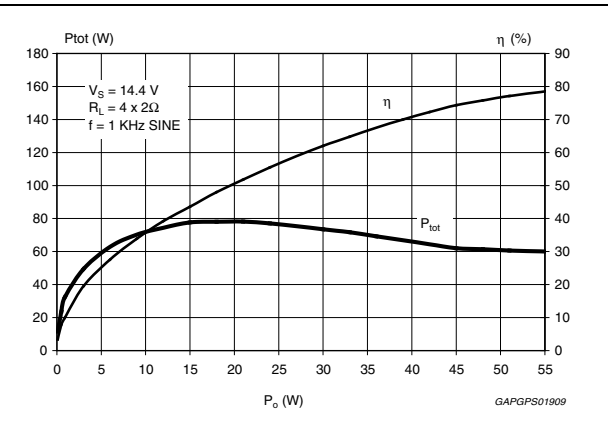


Figure 16. Power dissipation vs. output power ($R_L = 4 \Omega$, audio program simulation)

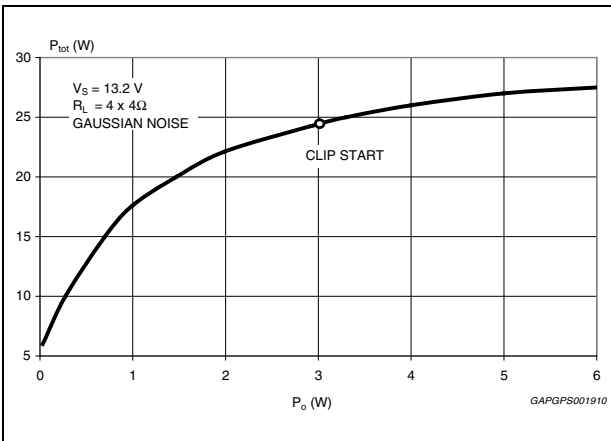


Figure 17. Power dissipation vs. output power ($R_L = 2 \Omega$, audio program simulation)

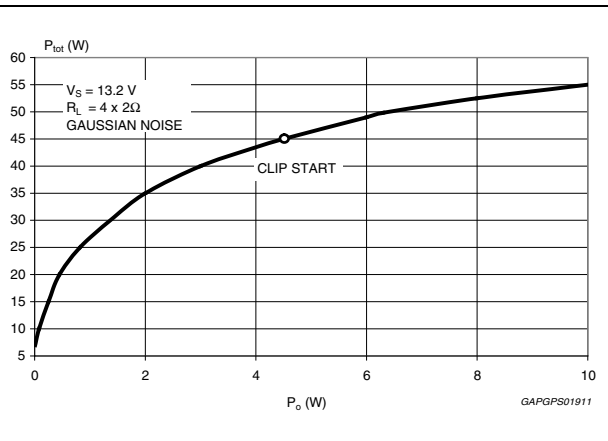
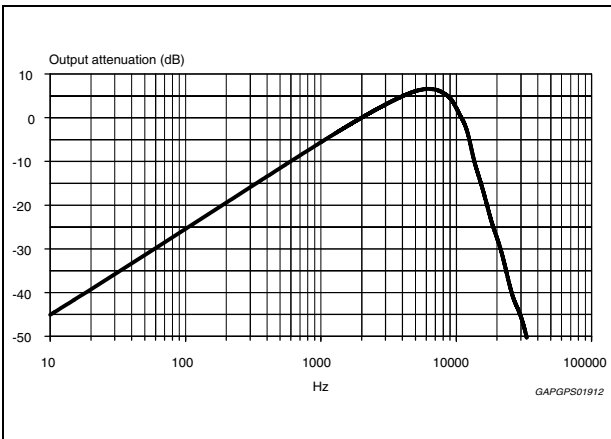


Figure 18. ITU R-ARM frequency response, weighting filter for transient pop



4 Application hints

Ref. to the circuit of [Figure 2](#).

4.1 SVR

Besides its contribution to the ripple rejection, the SVR capacitor governs the turn ON/OFF time sequence and, consequently, plays an essential role in the pop optimization during ON/OFF transients. To conveniently serve both needs, **its minimum recommended value is 10 μ F**.

4.2 Input stage

The TDA7850A's inputs are ground-compatible and can stand very high input signals (± 8 Vpk) without any performance degradation.

If the standard value for the input capacitors (0.1 μ F) is adopted, the low frequency cut-off will amount to 16 Hz.

4.3 Standby and muting

STANDBY and MUTING facilities are both CMOS compatible. In absence of true CMOS ports or microprocessors, a direct connection to Vs of these two pins is admissible but a 470k Ω equivalent resistance should be present between the power supply and the muting and stand-by pins.

R-C cells have always to be used in order to smooth down the transitions for preventing any audible transient noises.

About the stand-by, the time constant to be assigned in order to obtain a virtually pop-free transition has to be slower than 2.5V/ms.

4.4 DC offset detector

The TDA7850A integrates a DC offset detector to avoid that an anomalous DC offset on the inputs of the amplifier may be multiplied by the gain and result in a dangerous large offset on the outputs which may lead to speakers damage for overheating.

The feature works with the amplifier unmuted and no signal at the inputs.

The DC offset detection can be available at 2 different pins:

- Pin 2 (always enabled)
- Pin 26. Only enabled if Vmute (pin23) is set higher than 8V. If not (Vmute < 6 V) pin 26 will revert to the original HSD function.

4.5 Heatsink definition

Under normal usage (4 Ohm speakers) the heatsink's thermal requirements have to be deduced from [Figure 16](#), which reports the simulated power dissipation when real music/speech programmes are played out. Noise with gaussian-distributed amplitude was employed for this simulation. Based on that, frequent clipping occurrence (worst-case) will cause $P_{diss} = 26$ W. Assuming $T_{amb} = 70^{\circ}\text{C}$ and $T_{CHIP} = 150^{\circ}\text{C}$ as boundary conditions, the heatsink's thermal resistance should be approximately 2°C/W . This would avoid any thermal shutdown occurrence even after long-term and full-volume operation.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 19. Flexiwatt27 (horizontal) mechanical data and package dimensions

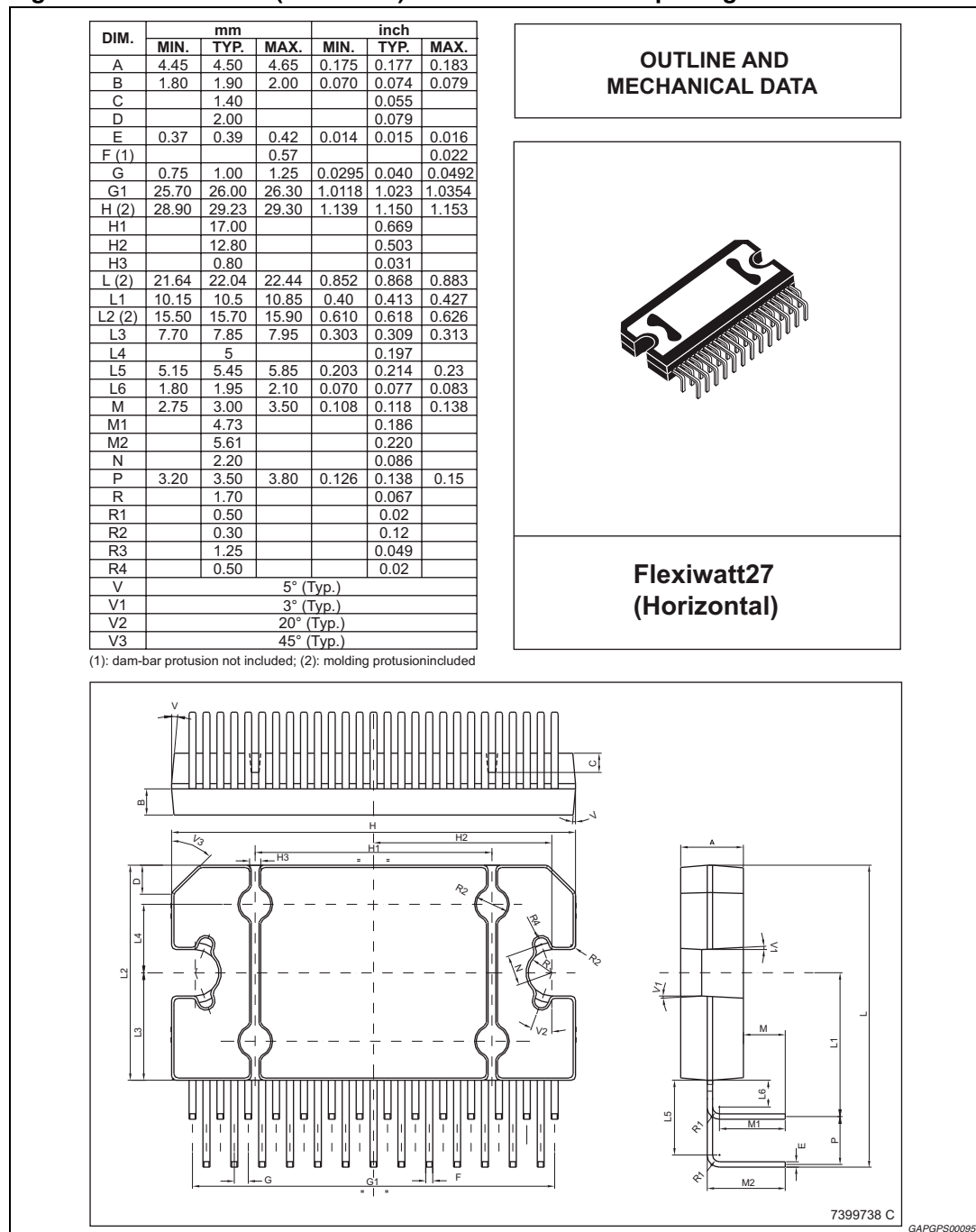
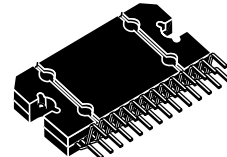


Figure 20. Flexiwatt27 (vertical) mechanical data and package dimensions

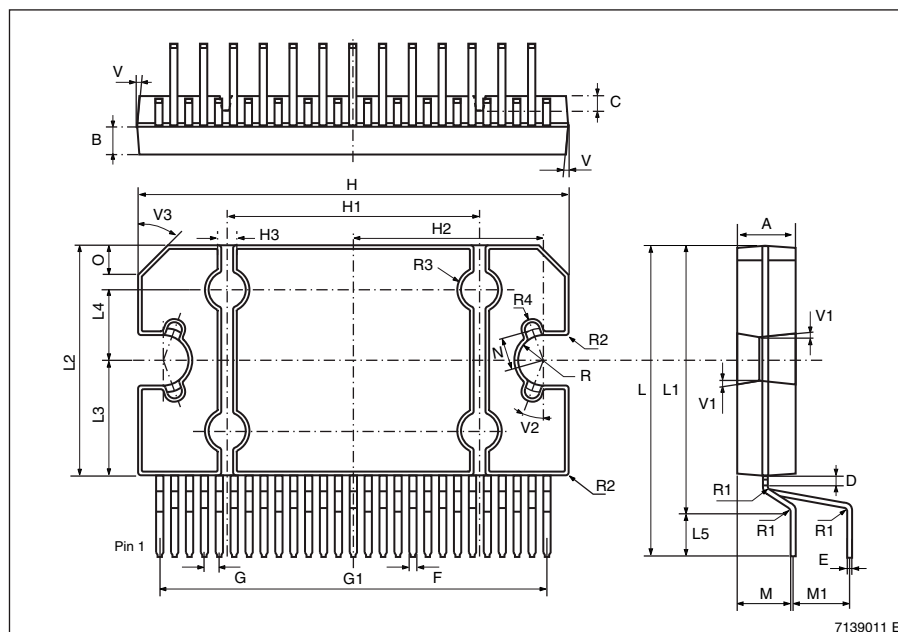
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F ⁽¹⁾			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H ⁽²⁾	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L ⁽²⁾	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 ⁽²⁾	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included.

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)

7139011 E
GAPGPS00096

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
09-Oct-2007	1	Initial release.
12-Sep-2008	2	Updated the values of V_{OS} and THD parameters on the Table 4 .
07-Nov-2008	3	Modified max. values of the THD distortion in Table 4: Electrical characteristics on page 8.
14-Aug-2012	4	Updated Section 5: Package information .
17-Sep-2013	5	Updated Disclaimer.

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