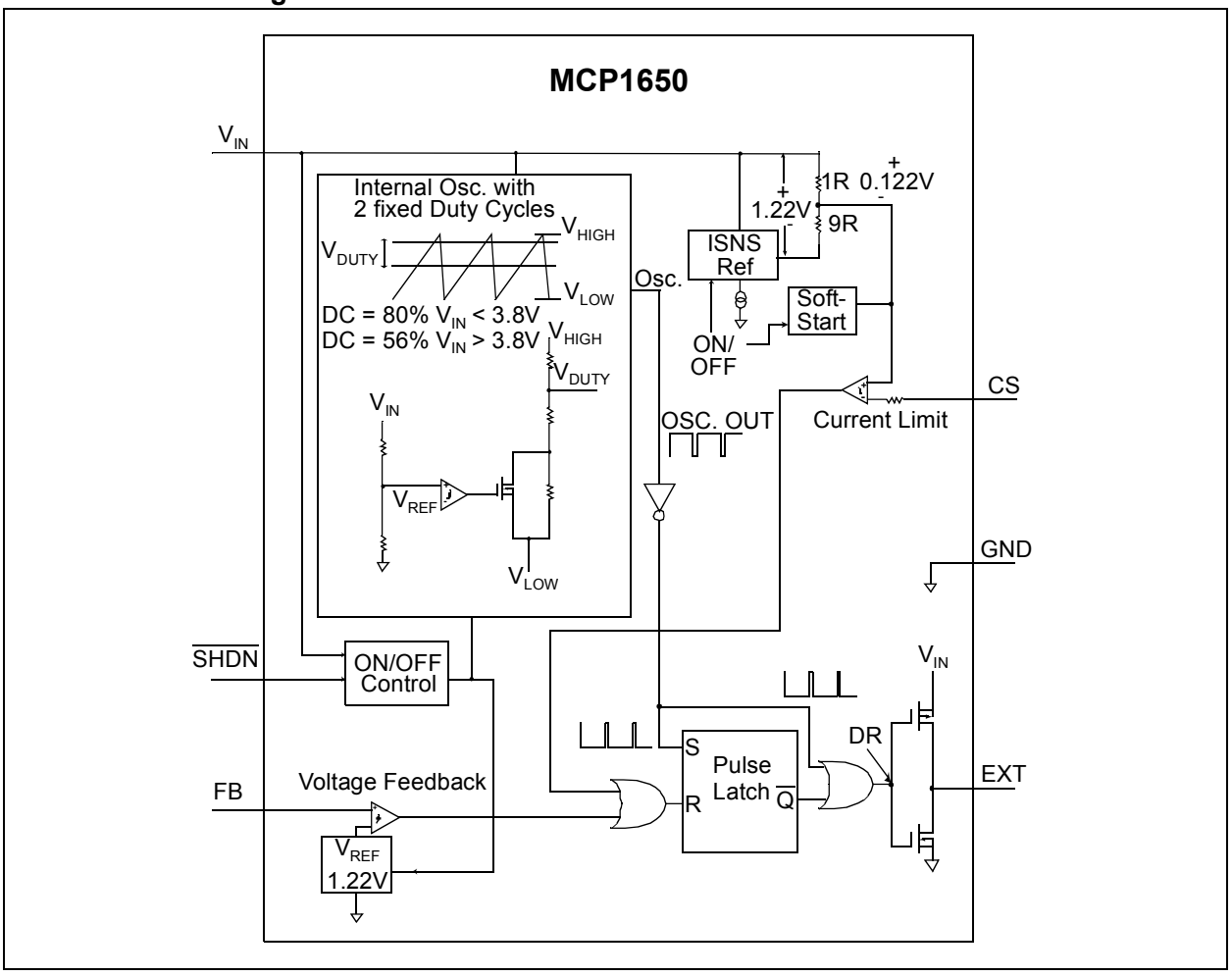
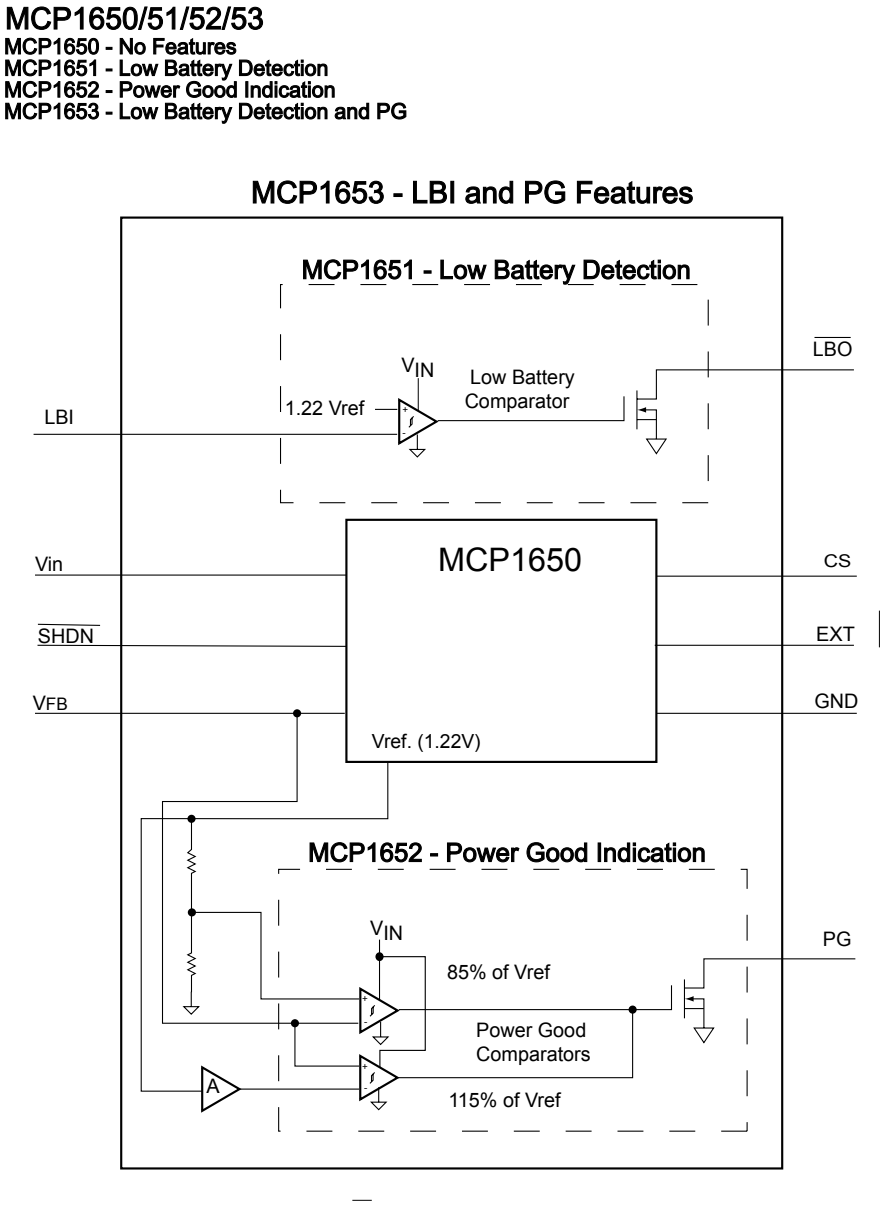
MCP1650 Block Diagram

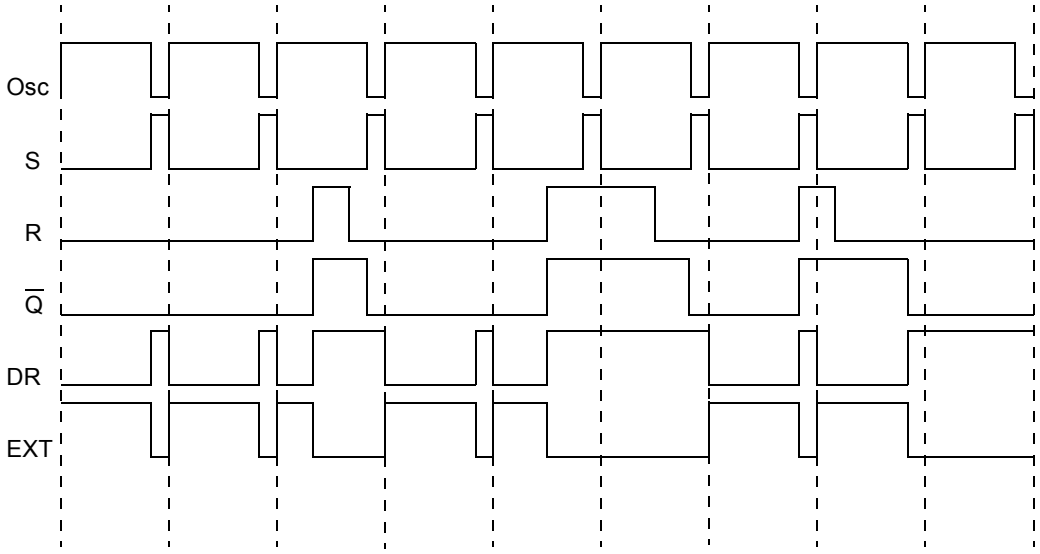


MCP1651/2/3 Block Diagram



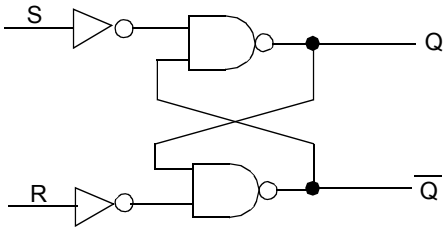
Timing Diagram

MCP1650/1/2/3 Timing Diagram



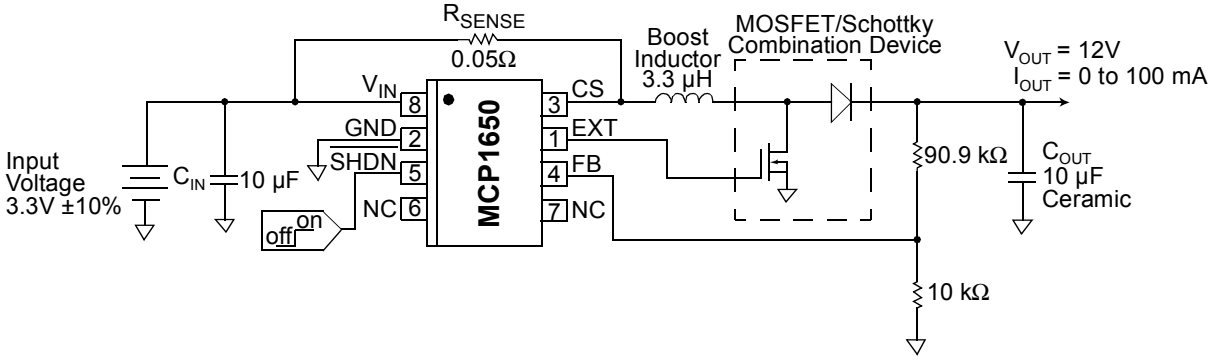
Latch Truth Table

S	R	$\overline{Q}$
0	0	$\overline{Qn}$
0	1	1
1	0	0
1	1	1



Typical Application Circuits

3.3V to 12V 100 mA Boost Converter



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} TO GND 6.0V

CS,FB,LBI,$\overline{LBO}$,$\overline{SHDN}$,PG,EXT..... GND – 0.3V to V_{IN} + 0.3V

Current at EXT pin ..... ±1A

Storage temperature ..... -65°C to +150°C

Operating Junction Temperature..... -40°C to +125°C

ESD protection on all pins ..... ≥ 4 kV HBM

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply at V_{IN} = +2.7V to +5.5V, $\overline{SHDN}$ = High, T_J = -40°C to +125°C. Typical values apply for V_{IN} = 3.3V, T_A +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Characteristics						
Supply Voltage	V_{IN}	2.7	—	5.5	V	
Undervoltage Lockout (S Option)	UVLO	2.4	2.55	2.7	V	V_{IN} rising edge
Under Voltage Lockout (R Option)	UVLO	1.85	2.0	2.15	V	V_{IN} rising edge
Undervoltage Hysteresis	$UVLO_{HYST}$	—	117	—	mV	
Shutdown Supply Current	$I_{\overline{SHD}}$	—	0.001	1	µA	$\overline{SHDN}$ = GND
Quiescent Supply Current	I_Q	—	120	220	µA	EXT = Open
Soft Start Time	T_{SS}	—	500	—	µs	
Feedback Characteristics						
Feedback Voltage	V_{FB}	1.18	1.22	1.26	V	All conditions
Feedback Comparator Hysteresis	V_{HYS}	—	12	23	mV	
Feedback Input Bias Current	I_{FBlk}	-50	—	50	nA	V_{FB} < 1.3V
Current Sense Input						
Current Sense Threshold	I_{SNS-TH}	75	114	155	mV	
Delay from Current Sense to Output	T_{dly_ISNS}	—	80	—	ns	
Ext Drive						
EXT Driver ON Resistance (High Side)	R_{HIGH}	—	8	18	Ω	
EXT Driver ON Resistance (Low Side)	R_{LOW}	—	4	12	Ω	
Oscillator Characteristics						
Switching Frequency	F_{OSC}	650	750	850	kHz	
Low Duty Cycle Switch-Over Voltage	$V_{LowDuty}$	—	3.8	—	V	V_{IN} rising edge
Duty Cycle Switch Voltage Hysteresis	DC_{Hyst}	—	92	—	mV	
Low Duty Cycle	DC_{LOW}	50	56	62	%	
High Duty Cycle	DC_{HIGH}	72	80	88	%	

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, all parameters apply at V_{IN} = +2.7V to +5.5V, $\overline{SHDN}$ = High, T_J = -40°C to +125°C. Typical values apply for V_{IN} = 3.3V, T_A +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Shutdown Input						
Logic High Input	$V_{IN-HIGH}$	50	—	—	% of V_{IN}	
Logic Low Input	V_{IN-Low}	—	—	15	% of V_{IN}	
Input Leakage Current	$I_{\overline{SHDN}}$	—	5	100	nA	$\overline{SHDN}$=V_{IN}
Low Battery Detect (MCP1651/MCP1653 Only)						
Low Battery Threshold	LBI_{TH}	1.18	1.22	1.26	V	LBI Input falling (All Conditions)
Low Battery Threshold Hysteresis	LBI_{THHYS}	95	123	145	mV	
Low Battery Input Leakage Current	I_{LBI}	—	10	—	nA	V_{LBI} = 2.5V
Low Battery Output Voltage	$V_{\overline{LBO}}$	—	53	200	mV	I_{LB} SINK = 3.2 mA, V_{LBI} = 0V
Low Battery Output Leakage Current	$I_{\overline{LBO}}$	—	0.01	1	µA	V_{LBI} = 5.5V, $V_{\overline{LBO}}$ = 5.5V
Time Delay from LBI to LBO	T_{D_LBO}	—	70	—	µs	L_{BI} Transitions from L_{BITH} + 0.1V to L_{BITH} - 0.1V
Power Good Output (MCP1652/MCP1653 Only)						
Power Good Threshold Low	V_{PGTH-L}	-20	-15	-10	%	Referenced to Feedback Voltage
Power Good Threshold High	V_{PGTH-H}	+10	+15	+20	%	Referenced to Feedback Voltage
Power Good Threshold Hysteresis	$V_{PGTH-HYS}$	—	5	—	%	Referenced to Feedback Voltage (Both Low and High Thresholds)
Power Good Output Voltage	$V_{\overline{PGOUT}}$	—	53	200	mV	I_{PG} SINK = 3.2 mA, V_{FB} = 0V
Time Delay from V_{FB} out of regulation to Power Good Output transition	T_{D_PG}	—	85	—	µs	V_{FB} Transitions from V_{FBTH} + 0.1V to V_{FBTH} -0.1V

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise noted, all parameters apply at V_{IN} = +2.7V to +5.5V, $\overline{SHDN}$ = High, T_A = -40°C to +125°C. Typical values apply for V_{IN} = 3.3V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_A	-40	—	+125	°C	
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Continuous
Thermal Package Resistances						
Thermal Resistance, MSOP-8	θ_{JA}	—	208	—	°C/W	Single-Layer SEMI G42-88 Board, Natural Convection
Thermal Resistance, MSOP-10	θ_{JA}	—	113	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 3.3V, V_{OUT} = 12V, C_{IN} = 10 µF (x5R or X7R Ceramic), C_{OUT} = 10 µF (X5R or X7R), I_{OUT} = 10 mA, L = 3.3 µH, $\overline{SHDN}$ > V_{IH}, T_A = +25°C.

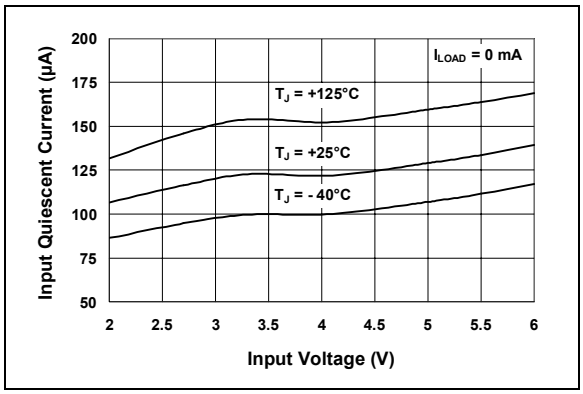


FIGURE 2-1: *Input Quiescent Current vs. Input Voltage.*

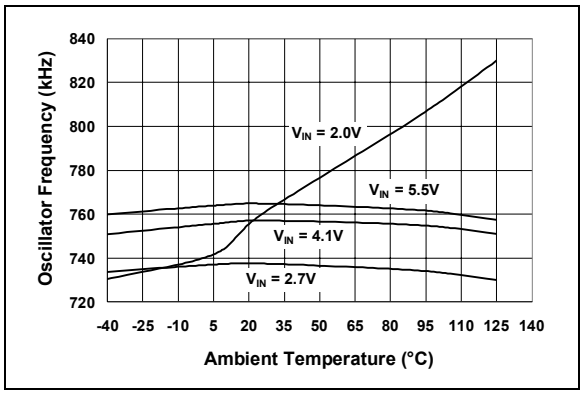


FIGURE 2-4: *Oscillator Frequency vs. Ambient Temperature.*

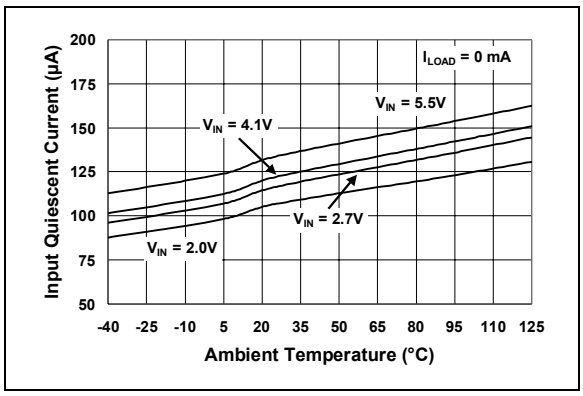


FIGURE 2-2: *Input Quiescent Current vs. Ambient Temperature.*

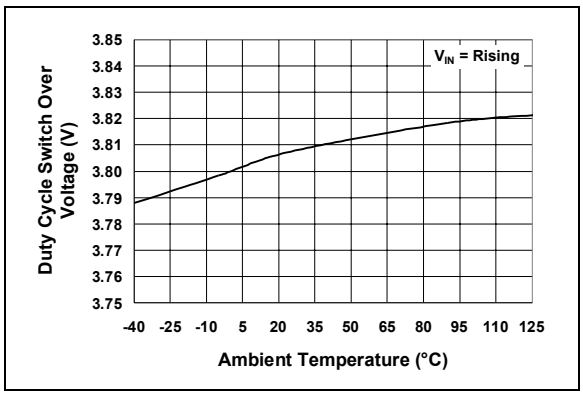


FIGURE 2-5: *Duty Cycle Switch-Over Voltage vs. Ambient Temperature.*

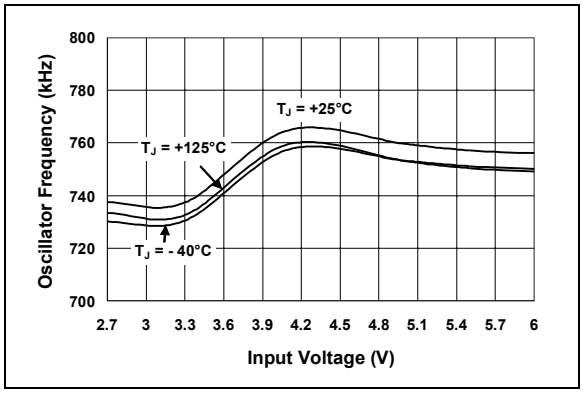


FIGURE 2-3: *Oscillator Frequency vs. Input Voltage.*

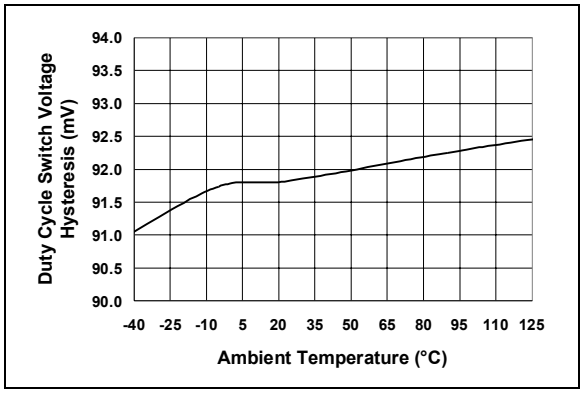


FIGURE 2-6: *Duty Cycle Switch-Over Hysteresis Voltage vs. Ambient Temperature.*

Note: Unless otherwise indicated, V_{IN} = 3.3V, VOUT = 12V, C_{IN} = 10 µF (x5R or X7R Ceramic), C_{OUT} = 10 µF (X5R or X7R), I_{OUT} = 10 mA, L = 3.3 µH, $\overline{SHDN}$ > V_{IH}, T_A = +25°C.

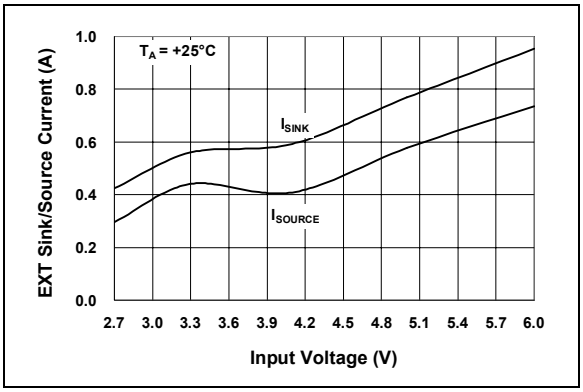


FIGURE 2-7: *EXT Sink and Source Current vs. Input Voltage.*

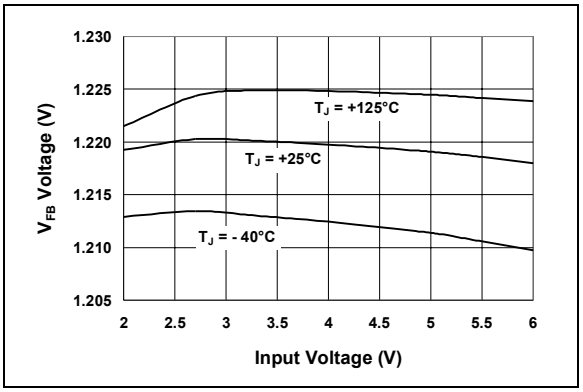


FIGURE 2-10: *Feedback Voltage vs. Input Voltage.*

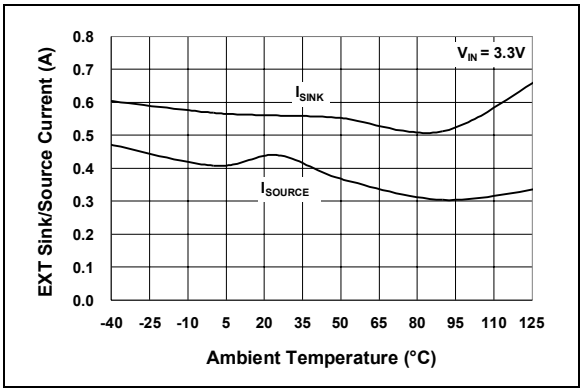


FIGURE 2-8: *EXT Sink and Source Current vs. Ambient Temperature.*

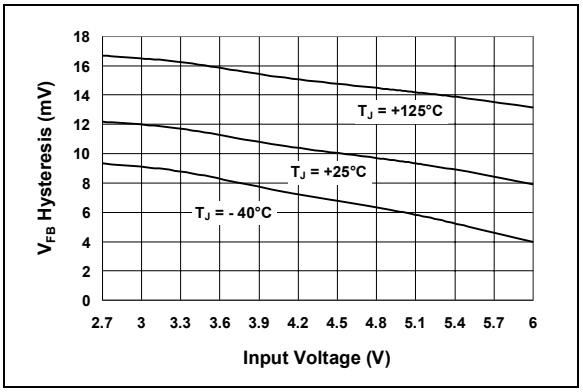


FIGURE 2-11: *Feedback Voltage Hysteresis vs. Input Voltage.*

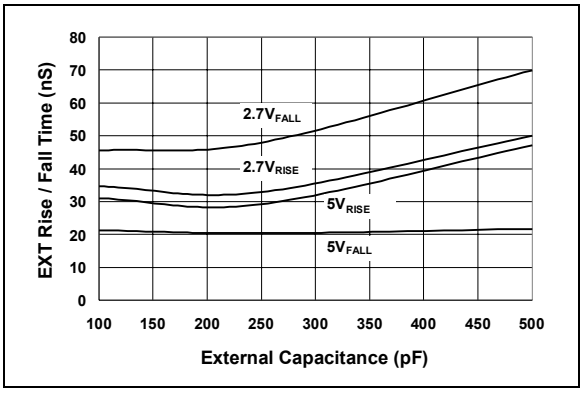


FIGURE 2-9: *EXT Rise and Fall Times vs. External Capacitance.*

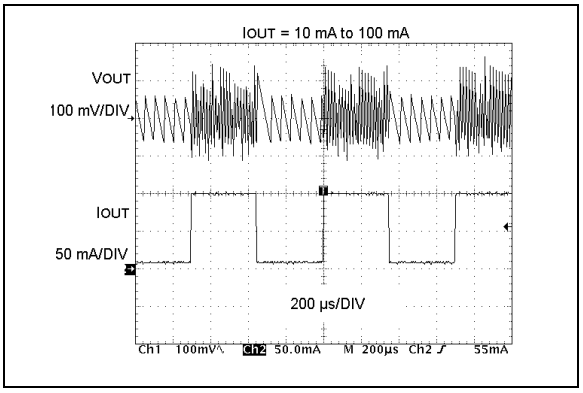


FIGURE 2-12: *Dynamic Load Response.*

Note: Unless otherwise indicated, V_{IN} = 3.3V, VOUT = 12V, C_{IN} = 10 µF (x5R or X7R Ceramic), C_{OUT} = 10 µF (X5R or X7R), I_{OUT} = 10 mA, L = 3.3 µH, $\overline{SHDN} > V_{IH}$, T_A = +25°C.

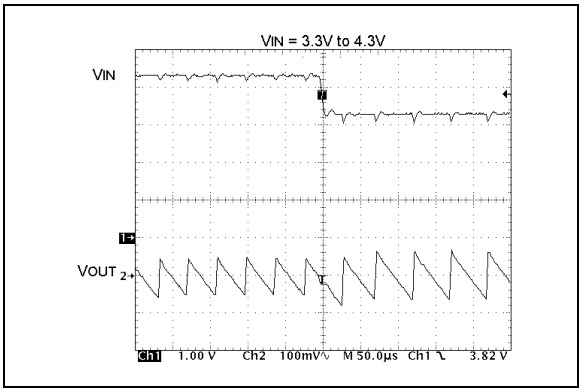


FIGURE 2-13: *Dynamic Line Response.*

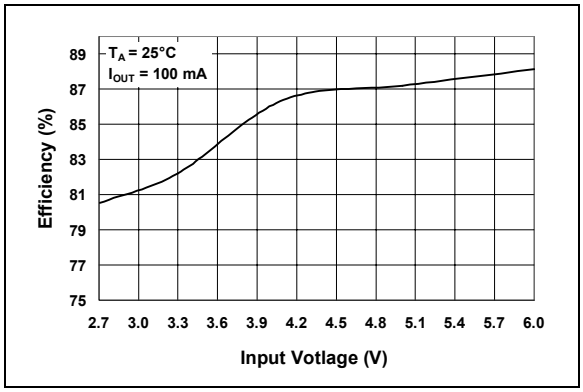


FIGURE 2-16: *Efficiency vs. Input Voltage.*

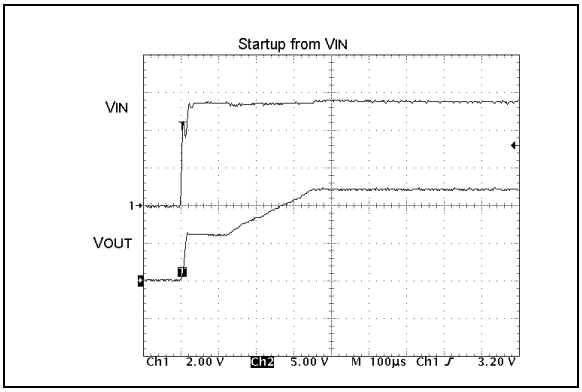


FIGURE 2-14: *Power-Up Timing (Input Voltage).*

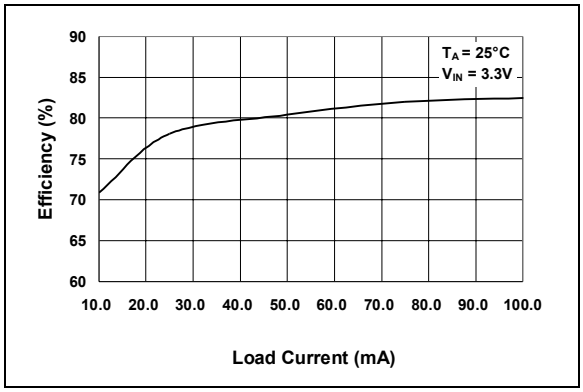


FIGURE 2-17: *Efficiency vs. Load Current.*

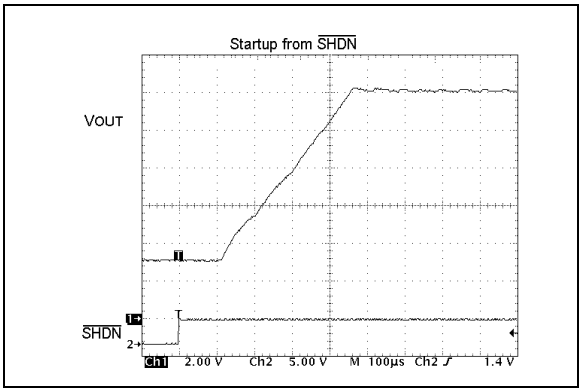


FIGURE 2-15: *Power-Up Timing (Shutdown).*

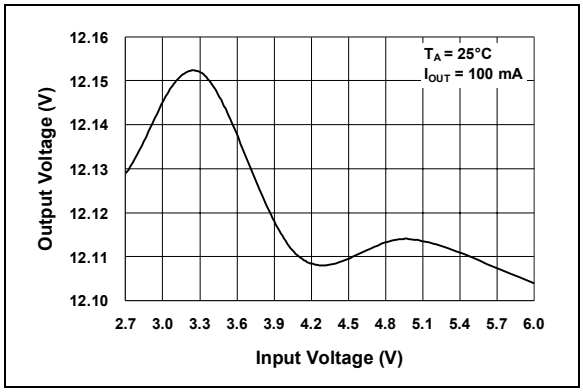


FIGURE 2-18: *Output Voltage vs. Input Voltage (Line Regulation).*

Note: Unless otherwise indicated, V_{IN} = 3.3V, VOUT = 12V, C_{IN} = 10 µF (x5R or X7R Ceramic), C_{OUT} = 10 µF (X5R or X7R), I_{OUT} = 10 mA, L = 3.3 µH, $\overline{SHDN}$ > V_{IH}, T_A = +25°C.

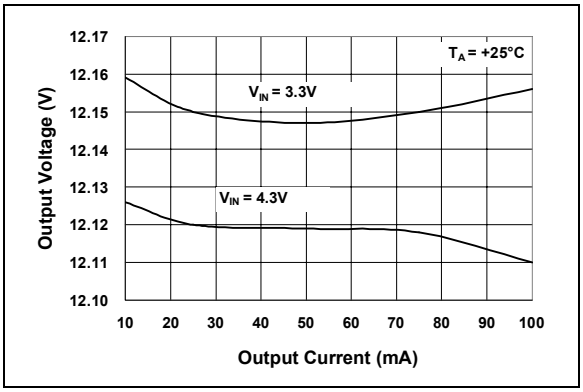


FIGURE 2-19: *Output Voltage vs. Output Current (Load Regulation).*

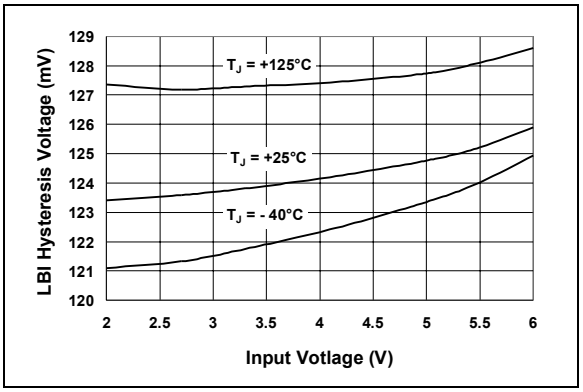


FIGURE 2-22: *LBI Hysteresis Voltage vs. Input Voltage.*

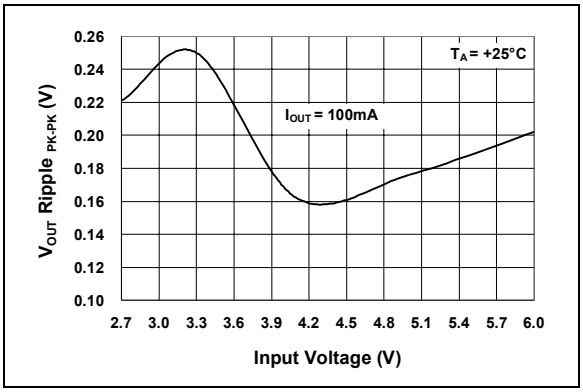


FIGURE 2-20: *Output Voltage Ripple vs. Input Voltage.*

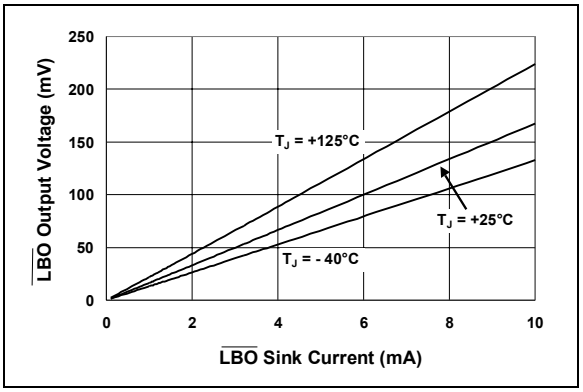


FIGURE 2-23: *$\overline{LBO}$ Output Voltage vs. $\overline{LBO}$ Sink Current.*

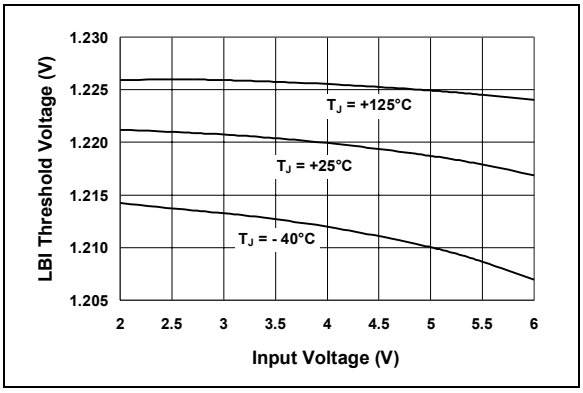


FIGURE 2-21: *LBI Threshold Voltage vs. Input Voltage.*

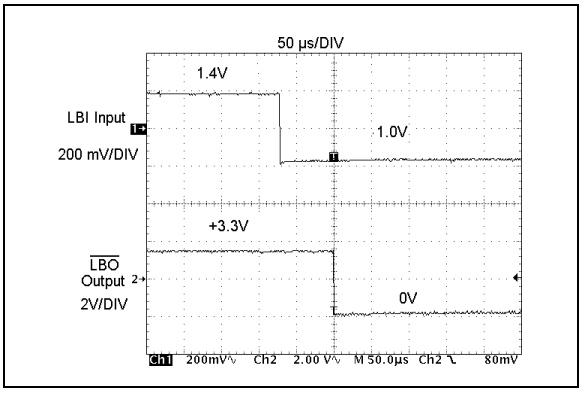


FIGURE 2-24: *$\overline{LBO}$ Output Timing.*

Note: Unless otherwise indicated, V_{IN} = 3.3V, VOUT = 12V, C_{IN} = 10 µF (x5R or X7R Ceramic), C_{OUT} = 10 µF (X5R or X7R), I_{OUT} = 10 mA, L = 3.3 µH, $\overline{SHDN}$ > V_{IH}, T_A = +25°C.

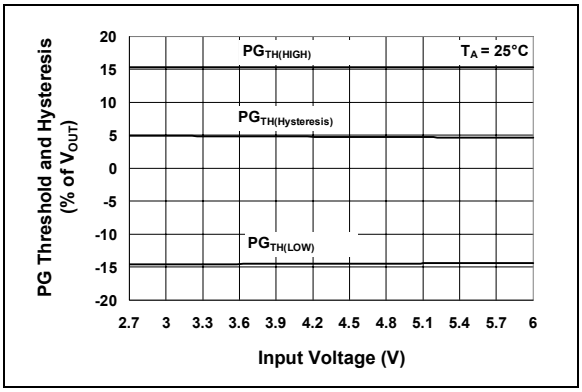


FIGURE 2-25: *PG Threshold and Hysteresis Percentage vs. Input Voltage.*

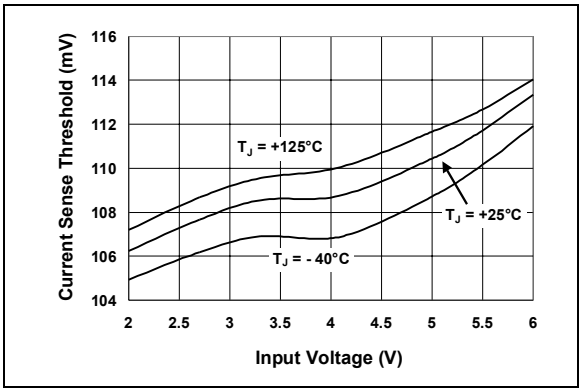


FIGURE 2-28: *Current Sense Threshold vs. Input Voltage.*

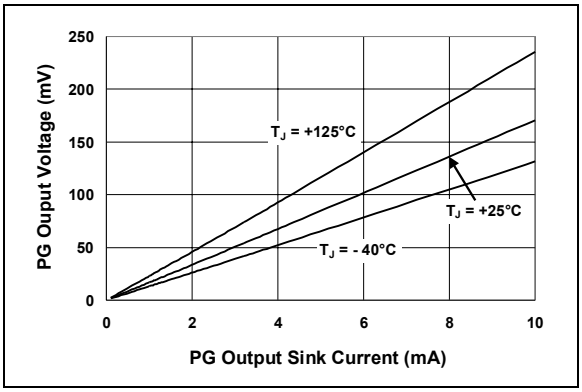


FIGURE 2-26: *PG Output Voltage vs. Sink Current.*

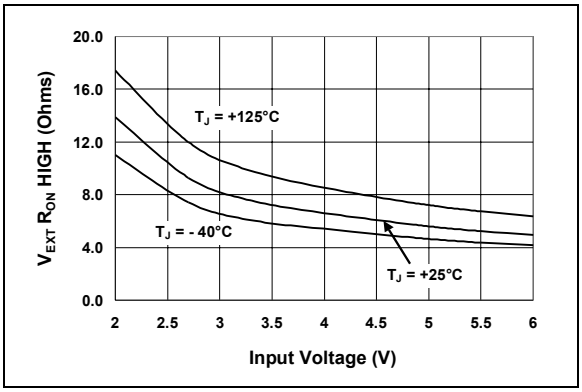


FIGURE 2-29: *V_{EXT} High Output Voltage vs. Input Voltage.*

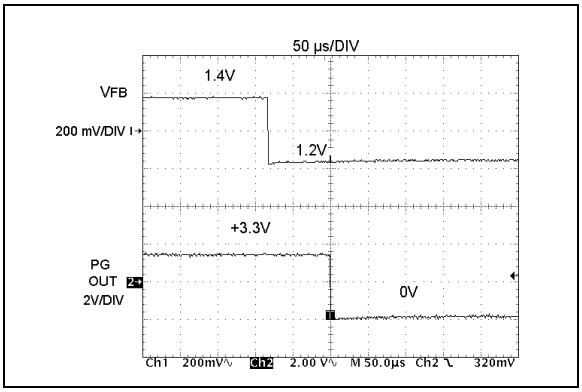


FIGURE 2-27: *PG Timing.*

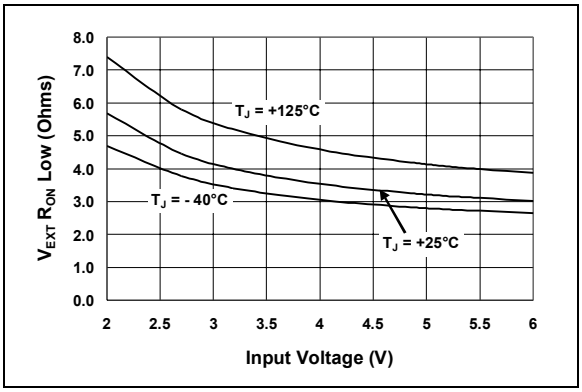


FIGURE 2-30: *V_{EXT} Low Output Voltage vs. Input Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. MCP1650	Pin No. MCP1651	Pin No. MCP1652	Pin No. MCP1653	Symbol	Function
1	1	1	1	EXT	External Gate Drive
2	2	2	2	GND	Ground
3	3	3	3	CS	Current Sense
4	4	4	4	FB	Feedback Input
5	5	5	6	$\overline{SHDN}$	Shutdown
—	6	—	7	LBI	Low Battery Input
—	7	—	8	$\overline{LBO}$	Low Battery Output
—	—	7	9	PG	Power Good Output
8	8	8	10	V_{IN}	Input Voltage

3.1 External Gate Drive (EXT)

EXT is the output pin that drives the external N-channel MOSFET on and off during boost operation. EXT is equal to GND for $\overline{SHDN}$ or UVLO conditions.

3.2 Circuit Ground (GND)

Connect the GND pin to circuit ground. See layout guidelines for suggested grounding physical layout.

3.3 Current Sense (CS)

Input peak current is sensed on CS through the external current sense resistor. When the sensed current is converted to a voltage, the current sense threshold is 122 mV below V_{IN} typical. If that threshold is exceeded, the pulse is terminated asynchronously.

3.4 Feedback Input (FB)

Connect output voltage of boost converter through external resistor divider to the FB pin for voltage regulation. The nominal voltage that is compared to this input for pulse termination is 1.22V.

3.5 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the boost converter on and off. For normal operation, tie this pin high or to V_{IN}. To turn off the device, tie this pin to low or ground.

3.6 Low Battery Input (LBI)

LBI is the input pin for the low battery comparator. When the voltage on this pin falls below the nominal 1.22V threshold setting, the $\overline{LBO}$ (Low Battery Output) open-drain is active-low.

3.7 Low Battery Output ($\overline{LBO}$)

$\overline{LBO}$ is an active-low, open-drain output capable of sinking 10 mA when the LBI pin is below the threshold voltage. $\overline{LBO}$ is high-impedance during $\overline{SHDN}$ or UVLO conditions.

3.8 Power Good (PG)

PG is an active-high, open-drain output capable of sinking 10 mA when the FB input pin is 15% below its typical value or more than 15% above its typical value, indicating that the output voltage is out of regulation. PG is high impedance during $\overline{SHDN}$ or UVLO condition.

3.9 Input Voltage (V_{IN})

V_{IN} is an input supply pin. Tie 2.7V to 5.5V input power source.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP1650/51/52/53 is a gated oscillator boost controller. By adding an external N-channel MOSFET, schottky diode and boost inductor, high-output power applications can be achieved. The 750 kHz hysteretic gated oscillator architecture enables the use of small, low-cost external components. By using a hysteretic approach, no compensation components are necessary for the stability of the regulator output.

Output voltage regulation is accomplished by comparing the output voltage (sensed through an external resistor divider) to a reference internal to the MCP1650/51/52/53. When the sensed output voltage is below the reference, the EXT pin pulses the external N-channel MOSFET on and off at the 750 kHz gated oscillator frequency. Energy is stored in the boost inductor when the external N-channel MOSFET is on and is delivered to the load through the external Schottky diode when the MOSFET is turned off. Several pulses may be required to deliver enough energy to pump the output voltage above the upper hysteretic limit. Once above the hysteretic limit, the internal oscillator is no longer gated to the EXT pin and no energy is transferred from input to output.

The peak current in the MOSFET is sensed to limit its maximum value. As with all boost topology converters, even though the MOSFET is turned off, there is still a DC path through the boost inductor and diode to the load. Additional protection circuity, such as fuses, are recommended for short circuit protection.

4.2 Input Voltage

The range of input voltage for the MCP1650/51/52/53 family of devices is specified from 2.7V to 5.5V. For the S-option devices, the undervoltage lockout (UVLO) feature will turn the boost controller off once the input voltage falls below 2.55V, typical. For the R-option devices, the UVLO is set to 2.0V. The R-option devices are recommended for use when “bootstrapping” the output voltage back to the input. The input of the MCP1650/51/52/53 device is supplied by the output voltage during boost operation. This can be used to derive output voltages from input voltages that start up at approximately 2V (2-cell alkaline batteries).

4.3 Fixed Duty Cycle

The MCP1650/51/52/53 family utilizes a unique two-step maximum duty cycle architecture to minimize input peak current and improve output ripple voltage for wide input voltage operating ranges. When the input voltage is below 3.8V, the duty cycle is typically 80%. For input voltages above 3.8V, the duty cycle is typically 56%. By decreasing the duty cycle at higher input voltages, the input peak current is reduced. For low input voltages, a longer duty cycle stores more energy during the on-time of the boost MOSFET. For applications that span the 3.8V input range, the inductor value should be selected to meet not only the minimum input voltage at 80% duty cycle, but 3.8V at 56% duty cycle as well. Refer to **Section 5.0 “Application Circuits/Issues”** for more information about selecting inductor values.

4.4 Shutdown Input Operation

The $\overline{\text{SHDN}}$ pin is used to turn the MCP1650/51/52/53 on and off. When the $\overline{\text{SHDN}}$ pin is tied low, the MCP1650/51/52/53 is off. When tied high, the MCP1650/51/52/53 will be enabled and begin boost operation as long as the input voltage is not below the UVLO threshold.

4.5 Soft-Start Operation

When power is first applied to the MCP1650/51/52/53, the internal reference initialization is controlled to slow down the start-up of the boost output voltage.This is done to reduce high inrush current required from the source. High inrush currents can cause the source voltage to drop suddenly and trip the UVLO threshold, shutting down the converter prior to it reaching steady-state operation.

4.6 Gated Oscillator Architecture

A 750 kHz internal oscillator is used as the base frequency of the MCP1650/51/52/53. The oscillator duty cycle is typically 80% when the input voltage is below a nominal value of 3.8V, and 56% when the input voltage is above a nominal value of 3.8V. Two duty cycles are provided to reduce the peak inductor current in applications where the input voltage varies over a wide range. High-peak inductor current results in undesirable high-output ripple voltages. For applications that have input voltage that cross this 3.8V boundary, both duty cycle conditions need to be examined to determine which one has the least amount of energy storage. Refer to **Section 5.0 “Application Circuits/Issues”** for more information about design considerations.

4.7 FB Pin

The output voltage is fed back through a resistor divider to the FB pin. It is then compared to an internal 1.22V reference. When the divided-down output is below the internal reference, the internal oscillator is gated on and the EXT pin pulses the external N-channel MOSFET on and off to transfer energy from the source to the load at 750 kHz. This will cause the output voltage to rise until it is above the 1.22V threshold, thereby gating the internal oscillator off. Hysteresis is provided within the comparator and is typically 12 mV. The rate at which the oscillator is gated on and off is determined by the input voltage, load current, hysteresis voltage and inductance. The output ripple voltage will vary depending on the input voltage, load current, hysteresis voltage and inductance.

4.8 PWM Latch

The gated oscillator is self-latched to prevent double and sporadic pulsing. The reset into the latch is asynchronous and can terminate the pulse during the on-time of the duty cycle. The reset can be accomplished by the feedback voltage comparator or the current limit comparator.

4.9 Peak Inductor Current

The external switch peak current is sensed on the CS pin across an optional external current sense resistor. If the CS pin falls more than 122 mV (typical) below V_{IN}, the current limit comparator is set and the pulse is terminated. This prevents the current from getting too high and damaging the N-channel MOSFET. In the event of a short circuit, the switch current will be low due to the current limit. However, there is a DC path from the input through the inductor and external diode. This is true for all boost-derived topologies and additional protection circuitry is necessary to prevent catastrophic damage.

4.10 EXT Output Driver

The EXT output pin is designed to directly drive external N-channel MOSFETs and is capable of sourcing 400 mA (typical) and sinking 800 mA (typical) for fast on and off transitions. The top side of the EXT driver is connected directly to V_{IN}, while the low side of the driver is tied to GND, providing rail-to-rail drive capability. Design flexibility is added by connecting an external resistor in series with the N-channel MOSFET to control the speed of the turn on and off. By slowing the transition speed down, there will be less high-frequency noise. Speeding the transition up produces higher efficiency.

4.11 Low Battery Detect

The Low-Battery Detect (MCP1651 and MCP1653 only) feature can be used to determine when the LBI input voltage has fallen below a predetermined threshold. The low-battery detect comparator continuously monitors the voltage on the LBI pin. When the voltage on the LBI pin is above the 1.22V + 123 mV hysteresis, the $\overline{LBO}$ pin will be high-impedance (open-drain). When in the high-impedance state, the leakage current into the $\overline{LBO}$ pin is typically less than 0.1 µA. As the voltage on the LBI pin decreases and is lower than the 1.22V typical threshold, the $\overline{LBO}$ pin will transition to a low state and is capable of sinking up to 10 mA. 123 mV of hysteresis is provided to prevent chattering of the $\overline{LBO}$ pin as a result of battery input impedance and boost input current.

4.12 Power Good Output

The Power Good Output feature (MCP1652 and MCP1653 only) monitors the divided-down voltage feedback into the FB pin. When the output voltage falls more than 15% (typical) below the regulated set point, the power good (PG) output pin will transition from a high-impedance state (open-drain) to a low state capable of sinking 10 mA. If the output voltage rises more than 15% (typical) above the regulated set point, the PG output pin will transition from high to low.

4.13 Device Protection

4.13.1 OVERCURRENT LIMIT

The Current Sense (CS) input pin is used to sense the peak input current of the boost converter. This can be used to limit how high the peak inductor current can reach. The current sense feature is optional and can be bypassed by connecting the V_{IN} input pin to the CS input pin. Because of the path from input through the boost inductor and boost diode to output, the boost topology cannot support a short circuit without additional circuitry. This is typical of all boost regulators.

5.0 APPLICATION CIRCUITS/ ISSUES

5.1 Typical Applications

The MCP1650/51/52/53 boost controller can be used in several different configurations and in many different applications. For applications that require minimum space, low cost and high efficiency, the MCP1650/51/52/53 product family is a good choice. It can be used in boost, buck-boost, Single-Ended Primary Inductive Converters (SEPIC), as well as in flyback converter topologies.

5.1.1 NON-BOOTSTRAP BOOST APPLICATIONS

Non-bootstrap applications are typically used when the output voltage is boosted to a voltage that is higher than the rated voltage of the MCP1650/51/52/53. For non-bootstrap applications, the input voltage is connected to the boost inductor through the optional current sense resistor and the V_{IN} pin of the MCP1650/51/52/53. For this type of application, the S-option devices (UVLO at 2.55V, typical) should be used. The gated oscillator duty cycle will be dependant on the value of the voltage on V_{IN}. If V_{IN} > 3.8V, the duty cycle will be 56%. If V_{IN} < 3.8V, the duty cycle will be 80%.

In non-bootstrap applications, output voltages of over 100V can be generated. Even though the MCP1650/51/52/53 device is not connected to the high boost output voltage, the drain of the external MOSFET and reverse voltage of the external Schottky diode are connected. The output voltage capacitor must also be rated for the output voltage.

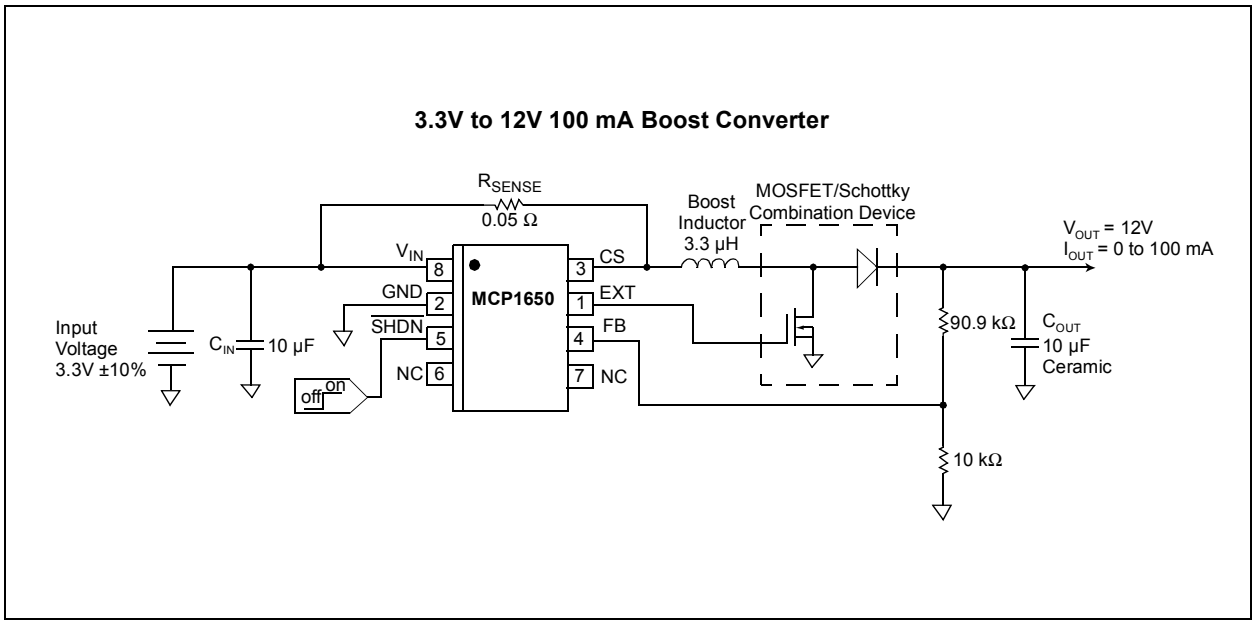


FIGURE 5-1: *Typical Non-Bootstrap Application Circuit (MCP1650/51/52/53).*

5.1.2 BOOTSTRAP BOOST APPLICATIONS

For bootstrap configurations, the higher-regulated boost output voltage is used to power the MCP1650/51/52/53. This provides a constant higher voltage used to drive the external MOSFET. The R-option devices (UVLO < 2.0V) can be used for applications that need to start up with the input voltage below 2.7V. For this type of application, the MCP1650/51/52/53 will start off of the lower 2.0V input and begin to boost the output up to its regulated value. As the output rises, so does the input voltage of the MCP1650/51/52/53. This provides a solution for 2-cell alkaline inputs for output voltages that are less than 6V.

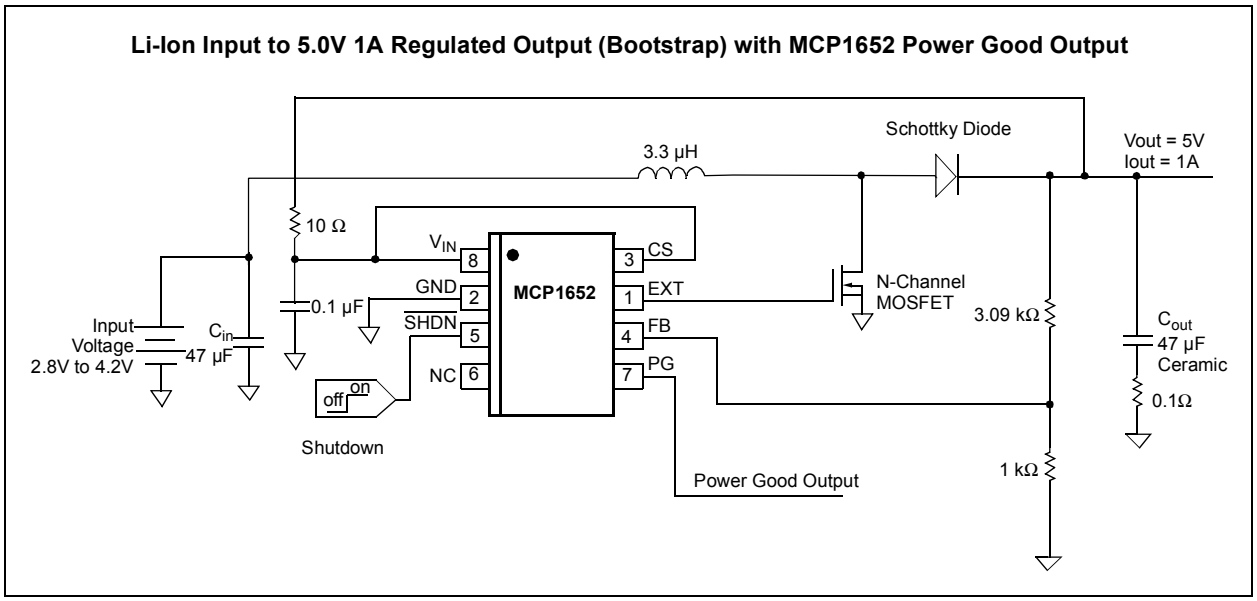


FIGURE 5-2: *Bootstrap Application Circuit MCP1650/51/52/53.*

5.1.3 SEPIC CONVERTER APPLICATIONS

In many applications, the input voltage can vary above and below the regulated output voltage. A standard boost converter cannot be used when the output voltage is below the input voltage. In this case, the MCP1650/51/52/53 can be used as a SEPIC controller. A SEPIC requires 2 inductors or a single coupled inductor, in addition to an AC coupling capacitor. As with the previous boost-converter applications, the SEPIC converter can be used in either a bootstrap or non-bootstrap configuration. The SEPIC converter can be a very popular topology for driving high-power LEDs. For many LEDs, the forward voltage drop is approximately 3.6V, which is between the maximum and minimum voltage range of a single-cell Li-Ion battery, as well as 3 alkaline or nickel metal batteries.

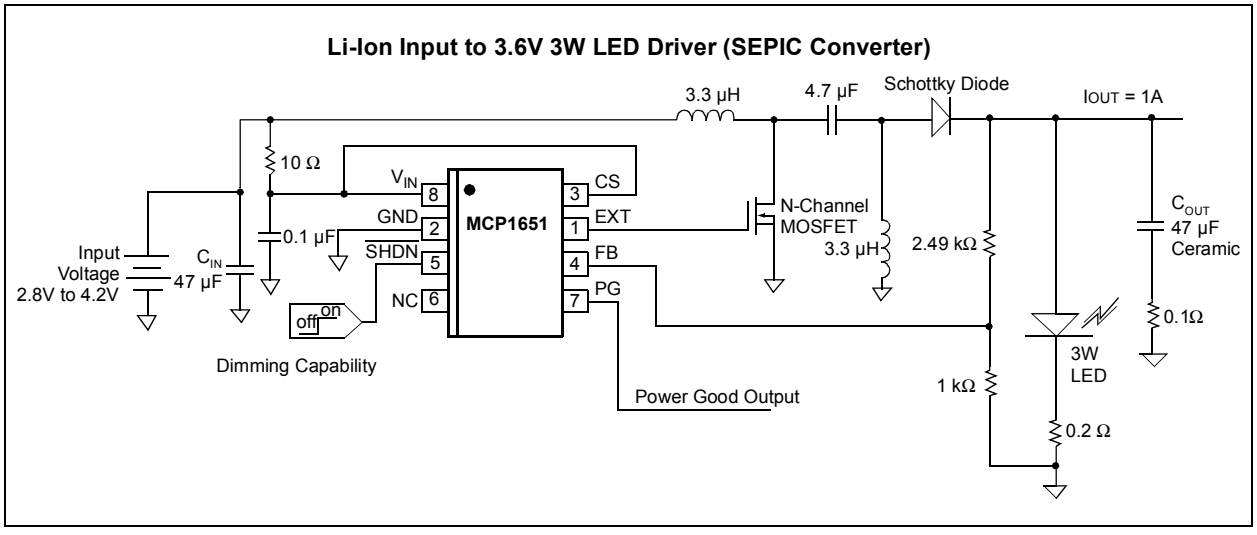


FIGURE 5-3: *SEPIC Converter Application Circuit MCP1650/51/52/53.*

5.2 Design Considerations

When developing switching power converter circuits, there are numerous things to consider and the MCP1650/51/52/53 family is no exception. The gated oscillator architecture does provide a simple control approach so that stabilizing the regulator output is an easier task than that of a fixed-frequency regulator.

The MCP1650/51/52/53 controller utilizes an external switch and diode allowing for a very wide range of conversion (high voltage gain and/or high current gain).

There are practical, as well as power-conversion, topology limitations. The MCP1650/51/52/53 gated oscillator hysteretic mode converter has similar limitations, as do fixed-frequency boost converters.

5.2.1 DESIGN EXAMPLE

Input Voltage	=	2.8V to 4.2V
Output Voltage	=	12V
Output Current	=	100 mA
Oscillator Frequency	=	750 kHz
Duty cycle	=	80% for V_{IN} < 3.8V
Duty cycle	=	56% for V_{IN} > 3.8V

Setting the output voltage:

$$R_{TOP} = R_{BOT} \times \left(\left(\frac{V_{OUT}}{V_{FB}} \right) - 1 \right)$$

Where:

R_{TOP} = Top Resistor Value
R_{BOT} = Bottom Resistor Value

By adjusting the external resistor divider, the output voltage of the boost converter can be set to the desired value. Due to the RC delay caused by the resistor divider and the device input capacitance, resistor values greater than 100 kΩ are not recommended. The feedback voltage is typically 1.22V.

For this example:

R_{BOT}	=	10 kΩ
V_{OUT}	=	12V
V_{FB}	=	1.22V
R_{TOP}	=	88.4 kΩ

90.9 KΩ was selected as the closest standard value.

5.2.1.1 Calculations

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where:

P_{OUT} = 12V X 100 mA
P_{OUT} = 1.2 Watts

$$P_{IN} = P_{OUT} / (Efficiency)$$

Where:

P_{IN} = 1.2W/80%
(80% is a good efficiency estimate)
P_{IN} = 1.5 Watts

For gated oscillator hysteretic designs, the switching frequency is not constant and will gate several pulses to raise the output voltage. Once the upper hysteresis threshold is reached, the gated pulses stop and the output will coast down at a rate determined by the output capacitor and the load. Using the gated oscillator switching frequency and duty cycle, it is possible to determine what the maximum boost ratio is for continuous inductor current operation.

$$V_{OUT} = \left(\frac{1}{1 - D} \right) \times V_{IN}$$

This relationship assumes that the output load current is significant and the boost converter is operating in Continuous Inductor Current mode. If the load is very light or a small boost inductance is used, higher boost ratio's can be achieved.

Calculate at minimum V_{IN}:

$$V_{OUTMAX} = \left(\frac{1}{1 - 0.8} \right) \times 2.8$$

The ideal maximum output voltage is 14V. The actual measured result will be less due to the forward voltage drop in the boost diode, as well as other circuit losses.

For applications where the input voltage is above and below 3.8V, another point must be checked to determine the maximum boost ratio. At 3.8V, the duty cycle changes from 80% to 56% to minimize the peak current in the inductor.

$$V_{OUTMAX} = \left(\frac{1}{1 - 0.56} \right) \times 3.8$$

For this case, V_{OUTMAX} = 8.63V less than the required 12V output specified. The size of the inductor has to decrease in order to operate the boost regulator in Discontinuous Inductor Current mode.

To determine the maximum inductance for Discontinuous Operating mode, multiply the energy going into the inductor every switching cycle by the number of cycles per second (switching frequency). This number must be greater than the maximum input power.

The equation for the energy flowing into the inductor is given below. The input power to the system is equal to energy times time.

$$Energy = \frac{1}{2} \times L \times I_{PK}^2$$

The inductor peak current is calculated using the equation below:

$$I_{PK} = \frac{V_{IN}}{L} \times T_{ON}$$

Using a typical inductance of 3.3 µH, the peak current in the inductor is calculated below:

F_{SW} = 750 kHz
T_{ON} = ($1/F_{SW}$ * Duty Cycle)
I_{PK} (2.8V) = 905 mA
Energy (2.8V) = 1.35 µ-Joules
Power (2.8V) = 1.01 Watts

At 3.8V and below, the converter can boost to 14V while operating in the Continuous mode.

I_{PK} (3.8V) = 860 mA
Energy at 3.8V = 1.22 µ-Joules
Power = 0.914 Watts

For this example, a 3.3 µH inductor is too large, a 2.2 µH inductor is selected.

F_{SW} = 750 kHz
T_{ON} = ($1/F_{SW}$ * Duty Cycle)
I_{PK} (2.8V) = 1.36A
Energy (2.8V) = 2.02 µ-Joules
Power (2.8V) = 1.52 Watts
I_{PK}(3.8V) = 1.29A
Energy at 3.8V = 1.83 µ-Joules
Power = 1.4 Watts

As the inductance is lowered, the peak current drawn from the input at all loads is increased. The best choice of inductance for high boost ratios is the maximum inductance value necessary while maintaining discontinuous operation.

For lower boost-ratio applications (3.3V to 5.0V), a 3.3 µH inductor or larger is recommended. In these cases, the inductor operates in Continuous Current mode.

5.2.2 MOSFET SELECTION

There are a couple of key consideration's when selecting the proper MOSFET for the boost design. A low R_{DSON} logic-level N-channel MOSFET is recommended.

5.2.2.1 MOSFET Selection Process.

1. Voltage Rating - The MOSFET drain-to-source voltage must be rated for a minimum of V_{OUT} + V_{FD} of the external boost diode. For example, in the 12V output converter, a MOSFET drain-to-source voltage rating of 12V + 0.5V is necessary. Typically, a 20V part can be used for 12V outputs.
2. Logic-Level R_{DSON} - The MOSFET carries significant current during the boost cycle on time. During this time, the peak current in the MOSFET can get quite high. In this example, a SOT-23 MOSFET was used with the following ratings:

IRLM2502 N-channel MOSFET

V_{BDS} = 20V (Drain Source Breakdown Voltage)
R_{DSON} = 50 milli-ohms (V_{GS} = 2.5V)
R_{DSON} = 35 milli-ohms (V_{GS} = 5.0V)
Q_G = Total Gate Charge = 8 nC
V_{GS} = 0.6V to 1.2V (Gate Source Threshold Voltage)

Selecting MOSFETs with lower R_{DSON} is not always better or more efficient. Lower R_{DSON} typically results in higher total gate charge and input capacitance, slowing the transition time of the MOSFET and resulting in increased switching losses.

5.2.3 DIODE SELECTION

The external boost diode also switches on and off at the switching frequency and requires very fast turn-on and turn-off times. For most applications, Schottky diodes are recommended. The voltage rating of the Schottky diode must be rated for maximum boost output voltage. For example, 12V output boost converter, the diode should be rated for 12V plus margin. A 20V or 30V Schottky diode is recommended for a 12V output application. Schottky diodes also have low forward-drop characteristics, another desired feature for switching power supply applications.

5.2.4 INPUT/OUTPUT CAPACITOR SELECTION

There are no special requirements on the input or output capacitor. For most applications, ceramic capacitors or low effective series resistance (ESR) tantalum capacitors will provide lower output ripple voltage than aluminum electrolytic. Care must be taken not to exceed the manufacturer's rated voltage or ripple current specifications. Low-value capacitors are desired because of cost and size, but typically result in higher output ripple voltage.

The input capacitor size is dependant on the source impedance of the application. The hysteretic architecture of the MCP1650/51/52/53 boost converter can draw relatively high input current peaks at certain line and load conditions. Small input capacitors can produce a large ripple voltage at the input of the converter, resulting in unsatisfactory performance.

The output capacitor plays a very important role in the performance of the hysteretic gated oscillator converter. In some cases, using ceramic capacitors can result in higher output ripple voltage. This is a result of the low ESR that ceramic capacitors exhibit. As shown in the application schematics, 100 milli-ohms of ESR in series with the ceramic capacitor will actually reduce the output ripple voltage and peak input currents for some applications. The selection of the capacitor and ESR will largely determine the output ripple voltage.

5.2.5 LOW BATTERY DETECTION

For low battery detection, the MCP1651 or MCP1653 device should be used. The low-battery detect feature compares the low battery input (LBI) pin to the internal 1.22V reference. If the LBI input is below the LBI threshold voltage, the low battery output ($\overline{LBO}$) pin will sink current (up to 10 mA) through the internal open-drain MOSFET. If the LBI input voltage is above the LBI threshold, the $\overline{LBO}$ output pin will be open or high impedance.

5.2.6 POWER GOOD OUTPUT

For power good detection, the MCP1652 or MCP1653 device is ideal. The power good feature compares the voltage on FB pin to the internal reference (±15%). If the FB pin is more than 15% above or below the power good threshold, the PG output will sink current through the internal open-drain MOSFET. If the output of the regulator is within ±15% of the output voltage, the PG pin will be open or high-impedance.

5.2.7 EXTERNAL COMPONENT MANUFACTURES

Inductors:

Sumida® Corporation	http://www.sumida.com/
Coilcraft®	http://www.coilcraft.com
BH Electronics®	http://www.bhelectronics.com
Pulse Engineering®	http://www.pulseeng.com/
Coiltronics®	http://www.cooperet.com/

Capacitors

MuRata®	http://www.murata.com/
Kemet®	http://www.kemet.com/
Taiyo-Yuden	http://www.taiyo-yuden.com/
AVX®	http://www.avx.com/

MOSFETs and Diodes:

International Rectifier	http://www.irf.com/
Vishay®/Siliconix	http://www.vishay.com/company/brands/siliconix/
ON Semiconductor®	http://www.onsemi.com/
Fairchild Semiconductor®	http://www.fairchildsemi.com/

6.0 TYPICAL LAYOUT

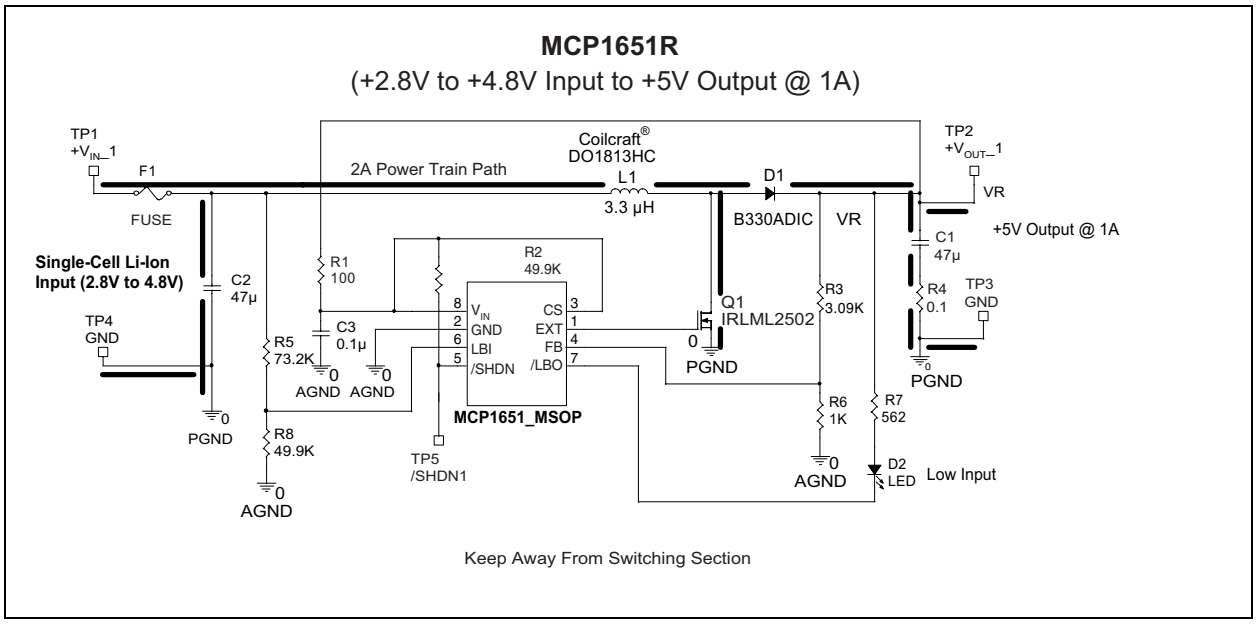


FIGURE 6-1: *MCP1650/51/52/53 Application Schematic.*

When designing the physical layout for the MCP1650/51/52/53, the highest priority should be placing the boost power train components in order to minimize the size of the high current paths. It is also important to provide ground-path separation between the large-signal power train ground and the small signal feedback path and feature grounds. In some cases, additional filtering on the V_{IN} pin is helpful to minimize MCP1650/51/52/53 input noise.

In this layout example, the critical power train paths are from input to output, $+V_{IN}$–1 to F_1 to C_2 to L_1 to Q_1 to GND. Current will flow in this path when the switch (Q_1) is turned on. When Q_1 is turned off, the path for current flow will quickly change to $+V_{IN}$–1 to F_1 to L_1 to D_1 to C_1 to R4 to GND. When starting the layout for this application, both of these power train paths should be as short as possible. The C_2, Q_1 and R_4 GND connections should all be connected to a single “Power Ground” plane to minimize any wiring inductance.

Bold traces are used to represent high-current connections and should be made as wide as is practical.

R_1 and C_3 is an optional filter that reduces the switching noise on the V_{IN} pin of the MCP1650/51/52/53. This should be considered for high-power applications (> 1W) and bootstrap applications where V_{IN} of the MCP1650/51/52/53 is supplied by the output voltage of the boost regulator.

The feedback resistor divider that sets the output voltage should be considered sensitive and be routed away from the power-switching components discussed previously.

As shown in the diagram, R_6, R_8 and the GND pin of the MCP1650/51/52/53 should be returned to an analog ground plane.

The analog ground plane and power ground plane should be connected at a single point close to the input capacitor (C_2).

Figure 6-2 represents the top wiring for the MCP1650/51/52/53 application shown.

As shown in Figure 6-2, the high-current wiring is short and wide. In this example, a 1 oz. copper layer is used for both the top and bottom layers. The ground plane connected to C2 and R4 are connected through the vias (holes) connecting the top and bottom layer. The feedback signal (from TP2) is wired from the output of the regulator around the high current switching section to the feedback voltage divider and to the FB pin of the MCP1650/51/52/53.

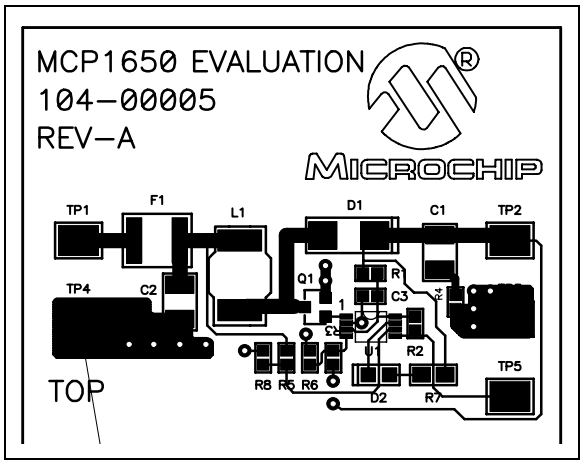


FIGURE 6-2: *Top Layer Wiring.*

Figure 6-3 represents the bottom wiring for the MCP1650/51/52/53 application shown.

Silk-screen reference designator labels are transparent from the top of the board. The analog ground plane and power ground plane are connected near the ground connection of the input capacitor (C_2). This prevents high-power, ground-circulating currents from flowing through the analog ground plane.

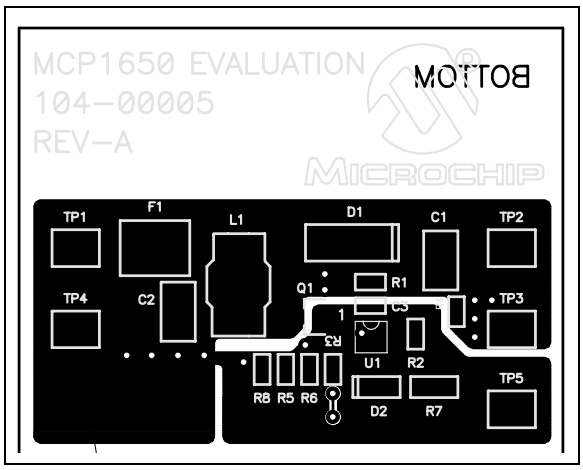
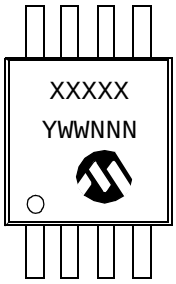


FIGURE 6-3: *Bottom Layer Wiring.*

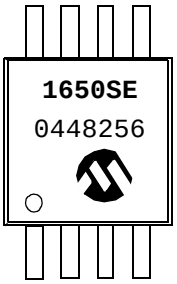
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

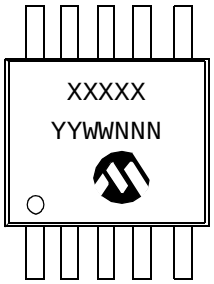
8-Lead MSOP (**MCP1650, MCP1651, MCP1652**)



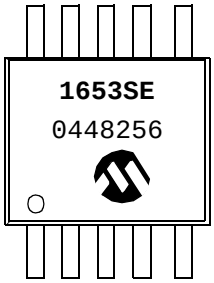
Example:



10-Lead MSOP (**MCP1653**)



Example:

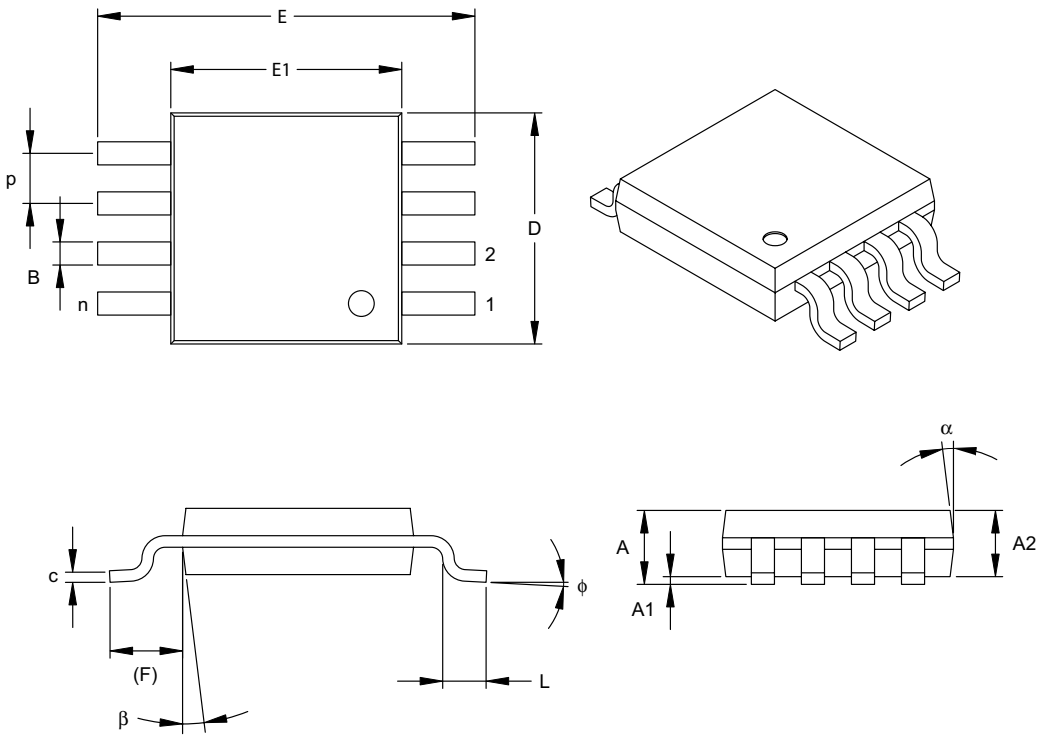


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

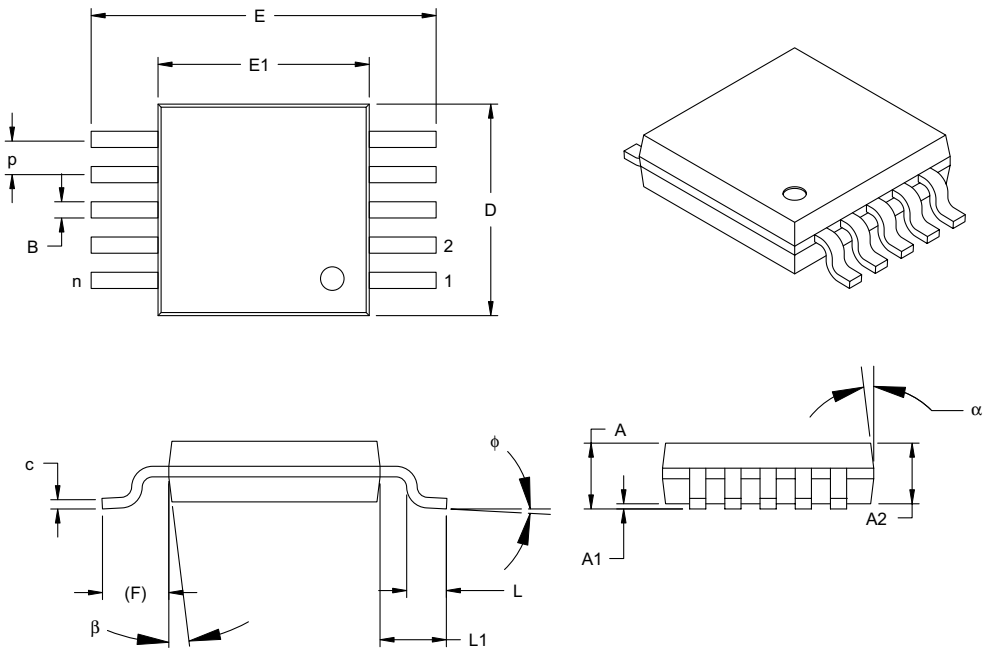
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

10-Lead Plastic Micro Small Outline Package (UN) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		10			10	
Pitch	p		.020 TYP			0.50 TYP.	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 BSC			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	-	.009	0.08	-	0.23
Lead Width	B	.006	.009	.012	0.15	0.23	0.30
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-021

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	XX
Device	UVLO Options	Temperature Range	Package

Device	MCP1650:	750 kHz Boost Controller
	MCP1651:	750 kHz Boost Controller
	MCP1652:	750 kHz Boost Controller
	MCP1653:	750 kHz Boost Controller
UVLO Options	R =	2.0V
	S =	2.55V
Temperature Range	E =	-40°C to +125°C
Package	MS =	Plastic Micro Small Outline (MSOP), 8-lead
	UN =	Plastic Micro Small Outline (MSOP), 10-lead

Examples:

a)	MCP1650R-E/MS:	2.0V Option
b)	MCP1650RT-E/MS:	2.0V Option, Tape and Reel
c)	MCP1650S-E/MS:	2.55V Option
d)	MCP1650ST-E/MS:	2.55V Option, Tape and Reel
a)	MCP1651R-E/MS:	2.0V Option
b)	MCP1651RT-E/MS:	2.0V Option, Tape and Reel
c)	MCP1651S-E/MS:	2.55V Option
d)	MCP1651ST-E/MS:	2.55V Option, Tape and Reel
a)	MCP1652R-E/MS:	2.0V Option
b)	MCP1652RT-E/MS:	2.0V Option, Tape and Reel
c)	MCP1652S-E/MS:	2.55V Option
d)	MCP1652ST-E/MS:	2.55V Option, Tape and Reel
a)	MCP1653R-E/UN:	2.0V Option
b)	MCP1653RT-E/UN:	2.0V Option, Tape and Reel
c)	MCP1653S-E/UN:	2.55V Option
d)	MCP1653ST-E/UN:	2.55V Option, Tape and Reel

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company’s quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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