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Absolute Maximum Ratings (Note 1)

AVDD to EP .....-0.5V to +3.9V
DVDD to EP .....-0.5V to +3.9V
IOVDD to EP .....-0.5V to +3.9V
IN+, IN- to EP .....-0.5V to +1.9V
All Other Pins to EP .....-0.5V to (V_{IOVDD} + 0.5V)
IN+, IN- Short Circuit to Ground or Supply .....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN/SWTQFN
(derate 47.6mW/°C above +70°C) 3809.5mW
Junction Temperature .....+150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN/SWTQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (ADD_, HIM, I2CSEL, GPI, $\overline{PWDN}$, MS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (BWS, CX/TP)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		10	µA
Input Current	I_{IN}			-150		150	µA
SINGLE-ENDED OUTPUTS (WS, SCK, SD, DOUT_, CNTL_, INTOUT, PCLKOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = '0'	V_{IOVDD} - 0.3			V
			DCS = '1'	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = '0'			0.3	V
			DCS = '1'			0.2	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
OUTPUT Short-Circuit Current	I_{OS}	DOUT_	V_O = 0V, DCS = '0'	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, DCS = '1'	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, DCS = '0'	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, DCS = '1'	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
OPEN-DRAIN INPUTS/OUTPUTS (GPIO0, GPIO1, RX/SDA, TX/SCL, $\overline{ERR}$, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL		-100		+5	µA
			LOCK, $\overline{ERR}$, GPIO_		-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)					10	pF
OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage (V_{IN}+) - (V_{IN}-)	V_{RODH}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode		30		60	mV
			High-immunity mode		50		100	
Differential Low Output Peak Voltage (V_{IN}+) - (V_{IN}-)	V_{RODL}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode		-60		-30	mV
			High-immunity mode		-100		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	Legacy reverse control-channel mode		30		60	mV
			High-immunity mode		50		100	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	Legacy reverse control-channel mode		-60		-30	mV
			High-immunity mode		-100		-50	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak) Voltage (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)				60	mV
			Activity detector low Threshold, (0x0B D[6:5] = 00)				47.5	
Differential Low Input Threshold (Peak) Voltage (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)		-60			mV
			Activity detector medium Threshold, (0x0B D[6:5] = 00)		-47.5			
Input Common-Mode Voltage ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_{IN}				80	100	130	Ω
SINGLE-ENDED INPUTS (IN+, IN-)								
Single-Ended High Input Threshold (Peak) Voltage (Figure 3)	$V_{ISH(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)					43	mV
		Activity detector low threshold, (0x0B D[6:5] = 00)					33	
Single-Ended Low Input Threshold (Peak) Voltage (Figure 3)	$V_{ISL(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)			-43			mV
		Activity detector medium threshold, (0x0B D[6:5] = 00)			-33			
Input Resistance (Internal)	R_I				40	50	65	Ω
POWER SUPPLY								
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 4)	I_{WCS}	BWS = low, $f_{PCLKOUT}$ = 16.6MHz	2% spread active	C_L = 5pF		131	164	mA
				C_L = 10pF		136	169	
			Spread spectrum disabled	C_L = 5pF		122	153	
				C_L = 10pF		127	158	
		BWS = low, $f_{PCLKOUT}$ = 33.3MHz	2% spread active	C_L = 5pF		144	179	
				C_L = 10pF		153	189	
			Spread spectrum disabled	C_L = 5pF		133	167	
				C_L = 10pF		142	177	
		BWS = low, $f_{PCLKOUT}$ = 66.6MHz	2% spread active	C_L = 5pF		175	216	
				C_L = 10pF		190	233	
			Spread spectrum disabled	C_L = 5pF		159	197	
				C_L = 10pF		174	214	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 4)	I_{WCS}	BWS = low, $f_{PCLKOUT}$ = 104MHz	2% spread active	C_L = 5pF		212	255	mA
				C_L = 10pF		234	278	
			Spread spectrum disabled	C_L = 5pF		190	228	
				C_L = 10pF		212	251	
		BWS = mid, $f_{PCLKOUT}$ = 36.6MHz	2% spread active	C_L = 5pF		154	191	
				C_L = 10pF		164	203	
			Spread spectrum disabled	C_L = 5pF		143	177	
				C_L = 10pF		154	189	
		BWS = mid, $f_{PCLKOUT}$ = 104MHz	2% spread active	C_L = 5pF		231	277	
				C_L = 10pF		257	305	
			Spread spectrum disabled	C_L = 5pF		209	249	
				C_L = 10pF		234	277	
Sleep Mode Supply Current	I_{CCS}					70	265	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = GND				20	195	µA
ESD PROTECTION								
IN+, IN- (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF				±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF		Contact discharge		±10		
				Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF		Contact discharge		±10		
				Air discharge		±20		
All Other Pins (Note 9)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF				±4		kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)								
Clock Frequency	$f_{PCLKOUT}$	BWS = low, DRS = '1'			8.33		16.66	MHz
		BWS = low, DRS = '0'			16.66		104	
		BWS = mid, DRS = '1'			18.33		36.66	
		BWS = mid, DRS = '0'			36.66		104	
		BWS = high, DRS = '1'			6.25		12.5	
		BWS = high, DRS = '0'			12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Note 6)			40	50	60	%
Clock Jitter	t_J	Period jitter, peak-to-peak, spread off, 3.12Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$ (Note 6)				0.05		UI
I^2C/UART PORT TIMING								
I^2C/UART Bit Rate					9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}			20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}			20		150	ns
I^2C TIMING (Figure 5)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			ns
			Mid		100			
			High		50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 12)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 13)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_b						100	pF
SWITCHING CHARACTERISTICS								
PCLKOUT Rise-and-Fall Time (Note 6, Figure 6)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	DCS = '1', C_L = 10pF		0.4		2.2	ns
			DCS = '0', C_L = 5pF		0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	DCS = '1', C_L = 10pF		0.25		1.8	
			DCS = '0', C_L = 5pF		0.3		2.0	
Parallel Data Rise-and-Fall Time (Note 6, Figure 7)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	DCS = '1', C_L = 10pF		0.5		3.1	ns
			DCS = '0', C_L = 5pF		0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	DCS = '1', C_L = 10pF		0.3		2.2	
			DCS = '0', C_L = 5pF		0.4		2.4	

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deserializer Delay	t_{SD}	Figure 8 (Notes 6, 14)	Spread spectrum enabled			6960	Bits
			Spread spectrum disabled			2160	
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission, Figure 1 (Note 6)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission, Figure 1 (Note 6)		180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), Figure 9				350	µs
Lock Time	t_{LOCK}	(Figure 10)	Spread spectrum enabled			3	ms
			Spread spectrum disabled			2	
Power-Up Time	t_{PU}	(Figure 11)				8	ms
I^2S/TDM OUTPUT TIMING (Note 6)							
WS Jitter	tj_{WS}	t_{WS} = 1/f_{WS}, (cycle-to-cycle), rising-to-falling edge or falling-to-rising edge	f_{WS} = 48kHz or 44.1kHz		1.2e-3 x t_{WS}	1.5e-3 x t_{WS}	ns
			f_{WS} = 96kHz		1.6e-3 x t_{WS}	2e-3 x t_{WS}	
			f_{WS} = 192kHz		1.6e-3 x t_{WS}	2e-3 x t_{WS}	
SCK Jitter (2-Channel I^2S)	tj_{SCK1}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13e-3 x t_{SCK}	16e-3 x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		39e-3 x t_{SCK}	48e-3 x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
SCK Jitter (8-Channel TDM)	tj_{SCK2}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{WS} = 48kHz or 44.1kHz		52e-3 x t_{SCK}	64e-3 x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		156e-3 x t_{SCK}	192e-3 x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.4 x t_{SCK}	0.52 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	C_L = 10pF, DCS = 1	0.3		3.1	ns
			C_L = 5pF, DCS = 0	0.4		3.8	

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SD, WS Valid Time Before SCK (2-Channel I²S)	t_{DVB1}	t_{SCK} = 1/f_{SCK} (Figure 12)	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (2-Channel I²S)	t_{DVA1}	t_{SCK} = 1/f_{SCK} (Figure 12)	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time Before SCK (8-Channel TDM)	t_{DVB2}	t_{SCK} = 1/f_{SCK} (Figure 12)	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (8-Channel TDM)	t_{DVA2}	t_{SCK} = 1/f_{SCK} (Figure 12)	0.20 x t_{SCK}	0.5 x t_{SCK}		ns

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: Not production tested. Guaranteed by design.

Note 7: HDCP not enabled (MAX9280A only). IOVDD current is not production tested. See Table 23 for additional supply current when HDCP is enabled

Note 8: Specified pin to ground.

Note 9: Specified pin to all supply/ground.

Note 10: Not production tested, guaranteed by bench characterization.

Note 11: The I²C bus standard t_{LOW} (min) = 0.5µs.

Note 12: The I²C bus standard $t_{VD:DAT}$ (max) = 0.45µs.

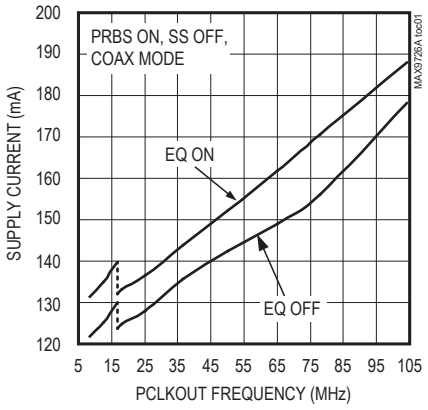
Note 13:. The I²C bus standard $t_{VD:ACK}$ (max) = 0.45µs.

Note 14: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = '1'.

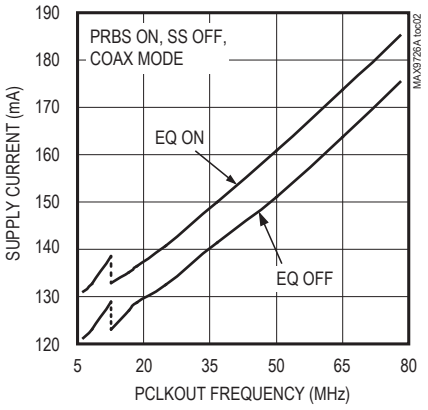
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

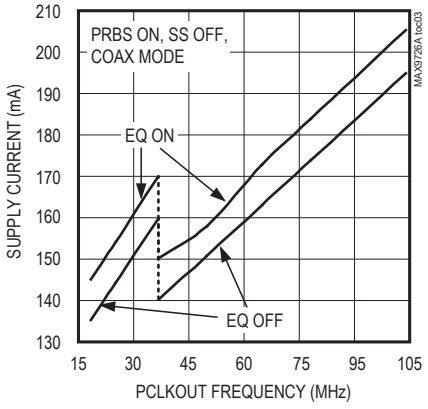
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



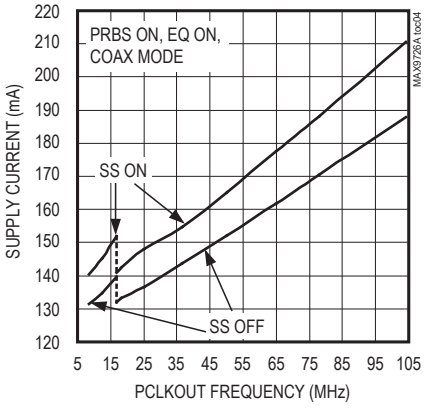
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



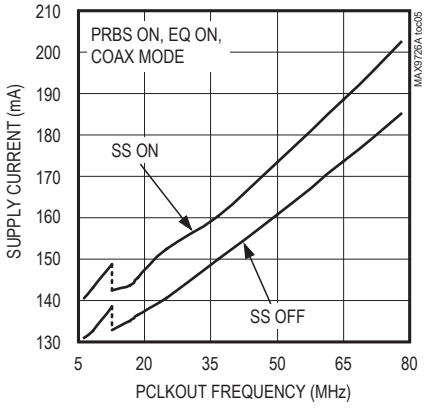
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = OPEN)



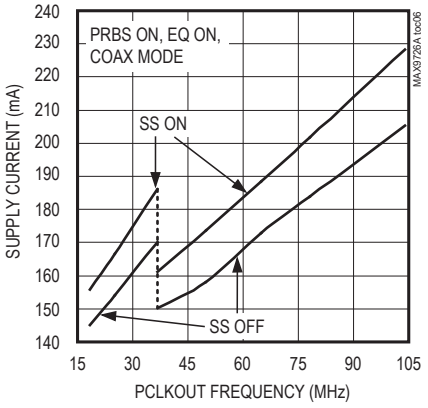
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



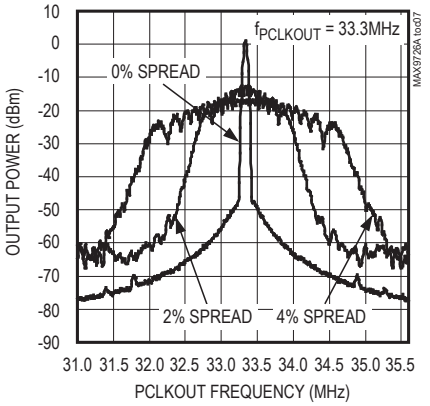
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = OPEN)



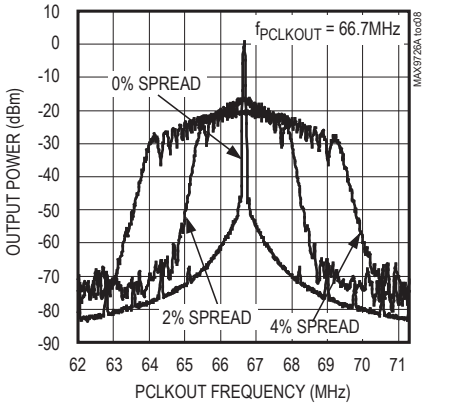
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

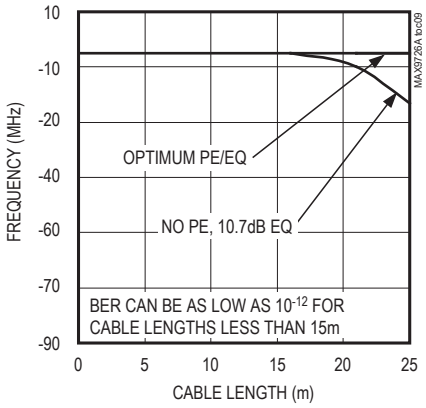
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



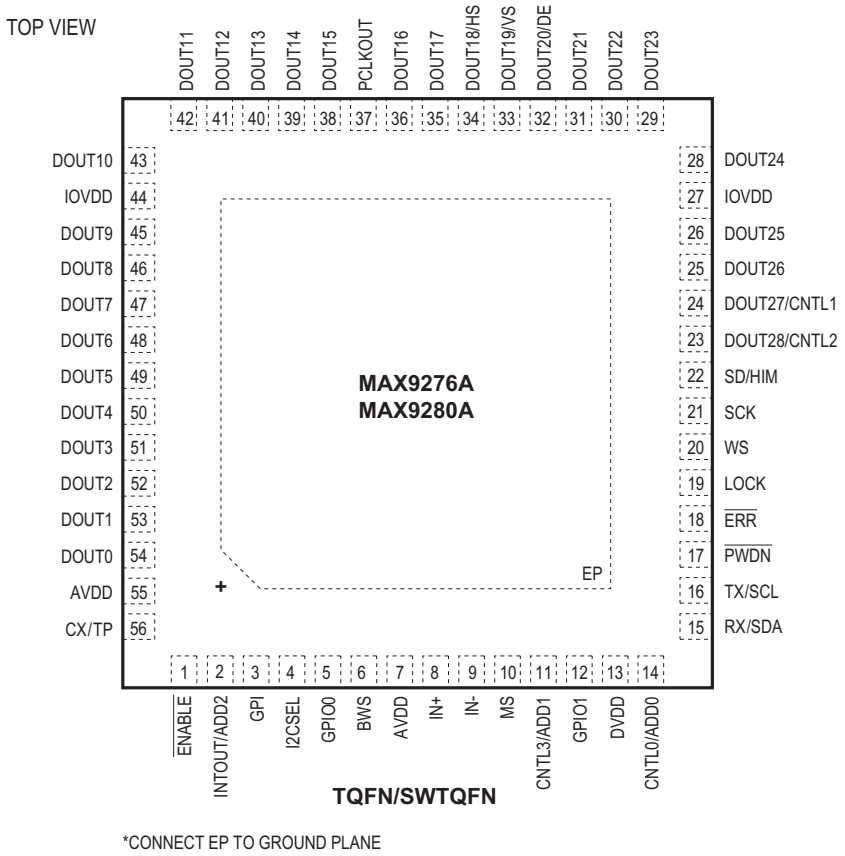
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



MAXIMUM PCLKOUT FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Active-Low Parallel Output-Enable Input With Internal Pulldown to EP. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT DOUT_ and CNTL_ outputs. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, DOUT_ and CNTL_ into high impedance.
2	INTOUT/ADD2	A/V Status Register Interrupt Output/Address Selection Input With Internal Pulldown to EP. Functions as ADD2 input at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to INTOUT output automatically after power-up. ADD2: Bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1. Connect INTOUT/ADD2 to IOVDD with a 30kΩ resistor to set high or leave open to set low. INTOUT: Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
3	GPI	General-Purpose Input With Internal Pulldown to EP. The serializer GPO (or INT) output follows GPI.
4	I2CSEL	I^2C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C interface. Set I2CSEL = low to select UART interface.
5	GPIO0	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD

Pin Description (continued)

PIN	NAME	FUNCTION
6	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low, with 6kΩ (max) pulldown for 24-bit mode. Set BWS = high, with 6kΩ (max) pullup to IOVDD for 32-bit mode. Set BWS = open for high-bandwidth mode.
7, 55	AVDD	3.3V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
8	IN+	Noninverting Coax/Twisted-Pair Serial Input
9	IN-	Inverting Coax/Twisted-Pair Serial Input
10	MS	Mode Select with Internal Pulldown to EP. Set MS = low, to select base mode. Set MS = high to select the bypass mode.
11	CNTL3/ADD1	Auxiliary Control Signal Output/Address Selection Input with Internal Pulldown to EP. Functions as ADD1 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL3 output automatically after power-up. ADD1: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect CNTL3/ADD1 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL3: Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9280A only).
12	GPIO1	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD
13	DVDD	3.3V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
14	CNTL0/ADD0	Auxiliary Control Signal Output/Address Selection Input with Internal Pulldown to EP. Functions as ADD0 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL0 output automatically after power-up. ADD0: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect CNTL0/ADD0 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL0: Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9280A only).
15	RX/SDA	UART Receive/I^2C Serial-Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I^2C Master/Slave.
16	TX/SCL	UART Transmit/I^2C Serial-Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I^2C Master/Slave.
17	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
18	$\overline{ERR}$	Error Output. Open-drain data error detection and/or correction indication output with internal 30kΩ pullup to IOVDD. $\overline{ERR}$ is high when $\overline{PWDN}$ is low
19	LOCK	Open-Drain Lock Output with Internal 30kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{PWDN}$ = low.

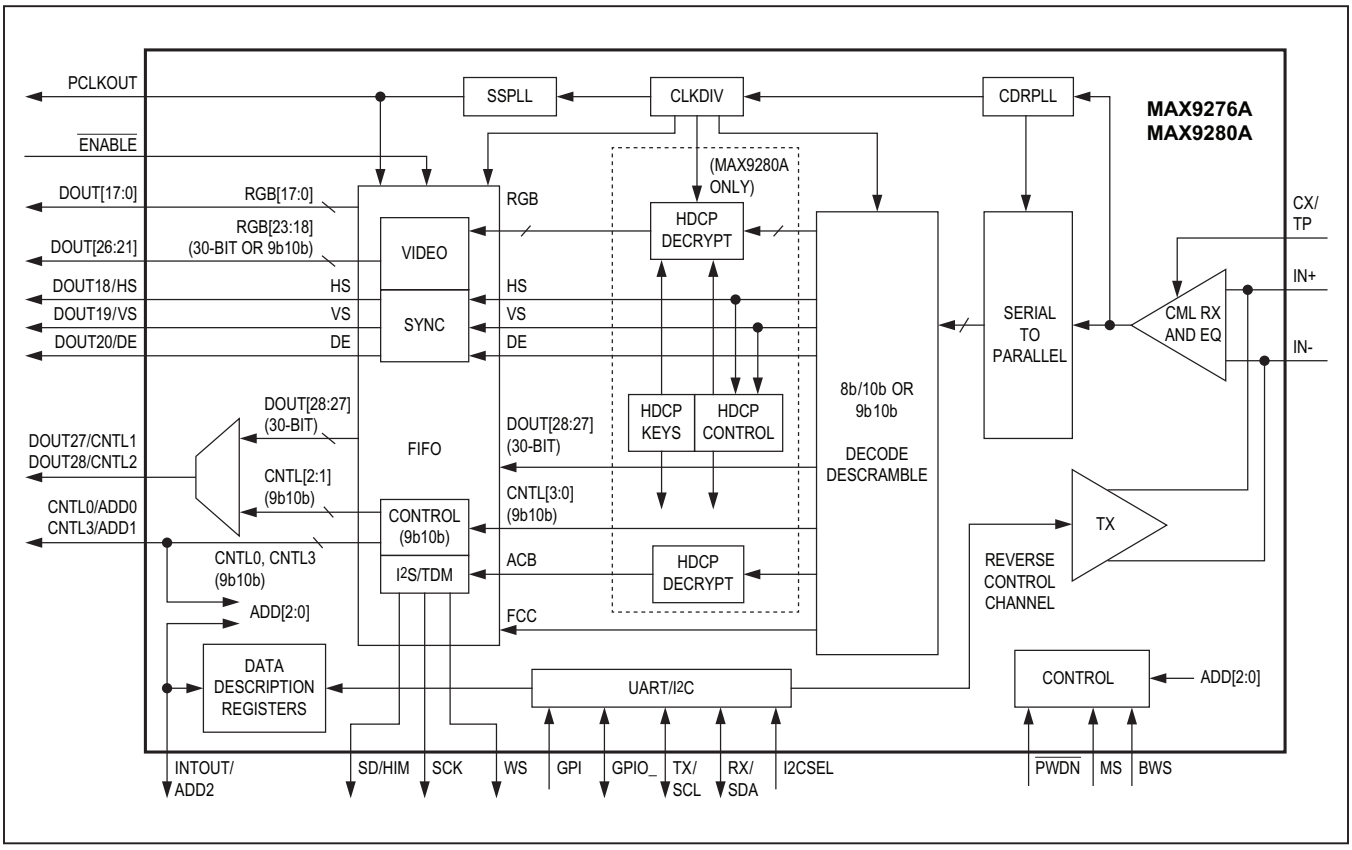
Pin Description (continued)

PIN	NAME	FUNCTION
20	WS	I²S/TDM Word-Select Input/Output. Powers up as an I²S output (deserializer-provided clock). Set AUDIOMODE bit = '1' to change WS to an input with internal pulldown to GND and supply WS externally (system provided clock).
21	SCK	I²S/TDM Serial-Clock Input/Output. Powers up as an I²S output (deserializer-provided clock). Set AUDIOMODE bit = '1' to change SCK to an input with internal pulldown to GND and supply WS externally (system provided clock).
22	SD/HIM	I²S/TDM Serial-Data Output/High-Immunity Mode Input. Functions as HIM input with internal pulldown to EP at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to SD output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. Connect SD/HIM to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. SD: Disable I²S/TDM encoding to serial data to use SD as an additional control/data output valid on the selected edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only).
23	DOUT28/CNTL2	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT28/CNTL2 remains high impedance in 24-bit mode (BWS = low) DOUT28 used only in 32-bit mode (BWS = high). DOUT28 not encrypted when HDCP is enabled (MAX9280A only). CNTL2 used only in high-bandwidth mode (BWS = open). CNTL2 not encrypted when HDCP is enabled (MAX9280A only).
24	DOUT27/CNTL1	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT27/CNTL1 remains high impedance in 24-bit mode (BWS = low) DOUT27 used only in 32-bit mode (BWS = high). DOUT27 not encrypted when HDCP is enabled (MAX9280A only). CNTL1 used only in high-bandwidth mode (BWS = open). CNTL1 not encrypted when HDCP is enabled (MAX9280A only)
25, 26, 28–31	DOUT[26:21]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only). DOUT[26:21] used only in 32-bit and high-bandwidth modes (BWS = high or open). DOUT[26:21] remains high-impedance in 24-bit mode.
27, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
32	DOUT20/DE	Parallel Data/Device Enable Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Device enable output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).
33	DOUT19/VS	Parallel Data/Vertical Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Vertical sync output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).
34	DOUT18/HS	Parallel Data/Horizontal Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Horizontal sync output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).

Pin Description (continued)

PIN	NAME	FUNCTION
35, 36, 38–43, 45–54	DOUT[17:0]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only)
37	PCLKOUT	Parallel Clock Output Used for DOUT[28:0]. Latches parallel data into the input of another device.
56	CX/TP	Three-Level Coax/Twisted Pair Select Input. Use 6kΩ (max) pullup to IOVDD or pulldown resistor for setting CX/TP = high or low. See Table 10 for function.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



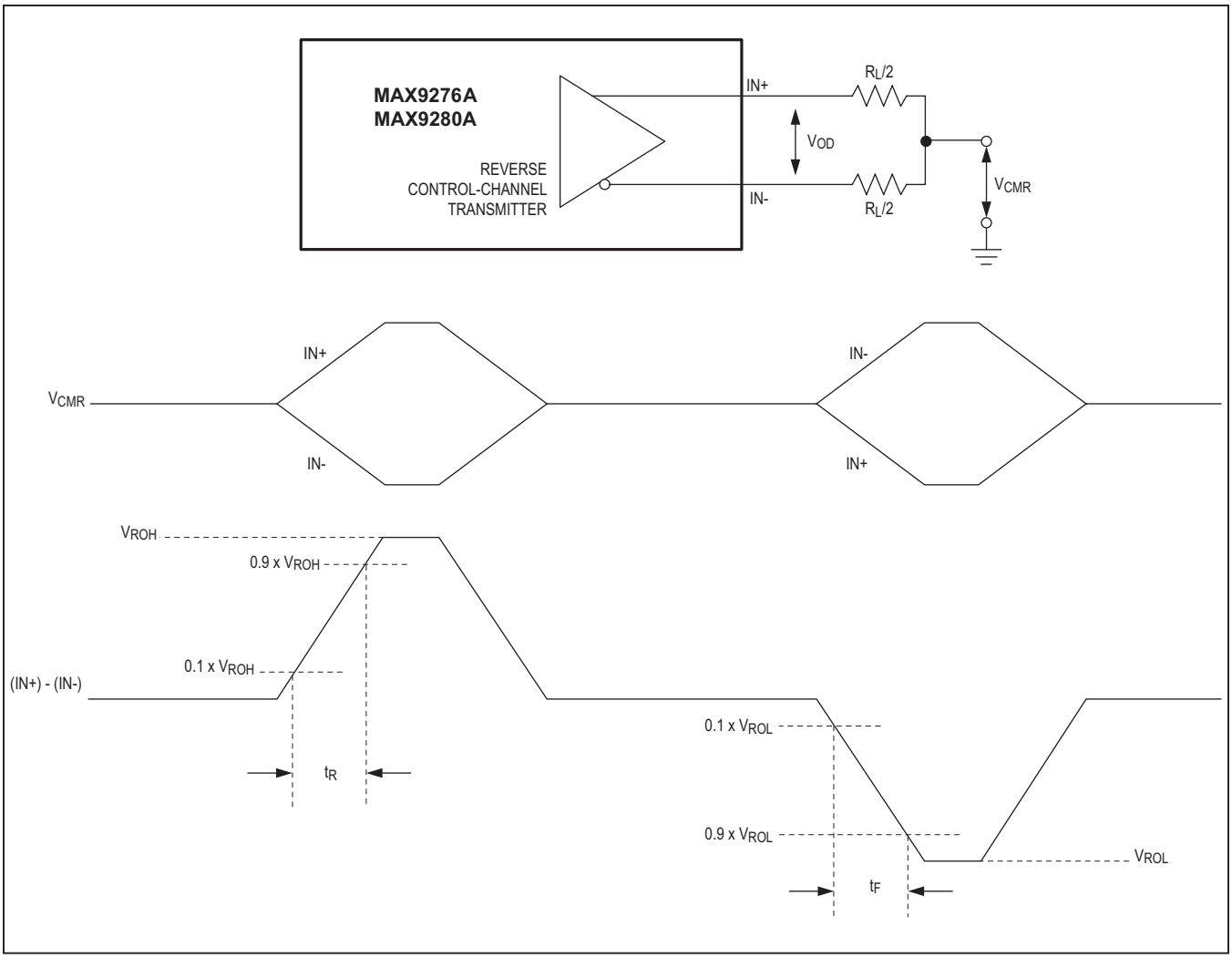


Figure 1. Reverse Control-Channel Output Parameters

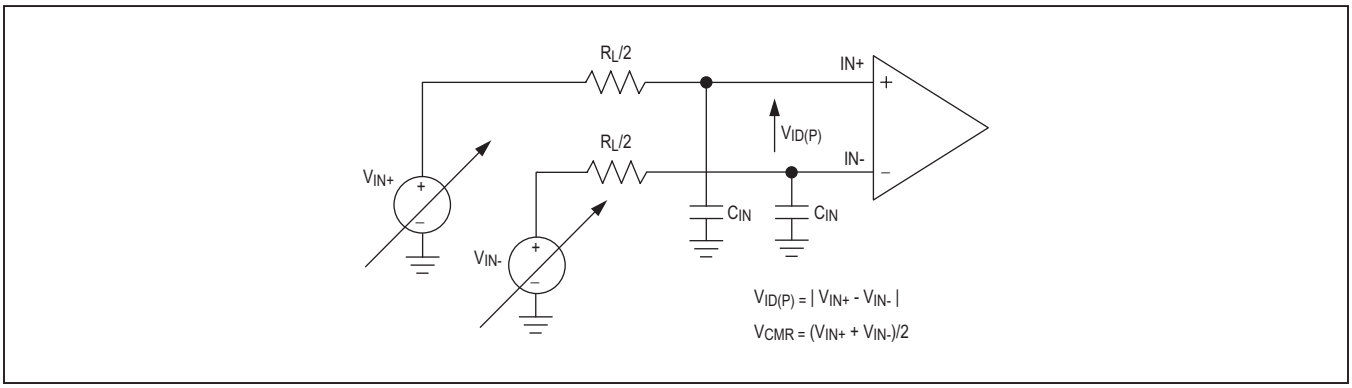


Figure 2. Test Circuit for Differential Input Measurement

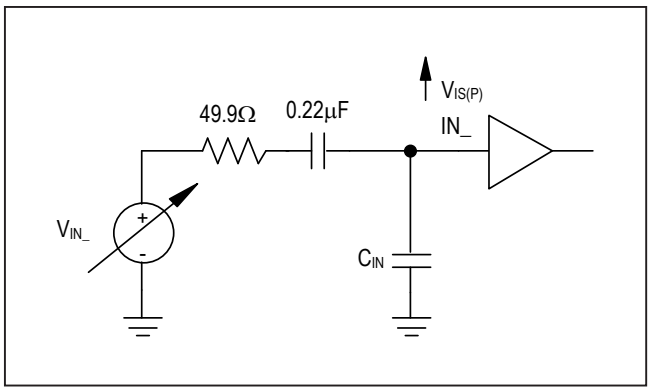


Figure 3. Test Circuit for Single-Ended Input Measurement

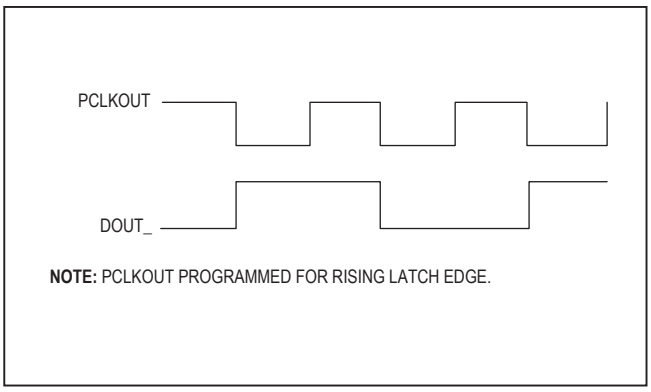


Figure 4. Worst-Case Pattern Output

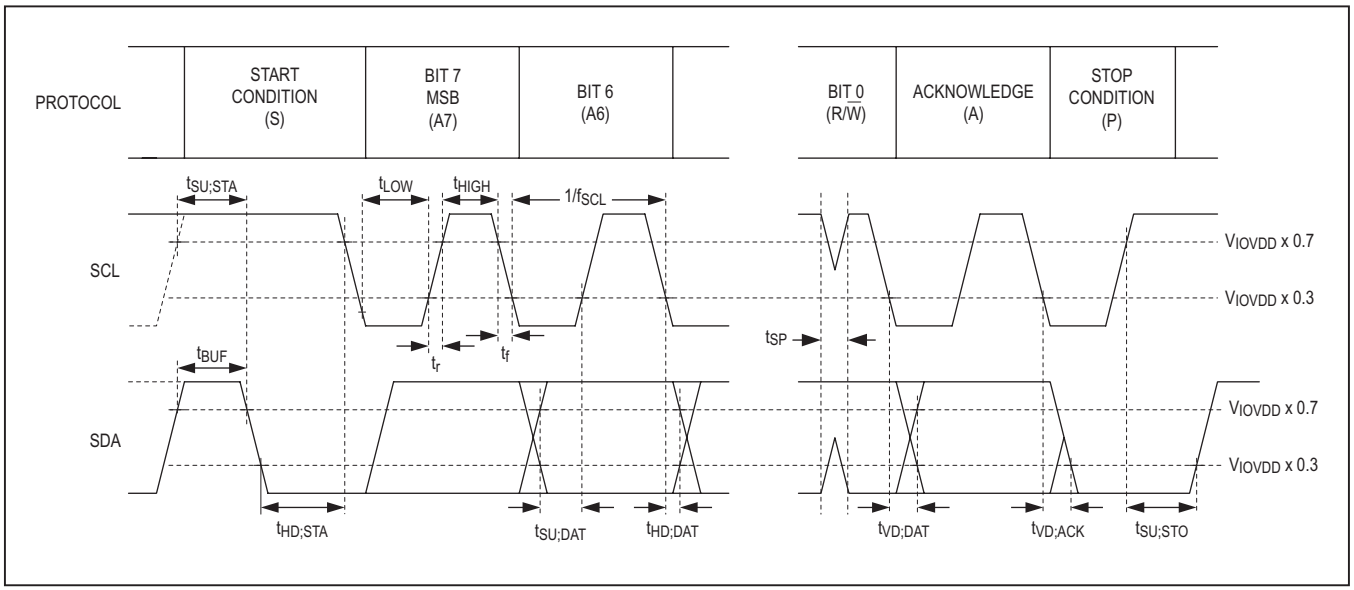


Figure 5. I²C Timing Parameters

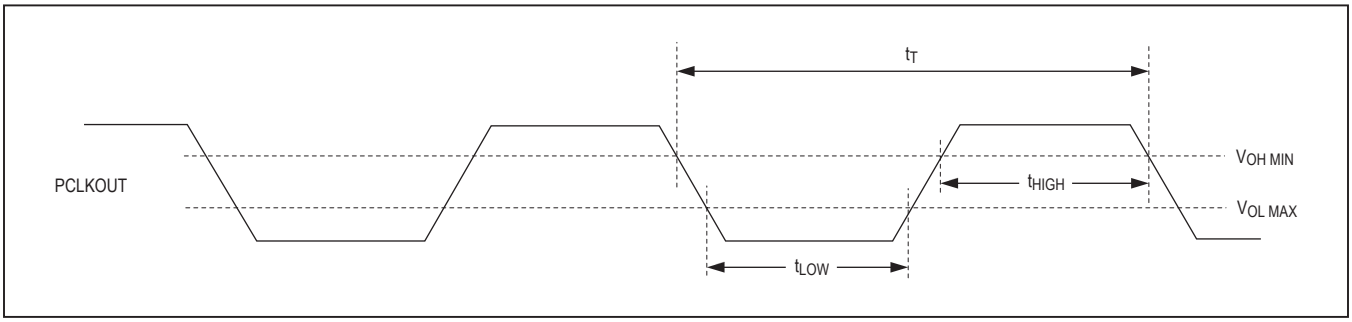


Figure 6. Parallel Clock Output Requirements

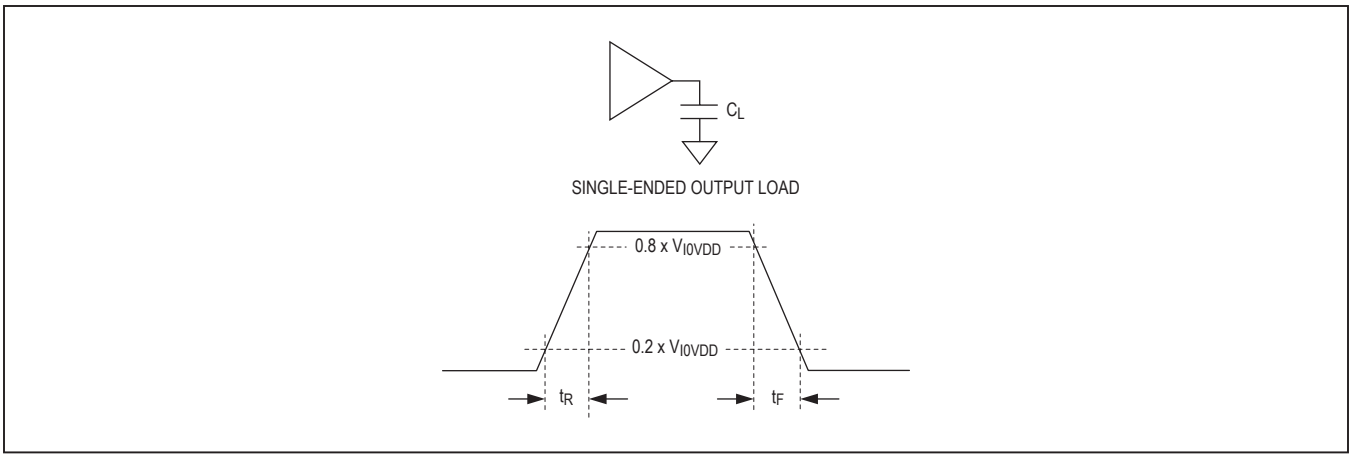


Figure 7. Output Rise-and-Fall Times

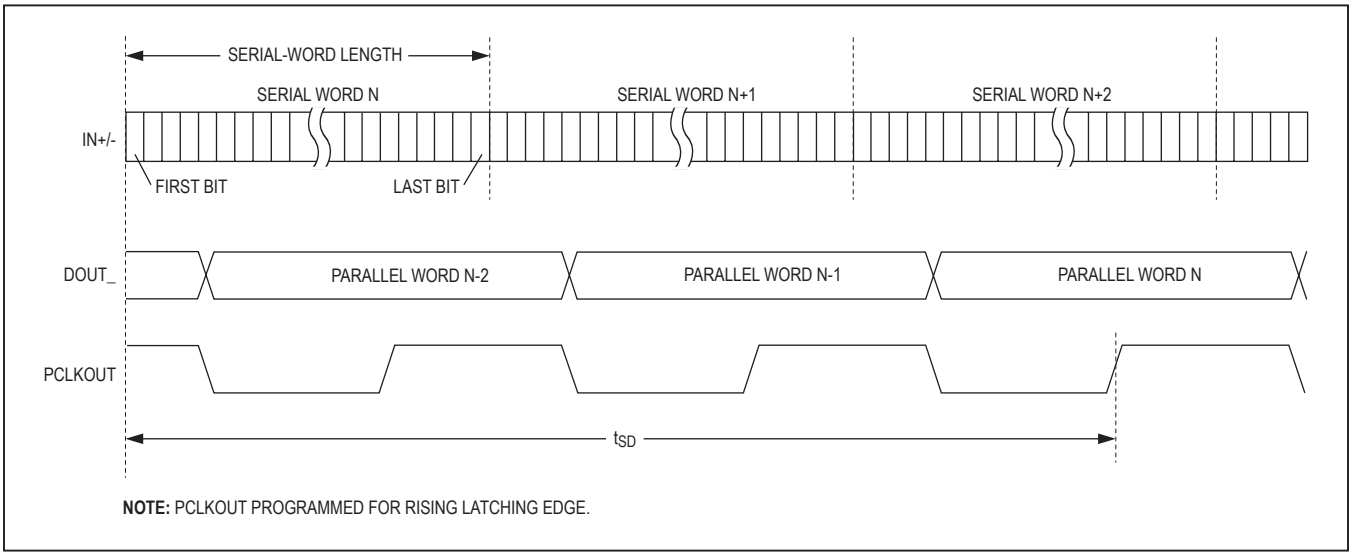


Figure 8. Deserializer Delay

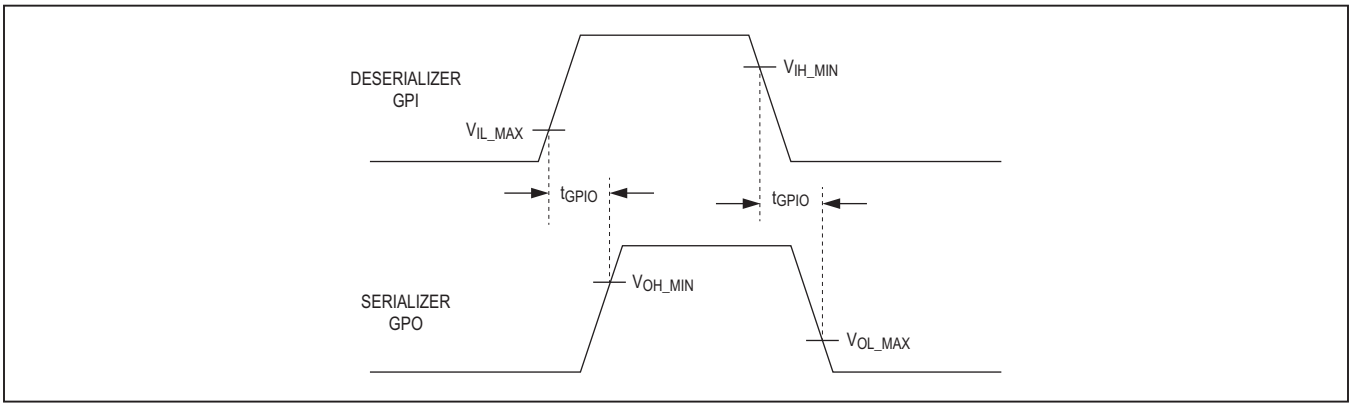


Figure 9. GPI-to-GPO Delay

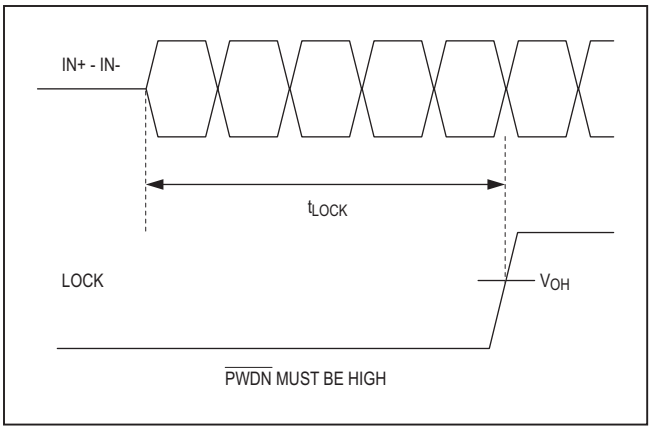


Figure 10. Lock Time

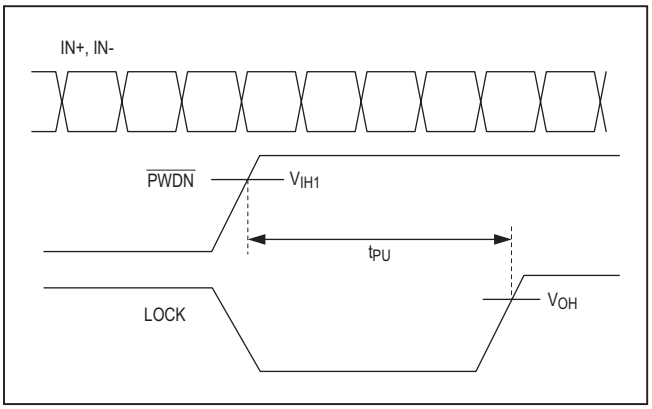


Figure 11. Power-Up Delay

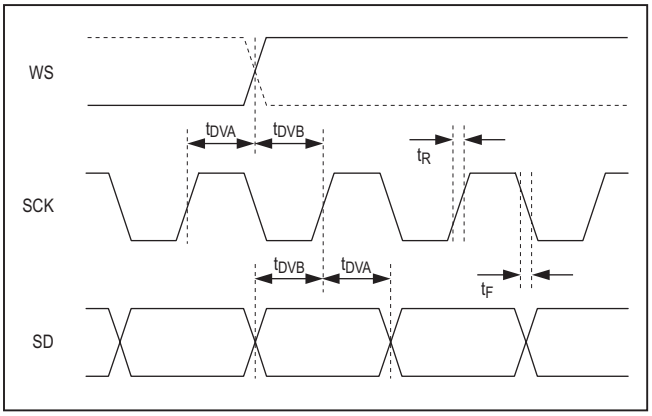


Figure 12. Output I²S Timing Parameters

Detailed Description

The MAX9276A/MAX9280A deserializers, when paired with the MAX9275/MAX9277/MAX9279/MAX9281 serializers, provides the full set of operating features, but is backward-compatible with the MAX9249–MAX9270 family of gigabit multimedia serial link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9280A has high-bandwidth digital content protection (HDCP) while the MAX9276A does not.

The deserializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Input equalization, combined with GMSL serializer pre/deemphasis, extends the cable length and enhances link reliability

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9280A only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the parallel output. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializers and are programmed using the control channel in base mode. The MAX9276A/MAX9280A holds its own device address and the device address of the serializer it is paired with. Similarly, the serializer holds its own device address and the address of the MAX9276A/MAX9280A. Whenever a device address is changed be sure to write the new address to both devices. The default device address of the deserializer is set by the ADD[2:0] and CX/TP inputs (see Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

Table 1. Device Address Defaults (Register 0x00, 0x01)

PIN				DEVICE ADDRESS (bin)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
CX/TP**	ADD2	ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
High/Low	Low	Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	80	90
High/Low	Low	Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	84	94
High/Low	Low	High	Low	1	0	0	X*	1	0	0	R/$\overline{W}$	88	98
High/Low	Low	High	High	0	1	0	X*	0	1	0	R/$\overline{W}$	44	54
High/Low	High	Low	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	C0	D0
High/Low	High	Low	High	1	1	0	X*	0	1	0	R/$\overline{W}$	C4	D4
High/Low	High	High	Low	1	1	0	X*	1	0	0	R/$\overline{W}$	C8	D8
High/Low	High	High	High	0	1	0	X*	1	0	0	R/$\overline{W}$	48	58
Open	Low	Low	Low	1	0	0	X*	0	0	X*	R/$\overline{W}$	80	92
Open	Low	Low	High	1	0	0	X*	0	1	X*	R/$\overline{W}$	84	96
Open	Low	High	Low	1	0	0	X*	1	0	X*	R/$\overline{W}$	88	9A
Open	Low	High	High	0	1	0	X*	0	1	X*	R/$\overline{W}$	44	56
Open	High	Low	Low	1	1	0	X*	0	0	X*	R/$\overline{W}$	C0	D2
Open	High	Low	High	1	1	0	X*	0	1	X*	R/$\overline{W}$	C4	D6
Open	High	High	Low	1	1	0	X*	1	0	X*	R/$\overline{W}$	C8	DA
Open	High	High	High	0	1	0	X*	1	0	X*	R/$\overline{W}$	48	5A

**X = 0 for the serializer address, X = 1 for the deserializer address*

***CX/TP determine the serial cable type CX/TP = open addresses only for coax mode.*

Output Bit Map

The output bit width depends on settings of the bus width (BWS) pin. Table 2 lists the bit map. Unused output bits are pulled low.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b/10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit mode, the first 21 bits contain video data. In 32-bit mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, the parity bit of the serial word (Figure 13, Figure 14).

Table 2. Output Map

SIGNAL	OUTPUT PIN	MODE		
		24-BIT MODE (BWS = LOW)	HIGH-BANDWIDTH MODE (BWS = MID	32-BIT MODE (BWS = HIGH)
R[5:0]	DOUT[5:0]	Used	Used	Used
G[5:0]	DOUT [11:6]	Used	Used	Used
B[5:0]	DOUT [17:12]	Used	Used	Used
HS, VS, DE	DOUT18/HS, DOUT19/VS, DOUT20/DE	Used**	Used**	Used**
R[7:6]	DOUT [22:21]	Used+	Used	Used
G[7:6]	DOUT [24:23]	Used+	Used	Used
B[7:6]	DOUT [26:25]	Used+	Used	Used
CNTL[2:1]	DOUT [28:27]/CNTL[2:1]	Not used	Used*/**	Used**
CNTL3, CNTL0	CNTL3/ADD1, CNTL0/ADD0	Not used	Used*/**	Not used
I2S/TDM	WS, SCK, SD/HIM	Used	Used	Used
AUX SIGNAL		Used	Used	Used

**See the High-Bandwidth Mode section for details on timing requirements.*

+Outputs used only when the respective color lookup tables are enabled.

***Not encrypted when HDCP is enabled (MAX9280A only).*

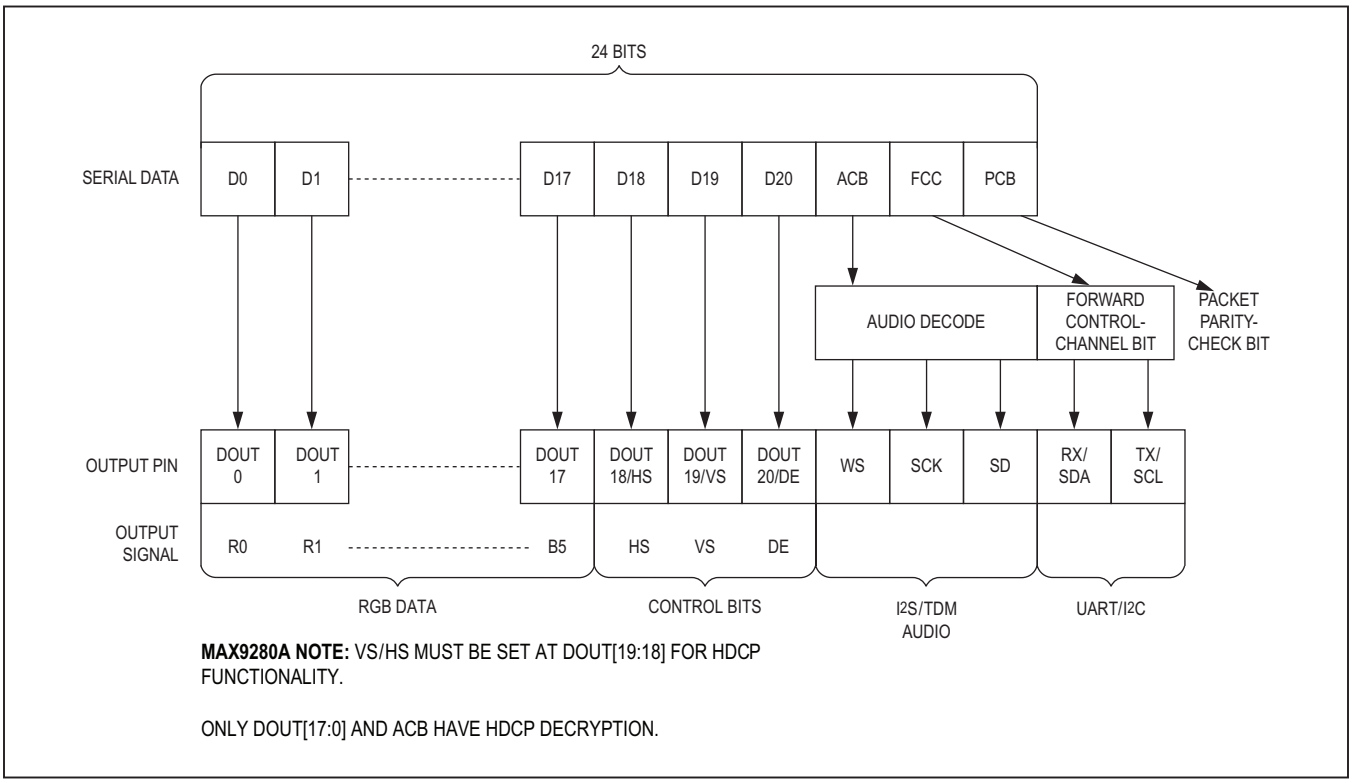


Figure 13. 24-Bit Mode Serial-Data Format

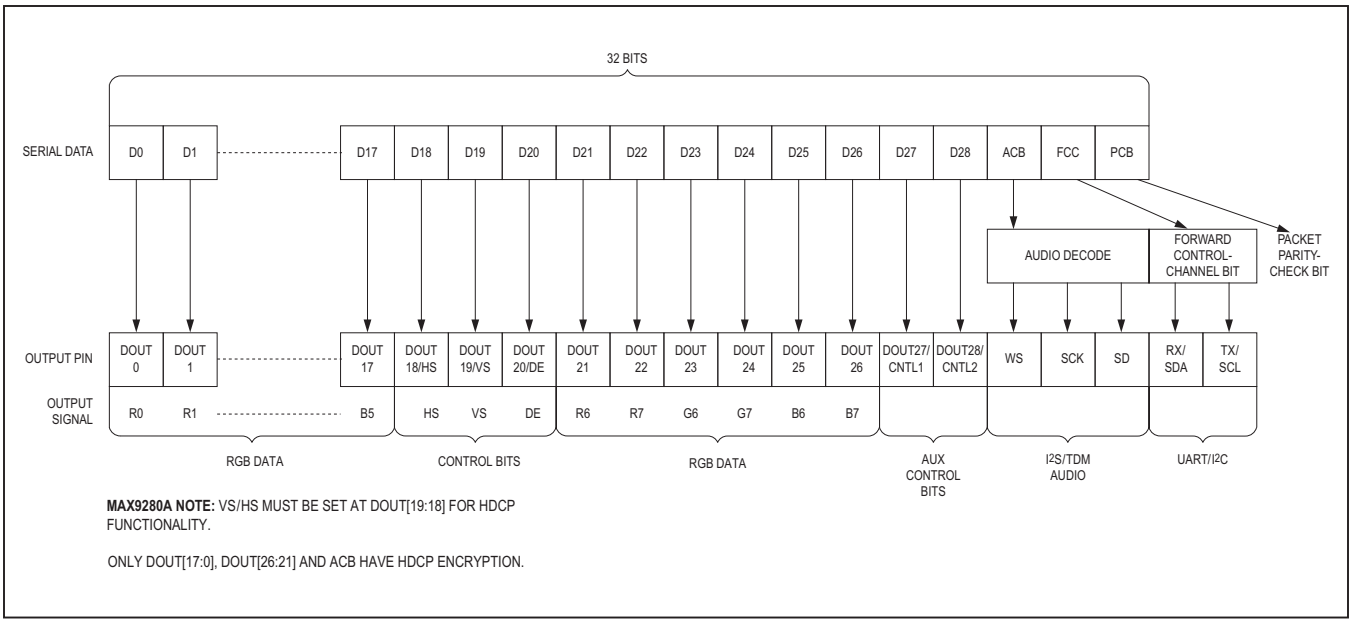


Figure 14. 32-Bit Mode Serial-Data Format

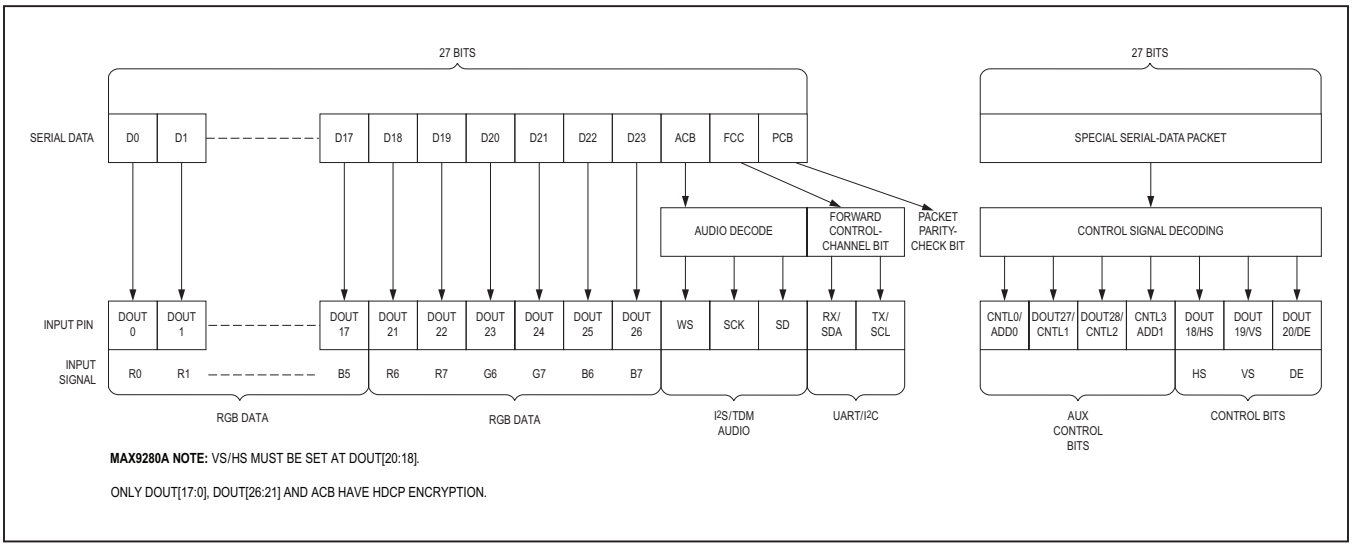


Figure 15. High-Bandwidth Mode Seria-Data Format

Table 3. Data-Rate Selection Table

DRS BIT SETTING	BWS PIN SETTING	PCLKOUT RANGE (MHz)
0 (high data rate)	Low (24-bit mode)	16.66 to 104
	Mid (high-bandwidth mode)	36.66 to 104
	High (32-bit mode)	12.5 to 78
1 (low data rate)	Low	8.33 to 16.66
	Mid	18.33 to 36.66
	High	6.25 to 12.5

The deserializer uses the DRS bit and the BWS input to set the PCLKOUT frequency range (Table 3). Set DRS = 1 for low data rate PCLKOUT frequency range of 6.25MHz to 16.66MHz. Set DRS = 0 for high data rate PCLKOUT frequency range of 12.5MHz to 104MHz.

High-Bandwidth Mode

The deserializer uses a 27-bit high-bandwidth mode to support 24-bit RGB at 104MHz pixel clock. Set BWS = open in both the serializer and deserializer to use high-bandwidth mode. In high-bandwidth mode, the deserializer decodes HS, VS, DE and CNTL[3:0] from special packets. Packets are sent by replacing a pixel before the rising edge and after the falling edge of the HS, VS, and DE signals. However, for CNTL[3:0], which is not always continuously sampled, packets always replace a pixel before the transition of the sampled CNTL[3:0]. Keep HS, VS, and DE low pulse widths at least 2 pixel clock cycles. By default, CNTL[3:0] are sampled continuously when DE is low. CNTL[3:0] are sampled only on HS/VS transitions when DE is high. If DE triggering of encoded packets is not desired, set the serializer's DISDETRIG = 0 and the CNTLTRIG bits to their desired value (register 0x15) to change the CNTL triggering behavior. Set DETREN = 0 on the deserializer when DE is not periodic.

Audio Channel

The audio channel supports 8kHz to 192kHz audio sampling rates and audio word lengths from 8 bits to 32 bits (2 channel I²S) or 64 to 256 bits (TDM64 to TDM256). The audio bit clock (SCK) does not have to be synchronized with PCLKOUT. The serializer automatically encodes audio data into a single-bit stream synchronous with PCLKOUT. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the SD/HIM is treated as an auxiliary control signal.

Since the audio data sent through the serial link is synchronized with PCLKOUT, low PCLKOUT frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various PCLKOUT frequencies. Spread-spectrum settings do not affect the I²S/TDM data rate or WS clock frequency.

Audio Channel Input

The audio channel input works with 8-channel TDM and stereo I²S, as well as non-standard formats. The input format is shown in Figure 16.

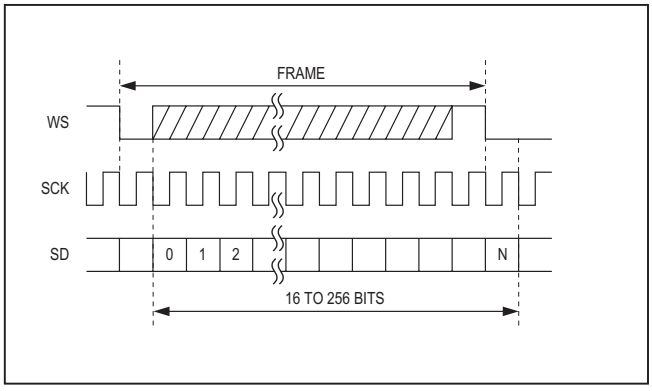


Figure 16. Audio Channel Input Format

Table 4. Maximum Audio WS Frequency (kHz) for Various PCLKOUT Frequencies

CHANNELS	BITS PER CHANNEL	PCLKOUT FREQUENCY (DRS = 0*) (MHz)										
		12.5	15.0	16.6	20.0	25.0	30.0	35.0	40.0	45.0	50.0	100
2	8	+	+	+	+	+	+	+	+	+	+	+
	16	+	+	+	+	+	+	+	+	+	+	+
	18	185.5	+	+	+	+	+	+	+	+	+	+
	20	174.6	+	+	+	+	+	+	+	+	+	+
	24	152.2	182.7	+	+	+	+	+	+	+	+	+
	32	123.7	148.4	164.3	+	+	+	+	+	+	+	+
4	8	+	+	+	+	+	+	+	+	+	+	+
	16	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	18	112.0	134.4	148.8	179.2	+	+	+	+	+	+	+
	20	104.2	125.0	138.3	166.7	+	+	+	+	+	+	+
	24	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	32	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
6	8	152.2	182.7	+	+	+	+	+	+	+	+	+
	16	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	18	80.2	93.3	106.6	128.4	160.5	+	+	+	+	+	+
	20	73.3	88.0	97.3	117.3	146.6	175.9	+	+	+	+	+
	24	62.5	75.0	83.0	100	125	150	175	+	+	+	+
	32	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
8	8	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	16	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
	18	62.5	75.0	83.0	100.0	125.0	150.0	175.0	+	+	+	+
	20	57.1	68.5	75.8	91.3	114.2	137.0	159.9	182.7	+	+	+
	24	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
	32	37.1	44.5	49.3	59.4	74.2	89.1	103.9	118.8	133.6	148.4	+

COLOR CODING
< 48kHz
48kHz to 96kHz
96kHz to 192kHz
> 192kHz

+Max WS rate is greater than 192kHz.

**DRS = 0 PCLKOUT frequency is equal to 2x the DRS = 1 PCLKOUT frequency.*

The period of the WS can be 8 to 256 SCK periods. The WS frame starts with the falling edge and can be low for 1 to 255 SCK periods. SD is one SCK period, sampled on the rising edge. MSB/LSB order, zero padding or any other significance assigned to the serial data does not affect operation of the audio channel. The polarity for WS and SCK edges is programmable.

Figure 17, Figure 18, Figure 19, and Figure 20 are examples of acceptable input formats.

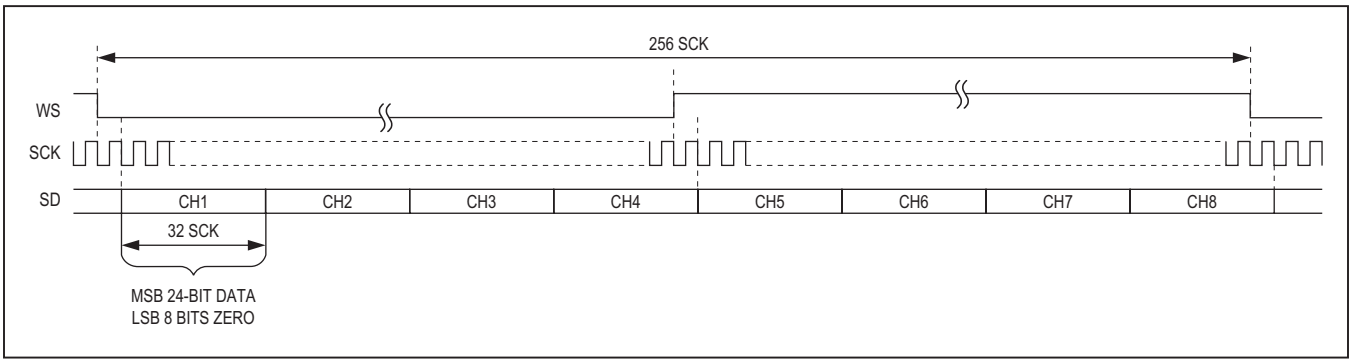


Figure 17. 8-Channel TDM (24-Bit Samples, Padded with Zeros)

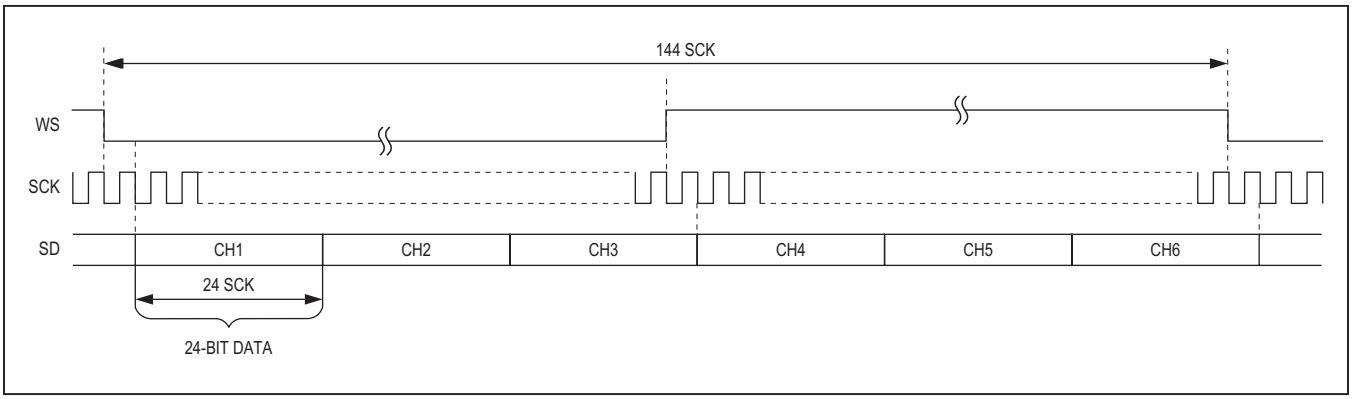


Figure 18. 6-Channel TDM (24-Bit Samples, No Padding)

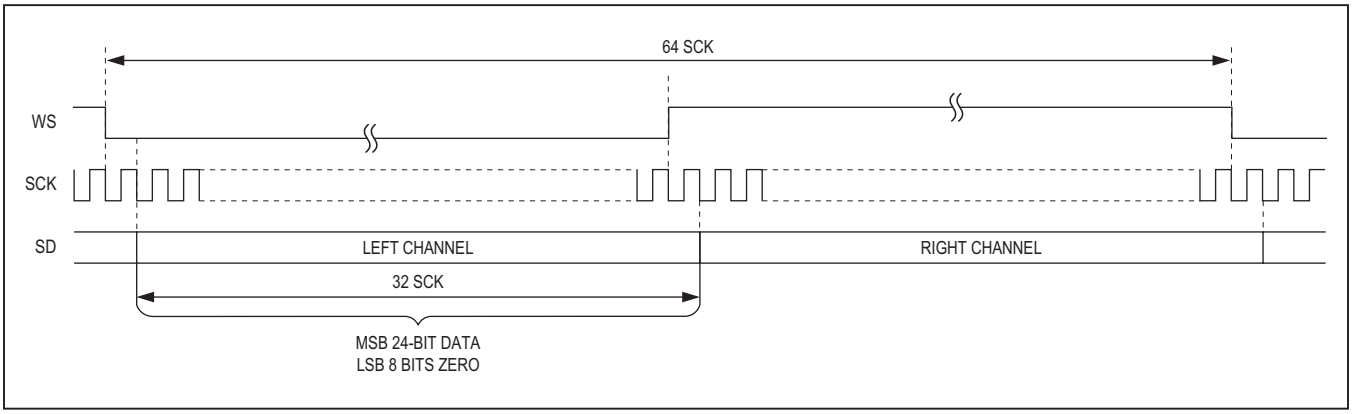


Figure 19. Stereo I²S (24-Bit Samples, Padded with Zeros)

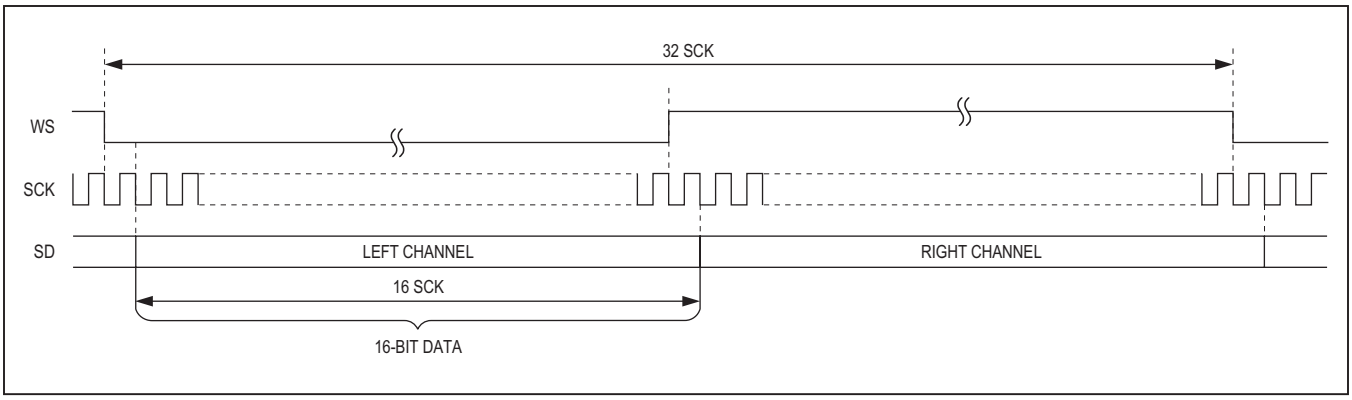


Figure 20. Stereo I²S (16-Bit Samples, No Padding)

Audio Channel Output

WS, SCK, and SD are output with the same timing relationship they had at the audio input, except that WS is always 50% duty cycle (regardless of the duty cycle of WS at the input).

The output format is shown in Figure 21.

WS and SCK can be driven by the audio source (clock master) or the audio sink (clock slave). Buffer underflow and overflow flags are available to the sink as clock slave via I²C for clock frequency adjustment. Data are sampled on the rising edge. WS and SCK polarity is programmable.

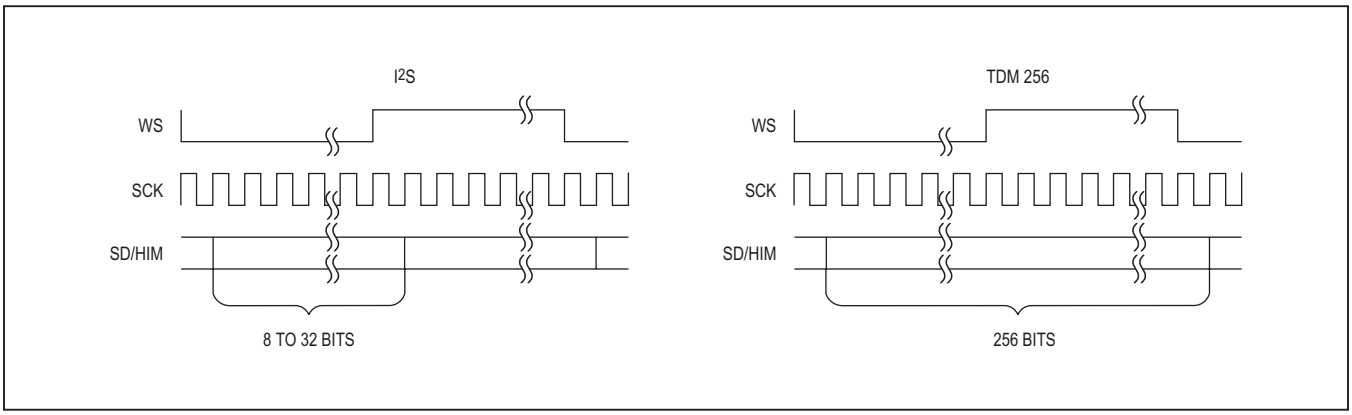


Figure 21. Audio Channel Output Format

Additional MCLK Output for Audio Applications

Some audio DACs, such as the MAX9850, do not require a synchronous main clock (MCLK), while other DACs require a separate MCLK for operation. For audio applications that cannot use WS or PCLKOUT directly, the deserializer provides a divided MCLK output at either DOUT28/CNTL2 or CNTL0/ADD0 (determined by MCLKPIN bit setting) at the expense of one less control line. By default, MCLK is turned off. Set MCLKDIV (deserializer register 0x12, D[6:0]) to a nonzero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set DOUT28/CNTL2 or CNTL0/ADD0 as a control output.

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where:

f_{SRC} is the MCLK source frequency (see Table 5)

MCLKDIV is the divider ratio from 1 to 127

Choose MCLKDIV values so that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from PCLKOUT (MCLKSRC = 0) are not affected by spread-spectrum settings in the deserializer. Enabling spread spectrum in the serializer, however, introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions. Alternatively, set MCLKWS = 1 (0x15 D1) to output WS from MCLK.

Audio Output Timing Sources

The deserializer has multiple options for audio data output timing. By default, the deserializer provides the output timing based on the incoming data rate (through a FIFO) and an internal oscillator.

To use a system sourced clock, set the AUDIOMODE bit to 1 (D5 of register 0x02) to set WS and SCK as inputs on the deserializer side. The deserializer uses a FIFO to smooth out the differences in input and output audio timing. Registers 0x78 and 0x79 store the FIFO overflow/underflow information for use with external WS/SCK timing. The FIFO drops data packets during FIFO overflow. By default, the FIFO repeats the last audio packet during FIFO underflow when no audio data is available. Set the AUDUFBEH bit (D2 of register 0x01D) to 1 to output all zeroes during underflow.

Reverse Control Channel

The serializer uses the reverse control channel to receive I^2C/UART, MS, and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 500µs after starting/stopping the forward serial link.

Table 5. f_{SRC} Settings

MCLKWS SETTING (REGISTER 0x15, D1)	MCLKSRC SETTING (REGISTER 0x12, D7)	DATA RATE SETTING	BIT-WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	0	High speed (DRS = 0)	24-bit or high-bandwidth mode	3 x f_{CLKOUT}
			32-bit mode	4 x f_{CLKOUT}
		Low speed (DRS = 1)	24-bit or high-bandwidth mode	6 x f_{CLKOUT}
			32-bit mode	8 x f_{CLKOUT}
	1	—	—	Internal oscillator (120MHz typ)
1	—	—	—	WS*

**MCLK is not divided when using WS as the MCLK source. The MCLK divider must still be set to a nonzero number for MCLK to be enabled.*

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel. The total maximum forward or reverse control-channel delay is 2µs (UART) or 2-bit times (I^2C) from the input of one device to the output of the other. I^2C delay is measured from a START condition to START condition.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I^2C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable.

When the peripheral interface is I^2C, the serializer/deserializer converts UART packets to I^2C that have device addresses different from those of the serializer or deserializer. The converted I^2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information.

Figure 22 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 23 shows the UART data format. Even parity is used Figure 24 and Figure 25 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication will be corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than 4 bit-times between bytes in a packet. Keep the UART Tx/Rx lines high for at least 16 bit-times before starting to send a new packet.

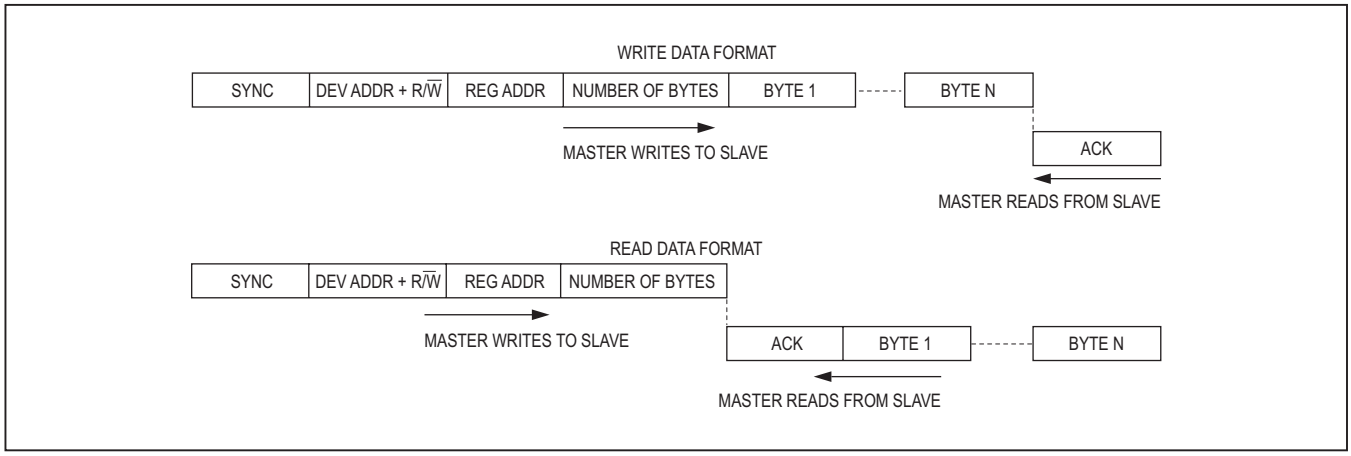


Figure 22. GMSL UART Protocol for Base Mode

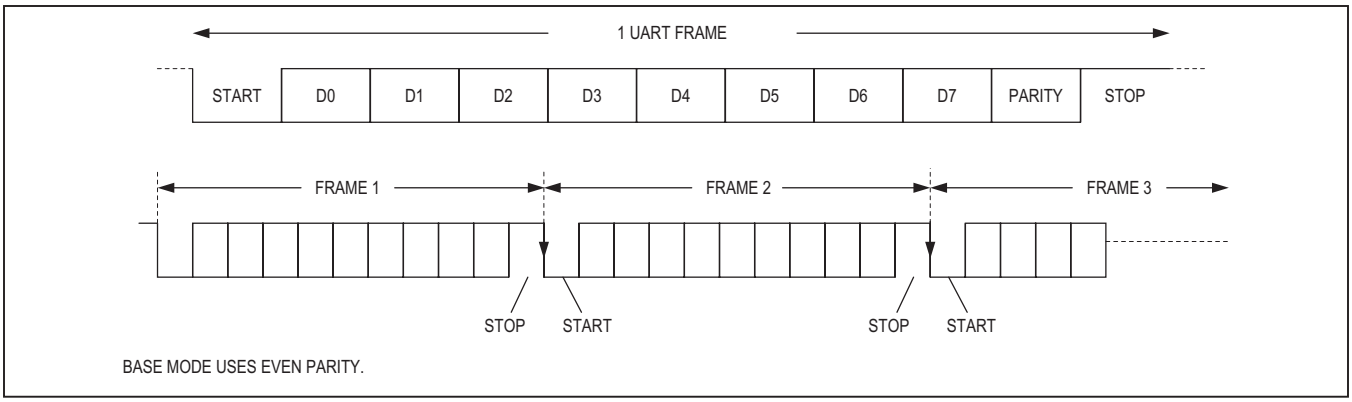


Figure 23. GMSL UART Data Format for Base Mode

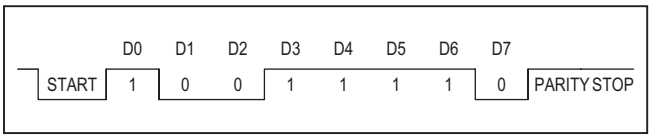


Figure 24. Sync Byte (0x79)

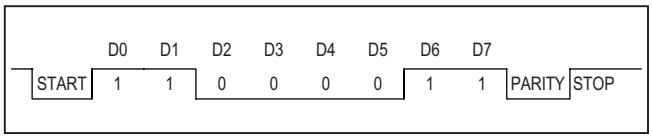


Figure 25. ACK Byte (0xC3)

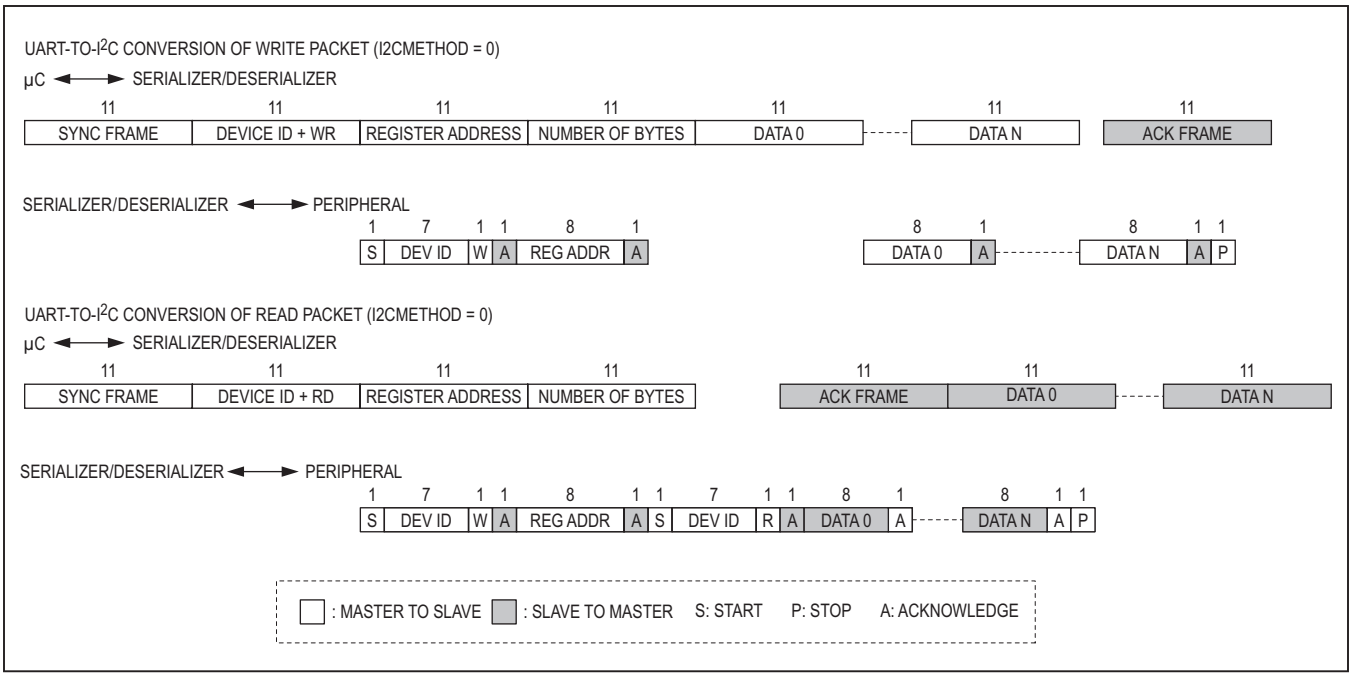


Figure 26. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

As shown in Figure 26, the remote-side device converts packets going to or coming from the peripherals from UART format to I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C bit rate is the same as the UART bit rate.

Interfacing Command-Byte-Only I²C Devices with UART

The deserializers' UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 27). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the deserializers ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLKOUT period ±10ns of jitter due to the asynchronous sampling of the UART signal by PCLKOUT. Set MS = high in the serializer to put the control channel into bypass mode. For applications with the µC connected to the deserializer, set the MS pin on the deserializer. There is a 1ms wait time between switching MS and the bypass control channel being active. Do not send a UART command at this time. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Although MS on either the serializer or deserializer sets the control-channel bypass mode, only the local-side device (connected to the µC) should be used to set bypass mode. Do not switch MS while a UART command is being sent. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

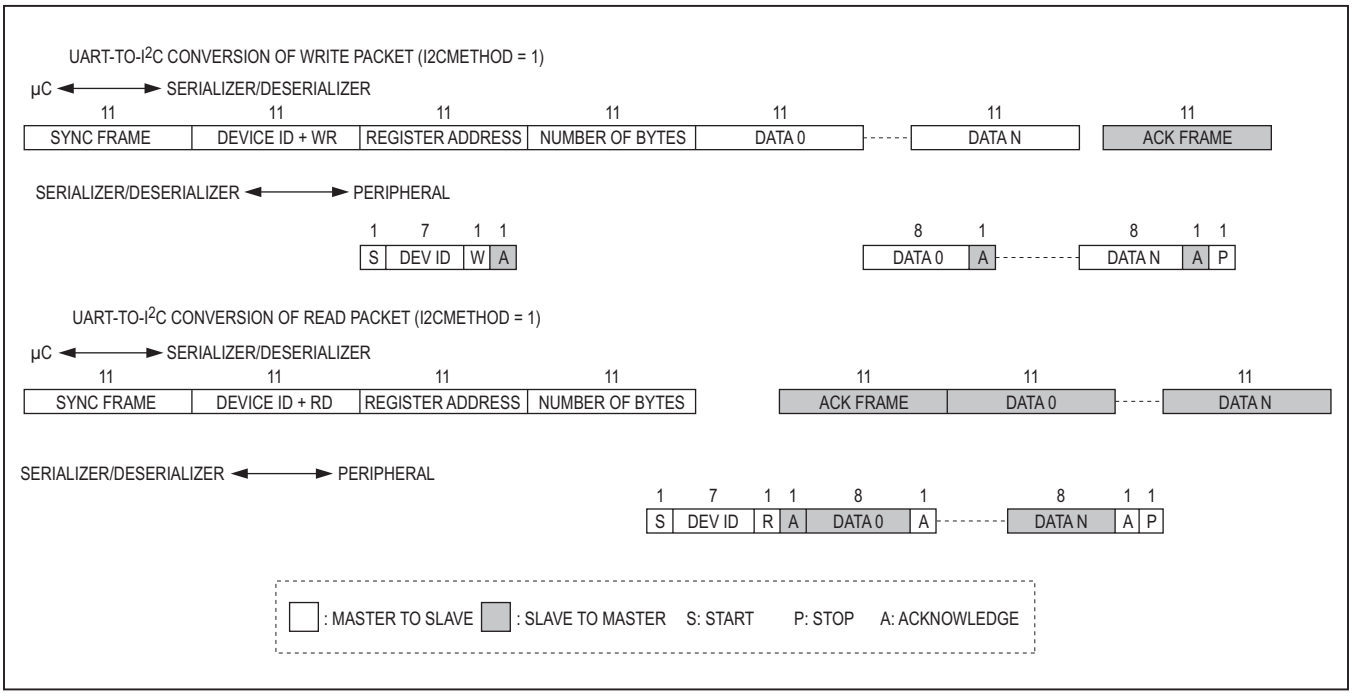


Figure 27. Format Conversion Between GMSL UART and I²C without Register Address (I2CMETHOD = 1)

I²C Interface

In I²C to I²C mode, the deserializer's control-channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local-side device's control-channel port, the remote-side device's control-channel port becomes an I²C master that interfaces with remote-side I²C peripherals. The I²C master must accept clock-stretching which is imposed by the deserializer (holding SCL LOW) The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 5) sent by a master, followed by the device's 7-bit slave address plus a R/W bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (see Figure 28). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 29). The data on SDA must remain stable while SCL is high.

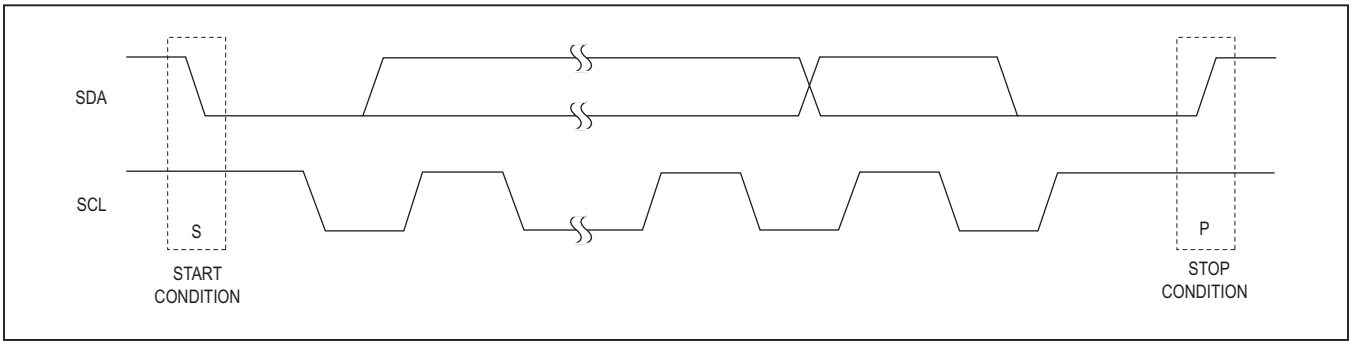


Figure 28. START and STOP Conditions

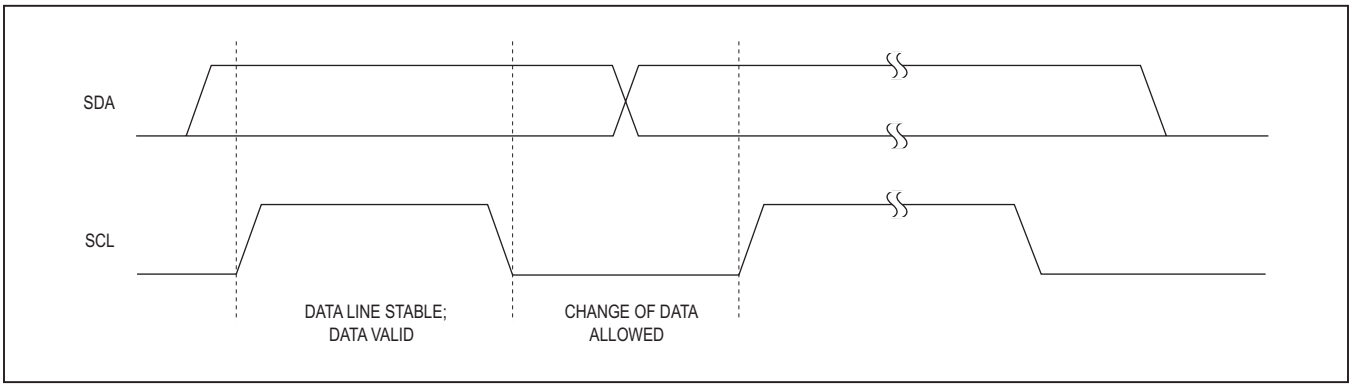


Figure 29. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 30). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active. To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

Slave Address

The deserializers have 7-bit long slave addresses. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command. The slave address for the deserializer is XX01XXX1 for read commands and XX01XXX0 for write commands. See Figure 31.

Bus Reset

The device resets the bus with the I2C START condition for reads. When the R/W bit is set to 1, the deserializers transmit data to the master, thus the master is reading from the device.

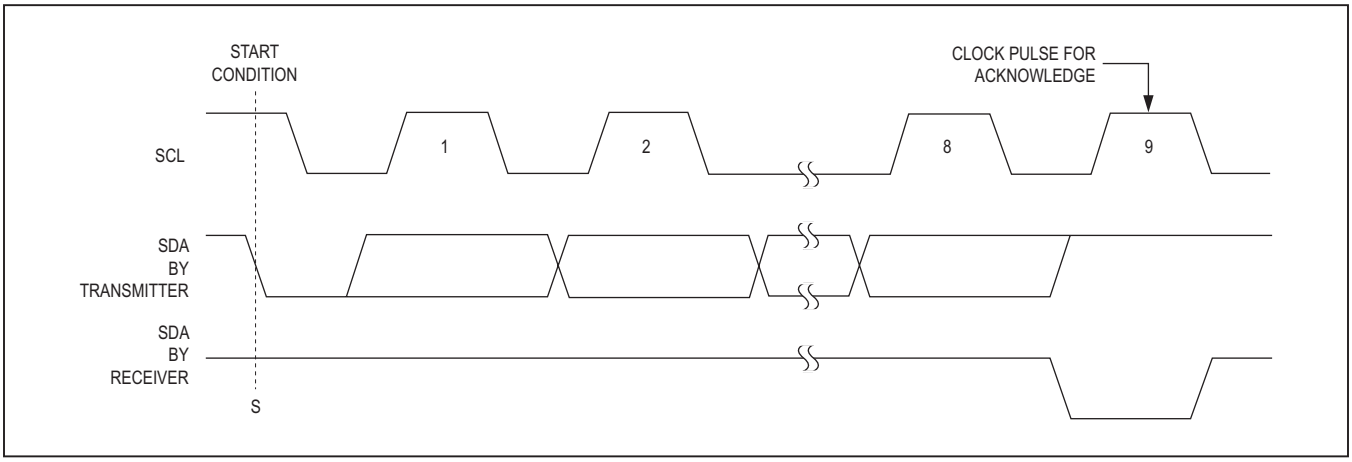


Figure 30. Acknowledge

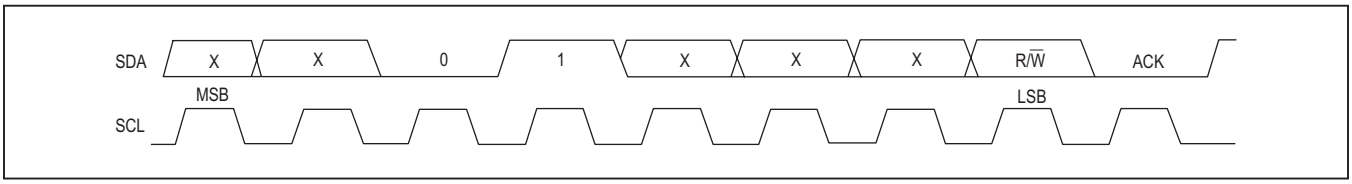


Figure 31. Slave Address

Format for Writing

Writes to the deserializers comprise the transmission of the slave address with the R/W bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 32). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 33). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

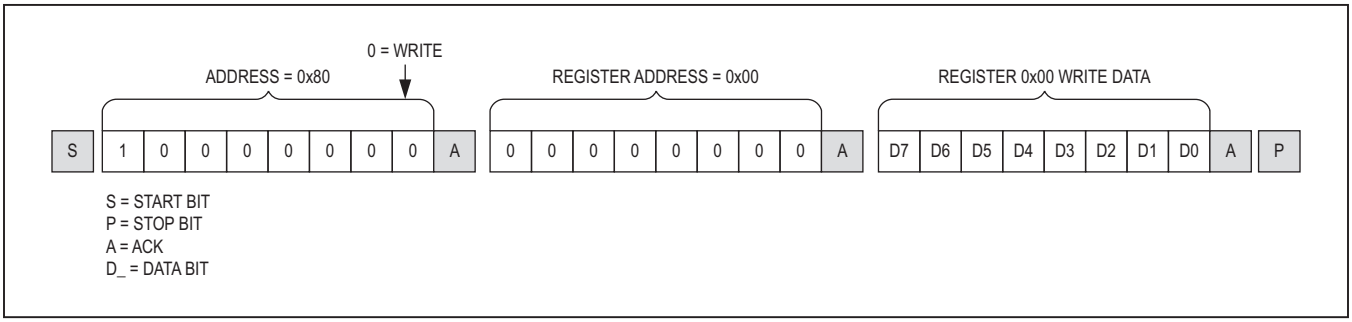


Figure 32. Format for I²C Write

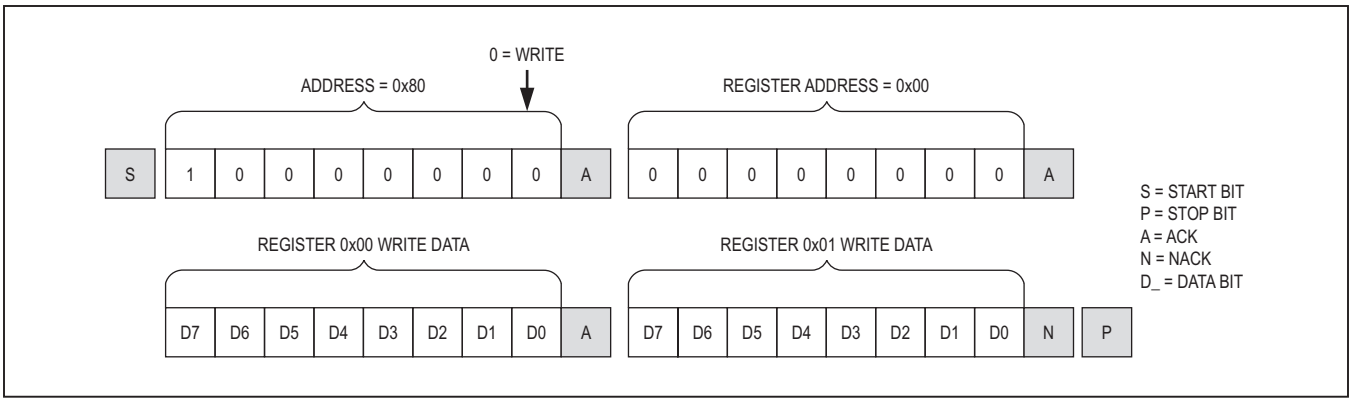


Figure 33. Format for Write to Multiple Registers

Format for Reading

The deserializers are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 34). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

I²C Communication with Remote-Side Devices

The deserializers support I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote-side I²C bit-rate range must be set according to the local-side I²C bit rate. Supported remote-side bit rates can be found in Table 6. Set the I2CMSTBT (register 0x1C) to set the remote I²C bit rate. If using a bit rate different from 400kbps, local and remote-side I²C setup and hold times should be adjusted by setting the I2CSLVSH register settings on both sides.

I²C Address Translation

The deserializers support I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x18 and 0x1A. Destination addresses (address to translate to) are stored in registers 0x19 and 0x1B.

In a multilink situation where there are multiple deserializers and/or peripheral devices connected to these serializers, the deserializers support broadcast commands to control these multiple devices. Select an unused device address to use as a broadcast device address. Program all the remote-side serializer devices to translate the broadcast device address (source address stored in registers 0x0F, 0x11) to the peripherals' address (destination address stored in registers 0x10, 0x12). Any commands sent to the broadcast address (selected unused address) will be sent to all deserializers and/or peripheral devices connected to the deserializers whose addresses match the translated broadcast address.

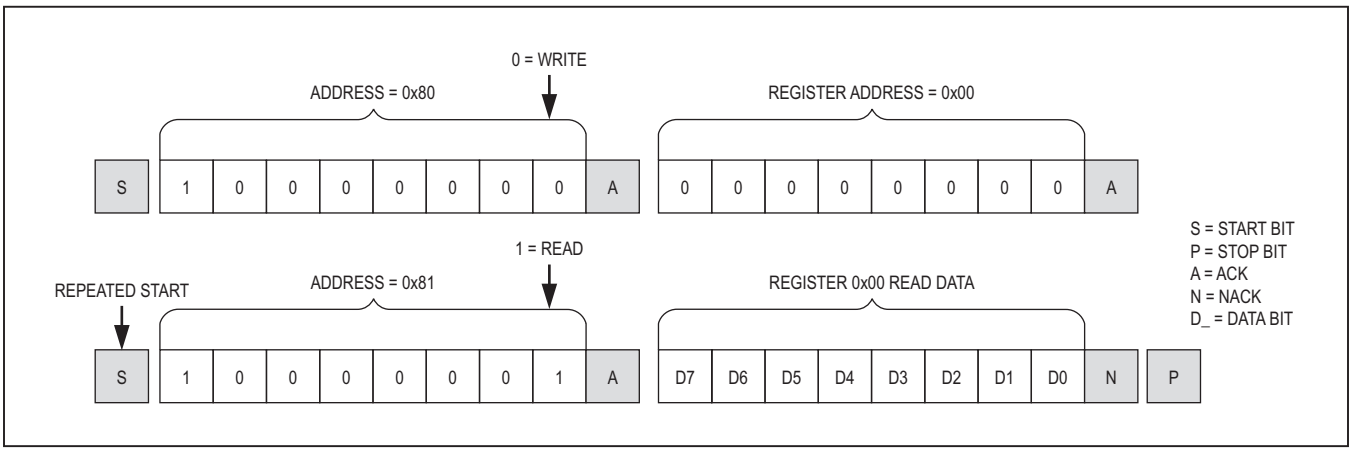


Figure 34. Format for I²C Read

Table 6. I²C Bit-Rate Ranges

LOCAL BIT RATE	REMOTE BIT-RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	ANY
20kbps > f > 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system. The GPI to GPO delay is 0.35ms max. Keep time between GPI transitions to a minimum 0.35ms. This includes transitions from the other deserializer in coax splitter mode. Bit D4 of register 0x06 in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SETGPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality. GPI/GPO commands will override and corrupt an I2C/UART command in progress.

Table 7. Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	**10.7 Power-up default**
1010	11.7
1011	13

Table 8. Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default.**
01	±2% spread spectrum.
10	No spread spectrum
11	±4% spread spectrum

Table 9. Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT MOD (DECIMAL)	SDIV UPPER LIMIT (DECIMAL)
4	208	15
2	208	30

Line Equalizer

The deserializer includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 11 selectable levels of compensation from 2.1dB to 13dB (Table 7). To select other equalization levels, set the corresponding register bits in the deserializer (0x05 D[3:0]). Use equalization in the deserializer, together with preemphasis in the serializer, to create the most reliable link for a given cable.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the deserializer output is programmable for spread spectrum. If the serializer, paired with the MAX9276A/MAX9280A, has programmable spread spectrum, do not enable spread for both at the same time or their interaction will cancel benefits. The deserializer will track the serializer spread and pass the spread to the deserializer output. The programmable spread-spectrum amplitudes are ±2%,and ±4% (Table 8).

The deserializer includes a sawtooth divider to control the spread modulation rate. Autodetection of the PCLKOUT operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[5:0]) allows the user to set a modulation frequency according to the PCLKOUT frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

Manual Programming of the Spread-Spectrum Divider

The modulation rate relates to the PCLKOUT frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLKOUT}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS value (0 or 1)

$f_{PCLKOUT}$ = PCLKOUT frequency

MOD = Modulation coefficient given in Table 9

SDIV = 5-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 9, set SDIV to the maximum value.

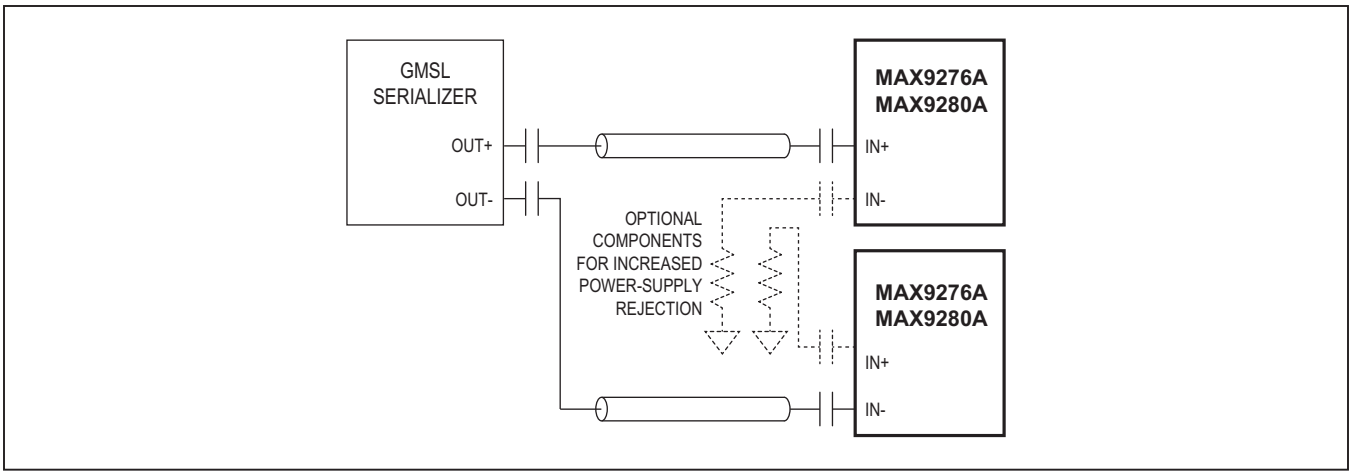


Figure 35. 2:1 Coax Splitter Connection Diagram

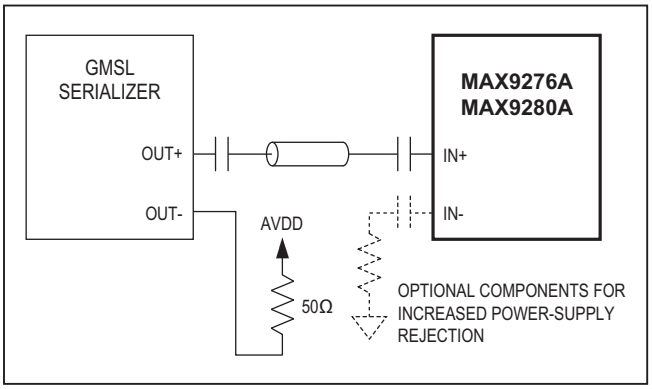


Figure 36. Coax Connection Diagram

Table 10. Configuration Input Map

CX/TP	FUNCTION
High	Coax+ input. 7-bit device address is XXXXXX0 (bin).
Mid	Coax- input. 7-bit device address is XXXXXX1 (bin).
Low	Twisted-pair input. 7-bit device address is XXXXXX0 (bin).

HS/VS/DE Tracking

The deserializer has tracking to filter out HS/VS/DE bit or packet errors. HS/VS/DE tracking is on by default when the device is in high-bandwidth mode (BWS = open), and off by default when in 24-bit or 32-bit mode (BWS = low or high). Set/clear HVTREN (D6 of register 0x15) to enable/disable HS/VS tracking. Set/clear DETREN (D5 of register 0x15) to enable/disable DE tracking. By default, the device uses a partial and full periodic tracking of HS/DE. Set HVTRMODE = 0 (D4 of register 0x15) to disable full periodic tracking. HS/VS/DE tracking can be turned on in 24-bit and 32-bit modes to track and correct against bit errors in HS/VS/DE link bits.

Serial Input

The device can receive serial data from two kinds of cable: 100Ω twisted pair and 50Ω coax. (Contact the factory for devices compatible with 75Ω cables).

Coax Splitter Mode

In coax mode, OUT+ and OUT- of the serializer are active. This enables the use as a 1:2 splitter (Figure 35). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control-channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique address to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to V_{DD} through a 50Ω resistor (Figure 36). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable forward and reverse channel links according to the communicating deserializer connection to prevent contention in I^2C to I^2C mode. Use ENREVP or ENREVN register bits to disable/enable the control-channel link. In UART mode, the serializer provides arbitration of the control-channel link.

Cable-Type Configuration Input

CX/TP determine the power-up state of the serial input. In coax mode, CX/TP also determine which coax input is active, along with the default device address (Table 10).

Color Lookup Tables

The deserializer includes three color lookup tables (LUT) to support automatic translation of RGB pixel values. This feature can be used for color gamma correction, brightness/contrast or for other purposes. There are three lookup tables, each 8 bits wide and 256 entries deep, enabling a 1-to-1 translation of 8-bit input values to any 8-bit output value for each color (24 bits total).

Programming and Verifying LUT Data

The µC must set the LUTPROG register bit to 1 before programming and verifying the tables. To program a LUT, the µC generates a write packet with register address set to the assigned register address for respective LUT (0x7D, 0x7E, or 0x7F). The deserializer writes data in the packet to the respective LUT starting from the LUT address location set in LUTADDR register. Successive bytes in the data packet are written to the next LUT address location, however each new data packet write starts from the address location stored in the LUTADDR register. Use 0x00 for LUTADDR and 0x00 as the number of bytes field in UART packet, when writing a 256 byte data-block, because 8-bit wide number of bytes field cannot normally represent 9-bit wide “256” value. There is no number of bytes field in I^2C-to-I^2C modes.

To read back the contents of an LUT, the µC generates a read packet with register address set to the assigned register address for respective LUT (0x7D, 0x7E, or 0x7F). The deserializer outputs read data from the respective LUT starting from the LUT address location set in the LUT_ADDR register. Similar to the write operation, use 0x00 for LUTADDR and 0x00 as the number of bytes field in UART packet, when reading a 256-byte data block.

LUT Color Translation

After power-up or going out of sleep or power-down modes, LUT translation is disabled and LUT contents are unknown. After program and verify operations are finished, in order to enable LUT translations, set LUTPROG bit to 0 and set the respective LUT enable bits (RED_LUT_EN, GRN_LUT_EN, BLU_LUT_EN) to 1 to enable the desired LUT translation function. Only the selected colors are translated by the LUT (the other colors are not touched). The µC does not need to fill in all three color lookup tables if all 3 color translations are not needed.

After a pixel is deserialized decoded and decrypted (if necessary) it is segmented into its color components Red, Green and Blue according to Table 11 and Figure 37. If LUT translation is enabled, each 8-bit pre-translation color value is used as address to the respective LUT table to look up the corresponding (translated) 8-bit color value.

LUT Bit Width

In 32-bit mode and high-bandwidth mode, 24 bits are available for color data (8 bits per color) and each LUT is used for 8-bit to 8-bit color translation. In 24-bit mode, the deserializer can receive only up to 18-bit color (6 bits per color). The LUT tables can translate from 6-bit to 6-bit, using the first 64 locations (0x00 to 0x3F). Program the MSB 2 bits of each LUT value to 00. Alternatively, program full 8-bit values to each LUT for 6-bit to 8-bit color translation.

Table 11. Pixel Data Format

DOUT [5:0]	DOUT [11:6]	DOUT [17:12]	DOUT 18	DOUT 19	DOUT 20	DOUT [22:21]	DOUT [24:23]	DOUT [26:25]
R[5:0]	G[5:0]	B[5:0]	HS	VS	DE	R[7:6]	G[7:6]	B[7:6]

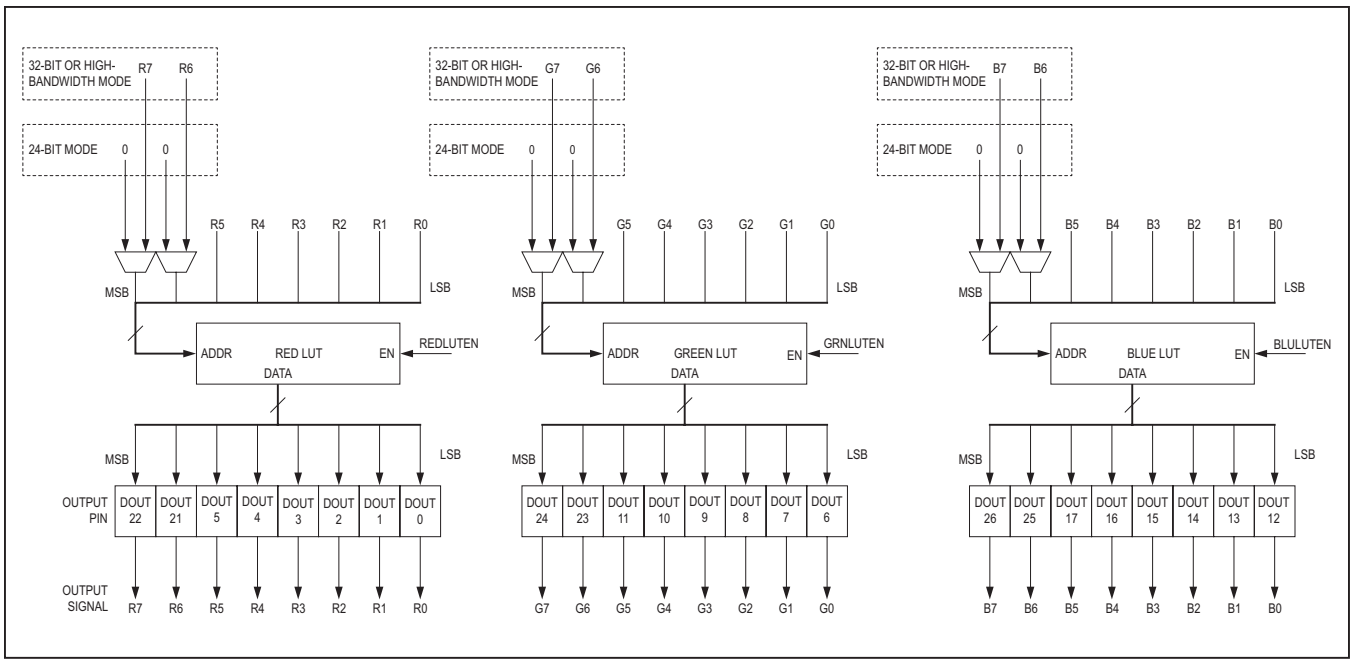


Figure 37. LUT Dataflow

Recommended LUT Program Procedure

1) Write LUTPROG = 1 to register 0x7C. Keep BLULUTEN = 0, GRNLUTEN = 0, REDLUTEN = 0 (write 0x08 to register 0x7C).
2) Write contents of red LUT with a single write packet. For 24-bit RGB, use 0x7D as register address and 0x00 as number of bytes (UART only) and write 256 bytes. For 18-bit RGB, use 0x7D as register address and 0x40 as number of bytes (UART only) and write 64 bytes. (Optional: Multiple write packets can be used if LUTADDR is set before each LUT write packet.)
3) Read contents of red LUT and verify that they are correct. Use the same register address and number of bytes used in the previous step.
4) Repeat steps 2 and 3 for the green LUT, using 0x7E as the register address
5) Repeat steps 2 and 3 for the blue LUT, using 0x7F as the register address

6a) To finish the program and verify routine, without enabling the LUT color translation, write LUTPROG = 0 (write 0x00 to register 0x7C).

6b) To finish the program and verify routine, and start LUT color translation, write LUTPROG = 0, BLULUTEN = 1, GRNLUTEN = 1, REDLUTEN = 1 (Write 0x07 to register 0x7C).

Table 12. Reverse Control-Channel Modes

HIGHIMM BIT OR SD/HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL-CHANNEL MODE	MAX UART/ I²C BIT RATE (kbps)
LOW (1)	X	Legacy reverse control-channel mode (compatible with all GMSL devices)	1000
HIGH (1)	0	High-immunity mode	500
	1	Fast high-immunity mode	1000

X = Don't care.

Table 13. Fast High-Immunity Mode Requirements

BWS SETTING	ALLOWED PCLKOUT FREQUENCY (MHz)
Low	> 40
High	> 30
Open	> 80

Fast high-immunity mode requires DRS = 0.

High-Immunity Reverse Control-Channel Mode

The deserializer contains a high-immunity reverse control-channel mode, which has increased robustness at half the bit rate over the standard GMSL reverse control-channel link (Table 12). Set HIM on the serializer and on the deserializer to use high-immunity mode at power-up. Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control-channel mode. The deserializer reverse channel mode is not available for 500µs/1.92ms after the reverse control-channel mode is changed through the serializer/deserializer's HIGHIMM bit setting, respectively. The user must set HIM or the HIGHIMM bits to the same value for proper reverse control-channel communication.

In high-immunity mode, Set HPFTUNE = 00 in the equalizer, if the serial bit rate = [PCLKOUT x 30 (BWS = low or open) or 40 (BWS = high)] is larger than 1Gbps when BWS is low or high. When BWS = open, set HPFTUNE = 00 when the serial bit rate is larger than 2GBps. In addition, use 47nF AC-coupling capacitors. Note that legacy reverse control-channel mode may not function when using 47nF AC-coupling capacitors.

By default, high-immunity mode uses a 500kbps bit rate. Set REVFAST =1 (D7 in register 0x1A in the serializer and register 0x11 in the deserializer) in both devices to use a 1Mbps bit rate. Certain limitations apply when using the fast high-immunity mode (Table 13).

Sleep Mode

The deserializers have sleep mode to reduce power consumption. The devices enter or exit sleep mode by a command from a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. Entering sleep mode resets the HDCP registers, but not the configuration registers. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

To wake up from the local side, send an arbitrary control-channel command to deserializer, wait for 5ms for the chip to power up and then write 0 to SLEEP register bit to make the wake-up permanent. To wake up from the remote side, enable serialization. The deserializer detects the activity on the serial link and then when it locks, automatically sets its SLEEP register bit to 0.

Power-Down Mode

The deserializers have a power-down mode which further reduces power consumption compared to sleep mode. Set PWDN low to enter power-down mode. In power-down, the parallel outputs remain high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins ADD[2:0], CX/TP, I2CSEL, SD/HIM, and BWS are latched.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 14 lists the startup procedure for display applications. Table 15 lists the startup procedure for image-sensing applications. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable for 2ms after power-up.

Table 14. Startup Procedure for Video-Display Applications

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to serializer	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low
1	Powers up	Powers up and loads default settings. Establishes video link when valid PCLK available	Powers up and loads default settings	Powers up and loads default settings. Locks to video link signal if available.
2	Enables serial link by setting SEREN = 1 or configuration link by setting SEREN = 0 and CLINKEN = 1 (if valid PCLK not available) and gets an acknowledge. Waits for link to be establish (~3ms)	—	Establishes configuration or video link	Locks to configuration or video link signal
3	Writes configuration bits in the serializer/deserializer and gets an acknowledge.	Configuration changed from default settings		Configuration changed from default settings
4	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for video link to be established (~3ms)	Establishes video link when valid PCLK available (if not already enabled)		Locks to video link signal (if not already locked)
5	Begin sending video data to input	Video data serialized and sent across serial link		Video data received and deserialized

Table 15. Startup Procedure for Image-Sensing Applications (CDS = High)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to deserializer	Sets all configuration inputs	Sets all configuration inputs	Sets all configuration inputs
1	Powers up	Powers up and loads default settings. Establishes video link when valid PCLK available.	Powers up and loads default settings. Goes to sleep after 8ms.	Powers up and loads default settings. Locks to video link signal if available.
2	Writes deserializer configuration bits and gets an acknowledge	—	—	Configuration changed from default settings
3	Wakes up the serializer by sending dummy packet, and then writing SLEEP = 0 within 8ms. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	—	Wakes up	—
4	Writes serializer configuration bits. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	Configuration changed from default settings		—
5	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for serial link to be established (~3ms)	Establishes video link when valid PCLK available (if not already enabled)		Locks to video link signal (if not already locked)
6	Begin sending video data to input	Video data serialized and sent across serial link		Video data received and deserialized

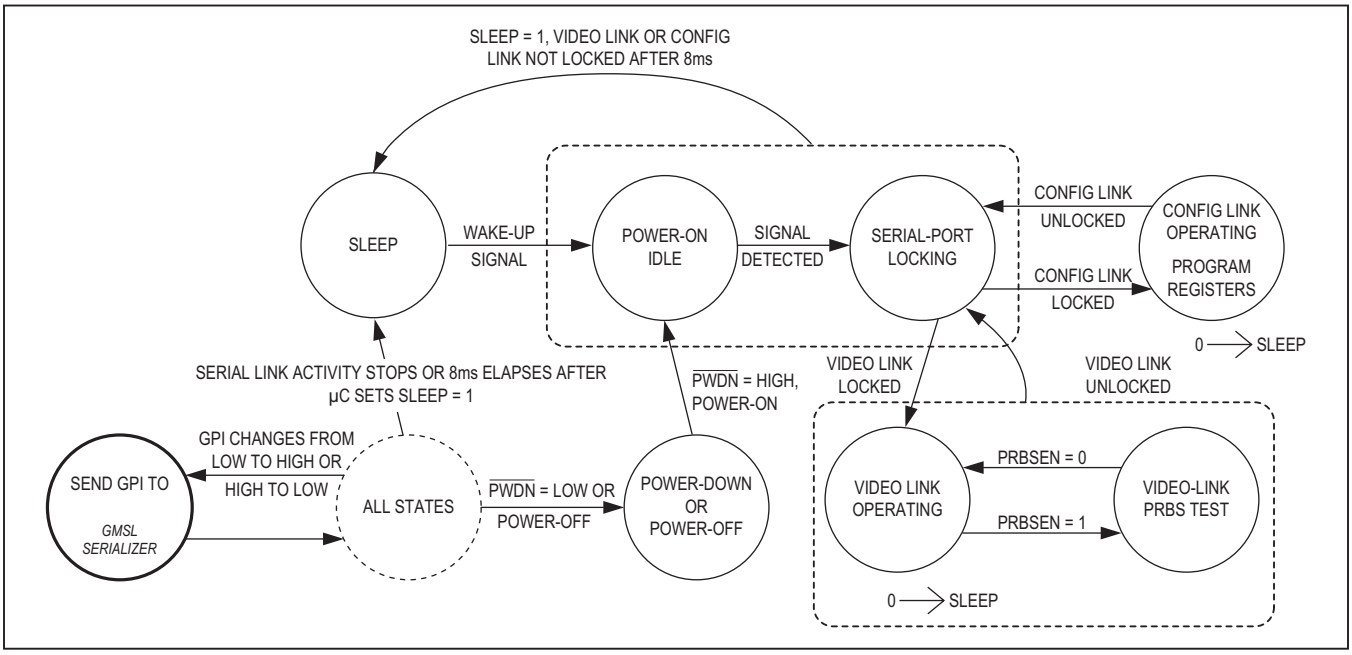


Figure 38. State Diagram

High-Bandwidth Digital Content Protection (HDCP)

Note: The explanation of HDCP operation in this data sheet is provided as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the HDCP System v1.3 Amendment for GMSL, which is available from DCP.

HDCP has two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the GMSL serializer. The GMSL serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the GMSL serializer and writes it to the deserializer. The µC then reads the GMSL serializer public key selection vector (AKSV) and writes it to the deserializer. The µC then reads the deserializer KSV (BKSV) and writes it to the GMSL serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the GMSL serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response-value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the GMSL serializer. The GMSL serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the GMSL serializer/deserializer.

During response-value generation and comparison, the host µC checks for a valid BKSV (having 20 1s and 20 0s is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3, Appendix C). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the GMSL serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The GMSL serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the GMSL serializer/deserializer provide response values for the enhanced link verification. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization. For this option, the GMSL serializer and deserializer generate 8-bit enhanced link-verification response values (PJ and PJ') every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the GMSL serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the GMSL serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The GMSL serializer/deserializer include features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater-authentication protocol, the deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on the repeater module). Both the GMSL serializer and deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater

modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

HDCP Authentication Procedures

The GMSL serializer generates a 64-bit random number exceeding the HDCP requirement. The GMSL serializer/deserializer internal one-time programmable (OTP) memories contain a unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The GMSL serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the HDCP 1.3 Amendment for GMSL for details). The µC must perform link integrity checks while encryption is enabled (see Table 17). Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the GMSL serializer before starting a new authentication attempt.

HDCP Protocol Summary

Table 16, Table 17, and Table 18 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

Table 16. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer to mask A/V data at the input of the GMSL serializer. Starts the link by writing SEREN = H or link starts automatically if $\overline{AUTOS}$ is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and makes sure the link is established.	—	—
5	Optionally writes a random-number seed to the GMSL serializer.	Combines seed with internally generated random number. If no seed provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the GMSL serializer.	Generates (stores) AN, and resets the START_AUTHENTICATION bit to 0.	—
7	Reads AN and AKSV from the GMSL serializer and writes to the deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from and deserializer writes to the GMSL serializer.	Generates R0, triggered by the µC's write of BKSV.	—

Table 16. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
9	Reads the INVALID_BKSV bit of the GMSL serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the deserializer and reads R0 from the GMSL serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, GMSL serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the GMSL serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and GMSL serializer (if the FC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the GMSL serializer).	Encryption enabled after the next VSYNC falling edge.	Decryption enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 17. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the GMSL serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the GMSL serializer and makes sure it is stable (matches the previous RI that it has read from the GMSL serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the FC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 18. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates PJ and updates the PJ register every 16 VSYNC cycles.	Generates PJ' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames, reads PJ from the GMSL serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful; go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after 3 mismatches. After the detection of failure of enhanced link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Example Repeater Network—Two µCs

The example shown in Figure 39 has one repeater and two µCs. Table 19 summarizes the authentication operation.

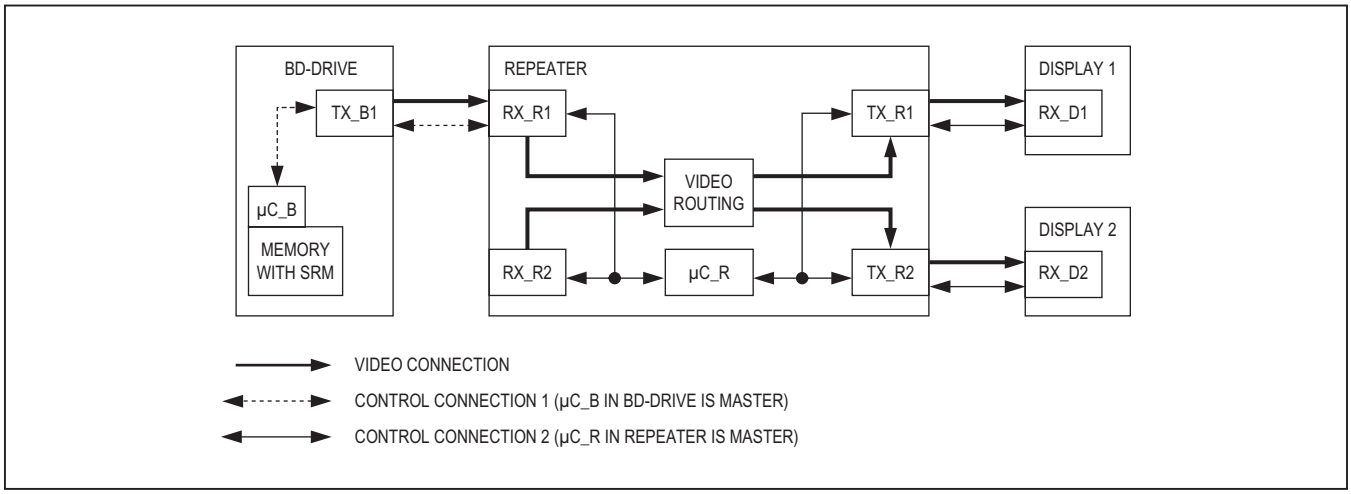


Figure 39. Example Network with One Repeater and Two µCs (Tx = GMSL Serializer's, Rx = Deserializer's)

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until proper acknowledge frame received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_R1 by the µC_B (step 7). For example, to satisfy this requirement, RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit, or µC_B can poll µC_R before starting authentication.	—	—

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
3	Makes sure that A/V data not requiring protection (low-value content) is available at the TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1, or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if $\overline{\text{AUTOS}}$ of transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.
5	Reads the locked bit of RX_R1 and makes sure the link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and makes sure the link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and makes sure the link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random number seed to TX_B1.	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change GPIO functionality used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_R1 (see steps 6–10 in Table 16).	—	TX_B1: According to commands from µC_B, generates AN, computes R0.	RX_R1: According to commands from µC_B, computes R0'.

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
8	—	When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol between the (TX_R1, RX_D1) and (TX_R2, RX_D2) links (see steps 6–10 in Table 16).	TX_R1, TX_R2: According to commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to commands from µC_R, computes R0'.
9	Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not complete yet so it makes sure A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.	—	TX_B1: Encryption enabled after next VSYNC falling edge.	RX_R1: Decryption enabled after next VSYNC falling edge.
10	—	When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.	TX_R1, TX_R2: Encryption enabled after next VSYNC falling edge.	RX_D1, RX_D2: Decryption enabled after next VSYNC falling edge.
11	Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until proper acknowledge frame is received and bit is read as 1.	Blocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until proper acknowledge frame received.	—	RX_R1: Control channel from serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.
12		Writes BKSVs of RX_D1 and RX_D2 to the KSV list in RX_R1. Then, calculates and writes the BINFO register of RX_R1.	—	RX_R1: Triggered by µC_R's write of BINFO, calculates hash value (V') on the KSV list, BINFO and the secret-value M0'.
13		Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.	—	RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
14	Reads the KSV list and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash value (V) on the KSV list, BINFO and the secret-value M0.	—
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV list and BKSV of RX_R1 in the Key Revocation list.	—	—	—
17	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
18	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) Host µC begins authentication with the HDCP repeater's input receiver.
2) When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
3) HDCP repeater's µC waits for a low-to-high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
4) HDCP repeater's µC resets the AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function for notification when encryption is enabled/disabled by an upstream µC.

Applications Information

Self PRBS Test

The serializers include a PRBS pattern generator which works with bit-error verification in the deserializer. To run the PRBS test, disable encryption (if used), set DISHSFILT, DISVSFILT, and DISDEFILT to '1', to disable glitch filter in the deserializer. Then, set PRBSEN = 1 (0x04, D5) in the serializer and then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer and then in the serializer.

Error Checking

The deserializers check the serial link for errors and store the number of decoding errors in the 8-bit registers DECERR (0x0D). If a large number of decoding errors are detected within a short duration (error rate ≥ 1/4), the deserializers lose lock and stop the error counter. The deserializers then attempt to relock to the serial data. DECERR reset upon successful video link lock, successful readout of the register (through µC), or whenever auto error reset is enabled. The deserializers use a separate PRBS Register during the internal PRBS test, and DECERR are reset to 0x00.

$\overline{ERR}$ Output

The deserializers have an open-drain ERR output. This output asserts low whenever the number of decoding errors exceeds the error thresholds during normal operation, or when at least 1 PRBS error is detected during PRBS test. $\overline{ERR}$ reasserts high whenever DECERR resets, due to DECERR readout, video link lock, or auto error reset.

Auto Error Reset

The default method to reset errors is to read the respective error registers in the deserializers (0x0D and 0x0E). Auto error reset clears the error counters DECERR and the $\overline{ERR}$ output ~1µs after ERR goes low. Auto error reset is disabled on power-up. Enable auto error reset through AUTORST (0x06, D5). Auto error reset does not run when the device is in PRBS test mode.

Dual µC Control

Usually systems have one microcontroller to run the control channel, located on the serializer side for display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously, and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention will occur if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher level protocol. In addition, the control channel does not provide arbitration between I^2C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock ($f_{PCLKOUT}$) and the control-channel clock (f_{UART}/f_{I2C}) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 500µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss-of-synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the GPI input. If other sources use the GPI input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Providing a Frame Sync (Camera Applications)

The GPI/GPO provide a simple solution for camera applications that require a Frame Sync signal from the ECU (e.g. surround-view systems). Connect the ECU Frame Sync signal to the GPI input, and connect GPO output to the camera Frame Sync input. GPI/GPO has a typical delay of 275µs. Skew between multiple GPI/GPO channels is typically 115µs. If a lower skew signal is required, connect the camera's frame sync input one of the deserializer's GPIOs and use an I^2C broadcast write command to change the GPIO output state. This has a maximum skew of 1.5µs, independent from the used I^2C bit rate.

Software Programming of the Device Addresses

The serializers and deserializers have programmable device addresses. This allows multiple GMSL devices, along with I^2C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

3-Level Configuration Inputs

CX/TP and BWS are 3-level inputs that control the serial interface configuration and power-up defaults. Connect 3-level inputs through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or open to set a mid level. For digital control, use three-state logic to drive the 3-level logic input.

Configuration Blocking

The deserializers can block changes to registers. Set CFGBLOCK to make registers 0x00 to registers 0x1F as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Compatibility with Other GMSL Devices

The deserializers are designed to pair with the MAX9275–MAX9281 serializers but interoperates with any GMSL serializers. See the Table 20 for operating limitations

Key Memory

Each device has a unique HDCP key set that is stored in secure nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

HS/VS/DE Inversion

The deserializer uses an active-high HS, VS, and DE for encoding and HDCP encryption. Set INVHSYNC, INVVSYNC, and INVDE in the serializer to invert active-low input signals for use with the GMSL devices. Set INVHSYNC, INVVSYNC, and INVDE in the deserializer (register 0x14) to output active-low signals for use with downstream devices.

WS/SCK Inversion

The deserializer uses standard polarities for I^2S. Set INVWS, INVSCK in the serializer (register 0x1B) to invert opposite polarity signals for use with the GMSL devices. Set INVWS, INVSCK in the deserializer (register 0x1D) to output reverse-polarity signals for downstream use.

Table 20. MAX9276A/MAX9280A Feature Compatibility

MAX9276A/MAX9280A FEATURE	GMSL SERIALIZER
HDCP (MAX9280A only)	If feature not supported in serializer, must not be turned on in the MAX9280A
High-bandwidth mode	If feature not supported in serializer, must only use 24-bit and 32-bit modes
I^2C to I^2C	If feature not supported in serializer, must use UART to I^2C or UART to UART
Coax	If feature not supported in serializer, must connect unused serial output through 200nF and 50Ω in series to V_{DD} and set the reverse control-channel amplitude to 100mV.
High-immunity control channel	If feature not supported in serializer, must use the legacy reverse control-channel mode
TDM encoding	If feature not supported in serializer, must use I^2S encoding (with 50% WS duty cycle), if supported
I^2S encoding	If feature not supported in serializer must disable I^2S in the MAX9276A/MAX9280A

Table 21. Staggered Output Delay

OUTPUT	OUTPUT DELAY RELATIVE TO DOUT0 (ns)	
	DISSTAG = 0	DISSTAG = 1
DOUT0–DOUT5, DOUT21, DOUT22	0	0
DOUT6–DOUT10, DOUT23, DOUT24	0.5	0
DOUT11–DOUT15, DOUT25, DOUT26	1	0
DOUT16–DOUT20, DOUT27, DOUT28	1.5	0
PCLKOUT	0.75	0

GPIOs

The deserializers have two open-drain GPIOs available when not used for HDCP purposes (see the *Notification of Start of Authentication and Enable of Encryption to Downstream Links* section), GPIO1OUT and GPIO0OUT (0x06, D3 and D1) set the output state of the GPIOs. Setting the GPIO output bits to '0' low pulls the output low, while setting the bits to '1' leaves the output undriven, and pulled high through internal/external pullup resistors. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06, D2 and D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Staggered Parallel Outputs

The deserializers stagger the parallel data outputs to reduce EMI and noise. Staggering outputs also reduces the power-supply transient requirements. By default, the deserializers stagger outputs according to Table 21. Disable output staggering through the DISSTAG bit (0x06, D7).

Internal Input Pulldowns

The control and configuration inputs (except 3-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

Choosing I²C/UART Pullup Resistors

I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential, 50Ω single ended). This leaves the capacitor selection to change the system time constant. Use at 0.22µF (using legacy reverse control channel), 47nF (using high-immunity reverse control channel), or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The deserializers use an AVDD and DVDD of 3.0V to 3.6V. All single-ended inputs and outputs except for the serial input derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Power-Supply Table

Power-supply currents shown in the *DC Electrical Characteristics* table is the sum of the currents from AVDD, DVDD, and IOVDD. IOVDD is measured at V_{IOVDD} = 3.6V. If using a different IOVDD voltage, the IOVDD worst-case supply current will vary according to Table 22. HDCP operation (MAX9280A only) draws additional current. This is shown in Table 23.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω, contact the factory for 75Ω operation). Table 24 lists the suggested cables and connectors used in the GMSL link.

Table 22. IOVDD Current Simulation Results

IOVDD WORST-CASE SUPPLY CURRENT		IOVDD SUPPLY VOLTAGE			
		1.9V	3.3V*	3.6V	
BWS = low, $f_{PCLKOUT}$ = 16.6MHz	C_L = 5pF	**4.4**	7.9	**8.6**	mA
	C_L = 10pF	**6.4**	12.4	**13.5**	
BWS = low, $f_{PCLKOUT}$ = 33.3MHz	C_L = 5pF	**8**	14.5	**15.8**	
	C_L = 10pF	**13.2**	23.1	**25.2**	
BWS = low, $f_{PCLKOUT}$ = 66.6MHz	C_L = 5pF	**14.9**	25.6	**27.9**	
	C_L = 10pF	**23.4**	40.7	**44.4**	
BWS = low, $f_{PCLKOUT}$ = 104MHz	C_L = 5pF	**21.6**	38.7	**42.2**	
	C_L = 10pF	**34.8**	60.3	**65.8**	
BWS = mid, $f_{PCLKOUT}$ = 36.6MHz	C_L = 5pF	**10.2**	18.2	**19.8**	
	C_L = 10pF	**16.6**	28.9	**31.5**	
BWS = mid, $f_{PCLKOUT}$ = 104MHz	C_L = 5pF	**25.1**	45	**49**	
	C_L = 10pF	**40.4**	70.2	**76.5**	

Table 23. Additional Supply Current from HDCP (MAX9280A Only)

PCLK (MHz)	MAXIMUM HDCP CURRENT (mA)
16.6	6
33.3	9
36.6	9
66.6	12
104	18

Table 24. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	Dacar 302	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 535-2	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

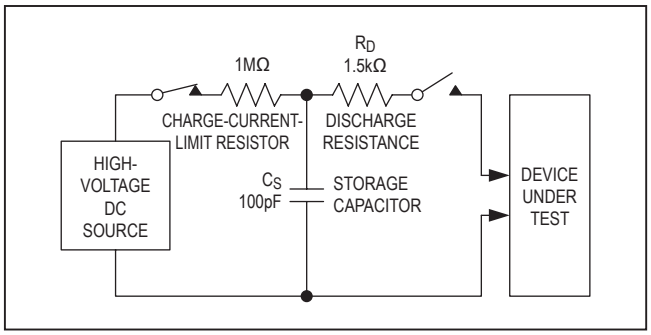


Figure 40. Human Body Model ESD Test Circuit

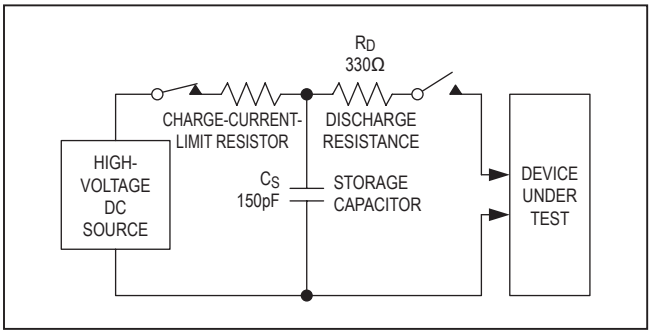


Figure 41. IEC 61000-4-2 Contact Discharge ESD Test Circuit

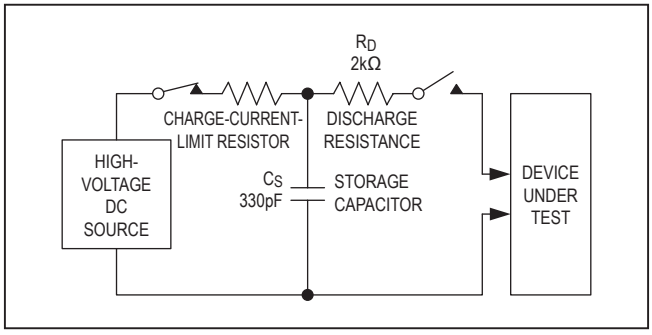


Figure 42. ISO 10605 Contact Discharge ESD Test Circuit

Board Layout

Separate LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance for STP. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax.

Route the PCB traces for differential CML channel in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 40). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 41). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 42).

Table 25. Register Table (see Table 26)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address (power-up default value depends on latched address pin level)	XX00XX0
	D0	—	0	Reserved	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address (power-up default value depends on latched address pin level)	XX01XXX
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x02	D[7:6]	SS	00	No spread spectrum	00
			01	±2% spread spectrum	
			10	No spread spectrum	
			11	±4% spread spectrum	
	D5	AUDIOMODE	0	WS, SCK configured as output (deserializer sourced clock)	0
			1	WS, SCK configured as input (system sourced clock)	
	D4	AUDIOEN	0	Disable I^2S/TDM channel	1
			1	Enable I^2S/TDM channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial-data rate	11
			01	1 to 2Gbps serial-data rate	
			10	2 to 3.12Gbps serial-data rate	
			11	Automatically detect serial-data rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread modulation rate only once after locking	00
			01	Calibrate spread-modulation rate every 2ms after locking	
			10	Calibrate spread-modulation rate every 16ms after locking	
			11	Calibrate spread-modulation rate every 256ms after locking	
	D5	—	0	Reserved	0
	D[4:0]	SDIV	00000	Auto calibrate sawtooth divider	00000
			XXXXX	Manual SDIV setting (see the *Manual Programming of the Spread-Spectrum Divider* section)	

Table 25. Register Table (see Table 26) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	LOCKED	0	LOCK output is low	0 (Read only)
			1	LOCK output is high	
	D6	OUTENB	0	Enable outputs (power-up default value depends on $\overline{\text{ENABLE}}$ pin value at power-up)	0, 1
			1	Disable outputs (power-up default value depends on $\overline{\text{ENABLE}}$ pin value at power-up)	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode (power-up default value depends on MS pin value at power-up)	0, 1
			1	Activate sleep mode (power-up default value depends on MS pin value at power-up)	
	D[3:2]	INTTYPE	00	Local control channel uses I^2C when I2CSEL = 0	01
			01	Local control channel uses UART when I2CSEL = 0	
			10, 11	Local control channel disabled	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending)	1
			1	Enable reverse control channel to serializer (sending)	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving)	1
			1	Enable forward control channel from serializer (receiving)	
0x05	D7	I2CMETHOD	0	I^2C conversion sends the register address when converting UART to I^2C	0
			1	Disable sending of I^2C register address when converting UART to I^2C (command-byte-only mode)	
	D[6:5]	HPFTUNE	00	7.5MHz equalizer highpass-filter cutoff frequency	01
			01	3.75MHz equalizer highpass-filter cutoff frequency	
			10	2.5MHz equalizer highpass-filter cutoff frequency	
			11	1.87MHz equalizer highpass-filter cutoff frequency	
	D4	PDEQ	0	Enable equalizer	0
			1	Disable equalizer	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain	1001
			0001	2.8dB equalizer boost gain	
			0010	3.4dB equalizer boost gain	
			0011	4.2dB equalizer boost gain	
			0100	5.2dB equalizer boost gain	
			0101	6.2dB equalizer boost gain	
			0110	7dB equalizer boost gain	
			0111	8.2dB equalizer boost gain	
			1000	9.4dB equalizer boost gain	
			1001	10.7dB equalizer boost gain. **Power-up default.**	
			1010	11.7dB equalizer boost gain	
			1011	13dB equalizer boost gain	
			11XX	Do not use	

Table 25. Register Table (see Table 26) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x06	D7	DISSTAG	0	Enable staggered outputs	0
			1	Disable staggered outputs	
	D6	AUTORST	0	Do not automatically reset error registers and outputs	0
			1	Automatically reset DECERR register 1µs after ERR asserts	
	D5	DISGPI	0	Enable GPI-to-GPO signal transmission to serializer	0
			1	Disable GPI-to-GPO signal transmission to serializer	
	D4	GPIIN	0	GPI input is low	0 (Read only)
			1	GPI input is high	
	D3	GPIO1OUT	0	Set GPIO1 to low	1
			1	Set GPIO1 to high	
	D2	GPIO1IN	0	GPIO1 input is low	0 (Read only)
			1	GPIO1 input is high	
	D1	GPIO0OUT	0	Set GPIO0 to low	1
			1	Set GPIO0 to high	
	D0	GPIO0IN	0	GPIO0 input is low	0 (Read only)
			1	GPIO0 input is high	
0x07	D[7:0]	—	01010100	Reserved	01010100
0x08	D[7:3]	—	00110	Reserved	00110
	D2	DISDEFILT	0	Enable DE glitch filter (power-up default when BWS = high or low)	0
			1	Disable DE glitch filter (power-up default when BWS = open)	
	D1	DISVSFILT	0	Enable VS glitch filter (power-up default when BWS = high or low)	0
			1	Disable VS glitch filter (power-up default when BWS = open)	
	D0	DISHSFILT	0	Enable HS glitch filter (power-up default when BWS = high or low)	0
			1	Disable HS glitch filter (power-up default when BWS = open)	
0x09	D[7:0]	—	11001000	Reserved	11001000
0x0A	D[7:0]	—	00010XXX	Reserved	00010XXX
0x0B	D[7:0]	—	00100000	Reserved	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter	00000000 (Read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter	00000000 (Read only)
0x0F	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x10	D[7:0]	—	XXXXXXXX	Reserved	(Read only)

Table 25. Register Table (see Table 26) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x11	D7	REVFAST	0	High-immunity reverse channel mode uses 500kbps bit rate	0
			1	High-immunity reverse channel mode uses 1Mbps bit rate	
	D[6:0]	—	0100010	Reserved	0100010
0x12	D7	MCLKSRC	0	MCLK derived from PCLKOUT (see Table 5)	0
			1	MCLK derived from internal oscillator	
	D[6:0]	MCLKDIV	0000000	MCLK disabled	0000000
			XXXXXXX	MCLK divider	
0x13	D[7:0]	—	0X000000	Reserved	0X000000
0x14	D7	INVVSYNC	0	No VS inversion at the output	0
			1	Invert VS at the output	
	D6	INVHSYNC	0	No HS inversion at the output	0
			1	Invert HS at the output	
	D5	INVDE	0	No DE inversion at the output	0
			1	Invert DE at the output	
	D4	DRS	0	High data-rate mode	0
			1	Low data-rate mode	
	D3	DCS	0	Normal parallel-output-driver current	0
			1	Boosted parallel-output-driver current	
	D2	DISRWAKE	0	Enable remote wake-up	0
			1	Disable remote wake-up	
	D1	ES	0	Output data valid on rising edge of PCLKOUT	0
			1	Output data valid on falling edge of PCLKOUT	
	D0	INTOUT	0	Drive INTOUT low	0
			1	Drive INTOUT high	

Table 25. Register Table (see Table 25) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x15	D7	AUTOINT	0	INTOUT pin output controlled by INTOUT bit above	1
			1	Writes to any AVINFO bytes sets INTOUT to high. Reads to any AVINFO bytes sets INTOUT to low	
	D6	HVTREN	0	Disable HS/VS tracking (power-up default value depends on state of BWS input value at power-up)	0, 1
			1	Enable HS/VS tracking (power-up default value depends on state of BWS input value at power-up)	
	D5	DETREN	0	Disable DE tracking (power-up default value depends on state of BWS input value at power-up)	0, 1
			1	Enable DE tracking (power-up default value depends on state of BWS input value at power-up)	
	D4	HVTRMODE	0	Partial periodic HS/VS and DE tracking	1
			1	Partial and full periodic HS/VS and DE tracking	
	D[3:2]	—	00	Reserved	00
	D1	MCLKWS	0	MCLK output operates normally	0
			1	WS is output from MCLK (MCLK mirrors WS)	
	D0	MCLKPIN	0	MCLK output on DOUT28/CNTL2	0
			1	MCLK output on CNTL0/ADD0	
0x16	D7	HIGHIMM	0	Legacy reverse control-channel mode (power-up default value depends on SD/HIM at power-up)	0, 1
			1	High-immunity reverse control-channel mode (power-up default value depends on SD/HIM at power-up)	
	D[6:0]	—	1011010	Reserved	1011010
0x17	D[7:0]	—	000XXXXX	Reserved	000XXXXX
0x18	D[7:1]	I2CSRCA	XXXXXXX	I²C address translator source A	0000000
	D0	—	0	Reserved	0
0x19	D[7:1]	I2CDSTA	XXXXXXX	I²C address translator destination A	0000000
	D0	—	0	Reserved	0
0x1A	D[7:1]	I2CSRCB	XXXXXXX	I²C address translator source B	0000000
	D0	—	0	Reserved	0
0x1B	D[7:1]	I2CDSTB	XXXXXXX	I²C address translator destination B	0000000
	D0	—	0	Reserved	0

Table 25. Register Table (see Table 26) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1C	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available	1
			1	I^2C-to-I^2C slave generates local acknowledge when forward channel is not available	
	D[6:5]	I2CSLVSH	00	352ns/117ns I^2C setup/hold time	01
			01	469ns/234ns I^2C setup/hold time	
			10	938ns/352ns I^2C setup/hold time	
			11	1046ns/469ns I^2C setup/hold time	
	D[4:2]	I2CMSTBT	000	8.47kbps (typ) I^2C-to-I^2C master bit-rate setting	101
			001	28.3kbps (typ) I^2C-to-I^2C master bit-rate setting	
			010	84.7kbps (typ) I^2C-to-I^2C master bit-rate setting	
			011	105kbps (typ) I^2C-to-I^2C master bit-rate setting	
			100	173kbps (typ) I^2C-to-I^2C master bit-rate setting	
			101	339kbps (typ) I^2C-to-I^2C master bit-rate setting	
			110	533kbps (typ) I^2C-to-I^2C master bit-rate setting	
			111	837kbps (typ) I^2C-to-I^2C master bit-rate setting	
	D[1:0]	I2CSLVTO	00	64µs (typ) I^2C-to-I^2C slave remote timeout	10
			01	256µs (typ) I^2C-to-I^2C slave remote timeout	
			10	1024µs (typ) I^2C-to-I^2C slave remote timeout	
			11	No I^2C-to-I^2C slave remote timeout	
0x1D	D[7:3]	—	00000	Reserved	00000
	D2	AUDUFBEH	0	Audio FIFO repeats last audio word when FIFO is empty	0
			1	Audio FIFO outputs all zeros when FIFO is empty	
	D1	INVSCK	0	Do not invert SCK at output	0
			1	Invert SCK at output	
	D0	INVWS	0	Do not invert WS at output	0
			1	Invert WS at output	

X =

Table 25. Register Table (see Table 26) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1E	D[7:0]	ID	00100X10	Device identifier (MAX9276A = 0x22) (MAX9280A = 0x26)	00100X10 (Read only)
0x1F	D[7:5]	—	000	Reserved	000 (Read only)
	D4	CAPS	0	Not HDCP capable (MAX9276A)	(Read only)
			1	HDCP capable (MAX9280A)	
	D[3:0]	REVISION	XXXX	Device revision	(Read only)
0x40 to 0x5F	D[7:0]	AVINFO	XXXXXXXX	Audio/Video format/status/information bytes	All zeroes
0x77	D[7:0]	—	XXXXXXXX	—	(Read only)
0x78	D[7:0]	AUDOUPER	XXXXXXXX	Audio FIFO last overflow/underflow period (AUDIOMODE = 1 only)	(Read only)
0x79	D7	AUDOU	0	Audio FIFO is in underflow (AUDIOMODE = 1 only)	(Read only)
			1	Audio FIFO is in overflow (AUDIOMODE = 1 only)	
	D[6:0]	—	0000XXX	Reserved	0000XXX (Read only)
0x7B	D[7:0]	LUTADDR	XXXXXXXX	LUT start address for write and read	00000000
0x7C	D[7:4]	—	0000	Reserved	0000
	D3	LUTPROG	0	Disable LUT write and read	0
			1	Enable LUT write and read	
	D2	BLULUTEN	0	Disable blue LUT	0
			1	Enable blue LUT	
	D1	GRNLUTEN	0	Disable green LUT	0
			1	Enable green LUT	
	D0	REDLUTEN	0	Disable red LUT	0
			1	Enable red LUT	
0x7D	D[7:0]	REDLUT	XXXXXXXX	Red LUT value (see Table 11)	00000000
0x7E	D[7:0]	GREENLUT	XXXXXXXX	Green LUT value (see Table 11)	00000000
0x7F	D[7:0]	BLUELUT	XXXXXXXX	Blue LUT value (see Table 11)	00000000

Don't care.

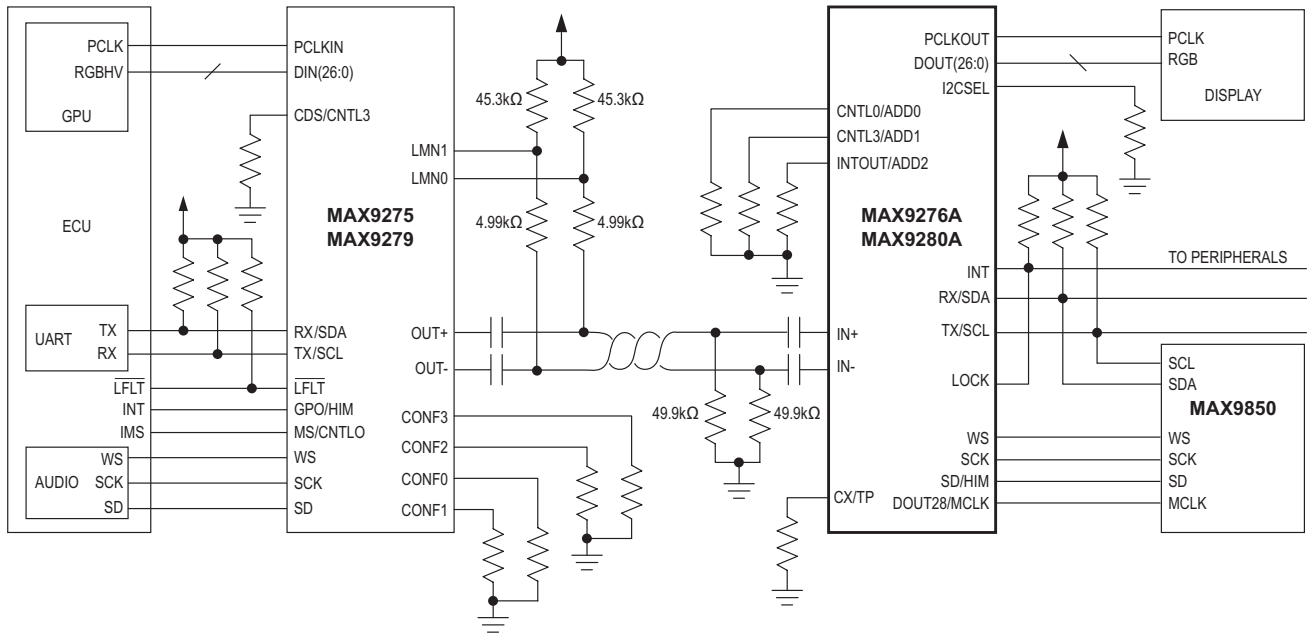
Table 26. HDCP Register Table (MAX9280A Only, see Table 25)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0X80 to 0x84	5	BKSV	Read only	HDCP receiver KSV	(Read only)
0X85 to 0x86	2	RI'	Read only	Link verification response	(Read only)
0X87	1	PJ'	Read only	Enhanced link verification response	(Read only)
0X88 to 0x8F	8	AN	Read/write	Session random number	0x0000000000000000
0X90 to 0x94	5	AKSV	Read/write	HDCP transmitter KSV	0x0000000000
0x95	1	BCTRL	Read/write	D7 = PD_HDCP 1 = Power down HDCP circuits 0 = HDCP circuits normal	0x00
				D[6:4] = Reserved	
				D3 = GPIO1_FUNCTION 1 = GPIO1 mirrors AUTH_STARTED 0 = normal GPIO1 operation	
				D2 = GPIO0_FUNCTION 1 = GPIO0 mirrors ENCRYPTION_ENABLE 0 = normal GPIO0 operation	
				D1 = AUTH_STARTED 1 = Authentication started (triggered by write to AKSV) 0 = Authentication not started	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	
0x96	1	BSTATUS	Read/write	D[7:2] = Reserved	0x00
				D1 = NEW_DEV_CONN 1 = Set to 1 if a new connected device is detected 0 = Set to 0 if no new device is connected	
				D0 = KSV_LIST_READY 1 = Set to 1 if KSV list and BINFO is ready 0 = Set to 0 if KSV list or BINFO is not ready	
0x97	1	BCAPS	Read/write	D[7:1] = Reserved	0x00
				D0 = REPEATER 1 = Set to one if device is a repeater 0 = Set to zero if device is not a repeater	
0x98 to 0x9F	8	—	Read only	Reserved	0x0000000000000000 (Read only)
0XA0 to 0xA3	4	V'.H0	Read/write	H0 part of SHA-1 hash value	0x00000000
0XA4 to 0xA7	4	V'.H1	Read/write	H1 part of SHA-1 hash value	0x00000000
0XA8 to 0xAB	4	V'.H2	Read/write	H2 part of SHA-1 hash value	0x00000000
0XAC to 0xAF	4	V'.H3	Read/write	H3 part of SHA-1 hash value	0x00000000
0XB0 to 0xB3	4	V'.H4	Read/write	H4 part of SHA-1 hash value	0x00000000

Table 26. HDCP Register Table (MAX9280A Only, see Table 25) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0XB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to one if more than seven cascaded devices attached 0 = Set to zero if seven or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to one if more than 14 devices attached 0 = Set to zero if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSVs downstream repeaters and receivers (maximum of 14 devices)	All zeros

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	21-0135	90-0046
56 SWTQFN-EP	T5688Y+5	21-100046	90-100023

Ordering Information

PART	PIN-PACKAGE	HDCP
MAX9276AGTN+	56 TQFN-EP*	No
MAX9276AGTN/V+	56 TQFN-EP*	No
MAX9276AGTN/VY+	56 SWTQFN-EP*	No
MAX9280AGTN+	56 TQFN-EP*	Yes**
MAX9280AGTN/V+	56 TQFN-EP*	Yes**
MAX9280AGTN/VY+***	56 SWTQFN-EP*	Yes**

Note: *All devices operate over the -40°C to +105°C temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V Denotes an automotive-qualified part.
SW = Side-wettable package.
**EP = Exposed pad.*
***HDCP parts require registration with Digital Content Protection, LLC.*
****Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/16	Initial release	—
1	3/17	Various updates, beginning with *AC Electrical Characteristics*	12, 13, 18, 20, 24, 32, 35, 40, 44, 57, 59, 63
2	3/18	Deleted QFND package and added side-wettable TQFN (SWTQFN) package in *General Description*, *Absolute Maximum Ratings*, *Package Thermal Characteristics*, *Pin Configuration*, *Package Information*, and *Ordering Information*; corrected AVINFO register address from "0x40 to 0x59" to "0x40 to 0x5F" in Table 25; added MAX9276AGTN/VY+ and MAX9280AGTN/VY+ (future product) to *Ordering Information*	1, 7, 17, 67, 70
3	10/19	Updated *Package Information*	70

