## **Recommended Operating Conditions** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V <sub>CC</sub> supply voltage	V <sub>CC</sub>		6 to 15	V
SOFTST input voltage range	VSOFTST		0 to VREG	V
FR input voltage range	$V_{FR}$		0 to VREG	V
MINSP input voltage range	V <sub>MINSP</sub>		0 to VREG	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# **Electrical Characteristics** at Ta = 25°C, $V_{CC} = 12$ V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
- arameter			min	typ	max	Onne
Circuit current 1	I <sub>CC</sub> 1			2.6	3.6	mA
Charge pump block						
Charge pump output voltage	V <sub>VG</sub>			17		٧
Regulator block						
5V regulator voltage	V <sub>VREG</sub>		4.75	5	5.25	V
Output on resistance			•			
Sum of high-/low-side output transistor on	Ron (H+L)	I <sub>O</sub> = 0.7A, V <sub>CC</sub> = 12V, VG = 17V		1.2	2	Ω
resistance Startup oscillator (OSC) pin		<u> </u>				
OSC pin charge current	losoC			-2.5		μА
OSC pin discharge current	IOSCC			2.5		
-	IoscD			2.5		μА
PWM input (PWMIN) pin	\\-\ \\-\ \\\-\ \\\\-\ \\\\-\ \\\\\\\\-\ \\\\\\		0.5		VDEO	١,,
High-level input voltage range	V <sub>PWMIN</sub> H		2.5		VREG	V
Low-level input voltage range	V <sub>PWMIN</sub> L		0		1	V
Range of PWM input frequency	fPWMIN		15		60	kHz
Minimum pulse width	T <sub>MINPW</sub>	Input HIGH voltage 5[V] and input LOW voltage 0[V]			0.2	μS
Duty cycle range is determined by	I.	, ,		l	J	
$(T_{MINPW} \times f_{PWMIN}) \times 100\%$ for minim $(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60$ [kHz], the input PWM duty When $f_{PWMIN} = 50$ [kHz], the input PWM duty	aximum cycle range = 1.2% cycle range = 1.0%	- 99.0%				
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN}$ = 60[kHz], the input PWM duty	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5%	- 99.0% - 99.5%				
$(1-T_{MINPW}\times f_{PWMIN})\times 100\% \text{ for m}$ When $f_{PWMIN}=60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN}=50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN}=25[\text{kHz}]$ , the input PWM duty	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5%	- 99.0% - 99.5%				
$(1-T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5%	- 99.0% - 99.5%	2.5		VREG	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty Forward/reverse switching pin	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%	- 99.0% - 99.5% - 99.7% Order of current application :	2.5		VREG 1	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty Forward/reverse switching pin High-level input voltage range	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT Order of current application:				
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty Forward/reverse switching pin High-level input voltage range	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT Order of current application:		0.25		
(1 – T <sub>MINIPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT		0.25	1	V
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage	aximum  cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA		0.25	0.35	V
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins  FG output pin low-level voltage  FG output pin leak voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG  ILFG	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V			0.35	V V μA
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins  FG output pin low-level voltage  FG output pin leak voltage  1/2FG output pin low-level voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG ILFG  V1/2FG	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA			0.35 1 0.35	V V μΑ V
(1 – T <sub>MINIPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage  1/2FG output pin low-level voltage	aximum  cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG  ILFG  V1/2FG  IL1/2FG	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V		0.25	0.35 1 0.35	V ν μΑ ν μΑ
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range Low-level input voltage range FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage	aximum      cycle range = 1.2%     cycle range = 1.0%     cycle range = 0.5%     cycle range = 0.3%      VFRH      VFRL      VFG     ILFG     V1/2FG     IL1/2FG     VRD	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA		0.25	0.35 1 0.35 1 0.35	V ν μΑ ν μΑ
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage RD output pin low-level voltage	aximum      cycle range = 1.2%     cycle range = 1.0%     cycle range = 0.5%     cycle range = 0.3%      VFRH      VFRL      VFG     ILFG     V1/2FG     IL1/2FG     VRD	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA		0.25	0.35 1 0.35 1 0.35	V ν μΑ ν μΑ
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage RD output pin low-level voltage RD output pin leak voltage RD output pin leak voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG ILFG V1/2FG IL1/2FG VRD ILRD	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA	0	0.25	0.35 1 0.35 1 0.35	V μΑ V μΑ V
(1 – T <sub>MINIPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range Low-level input voltage range FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage Current limiter circuit Limiter voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG ILFG V1/2FG IL1/2FG VRD ILRD	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA	0	0.25	0.35 1 0.35 1 0.35	V μΑ V μΑ V
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range Low-level input voltage range FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin low-level voltage 1/2FG output pin low-level voltage RD output pin low-level voltage RD output pin low-level voltage RD output pin leak voltage RD output pin leak voltage Current limiter circuit Limiter voltage Constraint protection circuit	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG ILFG V1/2FG IL1/2FG VRD ILRD  VRF	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA	0.225	0.25	0.35 1 0.35 1 0.35 1	V μΑ V μΑ V μΑ
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage Current limiter circuit Limiter voltage Constraint protection circuit CT pin high-level voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG  ILFG  V1/2FG  IL1/2FG  VRD  ILRD  VRF	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA	0.225	0.25 0.25 0.25	0.35 1 0.35 1 0.35 1 0.275	V
(1 – T <sub>MINPW</sub> x f <sub>PWMIN</sub> ) x 100% for m When f <sub>PWMIN</sub> = 60[kHz], the input PWM duty When f <sub>PWMIN</sub> = 50[kHz], the input PWM duty When f <sub>PWMIN</sub> = 25[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty When f <sub>PWMIN</sub> = 15[kHz], the input PWM duty Forward/reverse switching pin High-level input voltage range  Low-level input voltage range  FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage Current limiter circuit Limiter voltage Constraint protection circuit CT pin high-level voltage	aximum cycle range = 1.2% cycle range = 1.0% cycle range = 0.5% cycle range = 0.5% cycle range = 0.3%  VFRH  VFRL  VFG ILFG V1/2FG IL1/2FG VRD ILRD  VRF	- 99.0% - 99.5% - 99.7%  Order of current application: UOUT→VOUT→WOUT  Order of current application: UOUT→WOUT→VOUT  When I <sub>O</sub> is 2mA  When V <sub>FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA  When V <sub>1/2FG</sub> is 16V  When I <sub>O</sub> is 2mA	0.225 2.25 0.43	0.25 0.25 0.25 2.8 0.5	0.35 1 0.35 1 0.35 1 0.275	V

Continued on next page.

Continued from preceding page.

Description	Complete al	Conditions	Ratings			11.2	
Parameter	Symbol		min	typ	max	Unit	
Soft start circuit							
Soft start releasing voltage	VSOFTST			2.5		V	
SOFTST pin charge current	ISOFTST			0.6		μΑ	
Thermal protection circuit							
Thermal protection circuit operating	TSD	Design target *	150	180	210	°C	
temperature							

<sup>\*:</sup> Design target value and no measurement is made. The thermal protection circuit is incorporated to protect the IC from burnout or thermal destruction. Since it operates outside the IC's guaranteed operating range, the customer's thermal design should be performed so that the thermal protection circuit will not be activated when the fan is running under normal operating conditions.

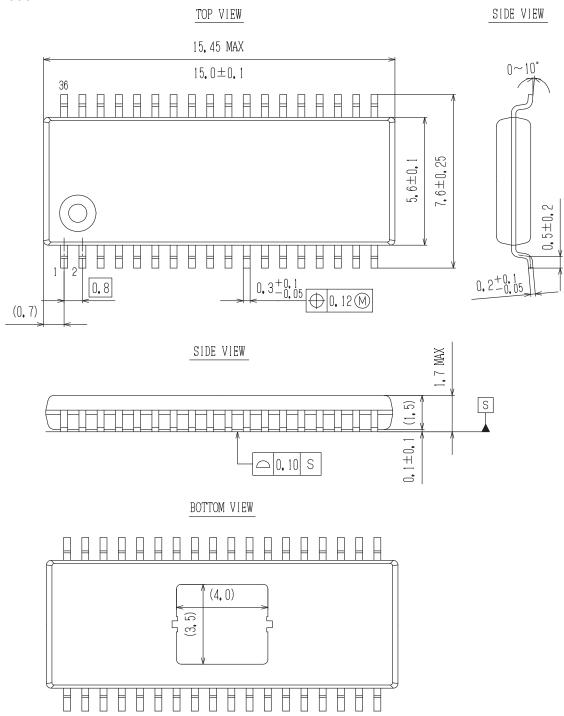
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# **Package Dimensions**

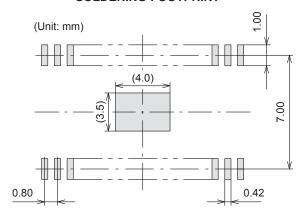
unit: mm

# SSOP36J (275mil) Exposed Pad CASE 940AH

ISSUE A



#### **SOLDERING FOOTPRINT\***



#### NOTES:

- 1. The measurements are for reference only, and unable to guarantee.
- 2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
- 3. After setting, verification on the product must be done.

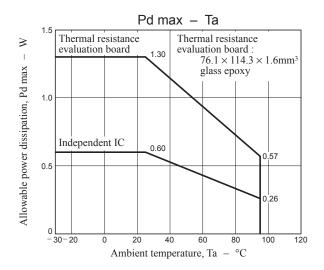
  (Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through–Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void gradient insufficient thickness of soldered joint or bond degradation could lead IC destruction because thermal conduction to substrate becomes poor.)
- \*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# GENERIC MARKING DIAGRAM\*

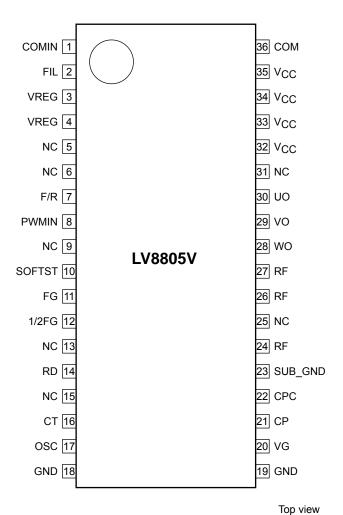


XXXXX = Specific Device Code Y = Year M = Month DDD = Additional Traceability Data

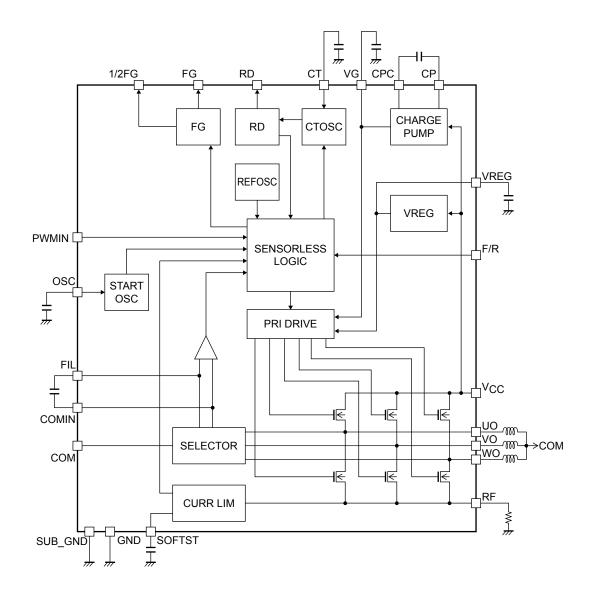
\*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "■", may or may not be present.



# **Pin Assignment**



# **Block Diagram**



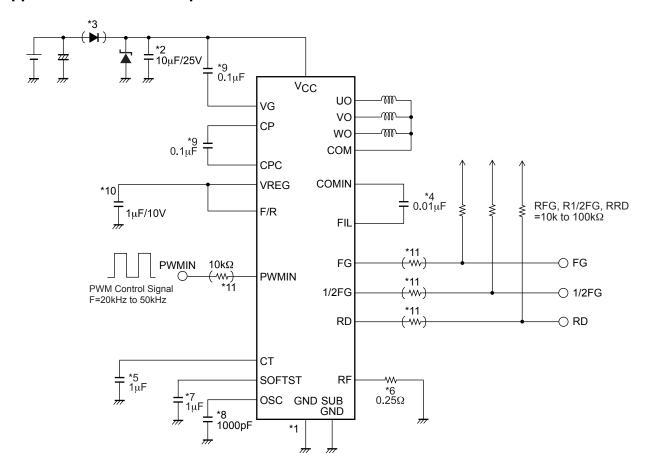
# Pin Function

Pin No.	Pin name	Function	Equivalent circuit
36	COM	Motor middle point connection.	VG _
1 2	COMIN	Motor position detection comparator filter pin. A capacitor must be connected between this pin and the FIL pin (pin 2).  Motor position detection comparator filter pin. A capacitor must be connected between this pin and the COMIN pin (pin 5).	36 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
3 4	VREG	Regulator voltage (5V) output. A capacitor must be connected between these pins and ground.	VCC VREF  WREF
5, 6, 9 13, 15, 25, 31	NC	No connection. These pins are not connected with the internal parts.	
7	F/R	Motor rotation direction switching. A high-level input causes current to flow into the motor in the order of U, V, and W and a low-level input in the order of U, W, and V. Changing the order of current application turns the motor in the opposite direction.	$\begin{array}{c} \text{VREG} \\ \text{Reverse signal} \\ \text{7} \\ \text{15k}\Omega \\ \text{7} \\ \text{Forward/reverse switching signal} \\ \end{array}$
8	PWMIN	PWM signal input pin. "H" The output transistor is turned on by the level voltage input. "L" The output transistor is turned off by the level voltage input, and the motor stops. The speed of the motor is controlled by controlling Duty of the input signal. When the pin opens, the motor becomes all velocities.	VREG  \$ 300kΩ    > 15kΩ
10	SOFTST	Soft start time setting. The motor can be started smoothly by connecting a capacitor between this pin and ground.	VREG 500Ω\$

Continued on next page.

Continued from preceding page. Pin No. Pin name Function Equivalent circuit FG pulse output. This pin outputs a Hall FG 11 (11)(12)(14) sensor system equivalent pulse signal. FG pulse output. This pin outputs 1/2 Hall 1/2FG 12 sensor system equivalent pulse signal. Motor lockup detection output. 14 RD Output is fixed high when motor is locked up. Motor lockup detection time setting. 16 СТ **VREG** When the motor lockup condition is detected, the protection time period before the protection circuit is activated is set by connecting a capacitor between this pin and ground. ≶500Ω (16)Motor startup frequency setting. A capacitor osc **VREG** 17 must be connected between this pin and ground. The startup frequency is adjusted by controlling the charge/discharge current and  $500\Omega$ capacitance of the capacitor. \_\_W\_\_ 500Ω GND pin. 18, 19 GND Charge pump step-up voltage output. 20 ۷G A capacitor must be connected between this Λ VCC pin and the V<sub>CC</sub> pin or ground. VREG Charge pump step-up pulse output pin. 21 СР (20) A capacitor must be connected between this pin and the CPC pin (pin 22). Charge pump step-up pin. 22 CPC A capacitor must be connected between this pin and the CP pin (pin 21). GND pin. SUB GND 23 Power supply for the IC and motor. 32, 33, Vcc Capacitors must be connected between (34)(35) 34, 35 these pins and ground. -Output pins. Connect these pins to the U, V, UO 30 (30) and W of the motor coil. 29 VO  $\dashv$ 28 WO (26)(27) Output current detection pins. The drive 24, 26, RF current is detected by connecting a resistor between these pins and ground. 27

## **Application Circuit Example**



#### \*1. Power supply and GND wiring

The GND is connected to the control circuit power supply system.

#### \*2. Power-side power stabilization capacitor

For the power-side power stabilization capacitor, use a capacitor of  $10\mu\text{F}$  or more.

Connect the capacitor between V<sub>CC</sub> and GND with a thick and along the shortest possible route.

The  $V_{CC}$  pins (pins 32, 33, 34, and 35) must be short-circuited on the print pattern.

The GND pins (pins 18 and 19) and the SUB\_GND pin (pin 23) must be short-circuited on the print pattern.

LV8805V uses synchronous rectification for high efficiency drive. Synchronous rectification is effective for heat reduction and higher efficiency. However, it may increase supply voltage.

If the supply voltage shall increase, make sure that it does not exceed the maximum ratings by inserting a zener diode between power supply and GND.

### \*3. Reverse connection protection diode

This diode protects reverse connection.

Insert a diode between power supply and  $V_{CC}$  pin to protect the IC from destruction due to reverse connection. Connection of this diode is not necessary required.

#### \*4. COMIN and FIL pins

These pins are used to connect the filter capacitor. The LV8805V uses the back EMF signal generated when the motor is running to detect the information on the rotor position. The IC determines the timing at which the output block applies current to the motor based on the position information obtained here. Insert a filter capacitor with a capacitance ranging from 1,000pF to 10,000pF (reference value) between the COMIN pin and FIL pin to prevent any motor startup misoperation that is caused by noise. However, care must be taken since an excessively high capacitance will give rise to deterioration in efficiency and delays in the output power-on timing while the motor is running at high speed. Furthermore, connect the capacitor between the COMIN pin and FIL pin as close as possible in order to avoid the effects of noise from other sources.

#### \*5. CT pin

This pin is used to connect the lock detection capacitor.

The constant-current charging and constant-current discharging circuits incorporated cause locking when the pin voltage reaches 2.5V, and releasing the lock protection when it drops to 0.5V. This pin must be connected to the GND when it is not going to be used.

## \*6. RF pins

These pins are used to set the current limit.

When the pin voltage exceeds 0.25V, the current is limited, and regeneration mode is established. In the application circuit, this voltage is set in such a way that the current limit will be established at 1A.

The calculation formula is given below.

RF resistance = 0.25V/target current limit value

All the RF pins (pins 24, 26 and 27) must be short-circuited on the print pattern.

#### \*7. SOFTST pin

This pin is used to set the soft start.

By connecting a capacitor between this pin and GND, the motor speed can be increased gradually.

When the pin voltage exceeds 2.5V, the soft start is released, and the LV8805V is switched to normal control.

If the soft start function is not going to be used, connect the pin to the VREG pin.

#### \*8. OSC pin

This pin is used to connect the capacitor for setting the startup frequency.

A capacitor with a capacitance ranging from about 500pF to 2,200pF (reference value) must be connected between this pin and GND.

The OSC pin determines the motor startup frequency, so be sure to connect a capacitor to it.

<How to select the capacitance>

Select a capacitance value that will result in the shortest possible startup time for achieving the target speed and produce minimal variations in the startup time. If the capacitance is too high, variations in the startup time will increase; conversely, if it is too low, the motor may idle. The optimum OSC constant depends on the motor characteristics and startup current, so be sure to recheck them when the type of motor used or circuit specifications are changed.

#### \*9. VG, CP, and CPC pins

These pins are used to connect the capacitors to generate the pre-drive voltage and stabilize the pre-drive power supply.

Be sure to connect these capacitors in order to generate the drive voltage for the high-side (upper) output DMOS transistor.

#### \*10. VREG pins

These are the control system power supply pin and regulator output pin, which create the power supply of the control unit. Be sure to connect a capacitor between this pin and GND in order to stabilize control system operation.

Since these pins are used to supply current for control and generate the charge pump voltage, connect a capacitor with a capacitance that is higher than that of the capacitor connected to the charge pump.

Both the VREG pins (pins 3 and 4) must be short-circuited on the print pattern.

#### \*11. Pin protection resistor

It is recommended that resistors higher than  $1k\Omega$  are connected serially to protect pins against misconnection such as GND open and reverse connection.

#### ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)	
LV8805V-MPB-H	SSOP36J (275mil) (Pb-Free / Halogen Free)	30 / Fan-Fold	
LV8805V-TLM-H	SSOP36J (275mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel	

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