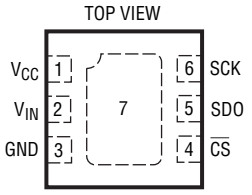
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) .....–0.3V to 6V
Analog Input Voltage (V_{IN}) ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2450C-1 ..... 0°C to 70°C
LTC2450I-1 .....–40°C to 85°C
Storage Temperature Range.....–65°C to 150°C

PIN CONFIGURATION



DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, $_{JA}$ = 102°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2450CDC-1#TRMPBF	LTC2450CDC-1#TRPBF	LDBZ	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2450IDC-1#TRMPBF	LTC2450IDC-1#TRPBF	LDBZ	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No missing codes)	(Note 3)	●	16			Bits
Integral Nonlinearity	(Note 4)	●		2	10	LSB
Offset Error		●		0.5	2	mV
Offset Error Drift				0.02		LSB/°C
Gain Error		●		0.01	0.02	% of FS
Gain Error Drift				0.02		LSB/°C
Transition Noise				1.4		μV_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range,otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	0		V_{CC}	
C_{IN}	IN Sampling Capacitance				0.35		pF
I_{DC_LEAK} (V_{IN})	IN DC Leakage Current	V_{IN} = GND (Note 5) V_{IN} = V_{CC} (Note 5)	● ●	–10 –10	1 1	10 10	nA nA
I_{CONV}	Input Sampling Current (Note 9)				50		nA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Sleep	 $\overline{CS}$ = GND (Note 6) $\overline{CS}$ = V_{CC} (Note 6)	 ● ●		 350 0.05	 600 0.5	 µA µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	V_{CC} – 0.3			V
V_{IL}	Low Level Input Voltage		●			0.3	V
I_{IN}	Digital Input Current		●	–10		10	µA
C_{IN}	Digital Input Capacitance				10		pF
V_{OH}	High Level Output Voltage	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage	I_O = –1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage Current		●	–10		10	µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time		●	14	16.6	21	ms
f_{SCK}	SCK Frequency Range		●			2	MHz
t_{lSCK}	SCK Low Period		●	250			ns
t_{hSCK}	SCK High Period		●	250			ns
t_1	$\overline{CS}$ Falling Edge to SDO Low-Z	(Notes 7, 8)	●	0		100	ns
t_2	$\overline{CS}$ Rising Edge to SDO Hi-Z	(Notes 7, 8)	●	0		100	ns
t_3	$\overline{CS}$ Falling Edge to SCK Falling Edge		●	100			ns
t_{KQ}	SCK Falling Edge to SDO Valid	(Note 7)	●	0		100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND. V_{CC} = 2.7V to 5.5V unless otherwise specified.

Note 3: Guaranteed by design, not subject to test.

Note 4: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band. Guaranteed by design, test correlation and 3 point transfer curve measurement.

Note 5: $\overline{CS}$ = V_{CC}. A positive current is flowing into the DUT pin.

Note 6: SCK = V_{CC} or GND. SDO is high impedance.

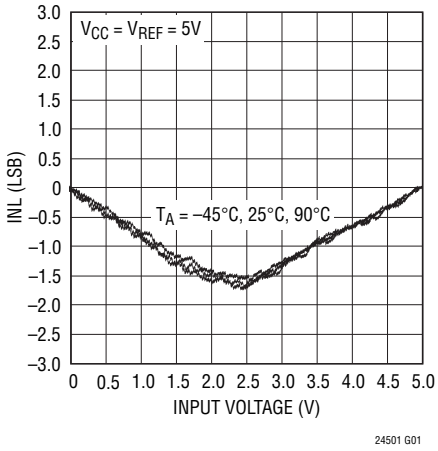
Note 7: See Figure 3.

Note 8: See Figure 4.

Note 9: Input sampling current is the average input current drawn from the input sampling network while the LTC2450-1 is actively sampling the input.

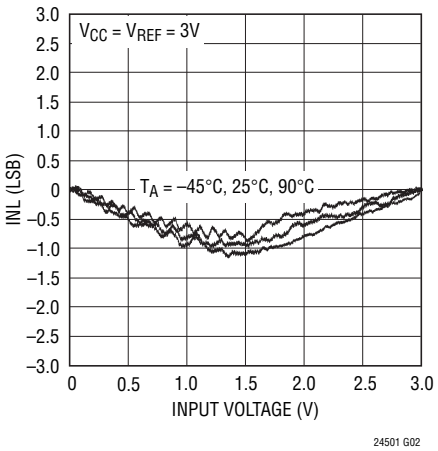
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity



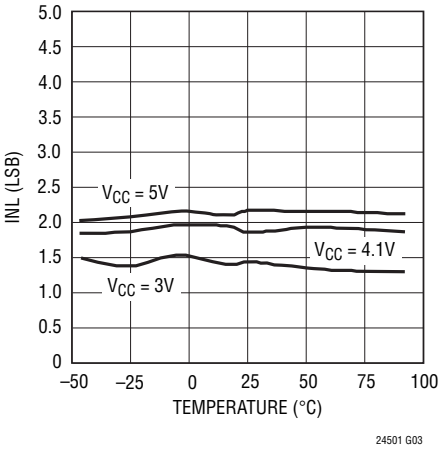
24501 G01

Integral Nonlinearity



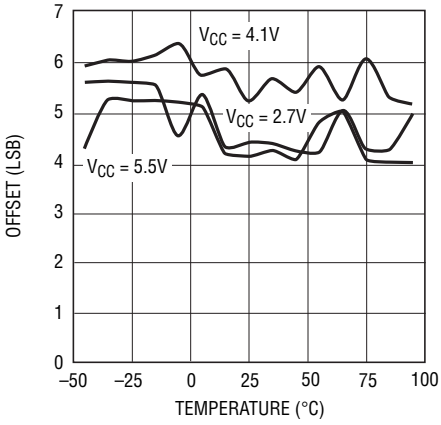
24501 G02

Maximum INL vs Temperature



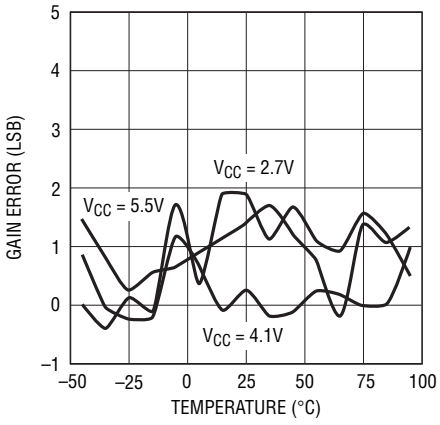
24501 G03

Offset Error vs Temperature



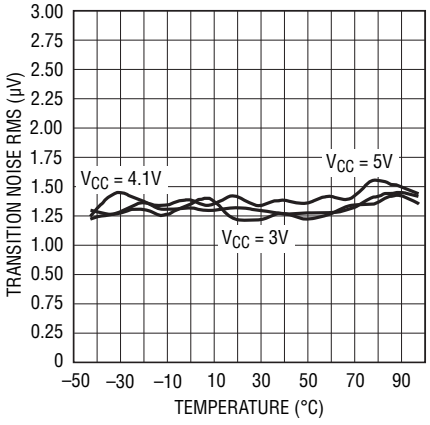
24501 G04

Gain Error vs Temperature



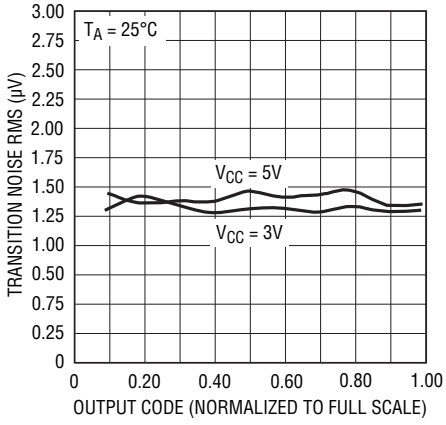
24501 G05

Transition Noise vs Temperature



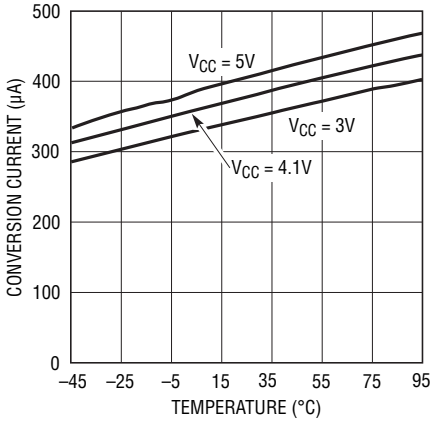
24501 G06

Transition Noise vs Output Code



24501 G07

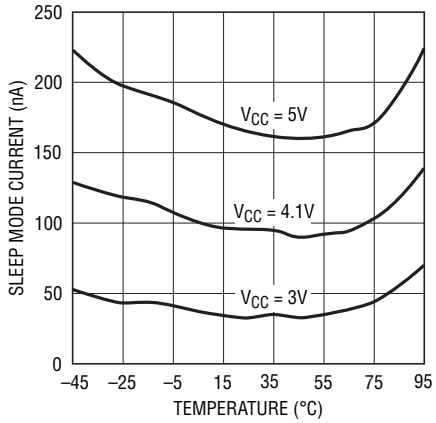
Conversion Mode Power Supply Current vs Temperature



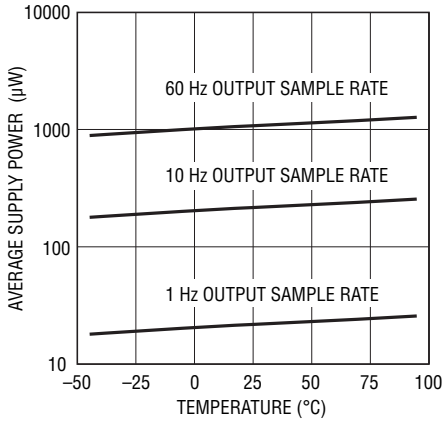
24501 G08

TYPICAL PERFORMANCE CHARACTERISTICS

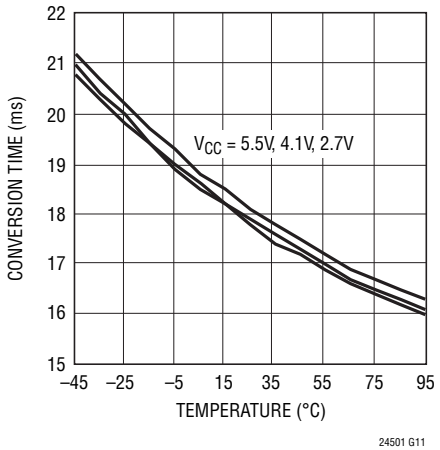
Sleep Mode Power Supply Current vs Temperature



Average Supply Power vs Temperature, V_{CC} = 3V



Conversion Period vs Temperature



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage and Converter Reference Voltage. Bypass to GND (Pin 3) with a 10µF capacitor in parallel with a low series inductance 0.1µF capacitor located as close to the part as possible.

V_{IN} (Pin 2): Analog Input Voltage.

GND (Pin 3): Ground. Connect to a ground plane through a low impedance connection.

$\overline{CS}$ (Pin 4): Chip Select (Active LOW) Digital Input. A LOW on this pin enables the SDO digital output. A HIGH on this pin places the SDO output pin in a high impedance state.

SDO (Pin 5): Three-State Serial Data Output. SDO is used for serial data output during the DATA OUTPUT state and can be used to monitor the conversion status.

SCK (Pin 6): Serial Clock Input. SCK synchronizes the serial data output. While digital data is available (the ADC is not in CONVERT state) and $\overline{CS}$ is LOW (ADC is not in SLEEP state) a new data bit is produced at the SDO output pin following every falling edge applied to the SCK pin.

Exposed Pad (Pin 7): Ground. The Exposed Pad must be soldered to the same point as Pin 3.

FUNCTIONAL BLOCK DIAGRAM

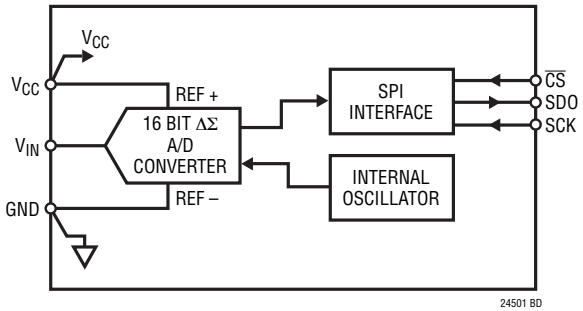


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2450-1 is a low power, delta-sigma analog-to-digital converter with a simple 3-wire interface (see Figure 1). Its operation is composed of three successive states: CONVERT, SLEEP and DATA OUTPUT. The operating cycle begins with the CONVERT state, is followed by the SLEEP state, and ends with the DATA OUTPUT state (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock input (SCK), and the active low chip select input ($\overline{CS}$).

The CONVERT state duration is determined by the LTC2450-1 conversion time (nominally 16.6 milliseconds). Once started, this operation can not be aborted except by a low power supply condition (V_{CC} < 2.1V) which generates an internal power-on reset signal.

After the completion of a conversion, the LTC2450-1 enters the SLEEP state and remains there until both the chip select and clock inputs are low ($\overline{CS}$ = SCK = LOW). Following this condition the ADC transitions into the DATA OUTPUT state.

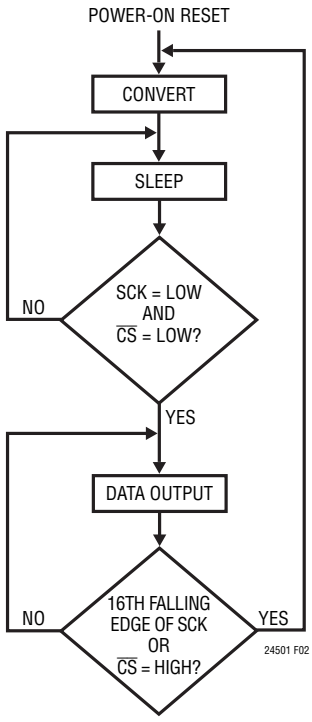


Figure 2. LTC2450-1 State Transition Diagram

While in the SLEEP state, whenever the chip select input is pulled high ($\overline{CS}$ = HIGH), the LTC2450-1's power supply current is reduced to less than 500nA. When the chip select input is pulled low ($\overline{CS}$ = LOW), and SCK is maintained at a HIGH logic level, the LTC2450-1 will return to a normal power consumption level. During the SLEEP state, the result of the last conversion is held indefinitely in a static register.

Upon entering the DATA OUTPUT state, SDO outputs the most significant bit (D15) of the conversion result. During this state, the ADC shifts the conversion result serially through the SDO output pin under the control of the SCK input pin. There is no latency in generating this data and the result corresponds to the last completed conversion. A new bit of data appears at the SDO pin following each falling edge detected at the SCK input pin. The user can reliably latch this data on every rising edge of the external serial clock signal driving the SCK pin (see Figure 3).

The DATA OUTPUT state concludes in one of two different ways. First, the DATA OUTPUT state operation is completed once all 16 data bits have been shifted out and the clock then goes low. This corresponds to the 16th falling edge of SCK. Second, the DATA OUTPUT state can be aborted at any time by a LOW-to-HIGH transition on the $\overline{CS}$ input. Following either one of these two actions, the LTC2450-1 will enter the CONVERT state and initiate a new conversion cycle.

Power-Up Sequence

When the power supply voltage V_{CC} applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When V_{CC} rises above this critical threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2450-1 starts a conversion cycle and follows the succession of states described in Figure 2. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage V_{CC} is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

APPLICATIONS INFORMATION

Ease of Use

The LTC2450-1 data output has no latency, filter settling delay or redundant results associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

The LTC2450-1 includes a proprietary input sampling scheme that reduces the average input current several orders of magnitude as compared to traditional delta sigma architectures. This allows external filter networks to interface directly to the LTC2450-1. Since the average input sampling current is 50nA, an external RC lowpass filter using a 1kΩ and 0.1µF results in <1LSB error.

Reference Voltage Range

The converter uses the power supply voltage (V_{CC}) as the positive reference voltage (see Figure 1). Thus, the reference range is the same as the power supply range, which extends from 2.7V to 5.5V. The LTC2450-1's internal noise level is extremely low so the output peak-to-peak noise remains well below 1LSB for any reference voltage within this range. Thus the converter resolution remains at 1LSB independent of the reference voltage. INL, offset, and full-scale errors vary with the reference voltage as indicated by the Typical Performance Characteristics graphs. These error terms will decrease with an increase in the reference voltage (as the LSB size in µV increases).

Input Voltage Range

The ADC is capable of digitizing true rail-to-rail input signals. Ignoring offset and full-scale errors, the converter will theoretically output an "all zero" digital result when the input is at ground (a zero scale input) and an "all one" digital result when the input is at V_{CC} (a full-scale input). In an under-range condition, for all input voltages less than the voltage corresponding to output code 0, the converter will generate the output code 0. In an over-range condition, for all input voltages greater than the voltage corresponding to output code 65535 the converter will generate the output code 65535.

Output Data Format

The LTC2450-1 generates a 16-bit direct binary encoded result. It is provided, MSB first, as a 16-bit serial stream through the SDO output pin under the control of the SCK input pin (see Figure 3).

During the data output operation the $\overline{CS}$ input pin must be pulled low ($\overline{CS}$ = LOW). The data output process starts with the most significant bit of the result being present at the SDO output pin (SDO = D15) once $\overline{CS}$ goes low. A new data bit appears at the SDO output pin following every falling edge detected at the SCK input pin. The output data can be reliably latched by the user using the rising edge of SCK.

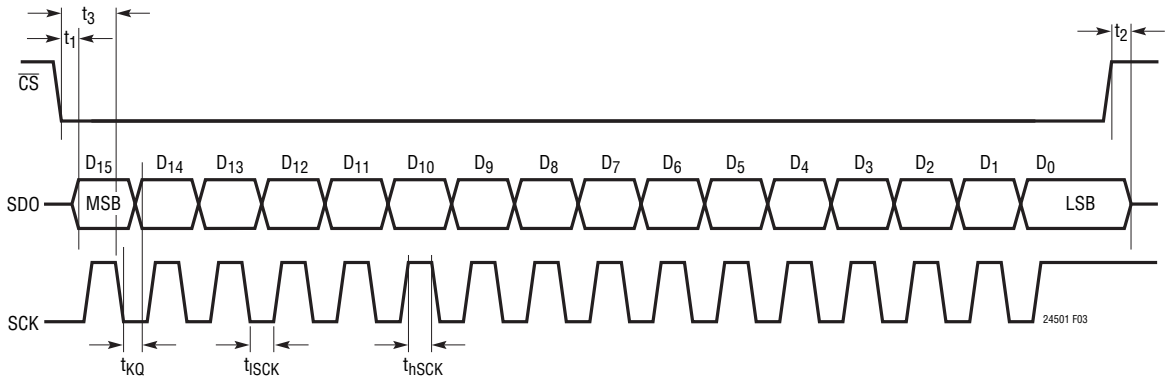


Figure 3. Data Output Timing

APPLICATIONS INFORMATION

Conversion Status Monitor

For certain applications, the user may wish to monitor the LTC2450-1 conversion status. This can be achieved by holding SCK HIGH during the conversion cycle. In this condition, whenever the $\overline{CS}$ input pin is pulled low ($\overline{CS}$ = LOW), the SDO output pin will provide an indication of the conversion status. SDO = HIGH is an indication of a conversion cycle in progress while SDO = LOW is an indication of a completed conversion cycle. An example of such a sequence is shown in Figure 4.

Conversion status monitoring, while possible, is not required for LTC2450-1 as its conversion time is fixed and equal at approximately 16.6ms (21ms maximum). Therefore, external timing can be used to determine the completion of a conversion cycle.

SERIAL INTERFACE

The LTC2450-1 transmits the conversion result and receives the start of conversion command through a synchronous 3-wire interface. This interface can be used during the CONVERT and SLEEP states to assess the conversion status and during the DATA OUTPUT state to read the conversion result, and to trigger a new conversion.

Serial Interface Operation Modes

The following are a few of the more common interface operation examples. Many more valid control and serial data output operation sequences can be constructed based upon the above description of the function of the three digital interface pins.

The modes of operation can be summarized as follows:

1) The LTC2450-1 functions with SCK idle high (commonly known as CPOL = 1) or idle low (commonly known as CPOL = 0).

2) After the 16th bit is read, the user can choose one of two ways to begin a new conversion. First, one can pull $\overline{CS}$ high ($\overline{CS}$ = ↑). Second, one can use a high-low transition on SCK (SCK = ↓).

3) At any time during the Data Output state, pulling $\overline{CS}$ high ($\overline{CS}$ = ↑) causes the part to leave the I/O state, abort the output and begin a new conversion.

4) When SCK = HIGH, it is possible to monitor the conversion status by pulling $\overline{CS}$ low and watching for SDO to go low. This feature is available only in the idle-high (CPOL = 1) mode.

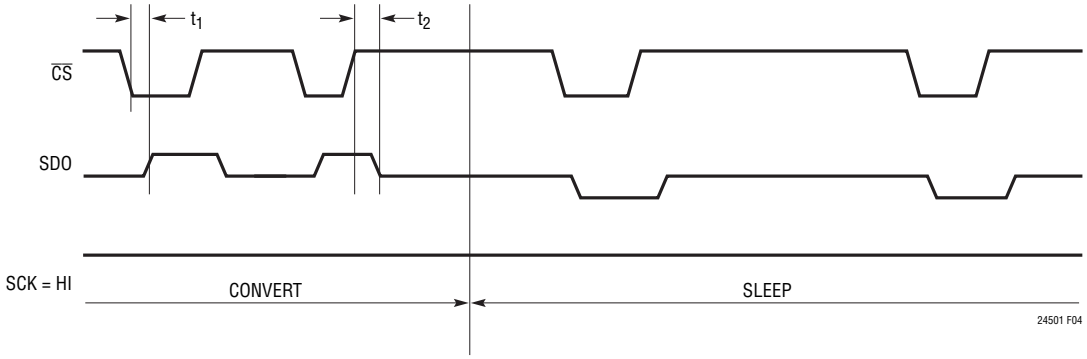


Figure 4. Conversion Status Monitoring Mode

APPLICATIONS INFORMATION

Serial Clock Idle-High (CPOL = 1) Examples

In Figure 5, following a conversion cycle the LTC2450-1 automatically enters the low power sleep mode. The user can monitor the conversion status at convenient intervals using $\overline{CS}$ and SDO.

$\overline{CS}$ is pulled LOW while SCK is HIGH to test whether or not the chip is in the CONVERT state. While in the CONVERT state, SDO is HIGH while $\overline{CS}$ is LOW. In the SLEEP state, SDO is LOW while $\overline{CS}$ is LOW. These tests are not required operational steps but may be useful for some applications.

When the data is available, the user applies 16 clock cycles to transfer the result. The $\overline{CS}$ rising edge is then used to initiate a new conversion.

The operation example of Figure 6 is identical to that of Figure 5, except the new conversion cycle is triggered by the falling edge of the serial clock (SCK). A 17th clock pulse is used to trigger a new conversion cycle.

Serial Clock Idle-Low (CPOL = 0) Examples

In Figure 7, following a conversion cycle the LTC2450-1 automatically enters the low power sleep state. The user determines data availability (and the end of conversion) based upon external timing. The user then pulls $\overline{CS}$ low ($\overline{CS}$ = ↓) and uses 16 clock cycles to transfer the result. Following the 16th rising edge of the clock, $\overline{CS}$ is pulled high ($\overline{CS}$ = ↑), which triggers a new conversion.

The timing diagram in Figure 8 is identical to that of Figure 7, except in this case a new conversion is triggered by SCK. The 16th SCK falling edge triggers a new conversion cycle and the $\overline{CS}$ signal is subsequently pulled high.

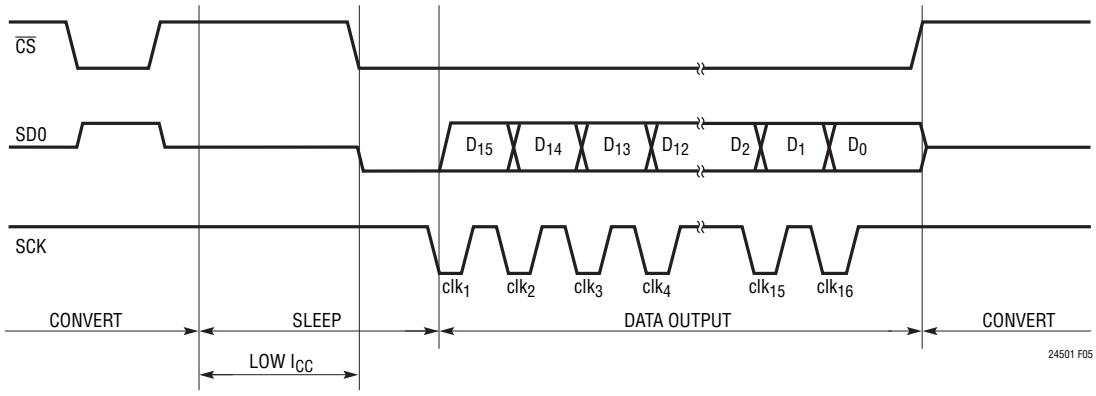


Figure 5. Idle-High (CPOL = 1) Serial Clock Operation Example. The Rising Edge of $\overline{CS}$ Starts a New Conversion

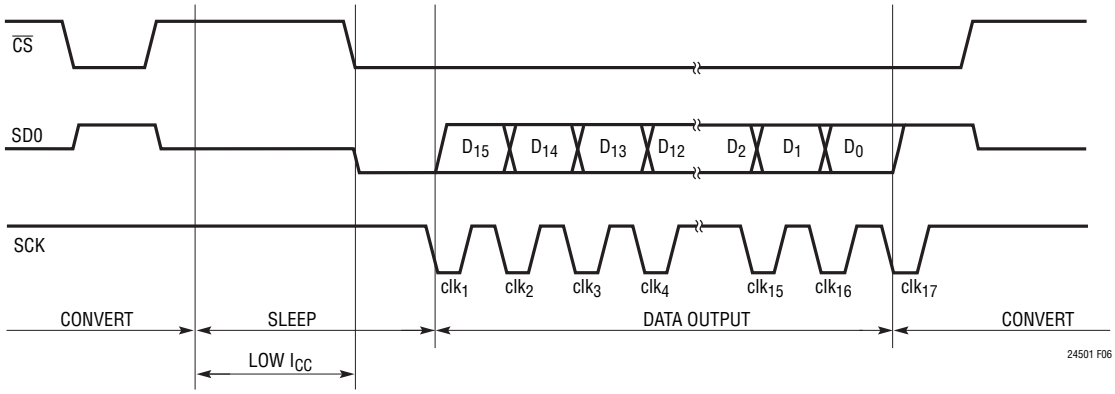


Figure 6. Idle-High (CPOL = 1) Clock Operation Example. A 17th Clock Pulse is Used to Trigger a New Conversion Cycle

APPLICATIONS INFORMATION

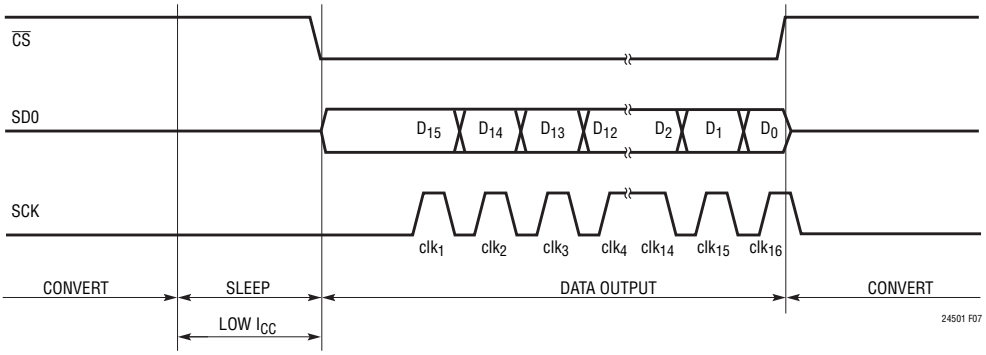


Figure 7. Idle-Low (CPOL = 0) Clock. $\overline{CS}$ Triggers a New Conversion

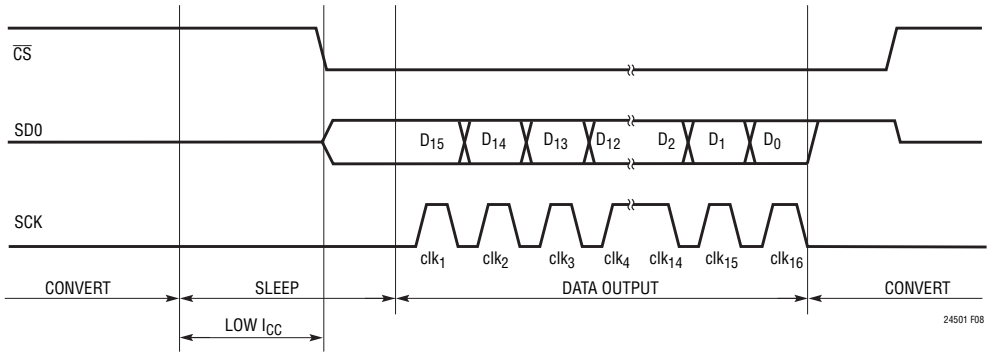


Figure 8. Idle-Low (CPOL = 0) Clock. The 16th SCK Falling Edge Triggers a New Conversion

Examples of Aborting Cycle using $\overline{CS}$

For some applications the user may wish to abort the I/O cycle and begin a new conversion. If the LTC2450-1 is in the data output state, a $\overline{CS}$ rising edge clears the remaining data bits from memory, aborts the output cycle and triggers a new conversion. Figure 9 shows an example of aborting an I/O with idle-high (CPOL = 1) and Figure 10 shows an example of aborting an I/O with idle-low (CPOL = 0).

A new conversion cycle can be triggered using the $\overline{CS}$ signal without having to generate any serial clock pulses as shown in Figure 11. If SCK is maintained at a LOW logic level, after the end of a conversion cycle, a new conversion operation can be triggered by pulling $\overline{CS}$ low and then high. When $\overline{CS}$ is pulled low ($\overline{CS}$ = LOW), SDO will output the most significant bit (D15) of the result of the just completed conversion. While a low logic level is maintained at SCK pin and $\overline{CS}$ is subsequently pulled high ($\overline{CS}$ = HIGH) the remaining 15 bits of the result (D14:D0) are discarded and a new conversion cycle starts.

Following the aborted I/O, additional clock pulses in the CONVERT state are acceptable, but excessive signal transitions on SCK can potentially create noise on the ADC during the conversion, and thus may negatively influence the conversion accuracy.

APPLICATIONS INFORMATION

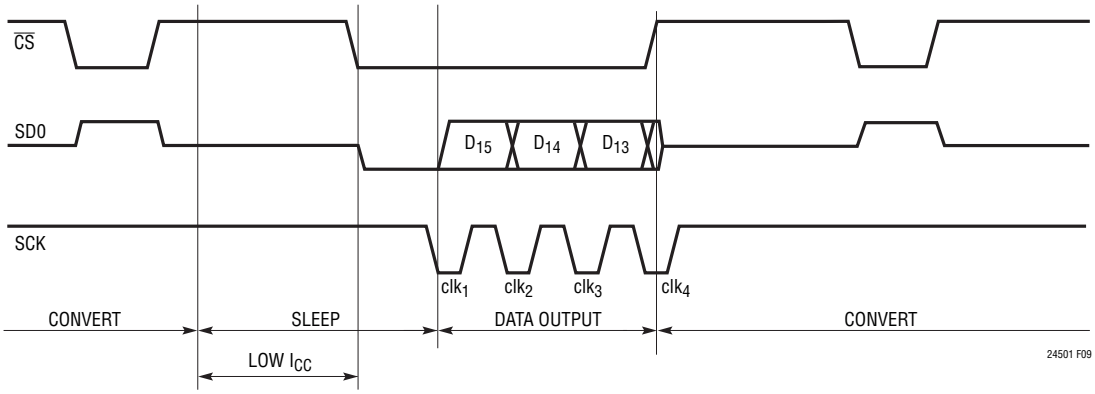


Figure 9. Idle-High (CPOL = 1) Clock and Aborted I/O Example

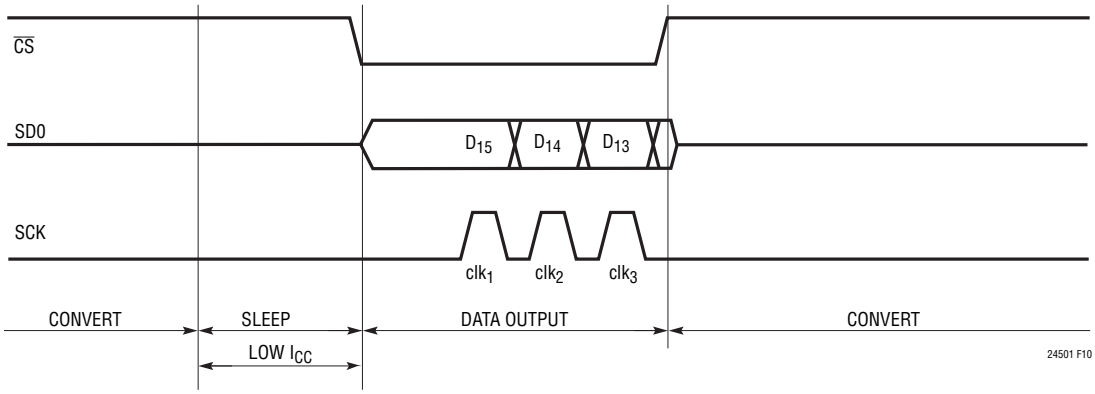


Figure 10. Idle-Low (CPOL = 0) Clock and Aborted I/O Example

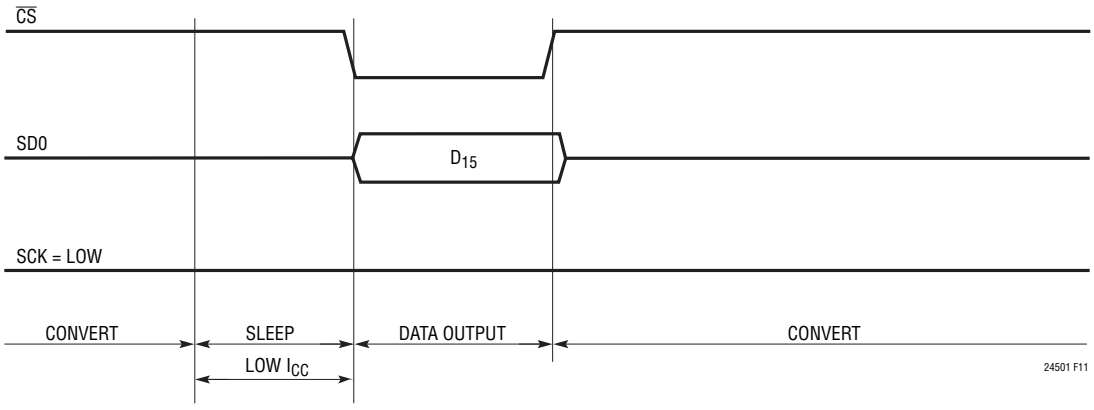


Figure 11. Idle-Low (CPOL = 0) Clock and Minimum Data Output Length Example

APPLICATIONS INFORMATION

2-Wire Operation

The 2-wire operation modes, while reducing the number of required control signals, should be used only if the LTC2450-1 low power sleep capability is not required. In addition the option to abort serial data transfers is no longer available. Hardwire $\overline{CS}$ to GND for 2-wire operation.

Figure 12 shows a 2-wire operation sequence which uses an idle-high (CPOL = 1) serial clock signal. The conversion status can be monitored at the SDO output. Following a conversion cycle, the ADC enters SLEEP state and the SDO output transitions from HIGH to LOW. Subsequently 16 clock pulses are applied to the SCK input in order to serially shift the 16 bit result. Finally, the 17th clock pulse is applied to the SCK input in order to trigger a new conversion cycle.

Figure 13 shows a 2-wire operation sequence which uses an idle-low (CPOL = 0) serial clock signal. The conversion status cannot be monitored at the SDO output. Following a conversion cycle, the LTC2450-1 bypasses the SLEEP state and immediately enters the DATA OUTPUT state. At this moment the SDO pin outputs the most significant bit (D15) of the conversion result. The user must use external timing in order to determine the end of conversion and result availability. Subsequently 16 clock pulses are applied to SCK in order to serially shift the 16-bit result. The 16th clock falling edge triggers a new conversion cycle.

PRESERVING THE CONVERTER ACCURACY

The LTC2450-1 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, antialiasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the very high accuracy capability of this part, some simple precautions are desirable.

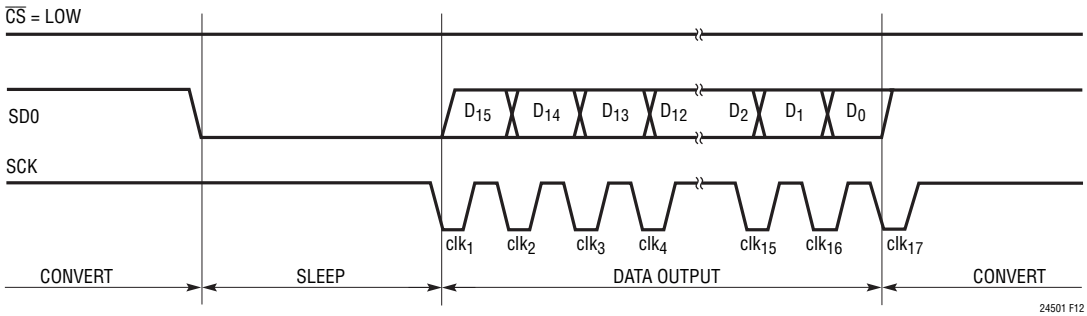


Figure 12. 2-Wire, Idle-High (CPOL = 1) Serial Clock, Operation Example

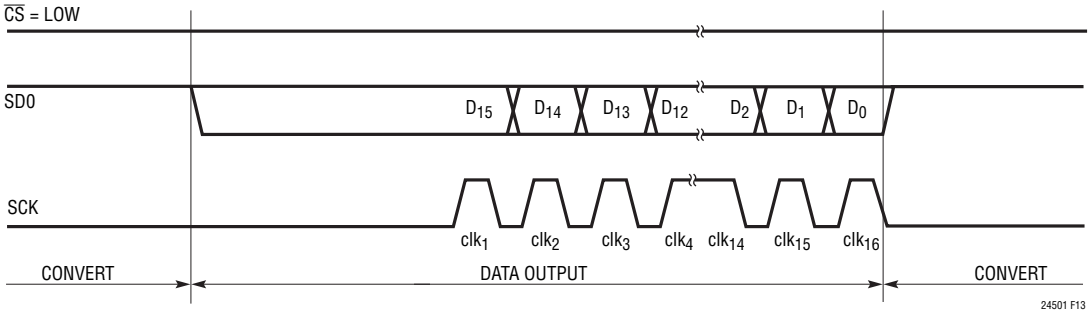


Figure 13. 2-Wire, Idle-Low (CPOL = 0) Serial Clock Operation Example

APPLICATIONS INFORMATION

Digital Signal Levels

The LTC2450-1's digital interface is easy to use. Its digital inputs (SCK and $\overline{CS}$) accept standard CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signal SDO is less of a concern because it is not active during the conversion cycle.

While a digital input signal is in the range 0.5V to V_{CC} –0.5V, the CMOS input receiver may draw additional current from the power supply. Due to the nature of CMOS logic, a slow transition within this voltage range may cause an increase in the power supply current drawn by the converter, particularly in the low power operation mode within the SLEEP state. Thus, for low power consumption it is highly desirable to provide relatively fast edges for the two digital input pins SCK and $\overline{CS}$, and to keep the digital input logic levels at V_{CC} or GND.

At the same time, during the CONVERT state, undershoot and/or overshoot of fast digital signals connected to the LTC2450-1 pins may affect the conversion result. Undershoot and overshoot can occur because of an impedance mismatch at the converter pin combined with very fast transition times. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance. Parallel termination is seldom an acceptable option in low power systems so a series resistor between 27Ω and 56Ω placed near the driver may eliminate this problem. The actual resistor value depends upon the trace impedance and connection topology. An alternate solution is to reduce the edge rate of the control signals, keeping in mind the concerns regarding slow edges mentioned above.

Particular attention should be given to configurations in which a continuous clock signal is applied to SCK pin during the CONVERT state. While LTC2450-1 will ignore this signal from a logic point of view the signal edges may create unexpected errors depending upon the relation between its frequency and the internal oscillator frequency. In such a situation it is beneficial to use edge rates of about 10ns and to limit potential undershoot to less than 0.3V below GND and overshoot to less than 0.3V above V_{CC}.

Noisy external circuitry can potentially impact the output under 2-wire operation. In particular, it is possible to get the LTC2450-1 into an unknown state if an SCK pulse is missed or noise triggers an extra SCK pulse. In this situation, it is impossible to distinguish SDO = 1 (indicating conversion in progress) from valid "1" data bits. As such, CPOL = 1 is recommended for the 2-wire mode. The user should look for SDO = 0 before reading data, and look for SDO = 1 after reading data. If SDO does not return a "0" within the maximum conversion time (or return a "1" after a full data read), generate 16 SCK pulses to force a new conversion.

Driving V_{CC} and GND

The V_{CC} and GND pins of the LTC2450-1 converter are directly connected to the positive and negative reference voltages, respectively. A simplified equivalent circuit is shown in Figure 14.

The power supply current passing through the parasitic layout resistance associated with these common pins will modify the ADC reference voltage and thus negatively affect the converter accuracy. It is thus important to keep the V_{CC} and GND lines quiet, and to connect these supplies through very low impedance traces.

In relation to the V_{CC} and GND pins, the LTC2450-1 combines internal high frequency decoupling with damping

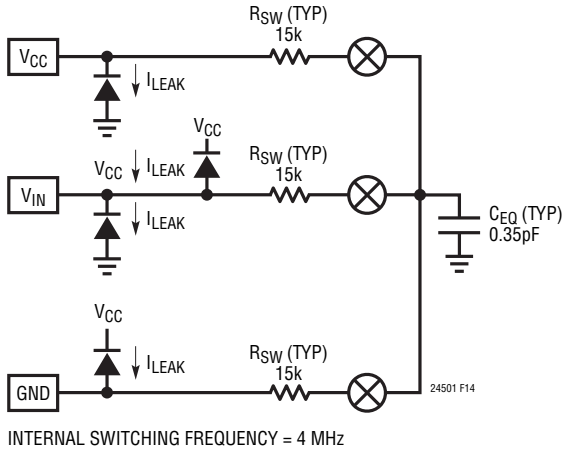


Figure 14. LTC2450-1 Analog Pins Equivalent Circuit

APPLICATIONS INFORMATION

elements which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF ceramic capacitor should be connected between the V_{CC} and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC package. It is also desirable to avoid any via in the circuit path starting from the converter V_{CC} pin, passing through these two decoupling capacitors and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

Very low impedance ground and power planes and star connections at both V_{CC} and GND pins are preferable. The V_{CC} pin should have two distinct connections: the first to the decoupling capacitors described above and the second to the power supply voltage. The GND pin should have three distinct connections: the first to the decoupling capacitors described above, the second to the ground return for the input signal source and the third to the ground return for the power supply voltage source.

Driving V_{IN}

The V_{IN} input drive requirements can be best analyzed using the equivalent circuit of Figure 15. The input signal V_{SIG} is connected to the ADC input pin V_{IN} through an equivalent source resistance R_S. This resistor includes both the actual generator source resistance and any additional optional resistor connected to the V_{IN} pin. An optional input capacitor C_{IN} is also connected to the ADC V_{IN} pin. This capacitor is placed in parallel with the ADC input parasitic capacitance C_{PAR}. Depending upon the PCB layout C_{PAR} has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 15 includes the converter equivalent internal resistor R_{SW} and sampling capacitor C_{EQ}.

There are some immediate trade-offs in R_S and C_{IN} without needing a full circuit analysis. Increasing R_S and C_{IN} can give the following benefits:

1) Due to the LTC2450-1's input sampling algorithm, the input current drawn by V_{IN} during the conversion cycle is 50nA. A high $R_S \bullet C_{IN}$ attenuates the high frequency components of the input current, and R_S values up to 1kΩ result in <1LSB error.

2) The bandwidth from V_{SIG} is reduced at V_{IN}. This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple antialiasing and input noise reduction.

3) Noise generated by the ADC is attenuated before it goes back to the signal source.

4) A large C_{IN} gives a better AC ground at V_{IN}, helping reduce reflections back to the signal source.

5) Increasing R_S protects the ADC by limiting the current during an outside-the-rails fault condition. R_S can be easily sized such as to protect against even extreme fault conditions.

There is a limit to how large $R_S \bullet C_{IN}$ should be for a given application. Increasing R_S beyond a given point increases the voltage drop across R_S due to the input current, to the point that significant measurement errors exist. Additionally, for some applications, increasing the $R_S \bullet C_{IN}$ product too much may unacceptably attenuate the signal at frequencies of interest.

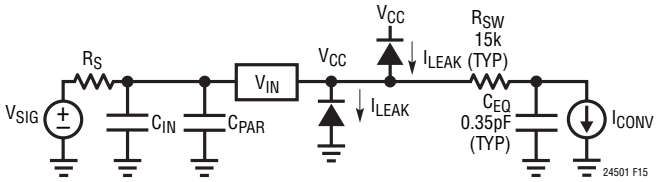


Figure 15. LTC2450-1 Input Drive Equivalent Circuit

APPLICATIONS INFORMATION

For most applications, it is desirable to implement C_{IN} as a high quality 0.1µF ceramic capacitor and $R_S \leq 1k$. This capacitor should be located as close as possible to the actual V_{IN} package pin. Furthermore the area encompassed by this circuit path as well as the path length should be minimized.

In the case of a 2-wire sensor which is not remotely grounded, it is desirable to split R_S and place series resistors in the ADC input line as well as in the sensor ground return line which should be tied to the ADC GND pin using a star connection topology.

Figure 16 shows the measured LTC2450-1 INL vs Input Voltage as a function of R_S value with an input capacitor $C_{IN} = 0.1µF$.

In some cases, R_S can be increased above these guidelines. The input current is zero while the ADC is either in sleep or I/O modes. Thus, if the time constant of the input R-C circuit $\tau = R_S \bullet C_{IN}$ is of the same order magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth $\cong 1/(2\pi \bullet R_S \bullet C_{IN})$.

Finally, if the recommended choice for C_{IN} is unacceptable for the user's specific application, an alternate strategy is to eliminate C_{IN} and minimize C_{PAR} and R_S. In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring and so on. The resultant INL vs V_{IN} is shown in Figure 17. The measurements of Figure 17 include a C_{PAR} capacitor corresponding to a minimum size layout pad and a minimum width input trace of about 1 inch length.

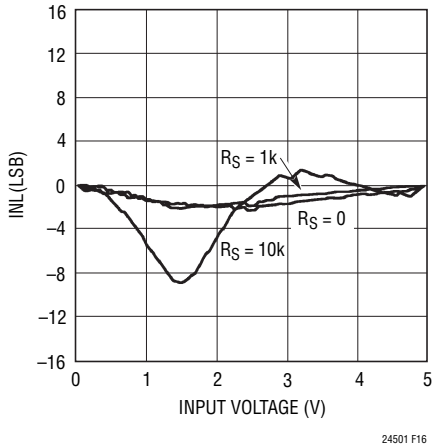


Figure 16. Measured INL vs Input Voltage, $C_{IN} = 0.1µF$, $V_{CC} = 5V$, $T_A = 25°C$

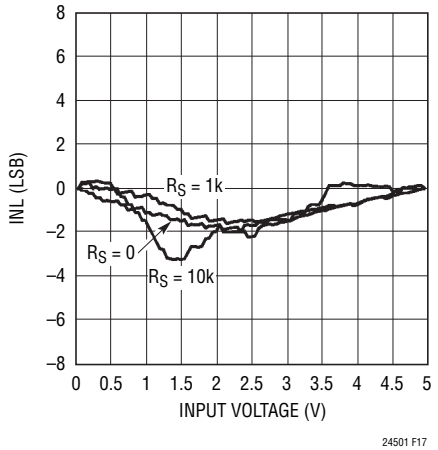


Figure 17. Measured INL vs V_{IN}, $C_{IN} = 0$, $V_{CC} = 5V$, $T_A = 25°C$

APPLICATIONS INFORMATION

Signal Bandwidth and Noise Equivalent Input Bandwidth

The LTC2450-1 includes a sinc[1] type digital filter with the first notch located at f_0 = 60Hz. As such the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2450-1 input signal attenuation with frequency at low frequencies is shown in Figure 18.

The LTC2450-1 input signal attenuation with frequency over a wide frequency range is shown in Figure 19.

The converter noise level is about 1.4μV_{RMS} and can be modeled by a white noise source connected at the input of a noise free converter.

For a simple system noise analysis the V_{IN} drive circuit can be modeled as a single pole equivalent circuit characterized by a pole location F_i and a noise spectral density n_i. If the converter has an unlimited bandwidth or at least a bandwidth substantially larger than F_i, then the total noise contribution of the external drive circuit would be $V_n = n_i \bullet \sqrt{\pi/2 \bullet F_i}$. Then, the total system noise level can be estimated as the square root of the sum of (V_n^2) and the square of the LTC2450-1 noise floor (≈2μV^2).

Aliasing

The LTC2450-1 signal acquisition circuit is a sampled data system and as such suffers from input signal aliasing. As can be seen from Figure 19, due to the very high over-sample ratios the high frequency input signal attenuation is reasonably good. Nevertheless a continuous time antialiasing filter connected at the input will preserve the converter accuracy when the input signal includes undesirable high frequency components. The antialiasing function can be accomplished using the R_S and C_{IN} components shown in Figure 15 sized such that $\tau = R_S \bullet C_{IN} > 450ns$.

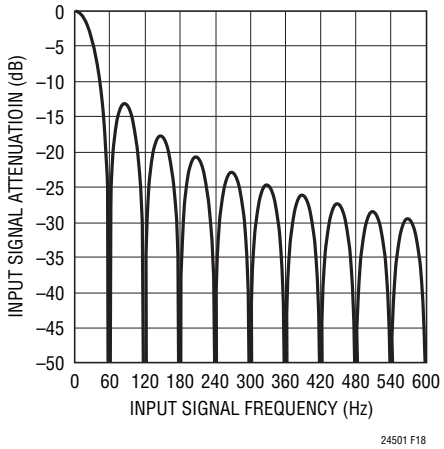


Figure 18. Input Signal Attenuation vs Frequency (Low Frequencies)

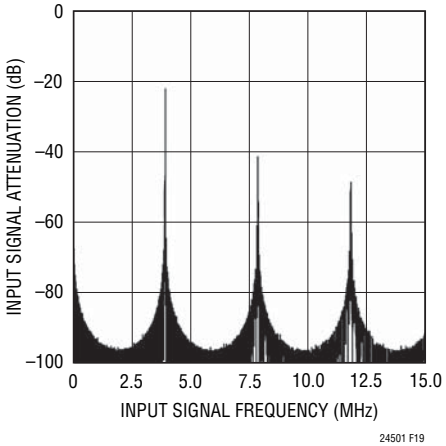
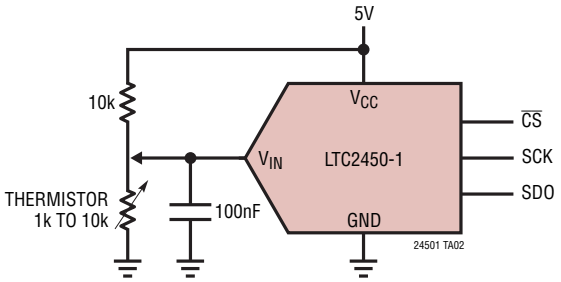


Figure 19. Input Signal Attenuation vs Frequency

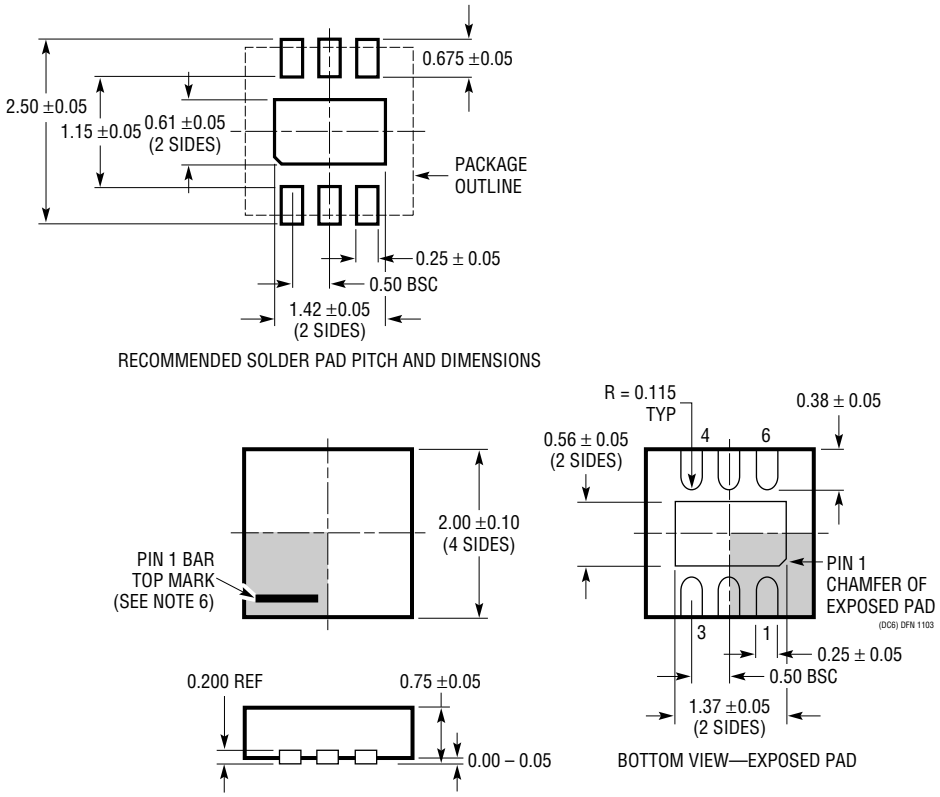
TYPICAL APPLICATION

Thermistor Measurement



PACKAGE DESCRIPTION

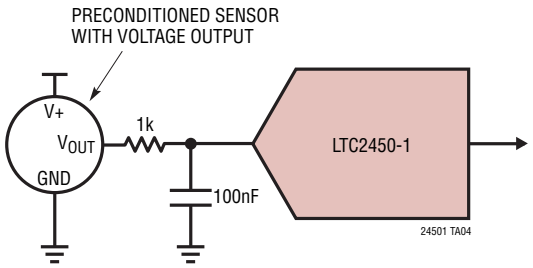
DC Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703)



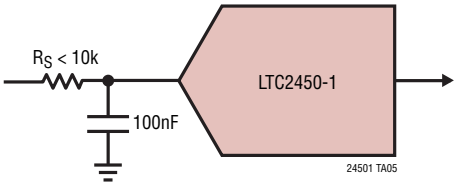
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

Easy Active Input



Easy Passive Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1236A-5	Precision Bandgap Reference, 5V	0.05% Maximum, 5ppm/°C Drift
LT1461	Micropower Series Reference, 2.5V	0.04% Maximum, 3ppm/°C Drift
LTC1860/LTC1861	12-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	12-Bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1864/LTC1865	16-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	16-bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC2440	24-Bit No Latency ΔΣ™ ADC	200nV$_{RMS}$ Noise, 8kHz Output Rate, 15ppm INL
LTC2450	Ultra Tiny, Easy to use 16-Bit ΔΣ ADC with Automatic Offset Calibration and 30Hz Output Rate	Pin Compatible with the LTC2450-1
LTC2480	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temperature Sensor, SPI	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2481	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temperature Sensor, I^{2}C	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2482	16-Bit, Differential Input, No Latency ΔΣ ADC, SPI	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2483	16-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2484	24-Bit, Differential Input, No Latency ΔΣ ADC, SPI	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2485	24-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C	Easy Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC6241	Dual, 18MHz, Low Noise, Rail-to-Rail Op Amp	550nV$_{P-P}$ Noise, 125µV Offset Maximum
LT6660	Micropower References in 2mm × 2mm DFN Package, 2.5V, 3V, 3.3V, 5V	20ppm/°C Maximum Drift, 0.2% Maximum

No Latency ΔΣ is a trademark of Linear Technololgy Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0408 REV C • PRINTED IN USA