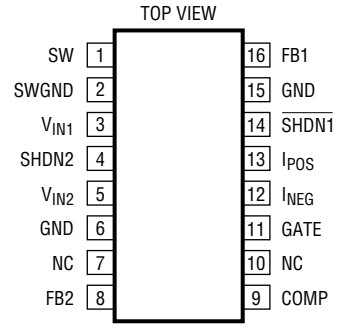
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, $\overline{SHDN1}$ Voltage 10V
SW Voltage ..... –0.4V to 36V
FB1 Voltage ..... V_{IN1} + 0.3V
Current into FB1, FB2 Pin ..... ±1mA
V_{IN2}, I_{POS}, I_{NEG} 22V
SHDN2 ..... V_{IN2}
Operating Ambient Temperature Range ..... 0°C to 70°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W, θ_{JC} = 40°C/W

ORDER PART NUMBER
LT3150CGN
GN PART MARKING
3150

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 1.5V, $V_{\overline{SHDN1}}$ = V_{IN1}, V_{IN2} = 12V, GATE = 6V, I_{POS} = I_{NEG} = 5V, V_{SHDN2} = 0.75V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Switching Regulator							
	V_{IN1} Minimum Operating Voltage				0.9	1.1	V
	V_{IN1} Maximum Operating Voltage					10	V
V_{FB1}	FB1 Reference Voltage		●	1.20	1.23	1.255	V
	FB1 Input Bias Current	Current Flows into Pin	●		27	80	nA
I_{Q1}	V_{IN1} Quiescent Current	$V_{\overline{SHDN1}}$ = 1.5V			3	4.5	mA
	V_{IN1} Quiescent Current in Shutdown	$V_{\overline{SHDN1}}$ = 0V, V_{IN1} = 2V $V_{\overline{SHDN1}}$ = 0V, V_{IN1} = 5V			0.01 0.01	0.5 1.0	µA µA
	FB1 Reference Line Regulation	1.5V ≤ V_{IN1} ≤ 10V			0.02	0.2	%/V
	Switching Frequency		●	1	1.4	1.9	MHz
	Maximum Duty Cycle		●	82	86		%
	Switch Current Limit	(Note 3)		550	800		mA
	Switch V_{CESAT}	I_{SW} = 300mA			300	350	mV
	Switch Leakage Current	V_{SW} = 5V			0.01	1	µA
	$\overline{SHDN1}$ Input Voltage High			1			V
	$\overline{SHDN1}$ Input Voltage Low					0.3	V
	$\overline{SHDN1}$ Input Bias Current	$V_{\overline{SHDN1}}$ = 3V, Current Flows into Pin $V_{\overline{SHDN1}}$ = 0V, Current Flows into Pin			25 0.01	50 0.1	µA µA
Linear Regulator Controller							
I_{Q2}	V_{IN2} Quiescent Current		●	5	12	19	mA
V_{FB2}	FB2 Reference Voltage		 ●	1.203 1.198	1.210 1.210	1.217 1.222	V V
	FB2 Line Regulation	10V ≤ V_{IN2} ≤ 20V	●		0.01	0.03	%/V
	FB2 Input Bias Current	FB2 = V_{FB2}, Current Flows out of Pin	●		–0.6	–4	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = 1.5V, $V_{\overline{SHDN1}}$ = V_{IN1}, V_{IN2} = 12V, GATE = 6V, I_{POS} = I_{NEG} = 5V, V_{SHDN2} = 0.75V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_{GATE} = 3V to 10V	●	69	84		dB
V_{OL}	GATE Output Swing Low (Note 4)	I_{GATE} = 0mA	●		2.5	3	V
V_{OH}	GATE Output Swing High	I_{GATE} = 0mA	●	V_{IN2} – 1.6	V_{IN2} – 1		V
	I_{POS} + I_{NEG} Supply Current	3V ≤ I_{POS} ≤ 20V	●	0.3	0.625	1	mA
	Current Limit Threshold Voltage		 ●	42 37	50 50	58 63	mV mV
	Current Limit Threshold Voltage Line Regulation	3V ≤ I_{POS} ≤ 20V	●		–0.20	–0.50	%/V
	SHDN2 Sink Current	Current Flows Into Pin	●	2.5	5.0	8.0	µA
	SHDN2 Source Current	Current Flows Out of Pin	●	–8	–15	–23	µA
	SHDN2 Low Clamp Voltage		●		0.1	0.25	V
	SHDN2 High Clamp Voltage		●	1.50	1.85	2.20	V
	SHDN2 Threshold Voltage		●	1.18	1.21	1.240	V
	SHDN2 Threshold Hysteresis		●	50	100	150	mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 130°C/W)$

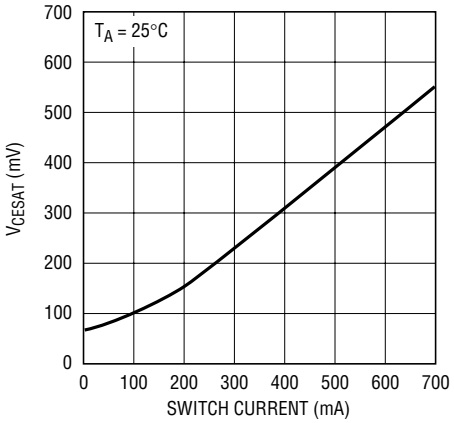
Note 3: Switch current limit is guaranteed by design and/or correlation to static test.

Note 4: The $V_{GS(th)}$ of the external MOSFET must be greater than 3V – V_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS

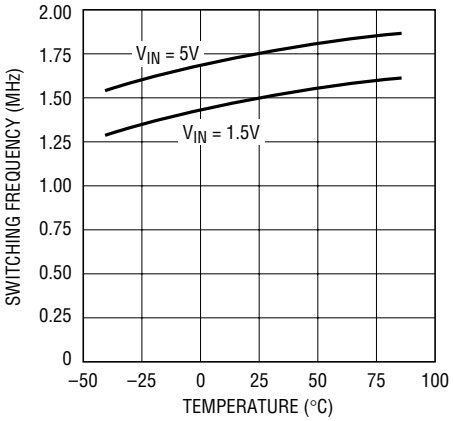
Boost Switching Regulator

Switch V_{CESAT} vs Switch Current



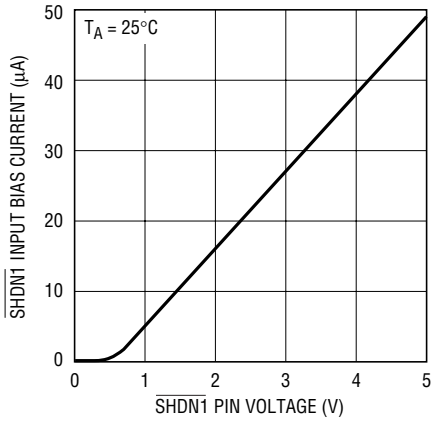
3150 G01

Oscillator Frequency vs Temperature



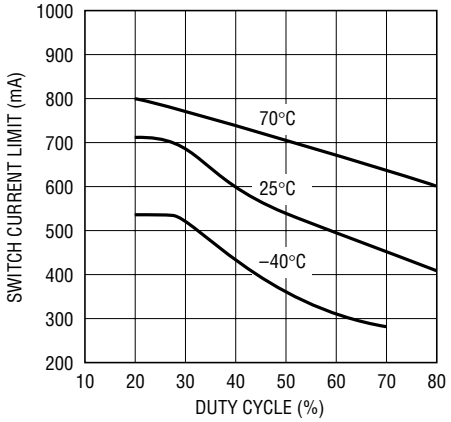
3150 G02

$\overline{SHDN1}$ Input Bias Current vs $V_{\overline{SHDN1}}$



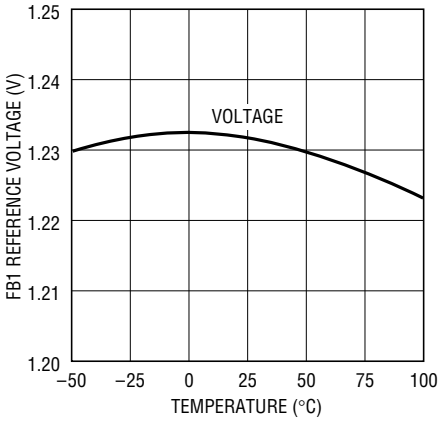
3150 G03

Switch Current Limit vs Duty Cycle



3150 G04

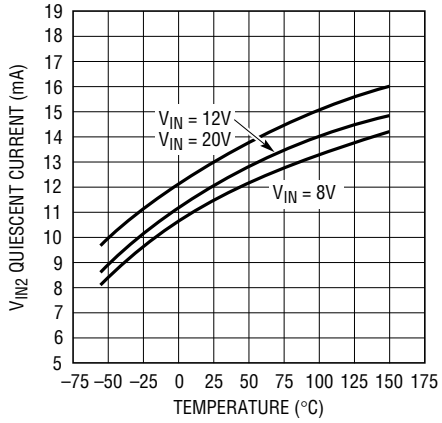
FB1 Reference Voltage vs Temperature



3150 G05

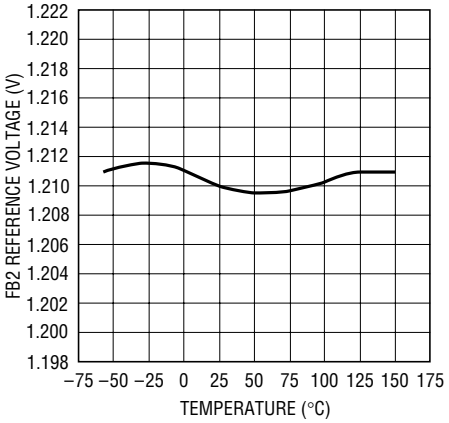
Linear Regulator Controller

V_{IN2} Quiescent Current vs Temperature



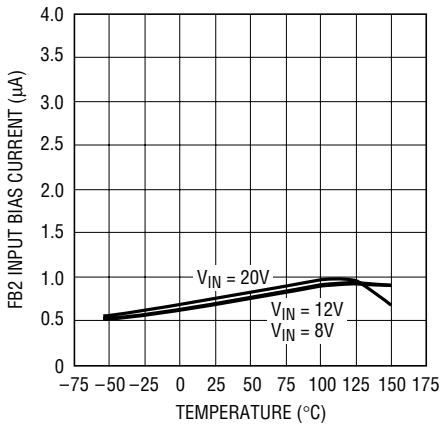
3150 G06

FB2 Reference Voltage vs Temperature



3150 G07

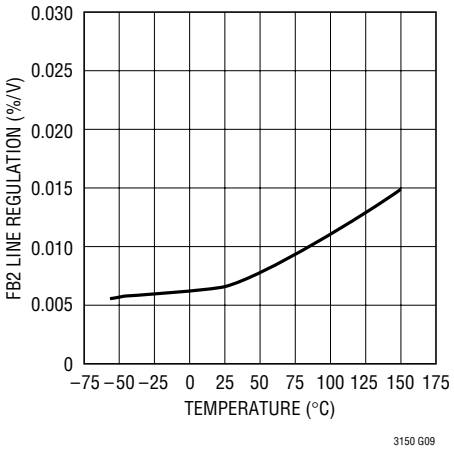
FB2 Input Bias Current vs Temperature



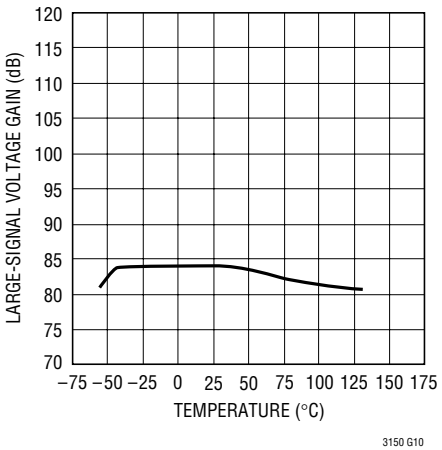
3150 G08

TYPICAL PERFORMANCE CHARACTERISTICS Linear Regulator Controller

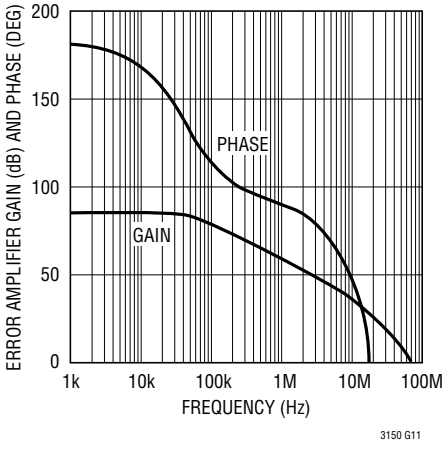
FB2 Line Regulation vs Temperature



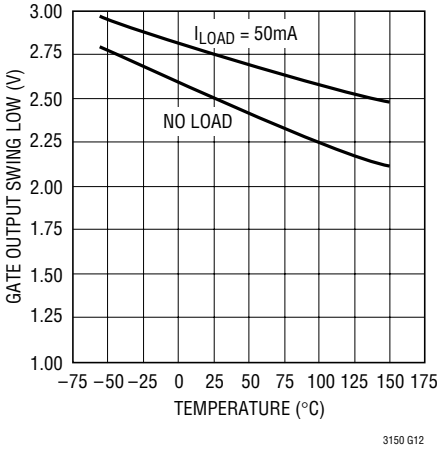
Error Amplifier Large-Signal Voltage Gain vs Temperature



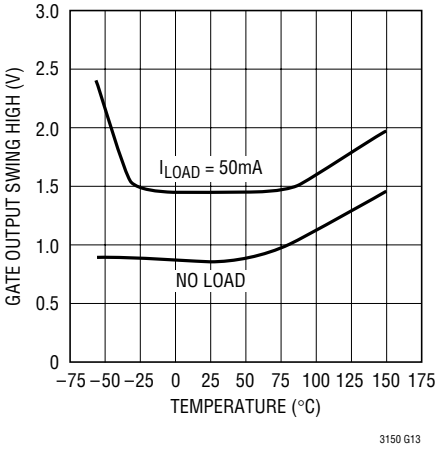
Gain and Phase vs Frequency



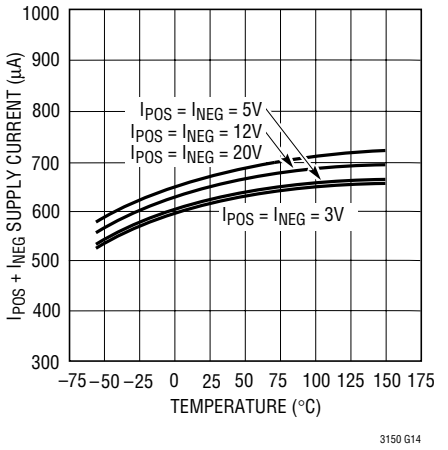
Gate Output Swing Low vs Temperature



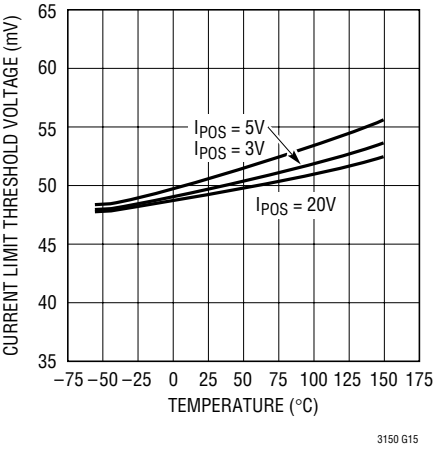
Gate Output Swing High (V_{IN2} – V_{GATE}) vs Temperature



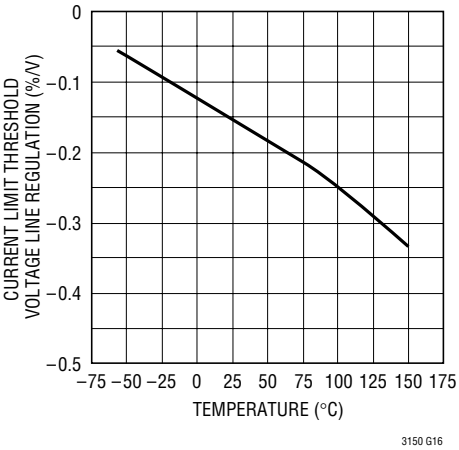
I_{POS} + I_{NEG} Supply Current vs Temperature



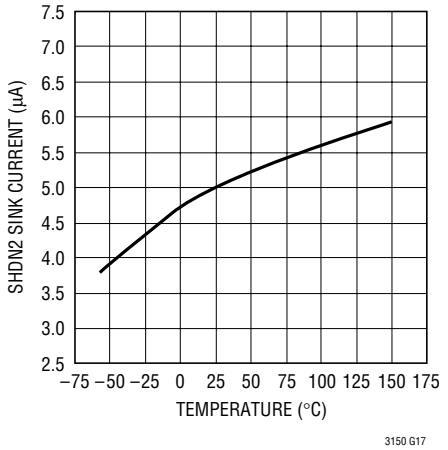
Current Limit Threshold Voltage vs Temperature



Current Limit Threshold Voltage Line Regulation vs Temperature

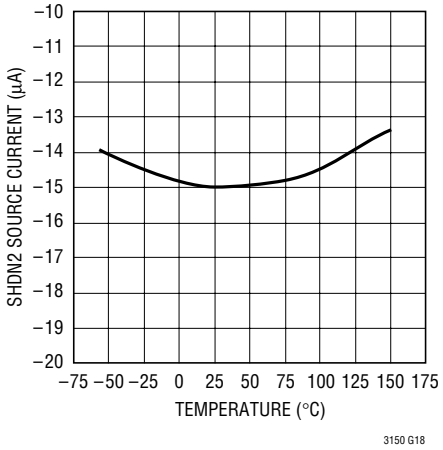


SHDN2 Sink Current vs Temperature

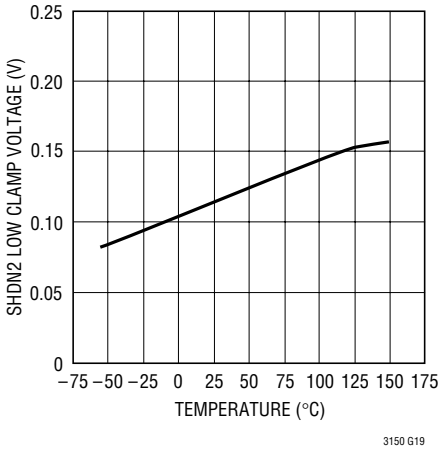


TYPICAL PERFORMANCE CHARACTERISTICS Linear Regulator Controller

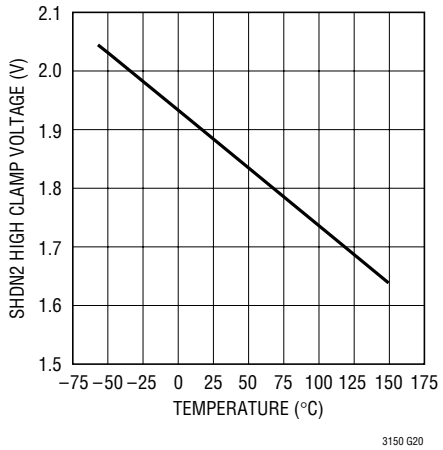
SHDN2 Source Current vs Temperature



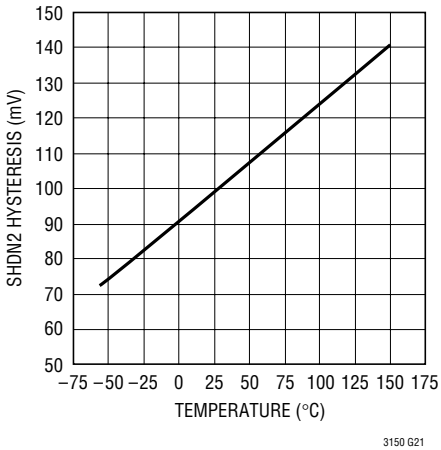
SHDN2 Low Clamp Voltage vs Temperature



SHDN2 High Clamp Voltage vs Temperature



SHDN2 Hysteresis vs Temperature



PIN FUNCTIONS

SW (Pin 1): Boost Converter Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

SWGND (Pin 2): Switch Ground. Tie directly to the local ground plane and the GNDs at Pins 6 and 15.

V_{IN1} (Pin 3): Boost Converter Input Supply Pin. Must be locally bypassed.

SHDN2 (Pin 4): This is a multifunction shutdown pin that provides GATE drive latchoff capability. A 15µA current source, that turns on when current limit is activated, charges a capacitor placed in series with SHDN2 to GND and performs a current limit time-out function. The pin is also the input to a comparator referenced to V_{REF} (1.21V). When the pin pulls above V_{REF}, the comparator latches the gate drive to the external MOSFET off. The comparator typically has 100mV of hysteresis and the SHDN2 pin can be pulled low to reset the latchoff function. This pin provides overvoltage protection or thermal shutdown protection when driven from various resistor divider schemes.

PIN FUNCTIONS

V_{IN2} (Pin 5): This is the input supply for the linear regulator control circuitry and provides sufficient gate drive compliance for the external N-channel MOSFET. The maximum operating V_{IN2} is 20V and the minimum operating V_{IN2} is set by V_{OUT} + (V_{GS} of the MOSFET at max I_{OUT}) + 1.6V (worst-case V_{IN2} to GATE output swing).

GND (Pin 6): Analog Ground. This pin is also the negative sense terminal for the internal 1.21V reference. Connect the LDO regulator external feedback divider network and frequency compensation components that terminate to GND directly to this pin for best regulation and performance. Also, tie this pin directly to SWGND (Pin 2) and GND (Pin 15).

NC (Pins 7, 10): No Connect.

FB2 (Pin 8): This is the inverting input of the error amplifier for the linear regulator. The noninverting input is tied to the internal 1.21V reference. Input bias current for this pin is typically 0.6μA flowing out of the pin. Tie this pin to a resistor divider network to set output voltage. Tie the top of the external resistor divider directly to the output load for best regulation performance.

COMP (Pin 9): This is the high impedance gain node of the error amplifier and is used for external frequency compensation. The transconductance of the error amplifier is 15 millimhos and open-loop voltage gain is typically 84dB. Frequency compensation is generally performed with a series RC + C network to ground.

GATE (Pin 11): This is the output of the error amplifier that drives N-channel MOSFETs with up to 5000pF of "effective" gate capacitance. The typical open-loop output impedance is 2Ω. When using low input capacitance MOSFETs (<1500pF), a small gate resistor of 2Ω to 10Ω dampens high frequency ringing created by an LC resonance due to the MOSFET gate's lead inductance and input capacitance. The GATE pin delivers up to 50mA for a few hundred nanoseconds when slewing the gate of the N-channel MOSFET in response to output load current transients.

I_{NEG} (Pin 12): This is the negative sense terminal of the current limit amplifier. A small sense resistor is connected in series with the drain of the external MOSFET and is connected between the I_{POS} and I_{NEG} pins. A 50mV threshold voltage in conjunction with the sense resistor value sets the current limit level. The current sense resistor can be a low value shunt or can be made from a piece of PC board trace. If the current limit amplifier is not used, tie the I_{NEG} pin to I_{POS} to defeat current limit. An alternative is to ground the I_{NEG} pin. This action disables the current limit amplifier and additional internal circuitry activates the timer circuit on the SHDN2 pin if the GATE pin swings to the V_{IN} rail. This option provides the user with a No R_{SENSE}™ current limit function.

I_{POS} (Pin 13): This is the positive sense terminal of the current limit amplifier. Tie this pin directly to the main input voltage from which the output voltage is regulated.

$\overline{\text{SHDN1}}$ (Pin 14): Boost Regulator Shutdown Pin. Tie to 1V or more to enable device. Ground to shut down. This pin must not float for proper operation. Connect $\overline{\text{SHDN1}}$ externally as it does not incorporate an internal pull-up or pull-down.

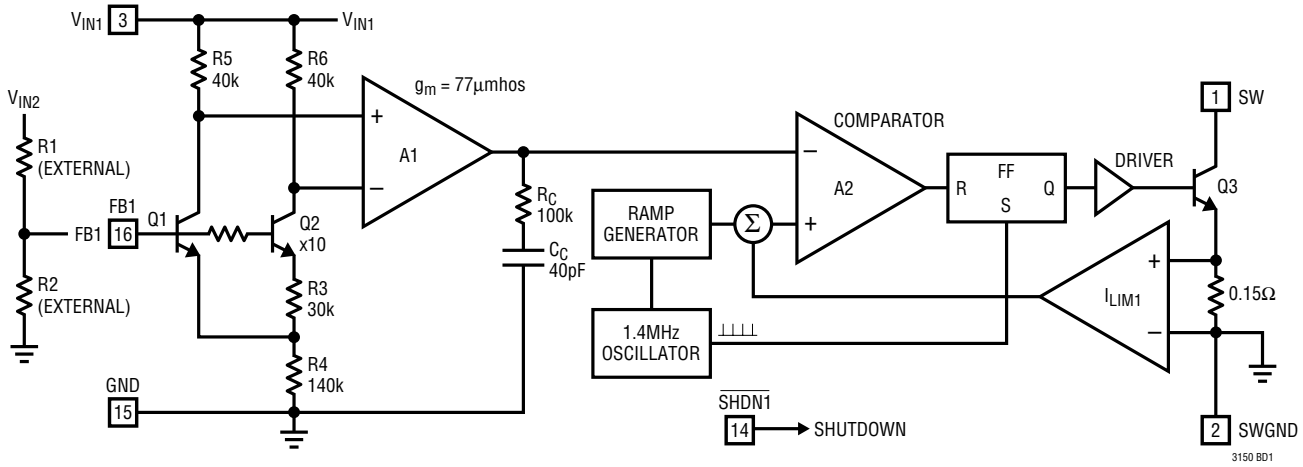
GND (Pin 15): Boost Converter Analog Ground. This pin is also the negative sense terminal for the FB1 1.23V reference. Connect the external feedback divider network, which sets the V_{IN2} supply voltage and terminates to GND, directly to this pin for best regulation and performance. Also, tie this pin directly to SWGND (Pin 2) and GND (Pin 6).

FB1 (Pin 16): Boost Regulator Feedback Pin. Reference voltage is 1.23V. Connect resistive divider tap here. Minimize trace area at FB1. Set $V_{OUT} = V_{IN2}$ according to $V_{OUT} = 1.23V(1 + R1/R2)$.

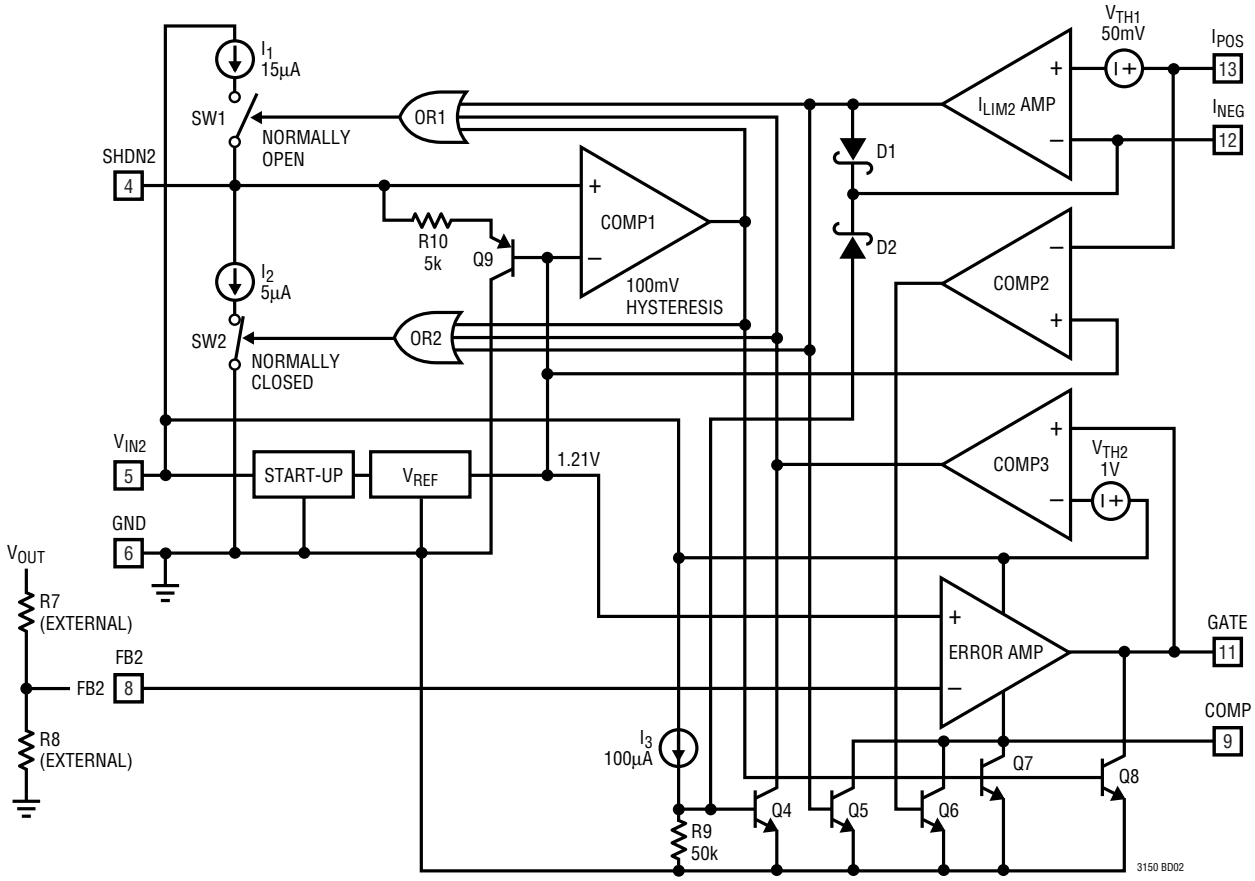
No R_{SENSE} is a trademark of Linear Technology Corporation.

BLOCK DIAGRAMS

Boost Switching Regulator



Linear Regulator Controller



APPLICATIONS INFORMATION

INTRODUCTION

With each new generation of computing systems, total power increases while system voltages fall. CPU core, logic and termination supplies below 1.8V are now common. Power supplies must not only regulate low output voltages, but must also operate from low input voltages. A low voltage, very low dropout linear regulator is an attractive conversion option for applications with output current in the range of several amperes. Component count and cost are low in comparison with switching regulator solutions and with low input-to-output differential voltages, efficiencies are comparable.

In addition to low input-to-output voltage conversion, these systems require stringent output voltage regulation. The output voltage specification includes input voltage change, output load current change, temperature change and output load current transient response. Total tolerances as low as ±2% are now required. For a 1.5V output voltage, this amounts to a mere ±30mV. Transient load current response is the most critical component as output current can cycle from zero to amps in tens of nanoseconds. These requirements mandate the need for a very accurate, very high speed regulator.

Historically employed solutions include monolithic 3-terminal linear regulators, PNP transistors driven by low cost control circuits and simple buck converter switching regulators. The 3-terminal regulator provides high integration, the PNP driven regulator provides low dropout performance and the switching regulator provides high electrical efficiency.

However, these solutions manifest a common trait of transient response measured in many microseconds. This fact translates to a regulator output decoupling capacitor scheme requiring several hundred microfarads of very low ESR bulk capacitance using multiple capacitors in parallel. This required bulk capacitance is in addition to the ceramic decoupling capacitor network that handles the transient load response during the first few hundred nanoseconds as well as providing high frequency noise immunity. The combined cost of all capacitors is a significant percentage of the total power supply cost.

The LT3150 controller IC is a unique, easy-to-use device that drives an external N-channel MOSFET as a source follower and realizes an extremely low dropout, ultrafast transient response regulator. The circuit achieves superior regulator bandwidth and transient load performance by eliminating expensive special polymer, tantalum or bulk electrolytic capacitors in the most demanding applications. Performance is optimized around the latest generation of low cost, low ESR, readily available ceramic capacitors. Users benefit directly by saving significant cost as all bulk capacitance is removed. Additional savings include insertion cost, purchasing/inventory cost and board space.

The precision-trimmed adjustable voltage LT3150 accommodates most power supply voltages. Proper selection of the N-channel MOSFET $R_{DS(ON)}$ allows user-settable dropout voltage performance. Transient load step performance is optimized for ceramic output capacitor networks allowing the regulator to respond to transient load changes in a few hundred nanoseconds. The output capacitor network typically consists of multiple 1µF to 10µF ceramic capacitors in parallel depending on the power supply requirements. The LT3150 also incorporates current limiting, on/off control for power supply sequencing and overvoltage protection or thermal shutdown with simple external components.

The LT3150 combines the benefits of low input voltage operation, very low dropout voltage performance, precision regulation and fast transient response. With low input/output differential voltage applications becoming the norm, an LT3150-based solution is a practical alternative to switching regulators providing comparable efficiency performance at an appreciable cost savings.

BLOCK DIAGRAM OPERATION

Gate drive for the external N-channel MOSFET in the linear regulator loop is provided by a current mode, internally compensated, fixed frequency step-up switching regulator. Referring to the Block Diagram, Q1 and Q2 form a bandgap reference core whose loop is closed around the output of the regulator. The voltage drop across R5 and R6

APPLICATIONS INFORMATION

is low enough such that Q1 and Q2 do not saturate, even when V_{IN1} is 1V. When there is no load, FB1 rises slightly above 1.23V, causing V_C (the error amplifier's output) to decrease. Comparator A2's output stays high, keeping switch Q3 in the off state. As increased output loading causes the FB1 voltage to decrease, A1's output increases. Switch current is regulated directly on a cycle-by-cycle basis by the V_C node. The flip flop is set at the beginning of each switch cycle, turning on the switch. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the V_C signal, comparator A2 changes state, resetting the flip flop and turning off the switch. More power is delivered to the output as switch current is increased. The output voltage, attenuated by external resistor divider R1 and R2, appears at the FB1 pin, closing the overall loop. Frequency compensation is provided internally by R_C and C_C. Transient response can be optimized by the addition of a phase lead capacitor C_{PL} in parallel with R1 in applications where large value or low ESR output capacitors are used.

As the load current is decreased, the switch turns on for a shorter period each cycle. If the load current is further decreased, the converter will skip cycles to maintain output voltage regulation.

The linear regulator controller section of the LT3150 Block Diagram consists of a simple feedback control loop and multiple protection functions. Examining the Block Diagram for the LT3150, a start-up circuit provides controlled start-up, including the precision-trimmed bandgap reference, and establishes all internal current and voltage biasing.

Reference voltage accuracy at the FB2 pin is specified as ±0.6% at room temperature and as ±1% over the full operating temperature range. This places the LT3150 among a select group of regulators with a very tightly specified reference voltage tolerance. The 1.21V reference is tied to the noninverting input of the main error amplifier in the feedback control loop.

The error amplifier consists of a single high gain g_m stage with a transconductance equal to 15 millimhos. The inverting terminal is brought out as the FB2 pin. The g_m stage provides differential-to-single ended conversion at the COMP pin. The output impedance of the g_m stage is about 1MΩ and thus, 84dB of typical DC error amplifier open-loop gain is realized along with a typical 75MHz uncompensated unity-gain crossover frequency. Note that the overall feedback loop's DC gain decreases from the gain provided by the error amplifier by the attenuation factor in the resistor divider network which sets the DC output voltage. External access to the high impedance gain node of the error amplifier permits typical loop compensation to be accomplished with a series RC + C network to ground.

A high speed, high current output stage buffers the COMP node and drives up to 5000pF of "effective" MOSFET gate capacitance with almost no change in load transient performance. The output stage delivers up to 50mA peak when slewing the MOSFET gate in response to load current transients. The typical output impedance of the GATE pin is typically 2Ω. This pushes the pole due to the error amplifier output impedance and the MOSFET input capacitance well beyond the loop crossover frequency. If the capacitance of the MOSFET used is less than 1500pF, it may be necessary to add a small value series gate resistor of 2Ω to 10Ω. This gate resistor helps damp the LC resonance created by the MOSFET gate's lead inductance and input capacitance. In addition, the pole formed by this resistance and the MOSFET input capacitance can be fine tuned.

Because the MOSFET pass transistor is connected as a source follower, the power path gain is much more predictable than designs that employ a discrete PNP transistor as the pass device. This is due to the significant production variations encountered with PNP Beta. MOSFETs are also very high speed devices which enhance the ability to produce a stable wide bandwidth control loop. An additional advantage of the follower topology is inherently good line rejection. Input supply disturbances do not propagate through to the output. The feedback loop for a regulator circuit is completed by providing an error signal to the FB2 pin. A resistor divider network senses the output voltage and sets the regulated DC bias point. In general, the LT3150 regulator feedback loop permits a loop crossover frequency on the order of 1MHz while maintaining good phase and gain margins. This unity-gain frequency is a factor of 20 to 30 times the bandwidth of currently implemented regulator

APPLICATIONS INFORMATION

solutions for microprocessor power supplies. This significant performance benefit is what permits the elimination of all bulk output capacitance.

Several other unique features are included in the design that increase its functionality and robustness. These functions comprise the remainder of the Block Diagram.

A high side sense, current limit amplifier provides active current limiting for the regulator. The current limit amplifier uses an external low value shunt resistor connected in series with the external MOSFET's drain. This resistor can be a discrete shunt resistor or can be manufactured from a Kelvin-sensed section of "free" PC board trace. All load current flows through the MOSFET drain and thus, through the sense resistor. The advantage of using high side current sensing in this topology is that the MOSFET's gain and the main feedback loop's gain remain unaffected. The sense resistor develops a voltage equal to $I_{OUT}(R_{SENSE})$. The current limit amplifier's 50mV threshold voltage is a good compromise between power dissipation in the sense resistor, dropout voltage impact and noise immunity. Current limit activates when the sense resistor voltage equals the 50mV threshold.

Two events occur when current limit activates: the first is that the current limit amplifier drives Q5 in the Block Diagram and clamps the positive swing of the COMP node in the main error amplifier to a voltage that provides an output load current of $50mV/R_{SENSE}$. This action continues as long as the output current overload persists. The second event is that a timer circuit activates at the SHDN2 pin. This pin is normally held low by a 5μA active pull-down that limits to ≈ 100mV above ground. When current limit activates, the 5μA pull-down turns off and a 15μA pull-up current source turns on. Placing a capacitor in series with the SHDN2 pin to ground generates a programmable time ramp voltage.

The SHDN2 pin is also the positive input of COMP1. The negative input is tied to the internal 1.21V reference. When the SHDN2 pin ramps above V_{REF}, the comparator drives Q7 and Q8. This action pulls the COMP and GATE pins low and latches the external MOSFET drive off. This condition reduces the MOSFET power dissipation to zero. The time period until the latched-off condition occurs is typically equal to $C_{SHDN2}(1.11V)/15\mu A$. For example, a 1μF capacitor on the SHDN2 pin yields a 74ms ramp time. In short, this unique circuit block performs a current limit time-out function that latches off the regulator drive after a predefined time period. The time-out period selected is a function of system requirements including start-up and safe operating area. The SHDN2 pin is internally clamped to typically 1.85V by Q9 and R10. The comparator tied to the SHDN2 pin has 100mV of typical hysteresis to provide noise immunity. The hysteresis is especially useful when using the SHDN2 pin for thermal shutdown.

Restoring normal operation after the load current fault is cleared is accomplished in two ways. One option is to recycle the V_{IN2} LT3150 supply voltage as long as an external bleed path for the SHDN2 pin capacitor is provided. The second option is to provide an active reset circuit that pulls the SHDN2 pin below V_{REF}. Pulling the SHDN2 pin below V_{REF} turns off the 15μA pull-up current source and reactivates the 5μA pull-down. If the SHDN2 pin is held below V_{REF} during a fault condition, the regulator continues to operate in current limit into a short. This action requires being able to sink 15μA from the SHDN2 pin at less than 1V. The 5μA pull-down current source and the 15μA pull-up current source are designed low enough in value so that an external resistor divider network can drive the SHDN2 pin to provide overvoltage protection or to provide thermal shutdown with the use of a thermistor in the divider network. Diode-ORing these functions together is simple to accomplish and provides multiple functionality for one pin.

If the current limit amplifier is not used, two choices present themselves. The simplest choice is to tie the I_{NEG} pin directly to the I_{POS} pin. This action defeats current limit and provides the simplest, no frills circuit. Applications in which the current limit amplifier is not used are where extremely low dropout voltages must be achieved and the 50mV threshold voltage cannot be tolerated.

However, a second available choice permits a user to provide short-circuit protection with no external sensing. This technique is activated by grounding the I_{NEG} pin. This action disables the current limit amplifier because Schottky diode D1 clamps the amplifier's output and prevents Q5 from pulling down the COMP node. In addition, Schottky diode D2 turns off pull-down transistor Q4. Q4 is normally on and

APPLICATIONS INFORMATION

holds internal comparator COMP3's output low. This comparator circuit, now enabled, monitors the GATE pin and detects saturation at the positive rail. When a saturated condition is detected, COMP3 activates the shutdown timer. Once the time-out period occurs, the output is shut down and latched off. The operation of resetting the latch remains the same. Note that this technique does not limit the FET current during the time-out period. The output current is only limited by the input power supply and the input/output impedance. Setting the timer to a short period in this mode of operation keeps the external MOSFET within its SOA (safe operating area) boundary and keeps the MOSFET's temperature rise under control.

Unique circuit design incorporated into the LT3150 alleviates all concerns about power supply sequencing. The issue of power supply sequencing is an important topic as the typical LT3150 application has two separate power supply inputs, V_{IN1} and V_{IN2}. If the V_{IN2} supply voltage is slow in ramping up or is held off by $\overline{SHDN1}$, insufficient MOSFET gate drive exists and therefore, the output voltage does not come up. This statement is true as long as the V_{IN1} input voltage is lower than the threshold of the external MOSFET. Prior to the boost converter powering up, V_{IN2} equals $V_{IN1} – V_F$ due to the DC path present through the boost inductor. If V_{IN1} is high enough, the MOSFET turns on and pulls the output voltage up. If this situation exists and the output must be held off, then pulling the SHDN2 pin high actively holds the output off. Pull the SHDN2 pin low to allow start-up, as the SHDN2 high logic state is a latched condition.

If V_{IN2} is present, but the V_{IN1} supply voltage tied to the I_{POS} pin is slow in ramping, then the feedback loop wants to drive the GATE pin to the positive V_{IN2} rail. This results in a large current as the V_{IN1} supply ramps up. However, undervoltage lockout circuit COMP2, which monitors the I_{POS} supply voltage, holds Q6 on and pulls the COMP pin low until the I_{POS} voltage increases to greater than the internal 1.21 reference voltage. The undervoltage lockout circuit then smoothly releases the COMP pin and allows the output voltage to come up in dropout from the input supply voltage. An additional benefit derived from the speed of the LT3150 feedback loop is that turn-on overshoot is virtually nonexistent in a properly compensated system.

BOOST REGULATOR COMPONENT SELECTION

Diode

Linear Technology recommends the use of a Schottky diode with the LT3150. For input supply voltages less than 2V, the Motorola MBR0520 or equivalent is a good choice due to its small size, low cost and low forward voltage. The average diode current equals the V_{IN2} supply current of 12mA typically. The peak diode current equals the peak switch current, which in these low input-to-output voltage applications ranges from 100mA to 200mA.

The diode's forward voltage during its conduction period directly affects the duty cycle of the boost converter. These low input-to-output voltage applications require the boost converter to operate at duty cycles close to the maximum and the difference of a few hundred millivolts in the diode forward voltage results in a duty cycle difference of several percent. For supply voltages greater than 2V, a 1N4148 is suitable and lowers cost.

Inductor

Use inductors with a saturation current rating (where inductance is approximately 70% of zero current inductance) of 0.2A or greater. Also, choose an inductor with a DCR of 2.5Ω or less. The inductor's DCR also affects the boost converter's duty cycle. A larger DCR value increases the required duty cycle. An inductance value between 4.7µH and 10µH works well in most applications.

Table 1 lists several 10µH inductors that work with the LT3150, although this is by no means an exhaustive list. Many magnetic vendors have components suitable for use in this boost application.

Input Capacitor

The input bypass capacitors serve as the reservoir capacitor for the boost regulator, the linear regulator and whatever other system circuitry the input supply powers. Therefore, the input capacitor network is most likely distributed along the input supply PCB plane.

However, the switching of current at high speed by the boost regulator mandates a local bypass capacitor at the V_{IN1} pin. Place this input capacitor physically close to the

APPLICATIONS INFORMATION

Table 1. Inductor Vendors

VENDOR	PHONE	URL	PART NUMBER	INDUCTANCE	DCR	I_{SAT}
Murata	(404) 436-1300	www.murata.com	LQH31CN100K03K LQH32CN100K23K	10µH 10µH	1.3Ω 0.44Ω	0.23A 0.3A
Panasonic	(800) 344-2112	www.panasonic.com	ELJPC100KF	10µH	2.2Ω	0.21A
Sumida	(847) 956-0666	www.sumida.com	CDRH3D16100	10µH	0.21Ω	0.55A
Taiyo Yuden	(800) 348-2496	www.t-yuden.com	LQLB2016T100M LQLB2518T100M	10µH 10µH	0.5Ω 0.25Ω	0.155A 0.165A
Toko	(847) 297-0070	www.toko.com	LLM3225-100K	10µH	1.7Ω	0.22A

V_{IN1} pin. ESR is not critical and in most cases, an inexpensive tantalum or ceramic capacitor with a value from 1µF to 4.7µF is appropriate.

Output Capacitor

The output capacitor choice is far more important. The capacitor's characteristics determines output voltage ripple. The output capacitor must have enough capacitance to satisfy the load under transient conditions and it must shunt the switched component of current coming through the diode. Output voltage ripple results because this switched current passes through the capacitor's finite output impedance. The capacitor must have low impedance at the 1.4MHz switching frequency of the LT3150. At this frequency, the capacitor's equivalent series resistance (ESR) usually dominates the impedance. Choosing a capacitor with lower ESR results in lower output voltage ripple.

However, consider loop stability when choosing the output capacitor because the LT3150 is internally compensated and no access is provided to this internal compensation. Small, low cost tantalum capacitors have some ESR. This ESR enhances stability due to the addition of a zero in the regulator feedback loop. Ceramic capacitors are very popular, having attractive characteristics such as near-zero ESR, small size and low cost. Replacing the tantalum output capacitor with a ceramic unit decreases the phase margin, in some cases to unacceptable levels. The addition of a phase lead capacitor and an isolating resistor in the feedback divider network can be used to stabilize the feedback loop, but the added component count and cost makes the use of a tantalum output capacitor the simpler and preferred choice.

The boost regulator output capacitor also serves as the V_{IN2} input bypass capacitor. Place this capacitor physically close to the V_{IN2} pin. This capacitor supplies the instantaneous current to slew the external MOSFET's gate capacitance quickly during an output load current transient.

LINEAR REGULATOR COMPONENT SELECTION

Output Capacitors

The LT3150 linear regulator is stable with a wide range of output capacitors (assuming the feedback loop is properly frequency compensated). However, using multiple, low value, very low ESR ceramic capacitors (1µF to 4.7µF) in parallel optimizes the load transient response of an LT3150 feedback loop. As is discussed in the Frequency Compensation section, the output capacitor value is critical because it sets the location of a pole in the feedback loop that determines the unity-gain crossover frequency. Therefore, the characteristics of ceramic capacitors warrant some discussion.

Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit very strong voltage and temperature coefficients. The X5R and X7R dielectrics yield highly stable characteristics and are more suitable for use as the output capacitor at fractionally increased cost. The X5R and X7R dielectrics both exhibit excellent voltage coefficient characteristics. The X7R type works over a larger temperature range and exhibits better temperature stability whereas X5R is less expensive and is available in higher values.

APPLICATIONS INFORMATION

Figures 1 and 2 show voltage coefficient and temperature coefficient comparisons between Y5V and X5R material. With the critical pole in the LT3150 feedback loop being set by the absolute value of the output capacitor, it is obvious why Linear Technology strongly recommends the use of ceramic capacitors with X5R or X7R dielectric material.

MOSFET Selection

MOSFET selection criteria include threshold voltage $V_{GS(TH)}$, maximum continuous drain current I_D, on-resistance $R_{DS(ON)}$, maximum drain-to-source voltage V_{DS} and package thermal resistance $R_{TH(JA)}$.

Linear Technology recommends the use of a logic-level threshold MOSFET in LT3150 applications. The V_{GS} range, as defined by the threshold voltage and the load current range, fits well within the boost regulator's capability and the output swing range of the error amplifier. The MOSFET's continuous drain current rating must equal or exceed the maximum load current and the maximum drain-to-source voltage must exceed the maximum input voltage.

The most critical specification is the MOSFET $R_{DS(ON)}$. Calculate the required $R_{DS(ON)}$ from the following formula:

$$\text{MOSFET } R_{DS(ON)} \leq \frac{V_{IN(MIN)} - V_{OUT(MIN)}}{3 \bullet I_{OUT(MAX)}}$$

The additional factor of three in the equation's denominator accounts for production variation, the temperature coefficient of $R_{DS(ON)}$, voltage dips in V_{IN} during transient output load steps and other operating point characteristics. Although the factor of three is slightly conservative, this imposes no cost penalty. As an example, consider the 1.8V to 1.5V at 4A application on the front page. Assuming the 1.8V input and the 1.5V output each have a ±5% tolerance,

$$R_{DS(ON)} = \frac{(0.95 \bullet 1.8V) - (0.95 \bullet 1.5V)}{3 \bullet 4A} \leq 23.8m\Omega$$

A Siliconix Si4410 MOSFET with an $R_{DS(ON)}$ of 20mΩ is a close match. Although the Si4410's 30V maximum V_{DS} and 8A maximum I_D ratings exceed the application's requirements, the Si4410's low cost makes it an excellent choice.

As the final criteria, consider the thermal resistance $R_{TH(JA)}$ of the MOSFET's package. The temperature rise in the MOSFET must be kept under control and within the manufacturer's maximum junction temperature specification. The power dissipated in the MOSFET is calculated by:

$$P_{MOSFET} = (V_{IN} - V_{OUT}) \bullet I_{OUT}$$

In the design example, P_{MOSFET} = (1.8V – 1.5V) • 4A = 1.2W. The Si4410's $R_{TH(JA)}$ is 50°C/W for its S0-8 package, which translates to a 60°C temperature rise above ambient. MOSFET manufacturers have significantly lowered the thermal resistance of modern devices with improved packages. These packages provide exposed backsides that directly transfer heat to the PCB board. These packages enable LT3150 applications with much higher output currents while keeping the MOSFET temperature in control.

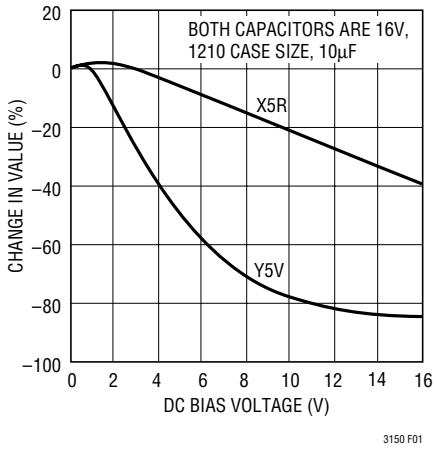


Figure 1. Ceramic Capacitor DC Bias Characteristics

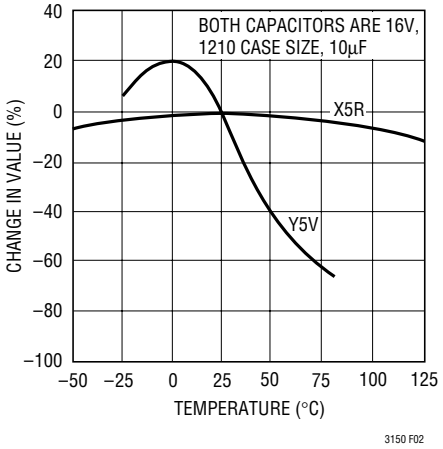


Figure 2. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

Frequency Compensation

Frequency compensation is the most critical step in designing an LT3150 application circuit. Frequency compensation stabilizes the feedback loop under all line, load and temperature conditions and determines the transient load step performance.

To start the frequency compensation process, gather the following application information. Determine the output voltage, the minimum and maximum output currents, the transconductance (g_{fs}) of the selected MOSFET at the minimum and maximum output currents and the output capacitor type (ceramic, tantalum, electrolytic).

Frequency compensation is accomplished with a passive network tied from the LT3150's COMP pin to ground. The LT3150 generally employs a Type-2 frequency compensation method. The "Type-2" method uses two poles and one zero. The output capacitor type determines how the zero in the feedback loop is set. Ceramic capacitors typically have very low ESR (equivalent series resistance) and therefore the COMP pin network sets the "zero" location. Tantalum and electrolytic capacitors typically have sufficient ESR such that the "zero" formed by the ESR and the capacitance value is used. Using tantalum or electrolytic capacitors in LT3150 applications is somewhat more challenging because the user must choose capacitors with the proper ESR plus capacitance value to place the zero at the correct spot in the frequency response.

Refer to the simplified LT3150 block diagram shown in Figure 3 during the frequency compensation discussion that follows.

Figure 4 illustrates the typical bode plot and the pole/zero locations with the use of low ESR ceramic output capacitors.

Figure 5 illustrates the typical bode plot and the pole/zero locations with the use of tantalum or electrolytic output capacitors.

In both output capacitor cases, the location of the first pole, P1, is set by the error amplifier COMP pin's open-loop output impedance, R_O, and compensation capacitor, C1. The low frequency gain is set by $g_{m1} \bullet R_O \bullet (V_{REF}/V_{OUT})$

In the case of low ESR ceramic capacitors, R1 in series with C1 in the COMP pin network sets the zero, Z1. With tantalum or electrolytic capacitors, the ESR in series with the output capacitor C_O sets Z1. Z1's location establishes the mid-band gain or "shelf" gain. For a given value of output capacitance, the "shelf" gain determines the regulator's transient response to an output load step, especially the output voltage's peak overshoot and undershoot. For a given output load current change, a corresponding delta in the MOSFET's V_{GS} occurs. This ΔV_{GS} divided by the "shelf gain" sets how much the FB2 must change and thus, results in output voltage perturbation. Higher "shelf" gain results in lower transient response peak deviations. Higher shelf gain also translates to a

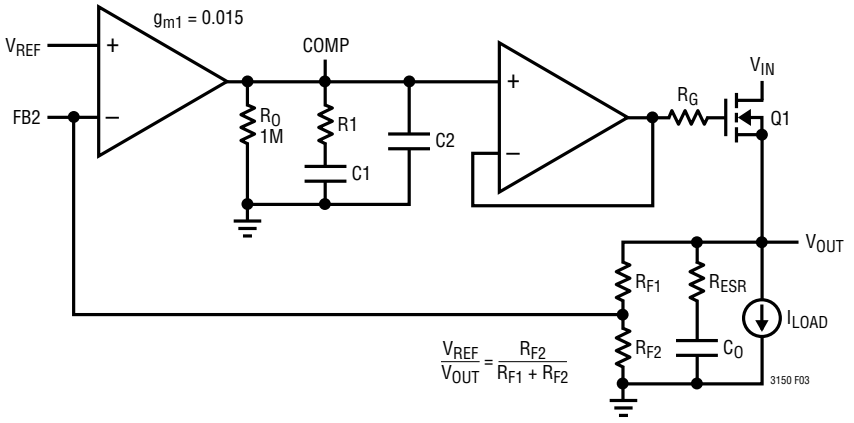


Figure 3. Simplified Block Diagram for Frequency Compensation

APPLICATIONS INFORMATION

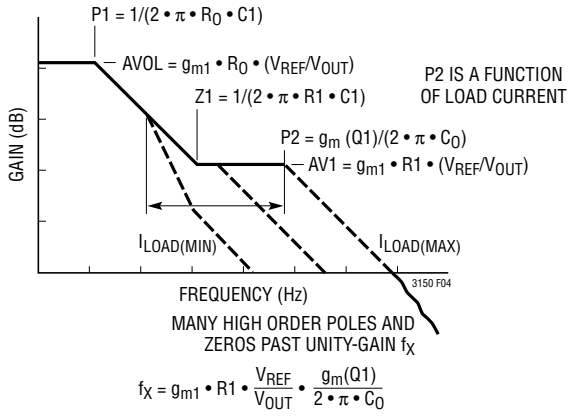


Figure 4. Typical Bode Plot for Low ESR Ceramic Output Capacitors

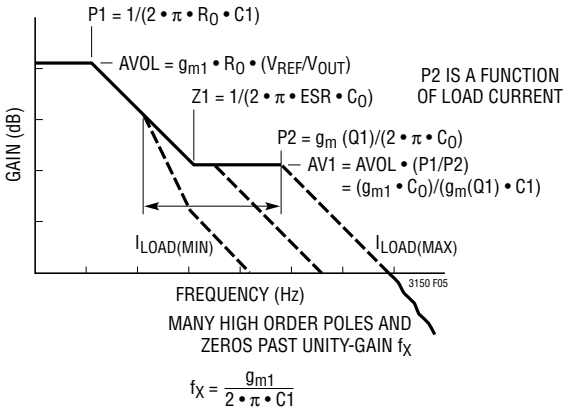


Figure 5. Typical Bode Plot for Tantalum or Electrolytic Output Capacitors

higher unity gain bandwidth crossover frequency, f_X. f_X must be set to a value that provides adequate phase and gain margin and this criteria limits the shelf gain value. If higher shelf gain is required for a given application, then increase output capacitance.

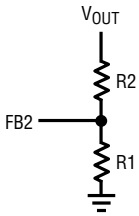
In both output capacitor cases, the location of the second pole, P2, is set by the MOSFET's transconductance, $g_m(Q1)$, and the value of the output capacitor, C_O. The output load current sets the transconductance of the MOSFET. P2 moves as a function of load current and consequently, so does the unity-gain crossover frequency, f_X. Figures 4 and 5 depict this behavior. At very low output currents, P2's location moves to a very low frequency. Therefore, set Z1 at a low enough frequency to provide adequate phase boost. A temptation is to set Z1's value equal to P2's value at minimum output load current. The bode plot then exhibits a single pole response at minimum output current. However, this either makes the "shelf gain" and f_X too high for stability or it makes the small signal settling time very long. Set Z1 above the minimum value for P2 so that at small output load currents, the second pole P2 occurs and then Z1 provides phase boost prior to crossing unity gain.

At the highest load current levels, several poles and zeros exist just beyond the unity-gain crossover frequency. Sometimes, the gain peaks back above unity and a high frequency, low level oscillation appears. A high frequency pole is necessary to roll off the response. In the case of ceramic output capacitors, capacitor C2 in Figure 4 sets this pole in combination with R1. In the case of electrolytic or tantalum output capacitors, some small ceramic capacitors in parallel with the main output capacitors usually provide the desired response.

Finally, look for very high frequency gate oscillations in the range of 2MHz to 10MHz. Small MOSFETs with low gate capacitance are most susceptible to this issue. This oscillation is typically caused by the MOSFET's "effective" gate capacitance and the MOSFET's parasitic source inductance resonating. The MOSFET's source inductance is the sum of the device's bond wire plus package lead inductance and the PCB trace inductance between the MOSFET's source and the actual output capacitors. Although the MOSFET's internal inductance is fixed, proper PCB layout techniques minimize the external inductance. Minimize the distance between the MOSFET's source and the output decoupling capacitors and run wide planes if possible. Connect the top of the feedback divider at the point closest to the actual load rather than the MOSFET source. If high frequency oscillations persist, a small value resistor in the range of 1Ω to 50Ω in series with the gate of the MOSFET typically eliminates this ringing. The inclusion of a gate resistor may permit the high frequency pole discussed in the preceding paragraph to be eliminated or fine tuned.

TYPICAL APPLICATIONS

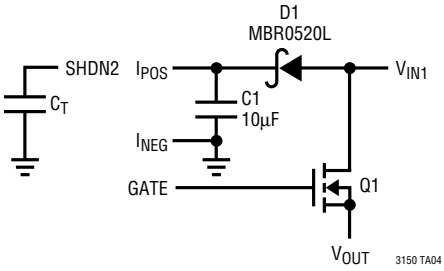
Setting the Linear Regulator Output Voltage



$V_{OUT} = 1.21V(1 + R2/R1)$

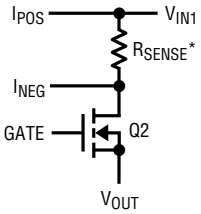
3150 TA03

Using No R_{SENSE} Current Limit



3150 TA04

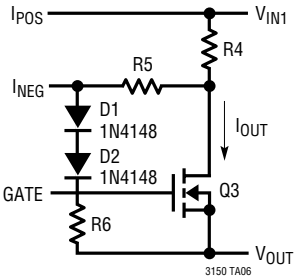
Setting Current Limit



*$I_{LIM} = 50mV/R_{SENSE}$
R_{SENSE} = DISCRETE SHUNT RESISTOR OR
R_{SENSE} = KELVIN-SENSED PC BOARD TRACE
ACTIVATING CURRENT LIMIT ALSO ACTIVATES THE SHDN2 PIN TIMER

3150 TA05

Current Limit with Foldback Limiting Example

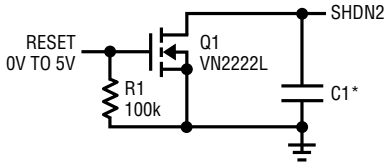


3150 TA06

SET R5 << R6

$$I_{OUT} = \frac{50mV}{R4}\left(\frac{R6}{R5 + R6}\right) - \frac{(V_{IN1} - V_{OUT} - 2V_F)}{R4}\left(\frac{R5}{R5 + R6}\right)$$

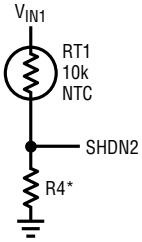
Shutdown Time-Out with Reset



*C1 = 15µA(t)/1.11V
t = SHUTDOWN LATCHOFF TIME

3150 TA07

Basic Thermal Shutdown

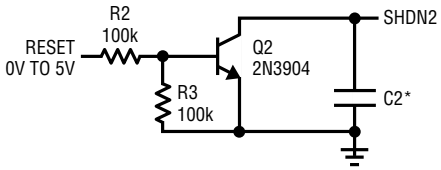


RT1 = DALE NTHS-1206N02
THERMALLY MOUNT RT1
IN CLOSE PROXIMITY
TO THE EXTERNAL
N-CHANNEL MOSFET

*CHOOSE R4 BASED ON V_{IN1} AND REQUIRED THERMAL SHUTDOWN TEMPERATURE

3150 TA08

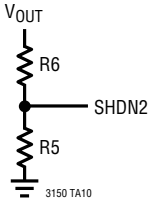
Shutdown Time-Out with Reset



*C2 = 15µA(t)/1.11V
t = SHUTDOWN LATCH-OFF TIME

3150 TA09

Overvoltage Protection

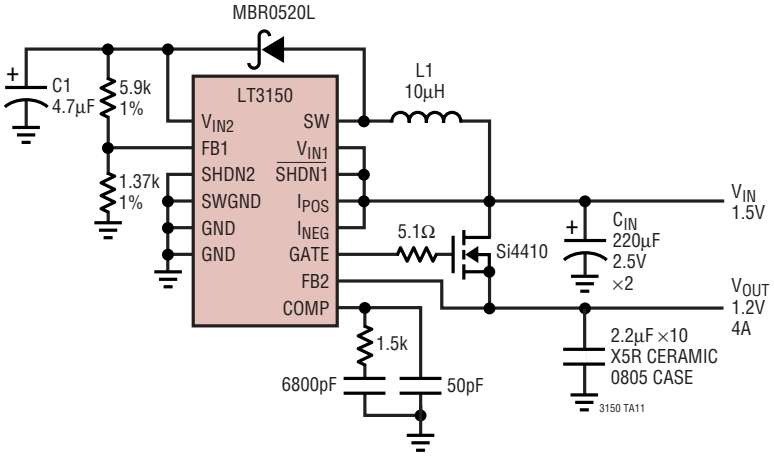


3150 TA10

$V_{OUT(uth)} = 1.21(R6/R5) + 5\mu A(R6)$
$V_{OUT(lth)} = 1.11(R6/R5) - 15\mu A(R6)$

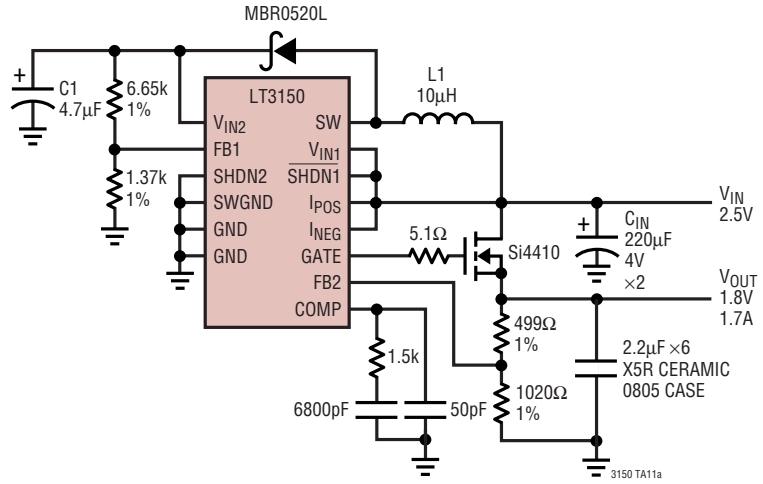
TYPICAL APPLICATIONS

1.5V to 1.2V, 4A Very Low Dropout Linear Regulator



C_{IN}: PANASONIC SP SERIES EEFUE0E221R 20%
C1: AVX TAJA475M020R 20V 20%
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100

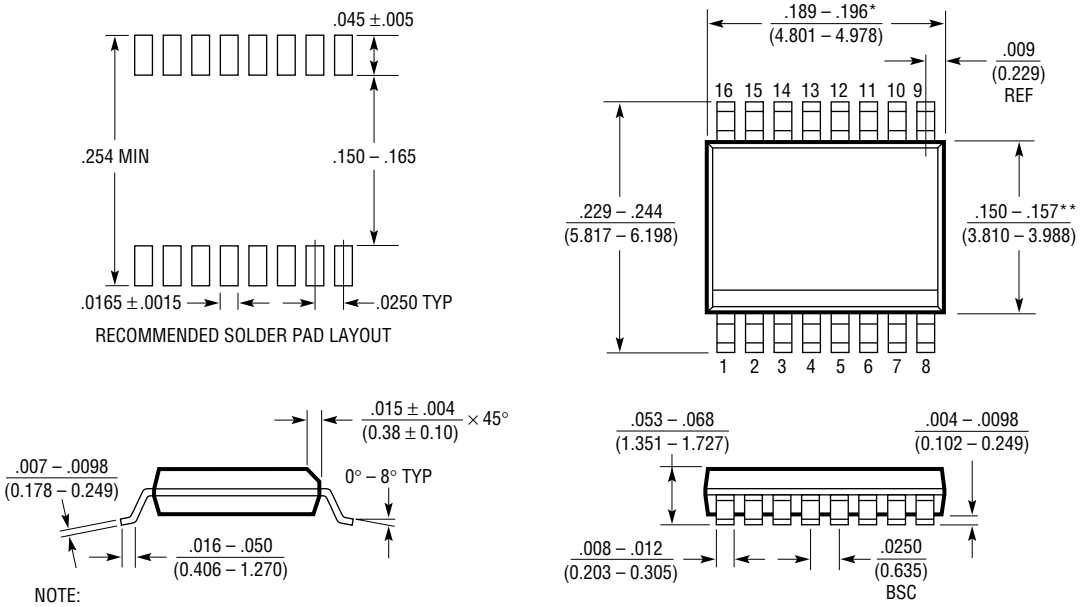
2.5V to 1.8V, 1.7A Low Dropout Linear Regulator



C_{IN}: PANASONIC SP SERIES EEFUE0G221R 20%
C1: AVX TAJA475M020R 20V 20%
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

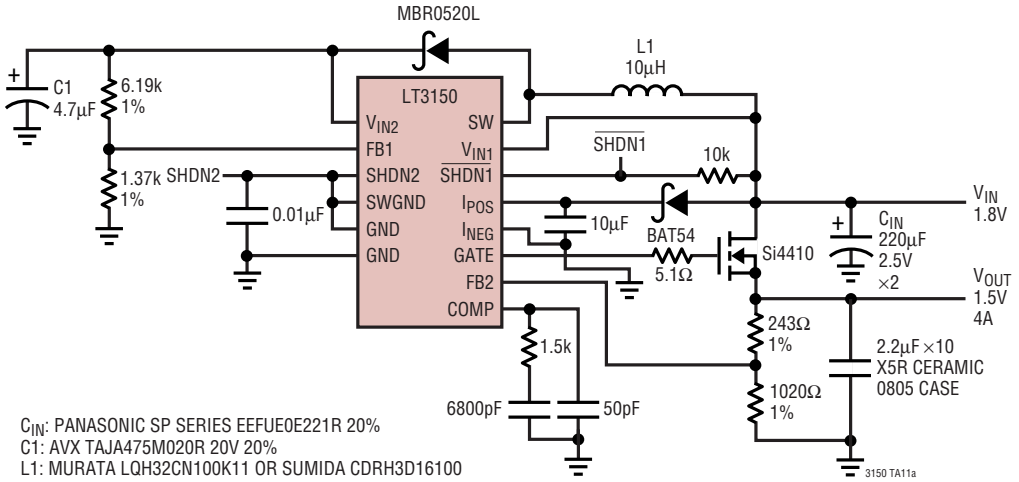
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

TYPICAL APPLICATION

1.8V to 1.5V, 4A Very Low Dropout Linear Regulator with No R_{SENSE} Current Limiting and Shutdown



C_{IN}: PANASONIC SP SERIES EEFUE0E221R 20%
C1: AVX TAJA475M020R 20V 20%
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1573	UltraFast Transient Response Low Dropout Regulator PNP Driver, Up to 5A	V_{IN}: 2.8V to 10V, V_{OUT}: 1.265V, Dropout Voltage: 0.35V, I_Q: 1.7mA, I_{SD}: 200µA, Requires External PNP Transistor, S8 Package
LT1575/LT1577	UltraFast Transient Response Low Dropout Regulator MOSFET Driver, Up to 10A	V_{IN}: 1.5V to 22V, V_{OUT}: 1.21V, Dropout Voltage: 0.15V, I_Q: 12mA, LT1577 is Dual Version, N8, S8 Packages
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, V_{OUT}: 1.22V, Dropout Voltage: 0.30V, I_Q: 20µA, I_{SD}: <1µA, Low Noise <20$\mu V_{RMS\ P-P}$, Stable with 1µF Ceramic Capacitors, ThinSOT Package
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, V_{OUT}: 1.22V, Dropout Voltage: 0.30V, I_Q: 25µA, I_{SD}: <1µA, Low Noise <20$\mu V_{RMS\ P-P}$, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, V_{OUT}: 1.22V, Dropout Voltage: 0.30V, I_Q: 30µA, I_{SD}: <1µA, Low Noise <20$\mu V_{RMS\ P-P}$, S8 Package
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.7V to 20V, V_{OUT}: 1.21V, Dropout Voltage: 0.34V, I_Q: 1mA, I_{SD}: <1µA,Low Noise <40$\mu V_{RMS\ P-P}$, "A" Version Stable with Ceramic Capacitors, DD, TO220-5 Packages
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, V_{OUT}: 1.22V, Dropout Voltage: 0.27V, I_Q: 30µA, I_{SD}: <1µA, Low Noise <20$\mu V_{RMS\ P-P}$, MS8 Package
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.1V to 20V, V_{OUT}: 1.21V, Dropout Voltage: 0.34V, I_Q: 1mA, I_{SD}: <1µA, Low Noise <40$\mu V_{RMS\ P-P}$, "A" Version Stable with Ceramic Capacitors, DD, T0220-5, SOT-223, S8 Packages
LTC3411	1.25A(I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, I_{OUT}: 1.25A, V_{REF}: 0.8V, I_{SD}: <1µA, MS and DFN Packages
LTC3412	2.5A(I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, I_{OUT}: 2.5A, V_{REF}: 0.8V, I_{SD}: <1µA, TSSOP16E Package

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