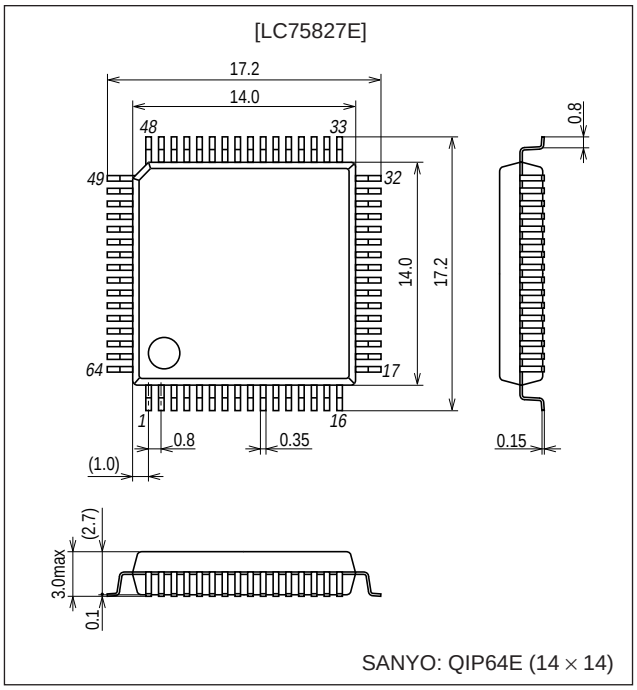
Package Dimensions

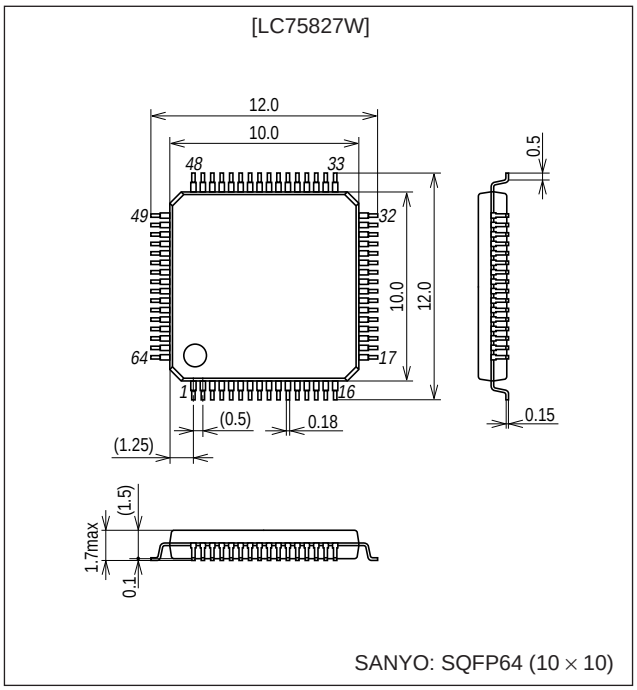
unit: mm

3159A-QIP64E



unit: mm

3190A-SQFP64

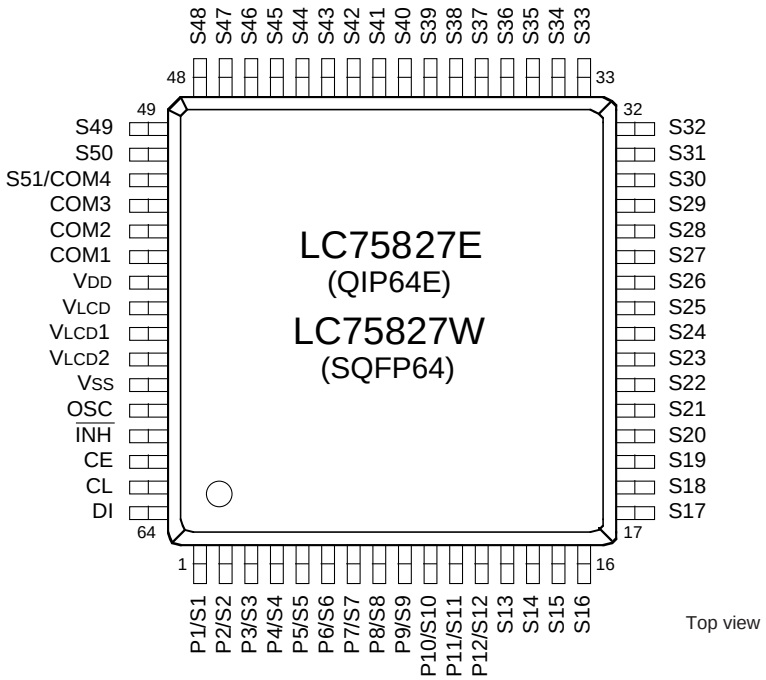


Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +7.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	–0.3 to +7.0	V
	$V_{IN}2$	OSC	–0.3 to V_{DD} + 0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$	–0.3 to V_{LCD} + 0.3	
Output voltage	$V_{OUT}1$	OSC	–0.3 to V_{DD} + 0.3	V
	$V_{OUT}2$	S1 to S51, COM1 to COM4, P1 to P12	–0.3 to V_{LCD} + 0.3	
Output current	$I_{OUT}1$	S1 to S51	300	µA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P12	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Pin Assignment



Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}	2.7		6.0	
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3 V_{LCD}	V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$		1/3 V_{LCD}	V_{LCD}	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
	$V_{IH}2$	OSC: external clock mode	0.7 V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2 V_{DD}	V
	$V_{IL}2$	OSC: external clock mode	0		0.3 V_{DD}	
Recommended external resistance	R_{OSC}	OSC: RC oscillation mode		39		kΩ
Recommended external capacitance	C_{OSC}	OSC: RC oscillation mode		1000		pF
Guaranteed oscillation range	f_{OSC}	OSC: RC oscillation mode	19	38	76	kHz
External clock frequency	f_{CK}	OSC: external clock mode Figure 4	19	38	76	kHz
External clock duty	D_{CK}	OSC: external clock mode Figure 4	30	50	70	%
Data setup time	t_{ds}	CL, DI: Figure 2, 3	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2, 3	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2, 3	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2, 3	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2, 3	160			ns
High level clock pulse width	$t_{øH}$	CL: Figure 2, 3	160			ns
Low level clock pulse width	$t_{øL}$	CL: Figure 2, 3	160			ns
Rise time	t_r	CE, CL, DI: Figure 2, 3		160		ns
Fall time	t_f	CE, CL, DI: Figure 2, 3		160		ns
$\overline{INH}$ switching time	t_c	$\overline{INH}$, CE: Figure 5, 6	10			µs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$		0.1 V_{DD}		V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$: V_I = 6.0 V			5.0	µA
	$I_{IH}2$	OSC: $V_I = V_{DD}$, external clock mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$: V_I = 0 V	–5.0			µA
	$I_{IL}2$	OSC: V_I = 0 V, external clock mode	–5.0			
Output high level voltage	$V_{OH}1$	S1 to S51: I_O = –20 µA	V_{LCD} – 0.9			V
	$V_{OH}2$	COM1 to COM4: I_O = –100 µA	V_{LCD} – 0.9			
	$V_{OH}3$	P1 to P12: I_O = –1 mA	V_{LCD} – 0.9			
Output low level voltage	$V_{OL}1$	S1 to S51: I_O = 20 µA			0.9	V
	$V_{OL}2$	COM1 to COM4: I_O = 100 µA			0.9	
	$V_{OL}3$	P1 to P12: I_O = 1 mA			0.9	
Output middle level voltage*1	$V_{MID}1$	COM1 to COM4: 1/2 bias, I_O = ±100 µA	1/2 V_{LCD} – 0.9		1/2 V_{LCD} + 0.9	V
	$V_{MID}2$	S1 to S51: 1/3 bias, I_O = ±20 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	
	$V_{MID}3$	S1 to S51: 1/3 bias, I_O = ±20 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	
	$V_{MID}4$	COM1 to COM4: 1/3 bias, I_O = ±100 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	
	$V_{MID}5$	COM1 to COM4: 1/3 bias, I_O = ±100 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	
Oscillator frequency	f_{OSC}	OSC: R_{OSC} = 39 kΩ, C_{OSC} = 1000 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD}: Power-saving mode			5	µA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, outputs open, f_{OSC} = 38 kHz		250	500	
	$I_{LCD}1$	V_{LCD}: Power-saving mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 6.0 V, outputs open, 1/2 bias, f_{OSC} = 38 kHz		100	200	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 6.0 V, outputs open, 1/3 bias, f_{OSC} = 38 kHz		60	120	

Note: *1 Excluding the bias voltage generation divider resistors built in the $V_{LCD}1$ and $V_{LCD}2$. (See Figure 1.)

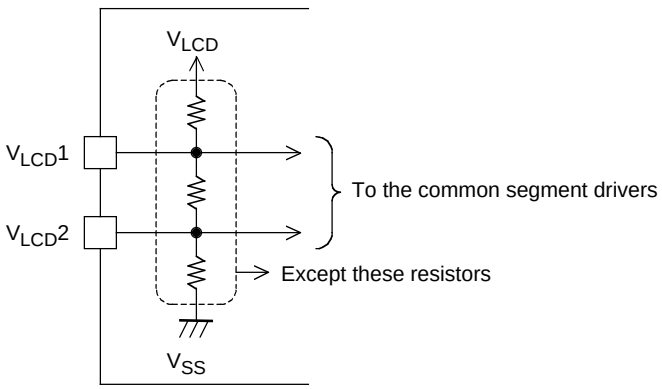


Figure 1

1. When CL is stopped at the low level

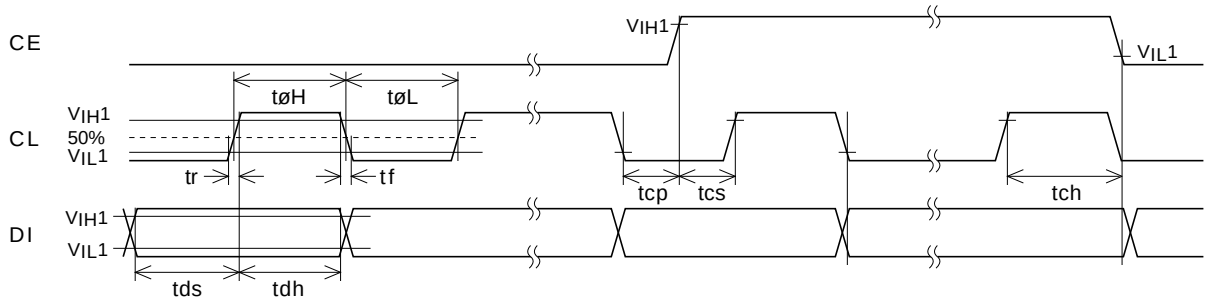


Figure 2

2. When CL is stopped at the high level

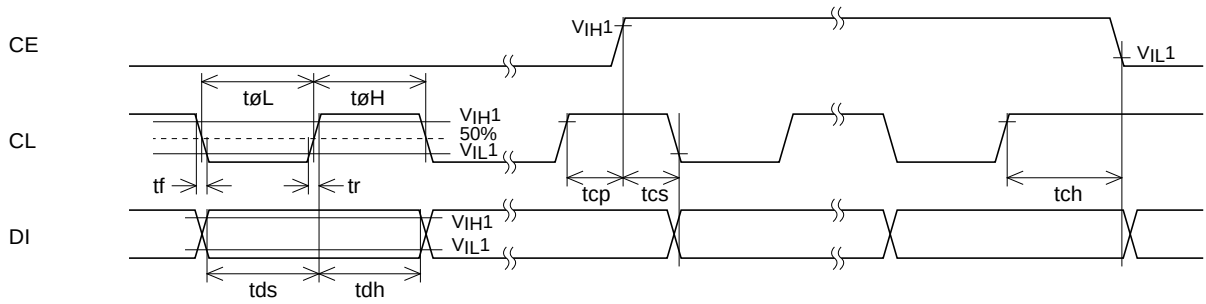
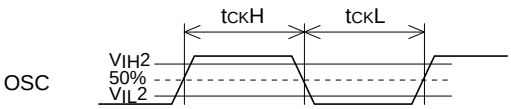


Figure 3

3. OSC Pin Clock Timing in External Clock Mode

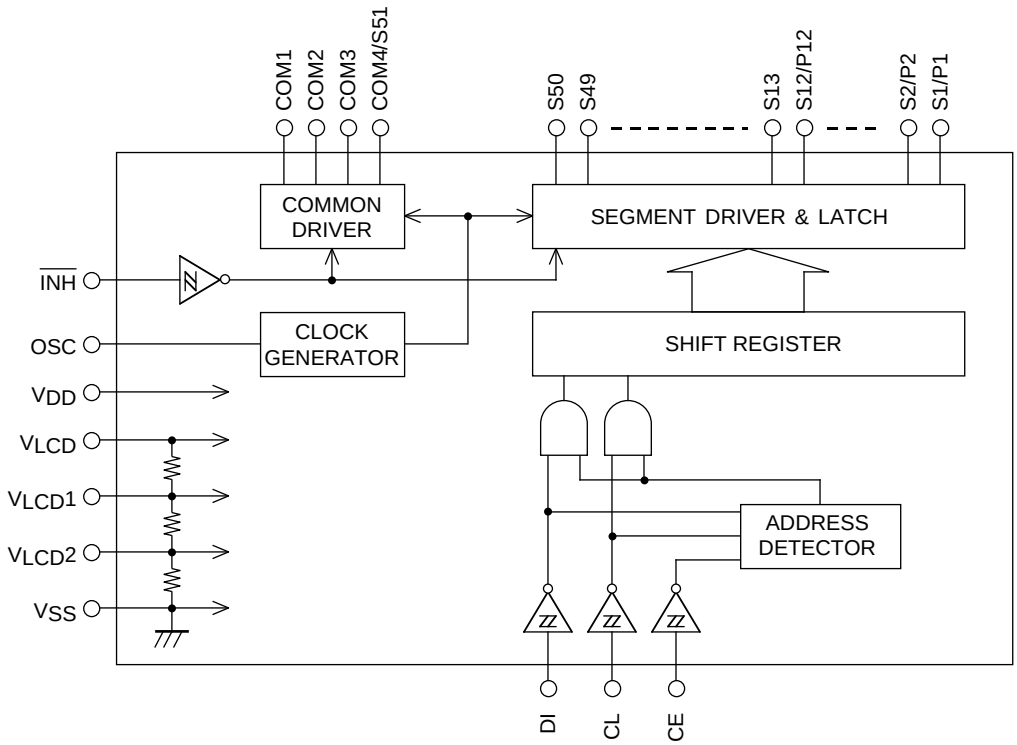


$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [Hz]}$$

$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

Figure 4

Block Diagram



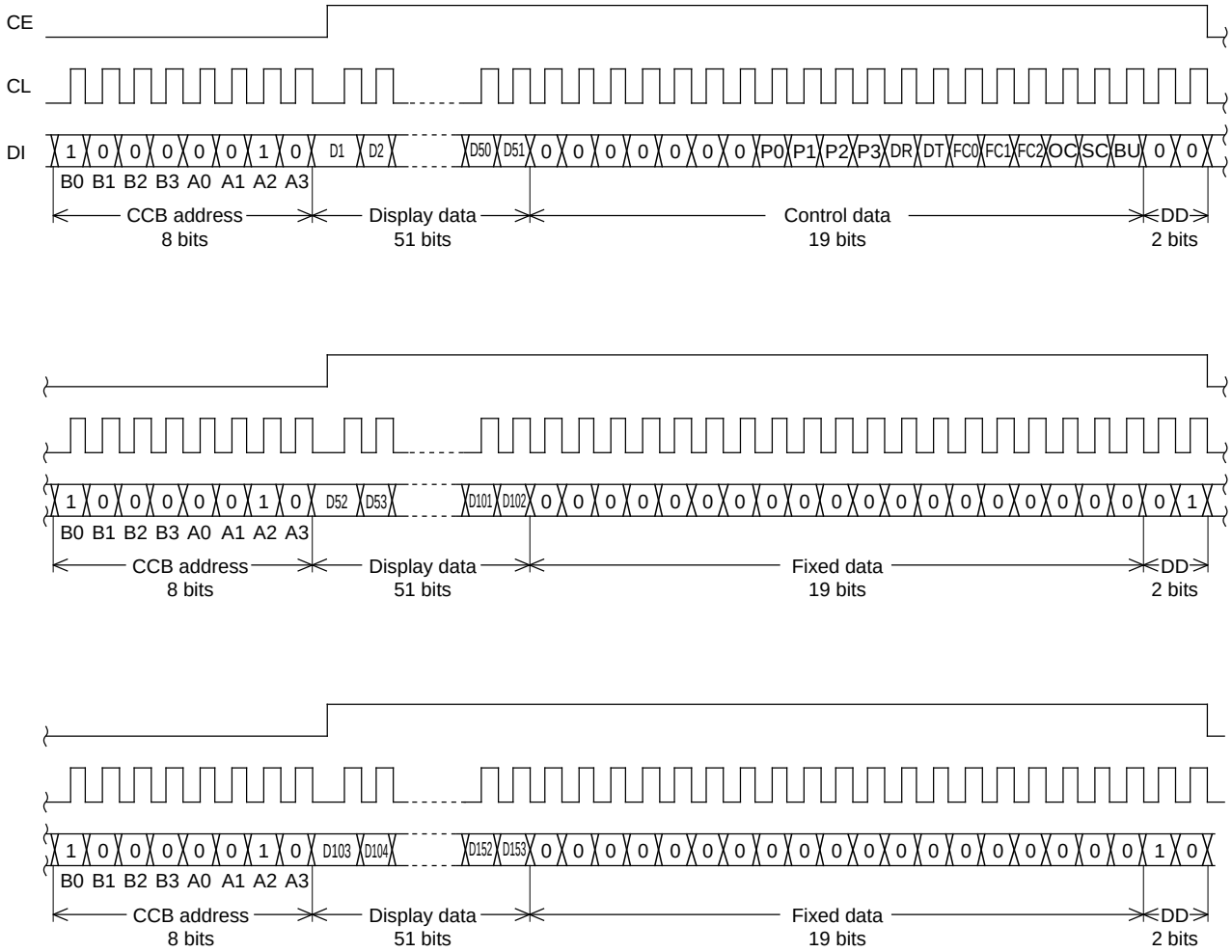
Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S12/P12 S13 to S50	1 to 12 13 to 50	Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S12/P12 can be used as general-purpose output ports when so set up by the control data.	—	O	Open
COM1 to COM3 COM4/S51	54 to 52 51	Common driver outputs. The frame frequency is f_O Hz. The COM4/S51 can be used for segment output in 1/3 duty.	—	O	Open
OSC	60	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can be used as the external clock input pin if external clock mode is selected with the control data.	—	I/O	V_{DD}
CE CL DI	62 63 64	Serial data transfer inputs. These pins are connected to the control microprocessor. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ —	I I I	GND
$\overline{INH}$	61	Display off control input • $\overline{INH}$ = low (V_{SS}).....Off S1/P1 to S12/P12 = low (V_{SS}) (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S13 to S50 = low (V_{SS}) COM1 to COM3 = low (V_{SS}) COM4/S51 = low (V_{SS}) OSC = Z (High impedance) • $\overline{INH}$ = high (V_{DD}).....On Note that serial data transfers can be performed when the display is forced off by this pin.	L	I	GND
$V_{LCD}1$	57	Used to apply the LCD drive 2/3 bias voltage externally. This pin must be connected to $V_{LCD}2$ when 1/2 bias drive is used.	—	I	Open
$V_{LCD}2$	58	Used to apply the LCD drive 1/3 bias voltage externally. This pin must be connected to $V_{LCD}1$ when 1/2 bias drive is used.	—	I	Open
V_{DD}	55	Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{LCD}	56	LCD driver block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{SS}	59	Ground pin. Connect to ground.	—	—	—

Serial Data Transfer Format

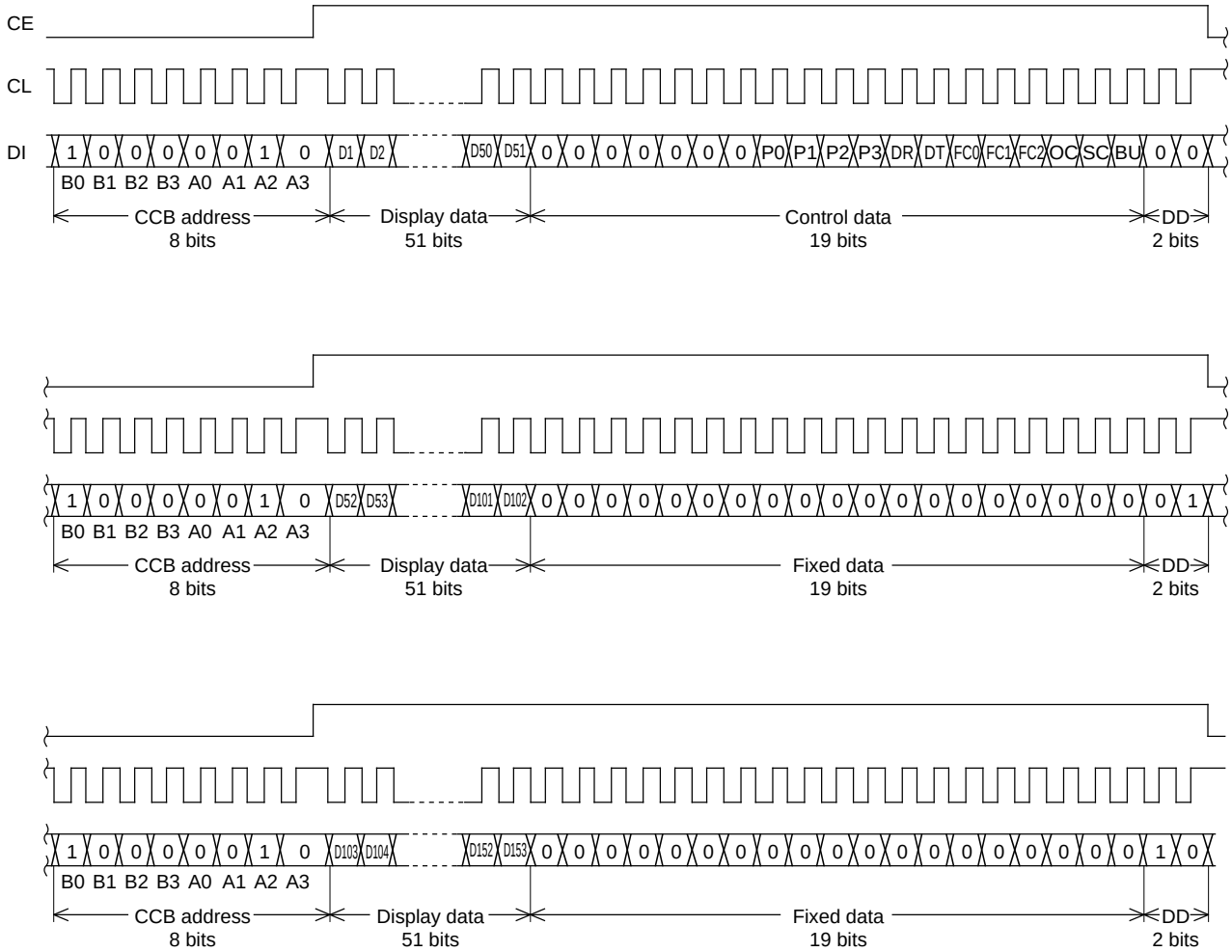
1. 1/3 duty

① When CL is stopped at the low level



Note: DD··Direction data.

② When CL is stopped at the high level

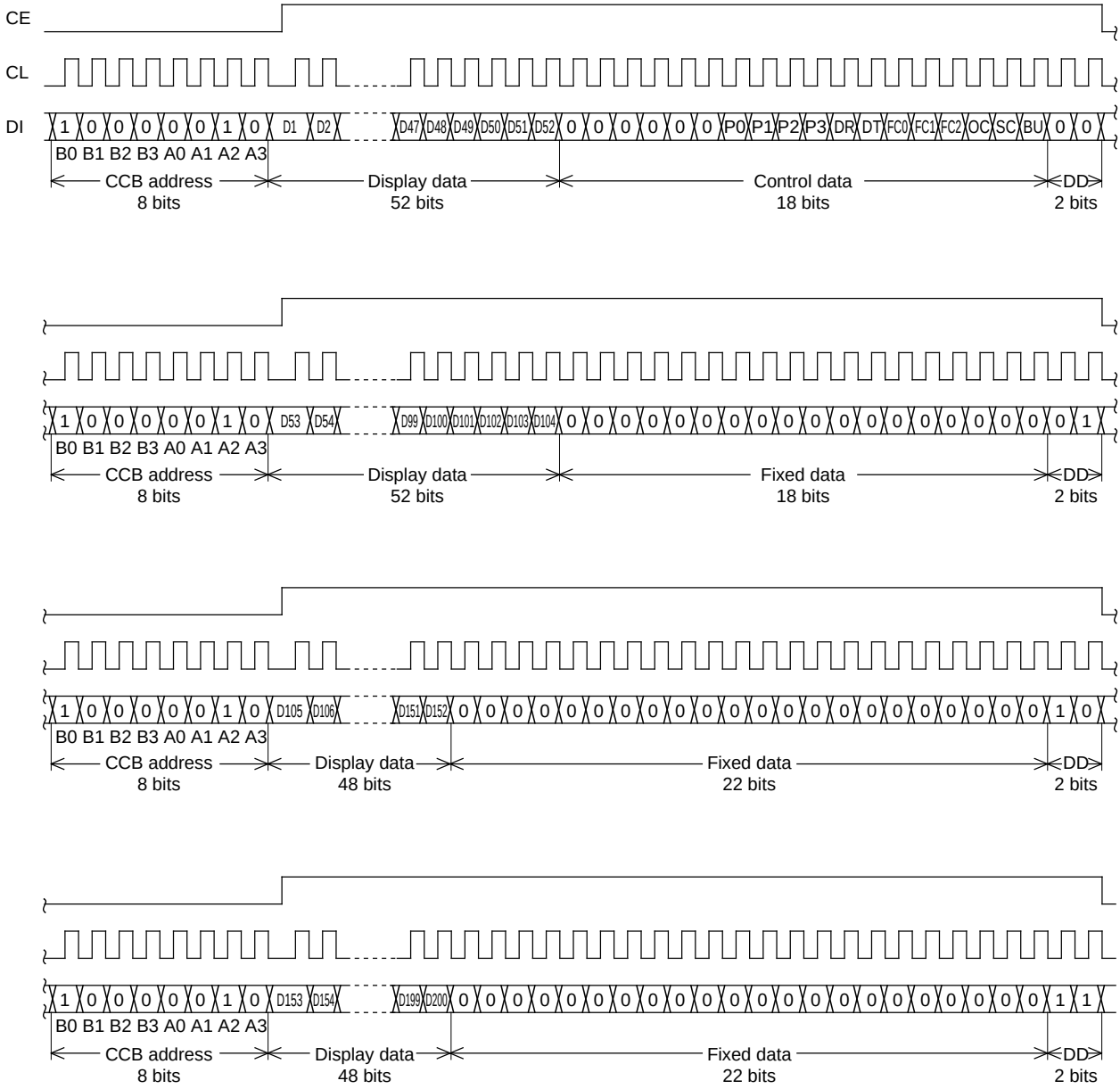


Note: DD···Direction data.

- CCB address.....41H
- D1 to D153.....Display data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- DR.....1/2 bias drive or 1/3 bias drive switching control data
- DT.....1/3 duty drive or 1/4 duty drive switching control data
- FC0 to FC2.....Common and segment output waveforms frame frequency setting control data
- OC.....Switches between RC oscillation mode and external clock mode
- SC.....Segments on/off control data
- BU.....Normal mode/power-saving mode control data

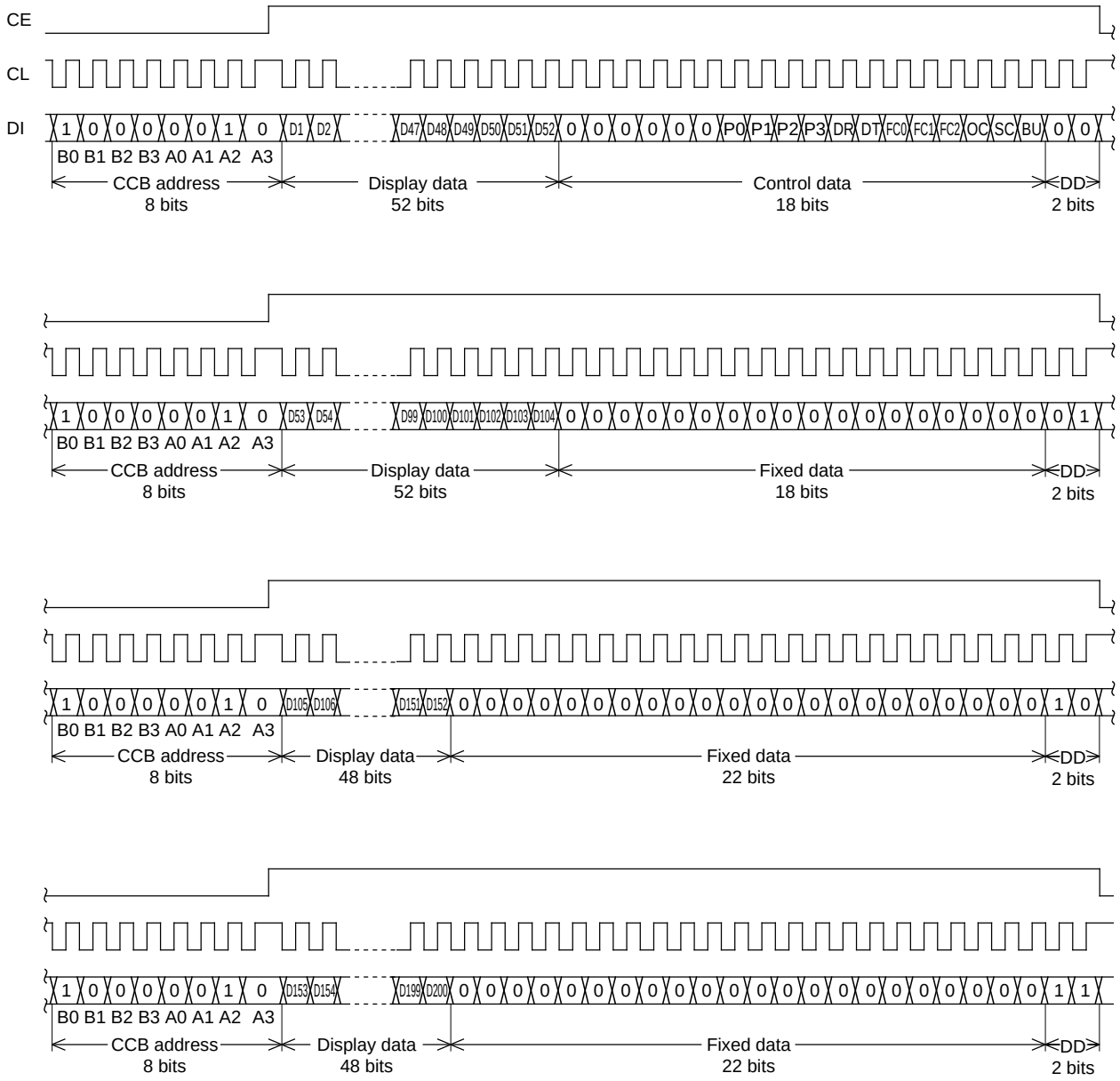
2. 1/4 duty

① When CL is stopped at the low level



Note: DD··Direction data.

② When CL is stopped at the high level



Note: DD··Direction data.

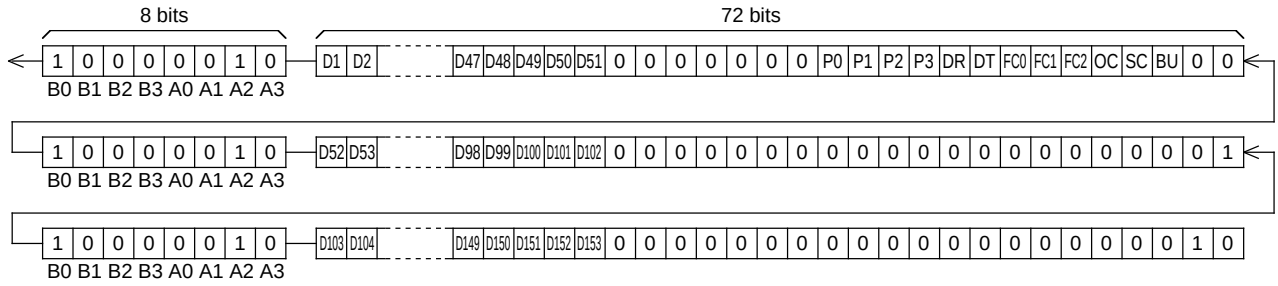
- CCB address.....41H
- D1 to D200.....Display data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- DR.....1/2 bias drive or 1/3 bias drive switching control data
- DT.....1/3 duty drive or 1/4 duty drive switching control data
- FC0 to FC2.....Common and segment output waveforms frame frequency setting control data
- OC.....Switches between RC oscillation mode and external clock mode
- SC.....Segments on/off control data
- BU.....Normal mode/power-saving mode control data

Serial Data Transfer Example

1. 1/3 duty

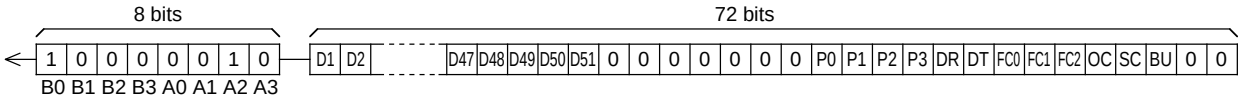
① When 103 or more segments are used

All 216 bits of serial data must be sent.



② When fewer than 103 segments are used

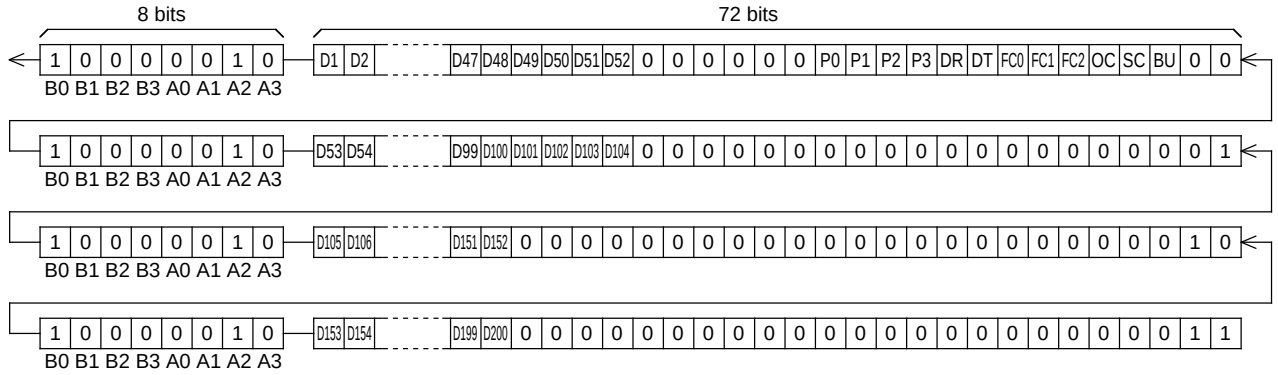
Either 72 or 144 bits of serial data may be sent, depending on the number of segments used. However, the serial data shown below (the D1 to D51 display data and the control data) must be sent.



2. 1/4 duty

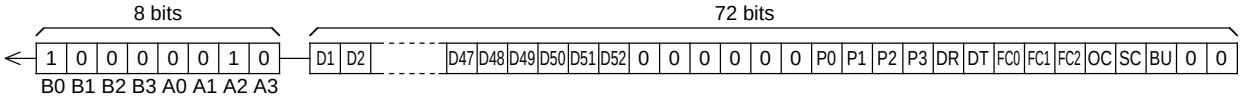
① When 153 or more segments are used

All 288 bits of serial data must be sent.



② When fewer than 153 segments are used

Either 72, 144, or 216 bits of serial data may be sent, depending on the number of segments used. However, the serial data shown below (the D1 to D52 display data and the control data) must be sent.



Control Data Functions

1. P0 to P3: Segment output port/general-purpose output port switching control data
   These control data bits switch the S1/P1 to S12/P12 output pins between their segment output port and general-purpose output port functions.

Control data				Output pin state											
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	S9/P9	S10/P10	S11/P11	S12/P12
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	S9	S10	S11	S12
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	S9	S10	S11	S12
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	S9	S10	S11	S12
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	S9	S10	S11	S12
1	0	0	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	S10	S11	S12
1	0	1	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	S11	S12
1	0	1	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	S12
1	1	0	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Note: Sn (n = 1 to 12): Segment output ports
Pn (n = 1 to 12): General-purpose output ports

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

Output pin	Corresponding display data	
	1/3 duty	1/4 duty
S1/P1	D1	D1
S2/P2	D4	D5
S3/P3	D7	D9
S4/P4	D10	D13
S5/P5	D13	D17
S6/P6	D16	D21
S7/P7	D19	D25
S8/P8	D22	D29
S9/P9	D25	D33
S10/P10	D28	D37
S11/P11	D31	D41
S12/P12	D34	D45

For example, when 1/4 duty drive scheme is used, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level (V_{LCD}) when the display data D13 is 1, and a low level (V_{SS}) when D13 is 0.

2. DR: 1/2 bias drive or 1/3 bias drive switching control data
   This control data bit selects either 1/2 bias drive or 1/3 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

3. DT: 1/3 duty drive or 1/4 duty drive switching control data
   This control data bit selects either 1/3 duty drive or 1/4 duty drive.

DT	Duty drive scheme	Output pin (COM4/S51) state
0	1/4 duty drive	COM4
1	1/3 duty drive	S51

Note: COM4: Common output
S51: Segment output

4. FC0 to FC2: Common and segment output waveforms frame frequency setting control data
   These control data bits set the frame frequency for common and segment output waveforms.

Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/768, f_{CK}/768
0	0	1	fosc/576, f_{CK}/576
0	1	0	fosc/384, f_{CK}/384
0	1	1	fosc/288, f_{CK}/288
1	0	0	fosc/192, f_{CK}/192

5. OC: Switches between RC oscillation mode and external clock mode.
   This control data bit selects the OSC pin function (RC oscillation mode or external clock mode).

OC	OSC pin function
0	RC oscillation mode
1	External clock mode

Note: An external resistor, Rosc, and an external capacitor, Cosc, must be connected to the OSC pin if RC oscillation mode is selected.

6. SC: Segments on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

7. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power-saving mode [In RC oscillation mode (OC = 0), the OSC pin oscillator is stopped, and in external clock mode (OC = 1), acceptance of the external clock signal is stopped. In this mode the common and segment output pins go to the V_{SS} levels. However, the S1/P1 to S12/P12 output pins that are set to be general-purpose output ports by the control data P0 to P3 can be used as general-purpose output ports.]

Display Data to Segment Output Pin Correspondence

1. 1/3 duty

Segment output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5/P5	D13	D14	D15
S6/P6	D16	D17	D18
S7/P7	D19	D20	D21
S8/P8	D22	D23	D24
S9/P9	D25	D26	D27
S10/P10	D28	D29	D30
S11/P11	D31	D32	D33
S12/P12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78

Segment output pin	COM1	COM2	COM3
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
COM4/S51	D151	D152	D153

Note: This applies to the case where the S1/P1 to S12/P12, and COM4/S51 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S21 output pin.

Display data			Segment output pin (S21) state
D61	D62	D63	
0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

2. 1/4 duty

Segment output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9/P9	D33	D34	D35	D36
S10/P10	D37	D38	D39	D40
S11/P11	D41	D42	D43	D44
S12/P12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100

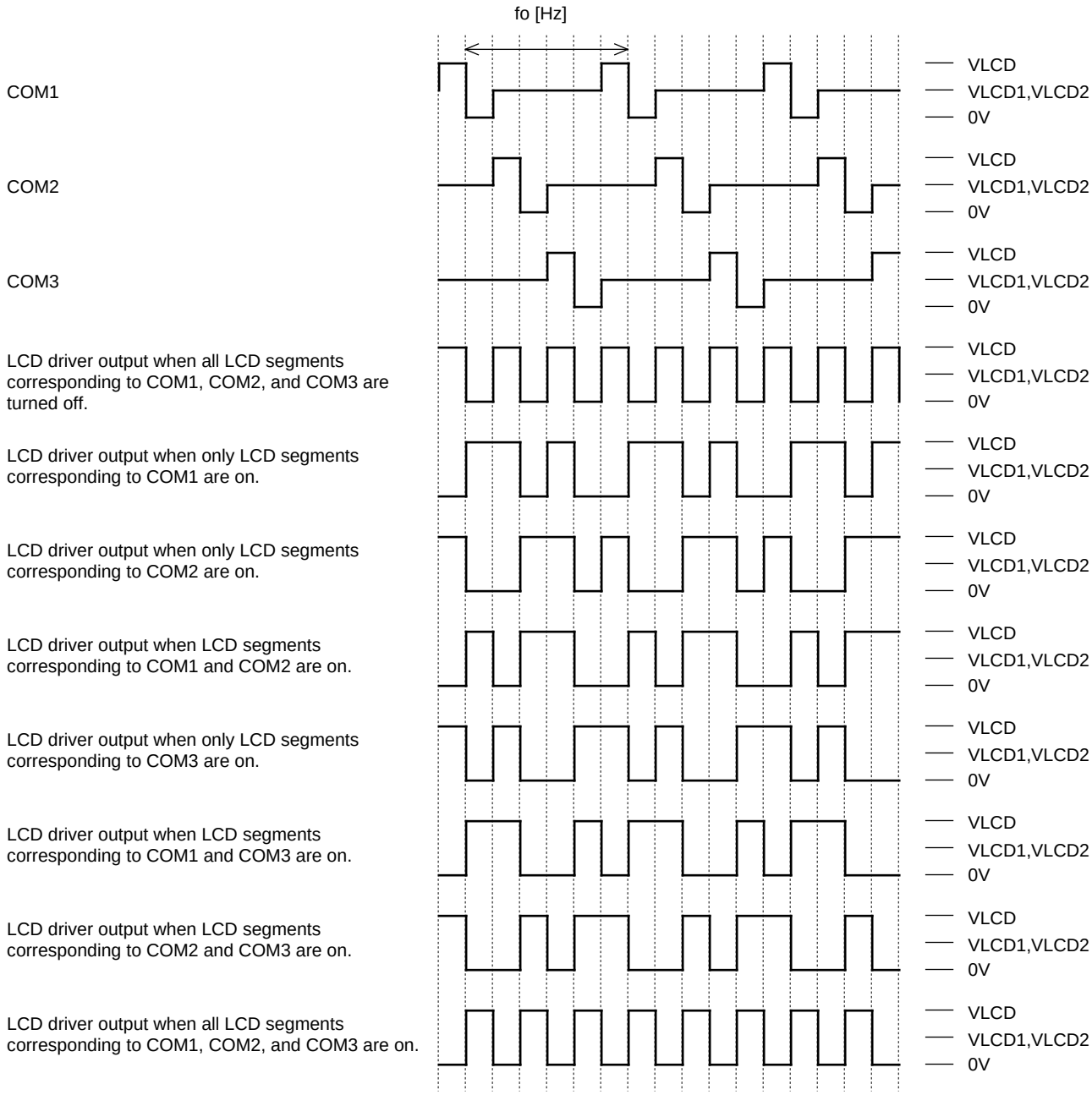
Segment output pin	COM1	COM2	COM3	COM4
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200

Note: This applies to the case where the S1/P1 to S12/P12 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S21 output pin.

Display data				Segment output pin (S21) state
D81	D82	D83	D84	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

1/3 Duty, 1/2 Bias Drive Technique



When the control data FC0 = 0, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{768} = \frac{fCK}{768}$

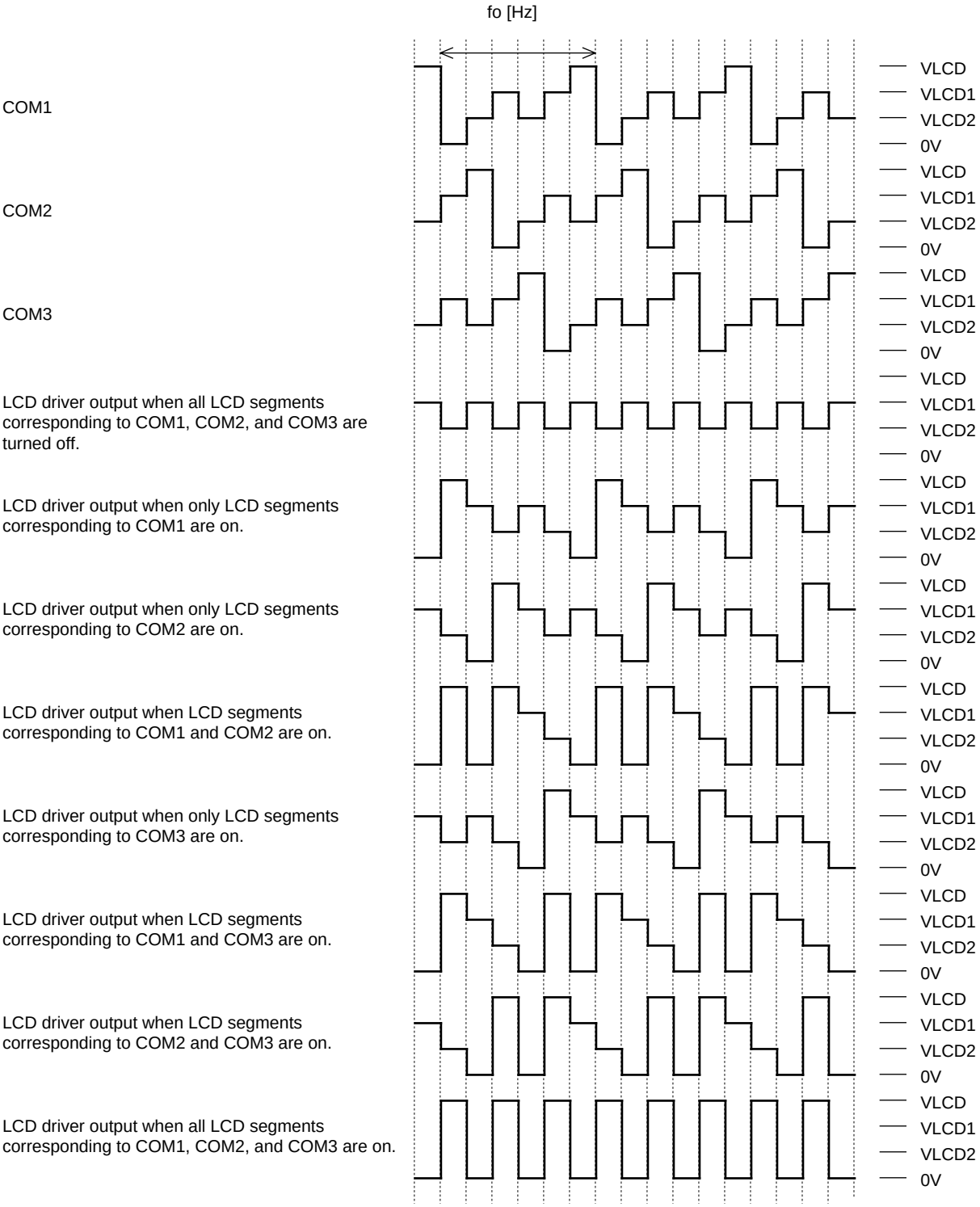
When the control data FC0 = 0, FC1 = 0, and FC2 = 1: $fo = \frac{fosc}{576} = \frac{fCK}{576}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 0: $fo = \frac{fosc}{384} = \frac{fCK}{384}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 1: $fo = \frac{fosc}{288} = \frac{fCK}{288}$

When the control data FC0 = 1, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{192} = \frac{fCK}{192}$

1/3 Duty, 1/3 Bias Drive Technique



When the control data FC0 = 0, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{768} = \frac{fCK}{768}$

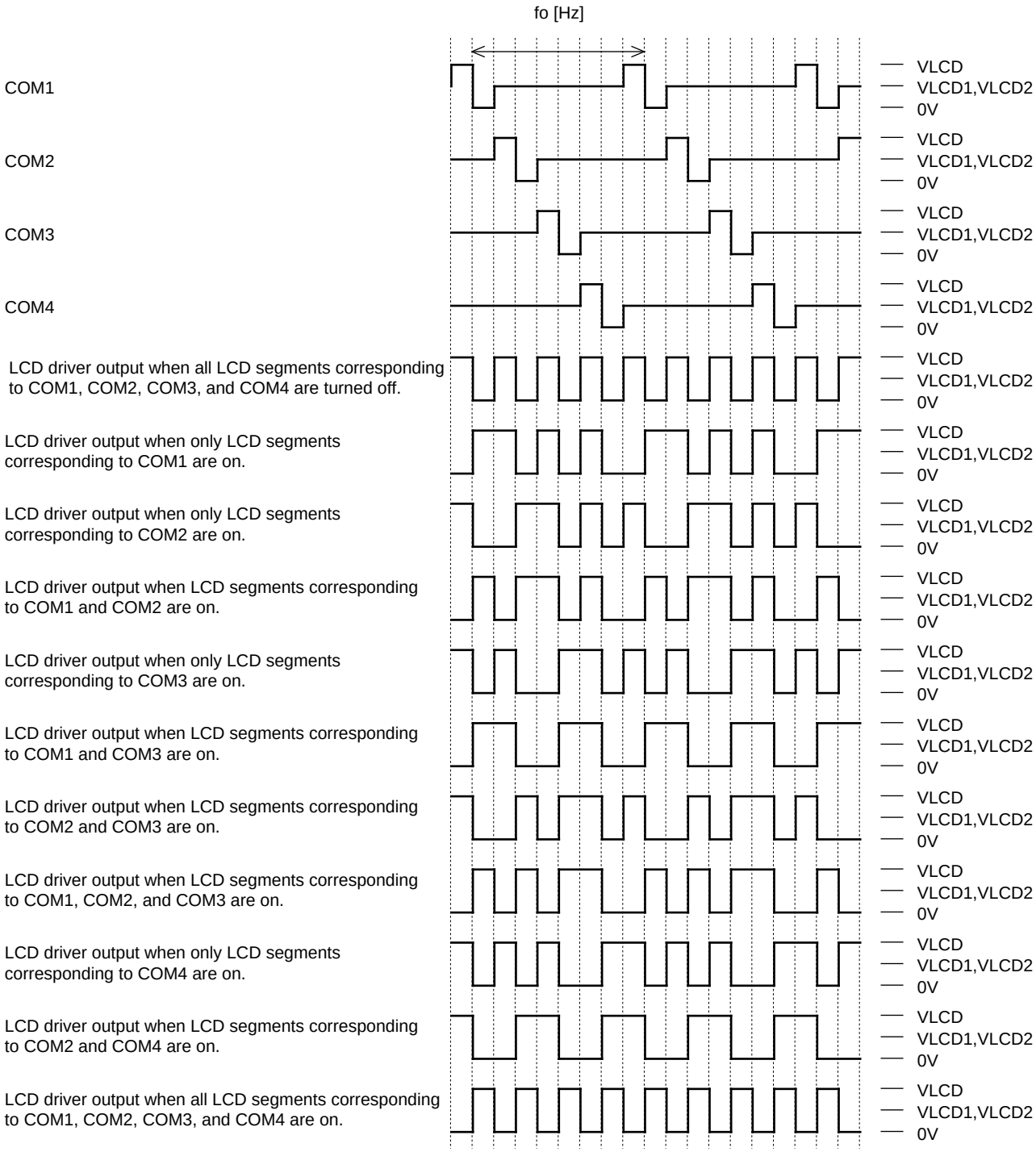
When the control data FC0 = 0, FC1 = 0, and FC2 = 1: $fo = \frac{fosc}{576} = \frac{fCK}{576}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 0: $fo = \frac{fosc}{384} = \frac{fCK}{384}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 1: $fo = \frac{fosc}{288} = \frac{fCK}{288}$

When the control data FC0 = 1, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{192} = \frac{fCK}{192}$

1/4 Duty, 1/2 Bias Drive Technique



When the control data FC0 = 0, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{768} = \frac{fCK}{768}$

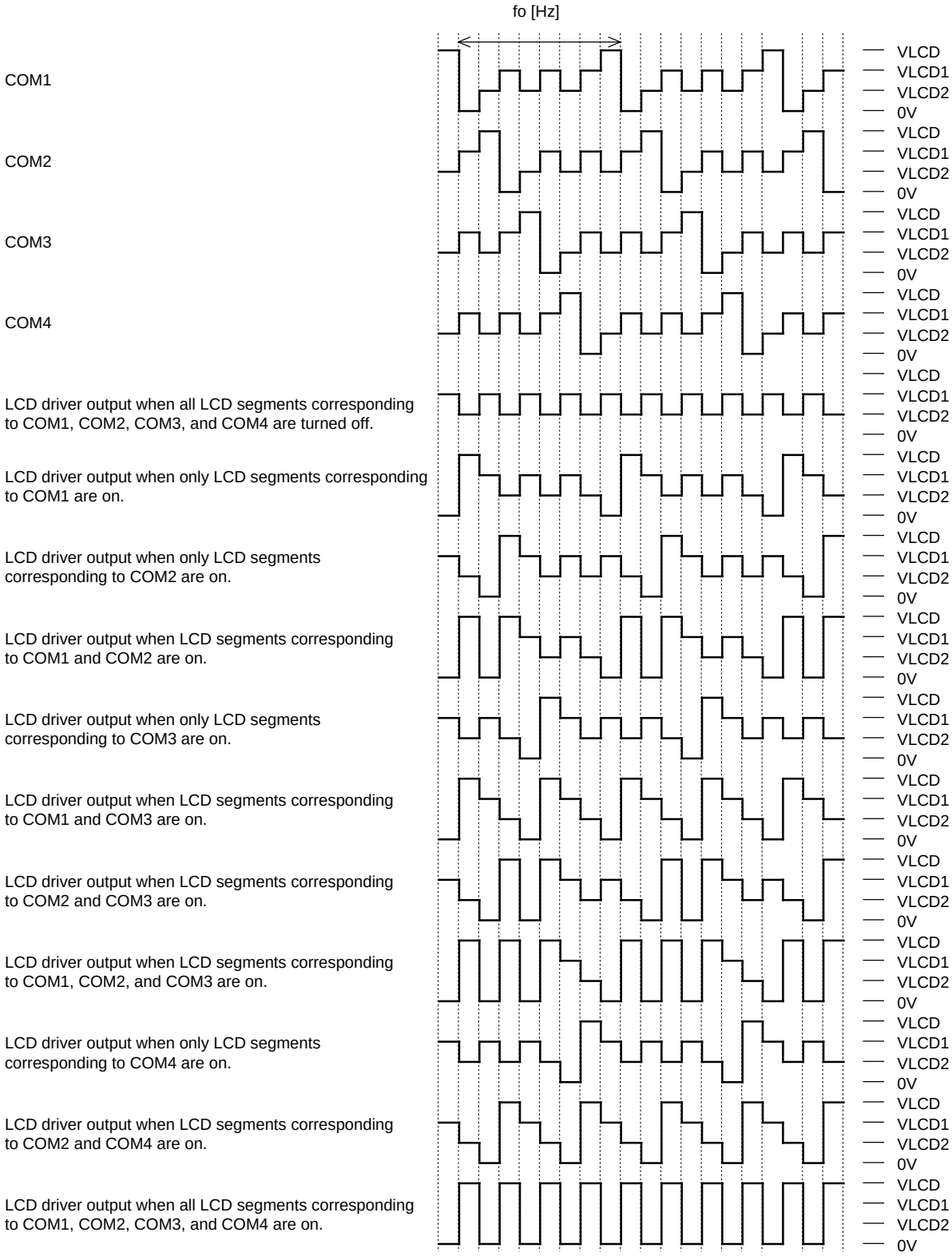
When the control data FC0 = 0, FC1 = 0, and FC2 = 1: $fo = \frac{fosc}{576} = \frac{fCK}{576}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 0: $fo = \frac{fosc}{384} = \frac{fCK}{384}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 1: $fo = \frac{fosc}{288} = \frac{fCK}{288}$

When the control data FC0 = 1, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{192} = \frac{fCK}{192}$

1/4 Duty, 1/3 Bias Drive Technique



When the control data FC0 = 0, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{768} = \frac{fCK}{768}$

When the control data FC0 = 0, FC1 = 0, and FC2 = 1: $fo = \frac{fosc}{576} = \frac{fCK}{576}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 0: $fo = \frac{fosc}{384} = \frac{fCK}{384}$

When the control data FC0 = 0, FC1 = 1, and FC2 = 1: $fo = \frac{fosc}{288} = \frac{fCK}{288}$

When the control data FC0 = 1, FC1 = 0, and FC2 = 0: $fo = \frac{fosc}{192} = \frac{fCK}{192}$

The $\overline{INH}$ pin and Display Control

Since the IC internal data (1/3 duty: the display data D1 to D153 and the control data, 1/4 duty: the display data D1 to D200 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S12/P12, S13 to S50, COM1 to COM3, and COM4/S51 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figures 5and 6.)

Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75827E and LC75827W power on and off.

- At power on: Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

1. 1/3 duty

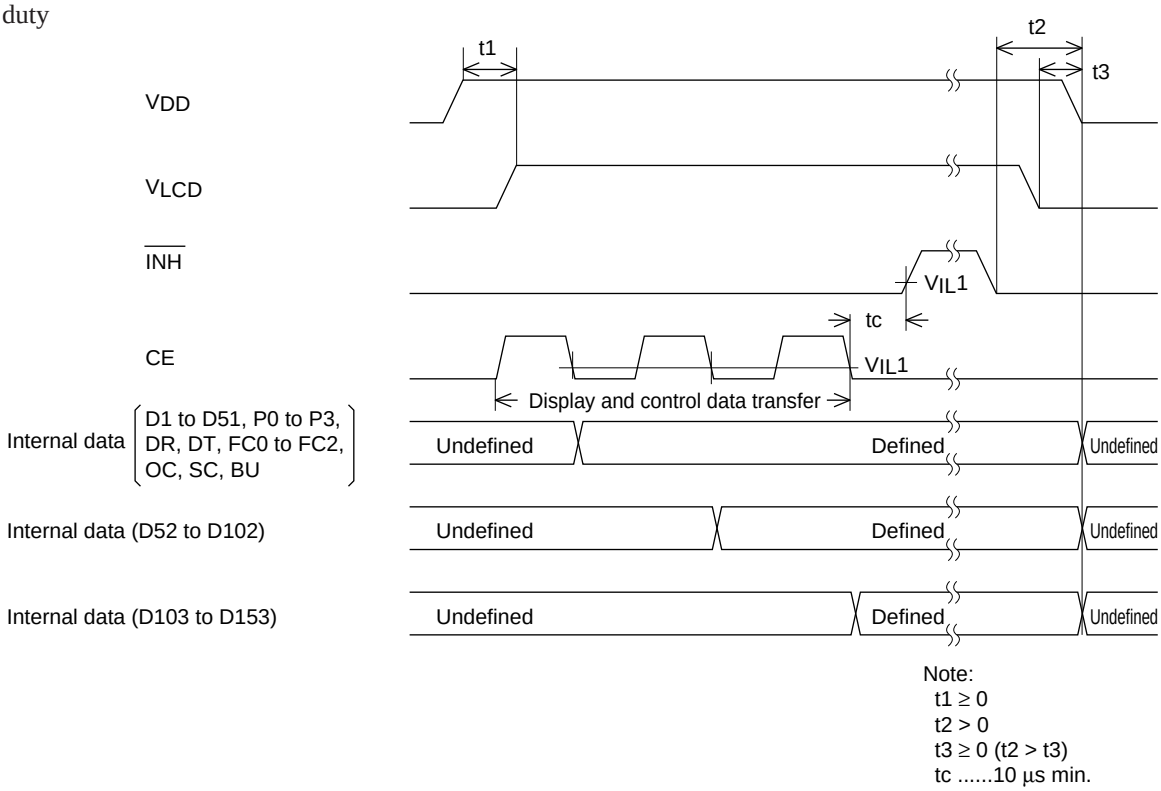


Figure 5

2. 1/4 duty

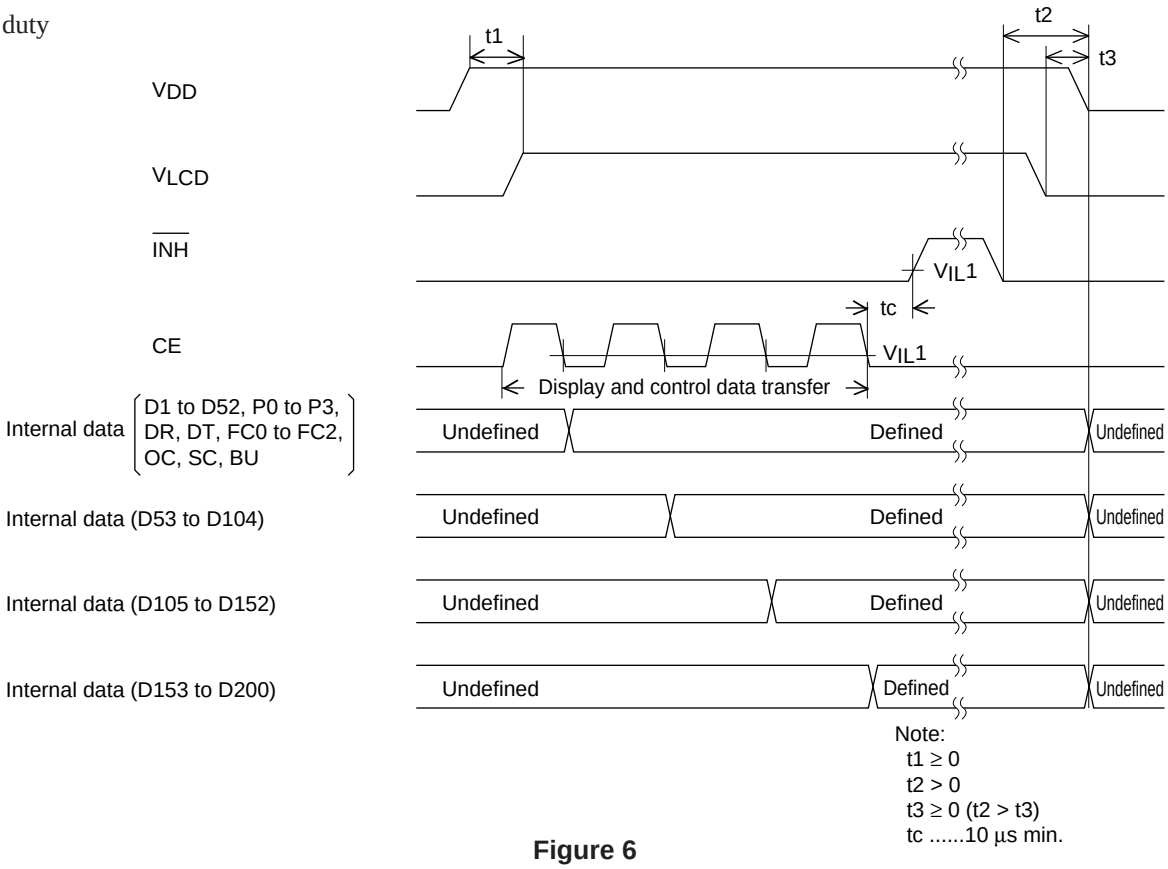


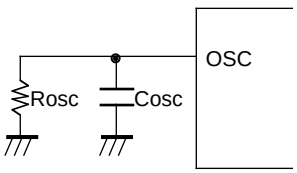
Figure 6

Notes on Controller Transfer of Display Data

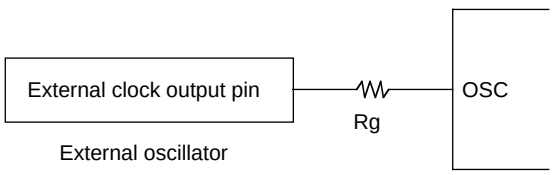
Since the LC75827E and LC75827W accept the display data (D1 to D153) divided into three separate transfer operations when using 1/3 duty drive scheme and the data (D1 to D200) divided into four separate transfer operations when 1/4 duty drive, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

OSC Pin Peripheral Circuit

1. RC oscillation mode (control data OC = 0)
   When RC oscillation mode is selected, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground.



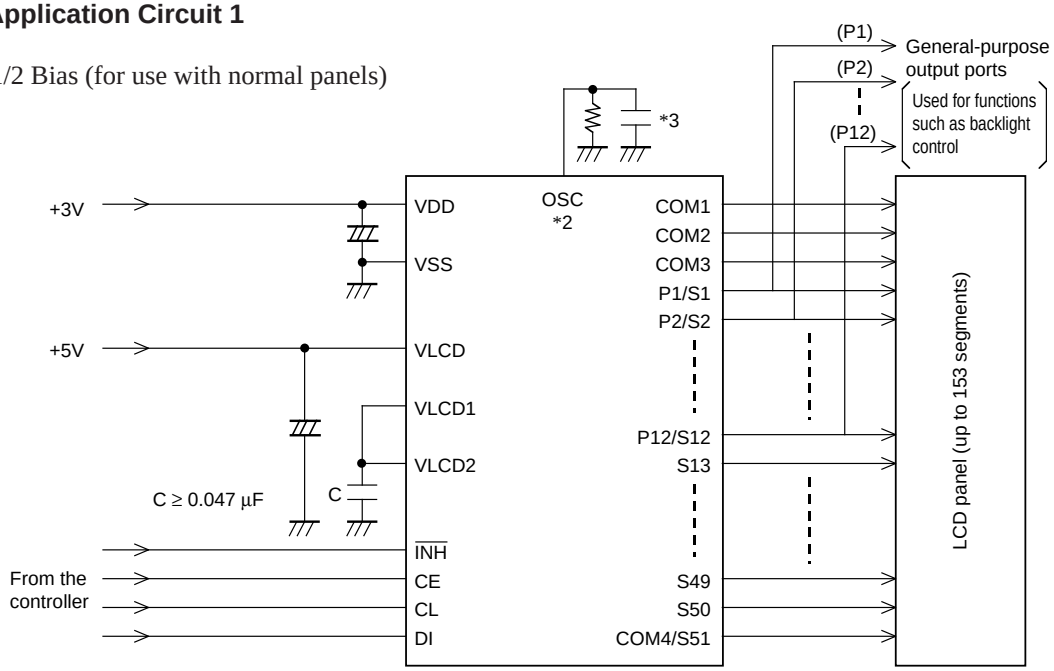
2. External clock mode (control data OC = 1)
   When external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. The value of this resistor is determined by the allowable current capacity of the external clock output pin. Note that the value must also be chosen so that the external clock waveform is not deformed significantly.



Note: The allowable current rating of the external clock output pin must be greater than VDD/Rg.

Sample Application Circuit 1

1/3 Duty, 1/2 Bias (for use with normal panels)

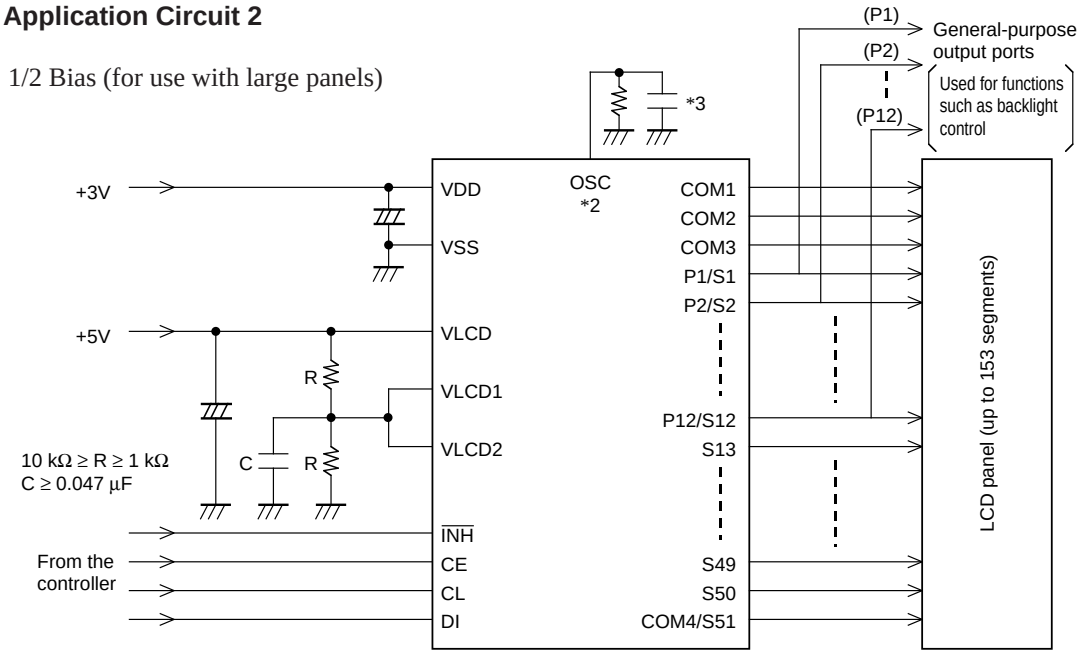


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 2

1/3 Duty, 1/2 Bias (for use with large panels)

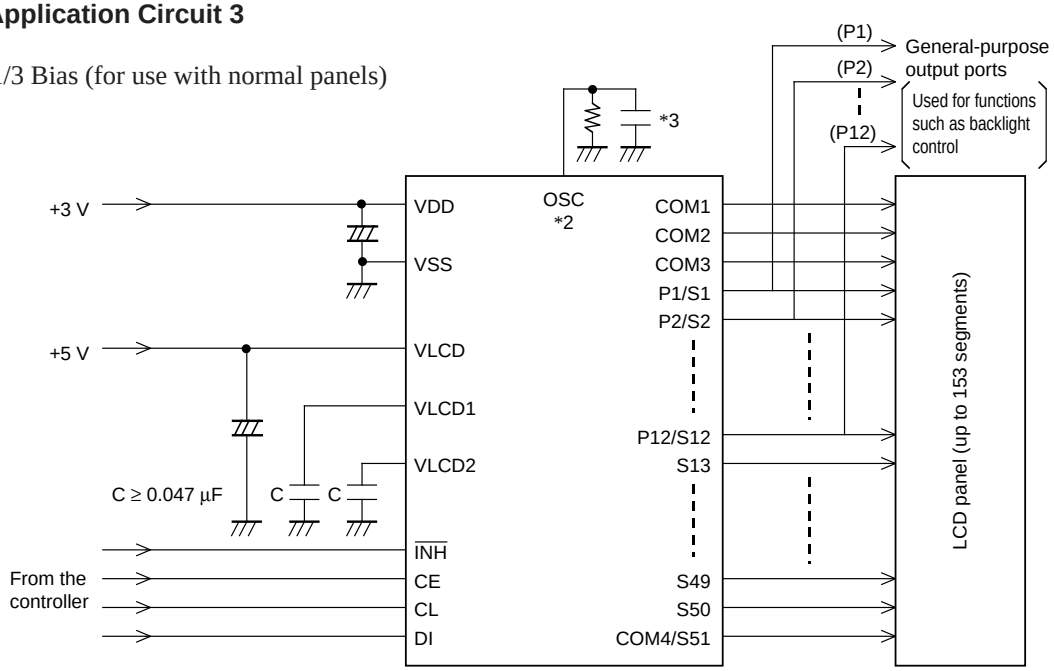


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 3

1/3 Duty, 1/3 Bias (for use with normal panels)

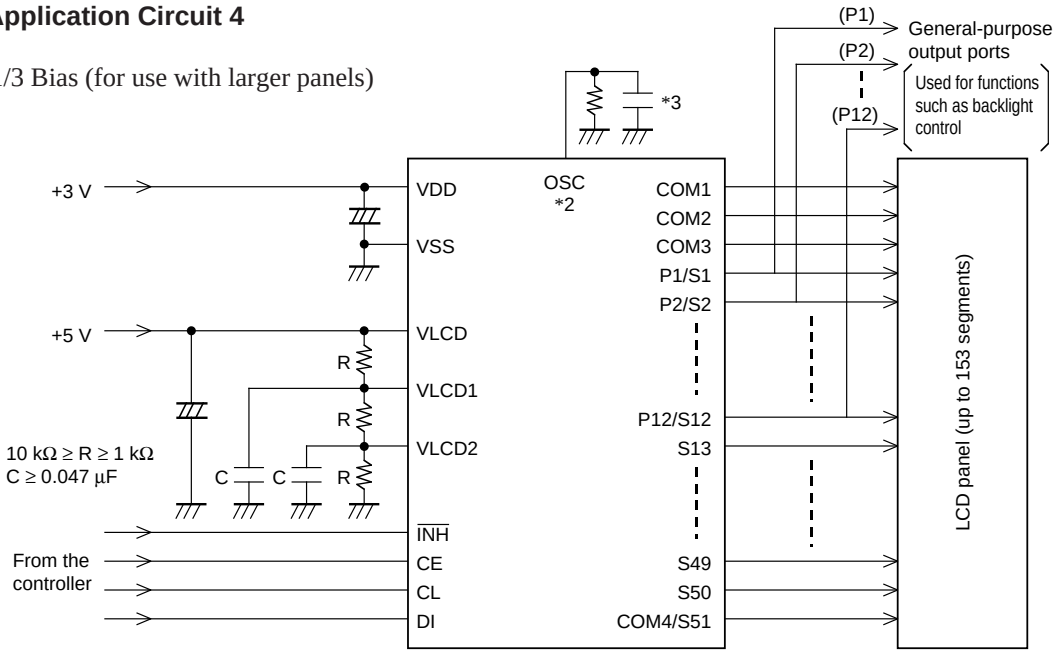


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 4

1/3 Duty, 1/3 Bias (for use with larger panels)

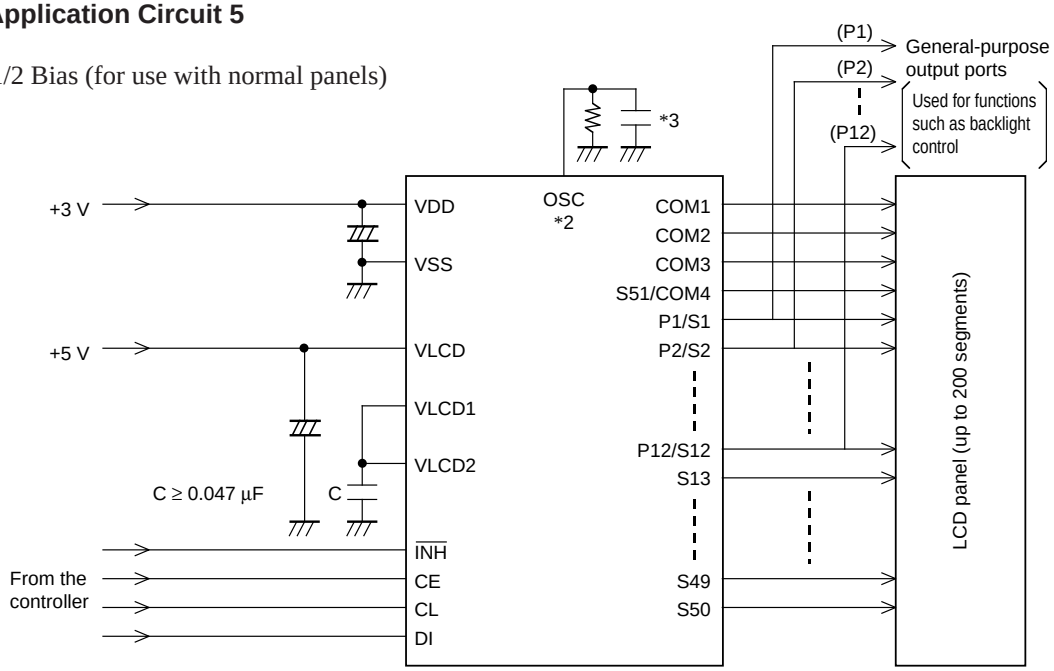


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 5

1/4 Duty, 1/2 Bias (for use with normal panels)

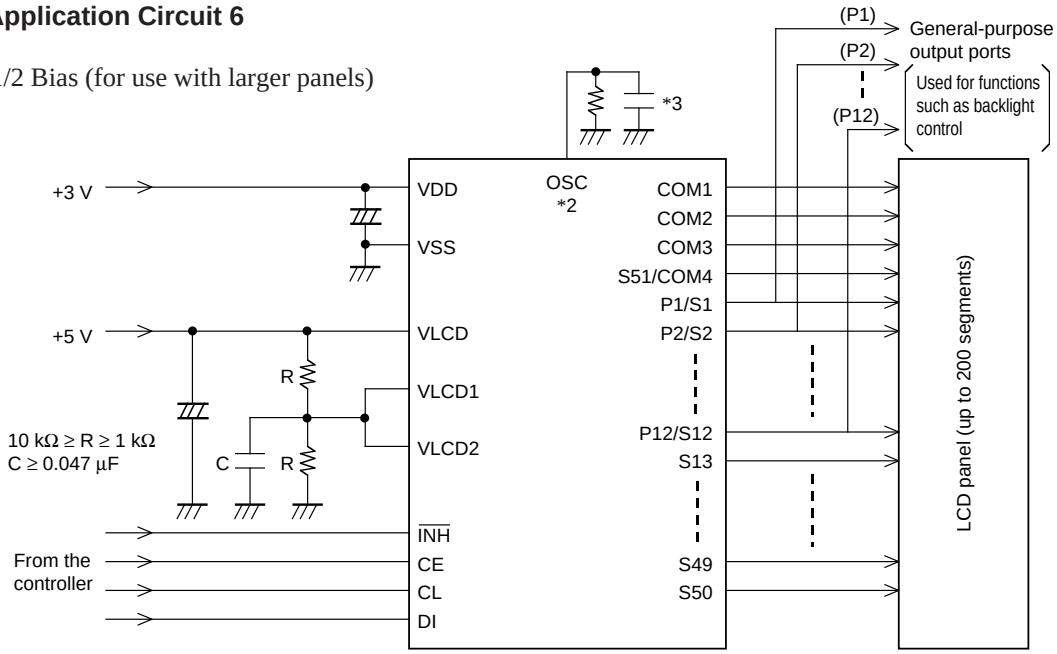


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 6

1/4 Duty, 1/2 Bias (for use with larger panels)

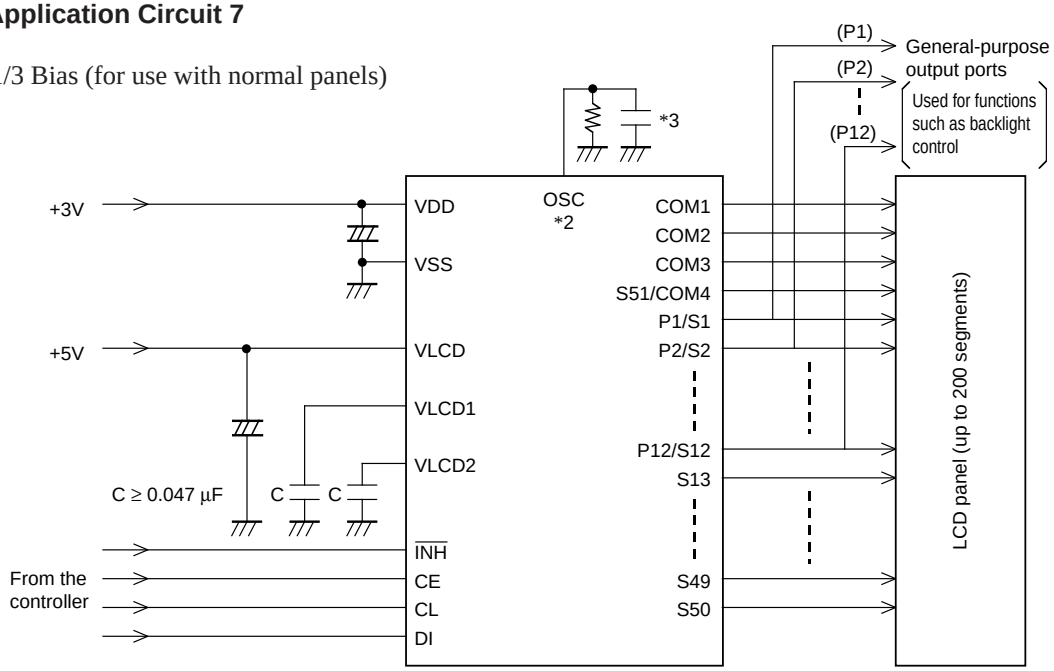


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 7

1/4 Duty, 1/3 Bias (for use with normal panels)

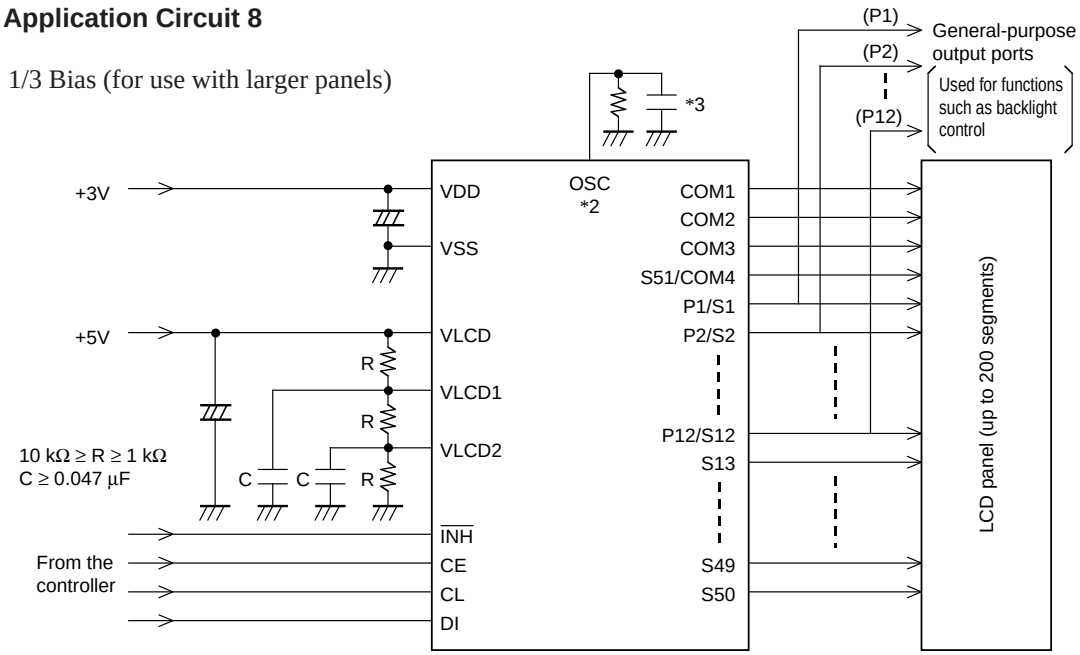


*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 8

1/4 Duty, 1/3 Bias (for use with larger panels)



*2 In RC oscillation mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. In external clock mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ) must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the “OSC Pin Peripheral Circuit” section.)

*3 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

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