

LA6245P

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		5 to 13	V

Electrical Characteristics at Ta = 25°C, V_{CC-S} = V_{CCP1} = V_{CCP2} = V_{CCREG} = 8V, V_{REF} = 2.5V, MUTE = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall]						
Quiescent current 1	I _{CC-ON}	All channel outputs on, MUTE pin: high		30	45	mA
Quiescent current 2	I _{CC-OFF}	All channel outputs off, MUTE pin: low		5	10	mA
Muting function on voltage	MUTE-ON		2.5			V
Muting function off voltage	MUTE-OFF				0.5	V
Switch on voltage	SW-ON		2.5			V
Switch off voltage	SW-OFF				0.5	V
REGSW on voltage	REG-ON		2.5			V
REGSW off voltage	REG-OFF				0.5	V
[BTL Amplifier] (Channel 1 to 4) (Output Amplifier Block)						
Input amplifier offset voltage	V _{OFF1}	*2	−50		50	mV
Output voltage	V _{O1}	R _L = 8Ω *1	5.7	6.2		V
I/O gain	V _{G1}	*2	5.4	6	6.6	Multiplier
Slew rate	SR1	With the amplifier operating independently, between outputs *3		2.0		V/μs
[Front End Operational Amplifier]						
OP-AMP_SINK 1	OP_SINK	Input operational amplifier sink current	2			mA
OP-AMP_SOURCE 1	OP_SOURCE	Input operational amplifier source current	300	500		μA
Input bias current	I _{BOP}				300	μA
Input voltage range	V _{IN}		0.5		5	V
High-level output voltage	V _{OHOP}		7.5	7.8		V
Low-level output voltage	V _{OLOP}			0.2	0.5	V
[VREF-IN Amplifier]						
Input voltage range	V _{REF-VIN}		1.3		4	V
[Independent Operational Amplifier]						
Output offset voltage	OP_VOFF		−6		6	mV
OP-AMP_SINK	OP_SINK	Input operational amplifier sink current	2			mA
OP-AMP_SOURCE	OP_SOURCE	Input operational amplifier source current	300	500		μA
Input bias current	IBOP				300	μA
Input voltage range	OP_VIN		0		V _{CC} −1.5	V
High-level output voltage	V _{OHOP}		7.5	7.8		V
Low-level output voltage	V _{OLOP}			0.2	0.5	V
[Power Supply Block] (uses an external pnp transistor: 2SB632K)						
Power supply output	V _{OUT}	I _O = 200mA	1.2	1.25	1.3	V
REG-IN sink current	REG-IN-SINK	The base current of the external PNP transistor	5.0	10		mA
Line regulation	ΔV _{OLN}	6V ≤ V _{CCREG} ≤ 12V, I _O = 200mA		10	50	mV
Load regulation	ΔV _{OLD}	5mA ≤ I _O ≤ 200mA		10	50	mV

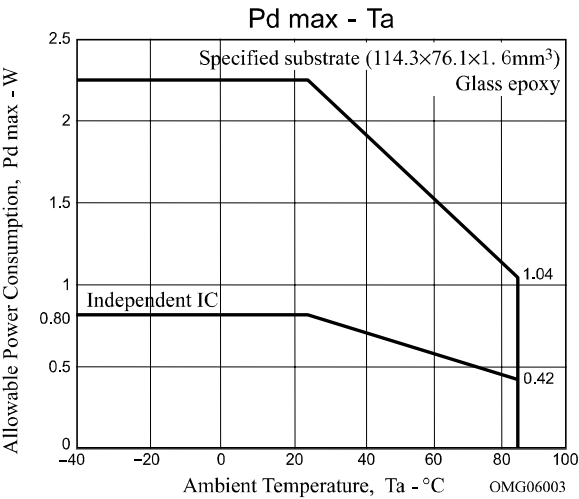
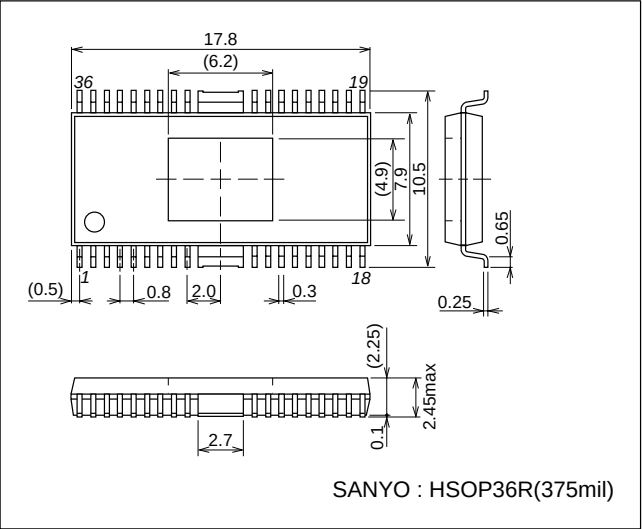
Note *1: The channel 1 input operational amplifier has a 0dB gain, i.e. it is a buffer amplifier.

*2: With the output in the saturated state.

*3: Design guarantee value

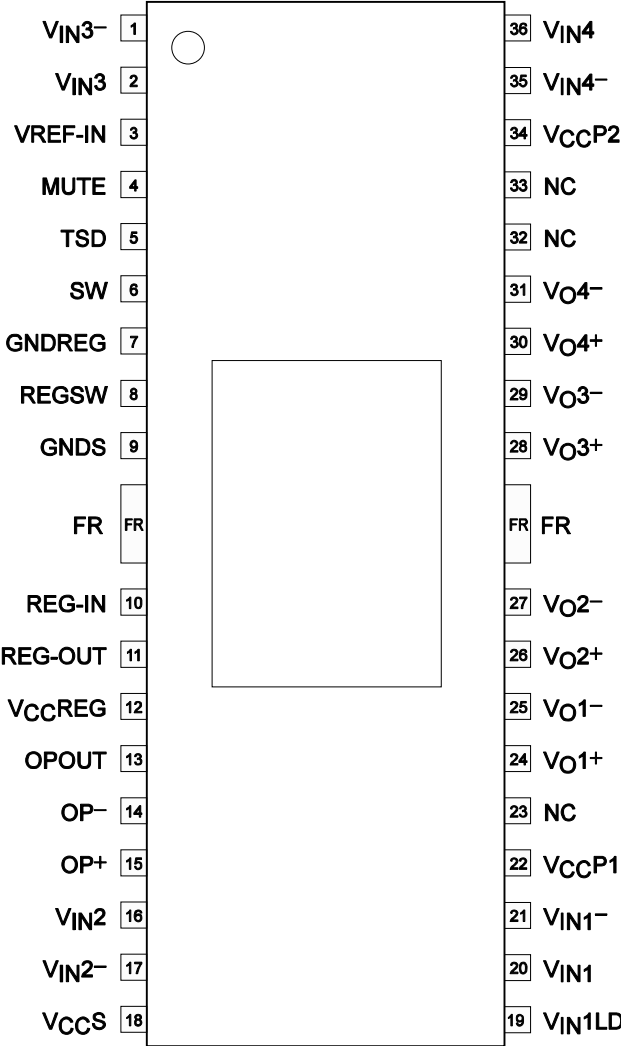
Package Dimensions

unit : mm
3251



Pin Assignment

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Top view

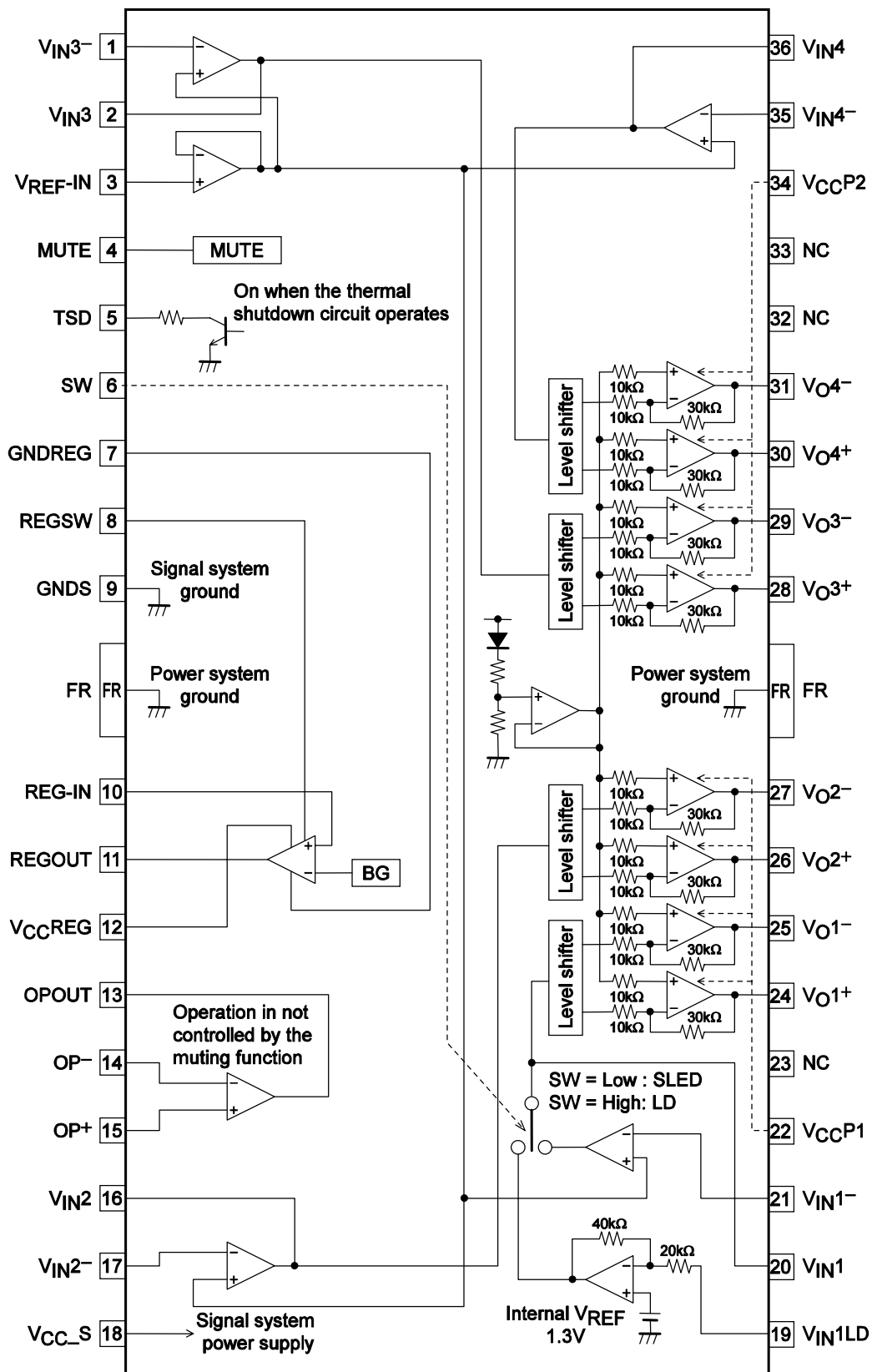
Pin Functions

Pin No.	Symbol	Pin description
1	V _{IN3} ⁻	Front end amplifier, channel 3 Input (-)
2	V _{IN3}	Front end amplifier, channel 3 Output
3	VREF-IN	Reference voltage input
4	MUTE	Muting control
5	TSD	This pin outputs a low level when the thermal shutdown circuit operates.
6	SW	Switches between the loading and sled inputs.
7	GNDREG	Regulator system ground
8	REGSW	Regulator on/off control
9	GNDS	Signal system ground
10	REG-IN	Connection for the voltage divider output used to set the regulator voltage
11	REG-OUT	Base connection of external PNP transistor
12	VCCREG	Regulator power supply
13	OPOUT	Independent operational amplifier output pin
14	OP ⁻	Independent operational amplifier (-)
15	OP ⁺	Independent operational amplifier (+)
16	V _{IN2}	Front end amplifier, channel 2 Output
17	V _{IN2} ⁻	Front end amplifier, channel 2 Input (-)
18	V _{CC_S}	Signal system power supply
19	V _{IN1LD}	Front end amplifier for the loading system input
20	V _{IN1}	Front end amplifier, channel 1 Output
21	V _{IN1} ⁻	Front end amplifier, channel 1 Input (-)
22	V _{CCP1}	Power stage power supply for channels 1 and 2
23	NC	No connection
24	V _{O1} ⁺	Channel 1 output (+)
25	V _{O1} ⁻	Channel 1 output (-)
26	V _{O2} ⁺	Channel 2 output (+)
27	V _{O2} ⁻	Channel 2 output (-)
28	V _{O3} ⁺	Channel 3 output (+)
29	V _{O3} ⁻	Channel 3 output (-)
30	V _{O4} ⁺	Channel 4 output (+)
31	V _{O4} ⁻	Channel 4 output (-)
32	NC	No connection
33	NC	No connection
34	V _{CCP2}	Channels 3 and 4 : power stage power supply
35	V _{IN4} ⁻	Front end amplifier, channel 4 Input (1)
36	V _{IN4}	Front end amplifier, channel 4 Output

Note: • The center frame (FR) is used as the power system ground (GNDP). Along with the signal system ground (GNDS), this level must be the lowest potential in the system.

- The V_{CC_S} (signal system power supply), V_{CCP1}, and V_{CCP2} (output stage power supplies) must be shorted together externally.

Block Diagram



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Pin Functions

Pin No.	Symbol	Pin description	Equivalent circuit
21 20 17 16 1 2 35 36	V_{IN1-} V_{IN1} V_{IN2-} V_{IN2} V_{IN3-} V_{IN3} V_{IN4-} V_{IN4}	Channel 1 to 4 inputs	
24 25 26 27 28 29 30 31	V_{O1+} V_{O1-} V_{O2+} V_{O2-} V_{O3+} V_{O3-} V_{O4+} V_{O4-}	Channel 1 to 4 outputs	
4 6	MUTE SW	MUTE pin SW pin	
3	V_{REF-IN}	Reference voltage	

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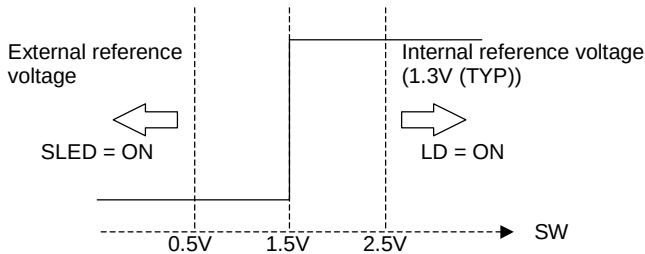
Pin No.	Symbol	Pin description	Equivalent circuit
5	TSD	Thermal shutdown detection During normal operation: the transistor will be in the off state When the thermal shutdown circuit operates: the transistor will be in the on state	
19	V _{IN1} LD	Loading system input	
15 14 13	OP+ OP- OPOUT	Independent operational amplifier Operation is not controlled by the muting function.	
8 12 10 11 7	REGSW V _{CC} REG REG-IN REG-OUT GNDREG	Variable regulator Connect the REG-OUT pin to the base of the external pnp transistor. Connect the output of the external voltage divider to REG-IN.	

Relationship between the MUTE pin and SW

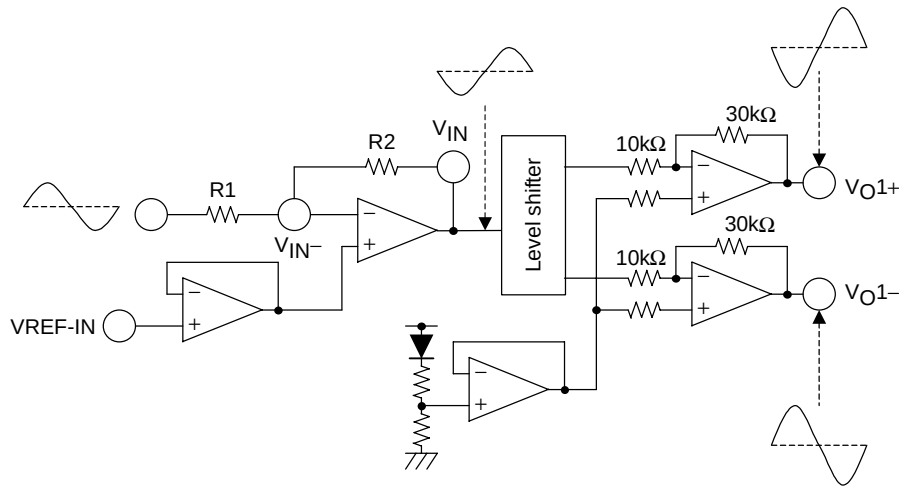
MUTE	SW	ch1	ch2 to ch4
H	H	LD ON	MUTE = OFF
H	L	SLED ON	MUTE = OFF
L	H	LD ON	MUTE = ON
L	L	MUTE = ON	MUTE = ON

The MUTE = off state is the operating state (play), and the MUTE = on state is the stopped state.

Internal reference voltage are external reference voltage



Overview of the input/output relationship

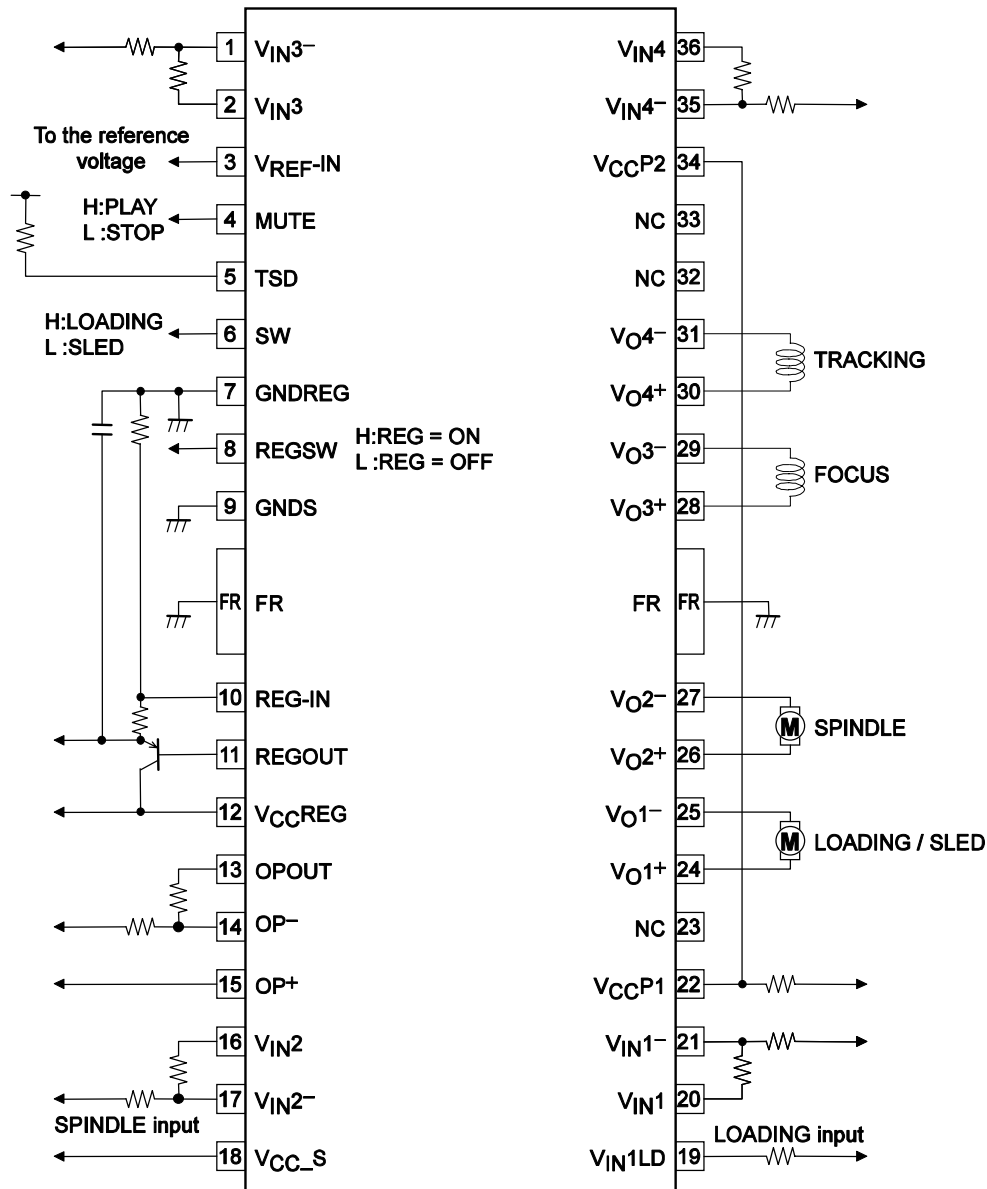


The resistors R1 and R2 in the V_{IN}1LD input block are internal to the IC.

REGSW Pin Operation

REGSW	REG
H	REG = ON
L	REG = OFF

Sample Application Circuit



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