## Contents

1	Block diagram	3
2	Pin connections	4
3	Thermal data	5
4	Maximum ratings	6
	Recommended operating conditions	6
5	Electrical characteristics	7
6	Circuit description	3
7	Typical characteristics	9
8	Package information 12	
	8.1 PowerSO20 package information	2
9	Revision history	4



## 1 Block diagram

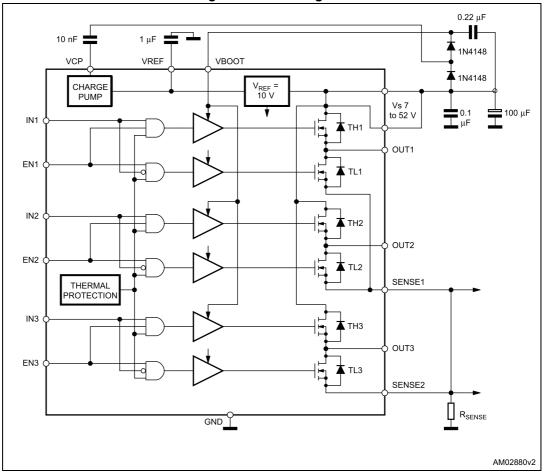
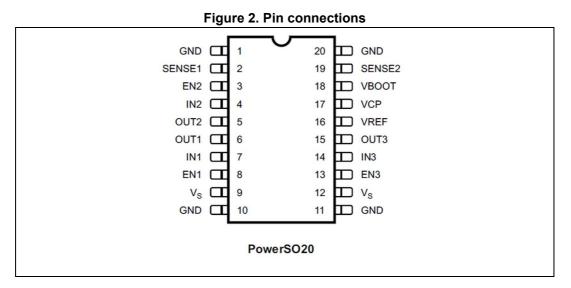


Figure 1. Block diagram



#### 2 Pin connections



#### Table 2. Pin functions

Pin no.	Name	Function
1, 10 11, 20	GND	Common ground terminal. In the PowerSO package these pins are used to dissipate the heat forward the PCB.
2	SENSE1	A sense resistor connected to this pin provides feedback for motor current control for the bridges 1 and 2.
3 8 13	EN 2 EN 1 EN 3	Enable of the channels 1/2/3. A logic LOW level on this pin switches off both power DMOS of the related channel.
4 7 14	IN 2 IN 1 IN 3	Logic input of channels 1/2/3. A logic HIGH level (when the corresponding EN pin is HIGH) switches ON the upper DMOS power transistor, while a logic LOW switches ON the corresponding low side power DMOS.
5 6 15	OUT 2 OUT 1 OUT 3	Output of the channels 1/2/3.
9, 12	Vs	Power supply voltage.
16	VREF	Internal voltage reference. A capacitor connected from this pin to GND increases the stability of the power DMOS drive circuit.
17	VCP	Bootstrap oscillator. Oscillator output for the external charge pump.
18	VBOOT	Overvoltage input to drive the upper DMOS
19	SENSE2	A sense resistor connected to this pin provides feedback for motor current control for the bridge 3.



# 3 Thermal data

Symbol	Parameter	PowerSO20	Unit
R <sub>th j-case</sub>	Thermal resistance junction case	1.5	°C/W



## 4 Maximum ratings

Table 4.	Absolute	maximum	ratings
	/		

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Power supply voltage	52	V
V <sub>IN</sub> , V <sub>EN</sub>	Input enable voltage	– 0.3 to 7	V
I <sub>peak</sub>	Pulsed output current <sup>(1)</sup>	5	А
V <sub>SENSE</sub>	Sensing voltage (DC voltage)	-1 to 4	V
V <sub>boot</sub>	Bootstrap peak voltage	62	V
V <sub>OD</sub>	Differential output voltage (between any of the 3 OUT pins)	60	V
f <sub>C</sub>	Commutation frequency	150	kHz
V <sub>REF</sub>	Reference voltage	12	V
P <sub>tot</sub>	Total power dissipation ( $T_A = 70 \ ^\circ C$ )	2.3	W
T <sub>stg</sub> , T <sub>j</sub>	Storage and junction temperature range	-40 to 150	°C

1. Pulse width limited only by junction temperature and the transient thermal impedance.

#### **Recommended operating conditions**

Symbol	Parameter	Value	Unit	
V <sub>S</sub>	Supply voltage	7 to 42	V	
V <sub>OD</sub>	Peak to peak differential voltage (between any of the 3 out pins)	52	V	
I <sub>out</sub>	DC output current (T <sub>A</sub> = 25 °C)	4	А	
Maria	Sensing voltage (pulsed t <sub>w</sub> < 300 nsec)	-4 to 4	V	
V <sub>SENSE</sub>	Sensing voltage (DC)	-1 to 1	V	
Tj	Junction temperature range	-40 to 125	°C	

#### Table 5. Recommended operating conditions



## 5 Electrical characteristics

 $V_S$  = 42 V;  $T_j$  = 25 °C unless otherwise specified.

Table 6. Electrical characteristics						
Parameter	Test condition	Min.	Тур.	Max.	Unit	
Supply voltage	-	7	-	52	V	
Reference voltage	-	-	10	-	V	
Quiescent supply current	-	-	6.5	-	mA	
Thermal shutdown	-	150	-	-	°C	
Dead time protection	-	-	300	-	ns	
OS transistor	•					
Leakage current	-	-	-	1	mA	
ON resistance	-	-	0.3	-	Ω	
in diode	·					
Forward ON voltage	I <sub>SD</sub> = 4 A; EN = LOW	-	1.2	-	V	
Reverse recovery time	I <sub>F</sub> = 4 A	-	900	-	ns	
Forward recovery time	-	-	200	-	ns	
Logic levels						
Input LOW voltage	-	-0.3	-	0.8	V	
Input HIGH voltage	-	2	-	7	V	
Input LOW current	V <sub>IN</sub> , V <sub>EN</sub> = L	-		-10	μA	
Input HIGH current	V <sub>IN</sub> , V <sub>EN</sub> = H	-	30	-	μA	
	ParameterSupply voltageReference voltageQuiescent supply currentThermal shutdownDead time protectionOS transistorLeakage currentON resistancein diodeForward ON voltageReverse recovery timeForward recovery timesInput LOW voltageInput HIGH voltageInput LOW current	ParameterTest conditionSupply voltage-Reference voltage-Quiescent supply current-Thermal shutdown-Dead time protection-OS transistor-Leakage current-ON resistance-in diode-Forward ON voltageI <sub>SD</sub> = 4 A; EN = LOWReverse recovery timeI <sub>F</sub> = 4 AForward recovery time-s-Input LOW voltage-Input LOW voltage-Input LOW currentV <sub>IN</sub> , V <sub>EN</sub> = L	ParameterTest conditionMin.Supply voltage-7Reference voltageQuiescent supply currentThermal shutdown-150Dead time protectionOS transistorLeakage currentON resistancein diodeISD = 4 A; EN = LOW-Forward ON voltage $I_F = 4 A$ -Forward recovery timesInput LOW voltage0.3Input LOW current $V_{IN}, V_{EN} = L$ -	ParameterTest conditionMin.Typ.Supply voltage-7-Reference voltage-10Quiescent supply current6.5Thermal shutdown-150-Dead time protection-300OS transistorLeakage currentON resistance0.3in diode $I_{SD} = 4 A; EN = LOW$ -1.2Reverse recovery time $I_F = 4 A$ -900Forward recovery timeInput LOW voltage0.3-Input LOW current $V_{IN}, V_{EN} = L$	Parameter     Test condition     Min.     Typ.     Max.       Supply voltage     -     7     -     52       Reference voltage     -     10     -       Quiescent supply current     -     -     10     -       Quiescent supply current     -     -     6.5     -       Thermal shutdown     -     150     -     -       Dead time protection     -     300     -       OS transistor     -     -     11       Leakage current     -     -     0.3     -       In diode     -     -     1.2     -       Forward ON voltage $I_{SD} = 4 A$ ; EN = LOW     -     1.2     -       Reverse recovery time $I_F = 4 A$ -     900     -       Forward recovery time $I_F = 4 A$ -     200     -       S     -     -     2.0     -     -       Input LOW voltage     -     -     -     7     10.8	

Table 6. Electrical characteristics



#### 6 Circuit description

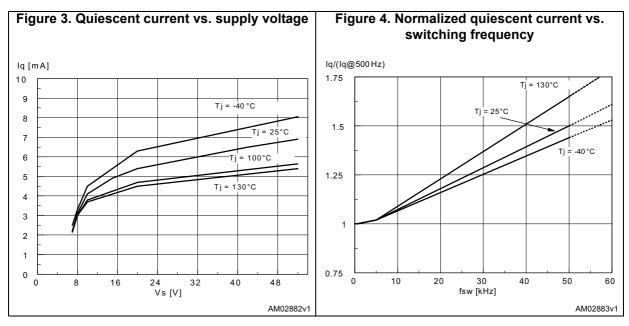
The L6234 is a triple half bridge designed to drive brushless DC motors. Each half bridge has 2 power DMOS transistors with  $R_{DSon}$  = 0.3  $\Omega$ .

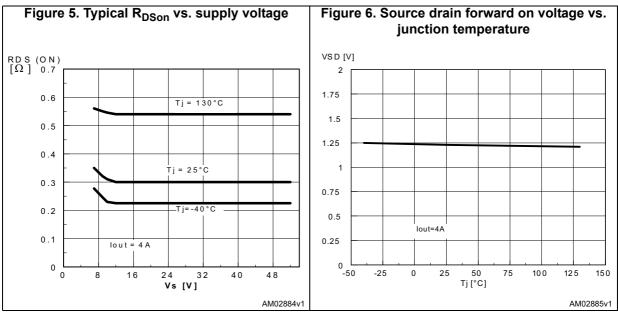
The 3 half bridges can be controlled independently by means of the 3 inputs IN1, IN2, IN3 and the 3 inputs EN1, EN2, and EN3. An external connection to the 3 common low side DMOS sources is provided to connect a sensing resistor for the constant current chopping application.

The driving stage and the logic stage are designed to work from 7 V to 52 V.

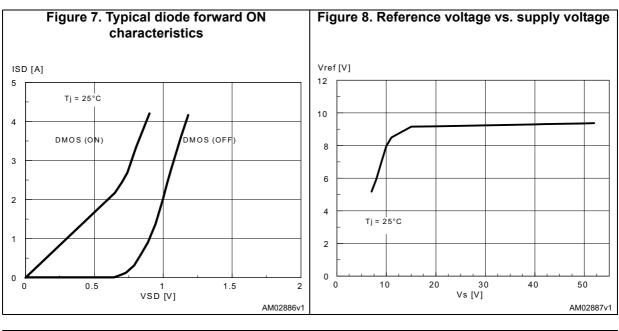


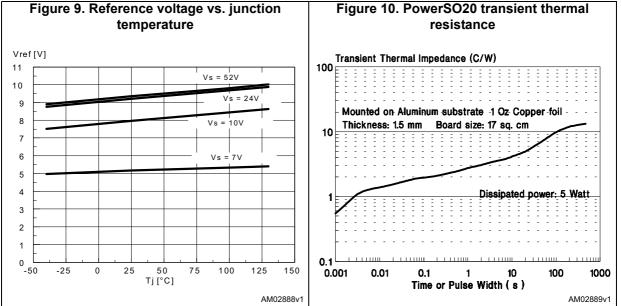
## 7 Typical characteristics



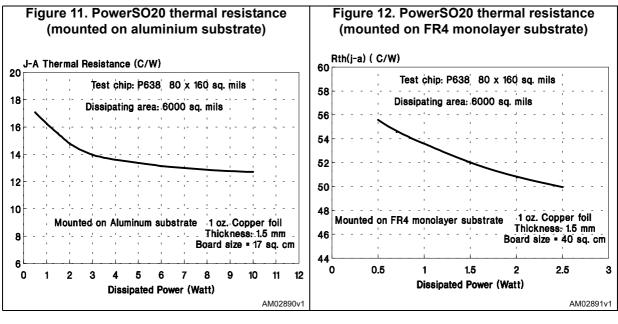


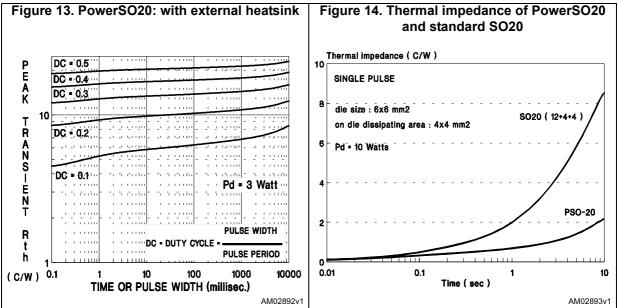














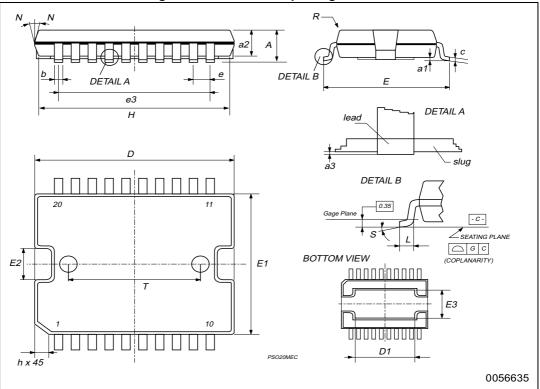
DocID1107 Rev 11

L6234

#### 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK<sup>®</sup> is an ST trademark.

#### 8.1 PowerSO20 package information







Cumhal		Dimensions (mm )	
Symbol	Min.	Тур.	Max.
А	-	-	3.6
a1	0.1	-	0.3
a2	-	-	3.3
a3	0	-	0.1
b	0.4	-	0.53
С	0.23	-	0.32
D <sup>(1)</sup>	15.8	-	16
D1	9.4	-	9.8
E	13.9	-	14.5
е	-	1.27	-
e3	-	11.43	-
E1 <sup>(1)</sup>	10.9	-	11.1
E2	-	-	2.9
E3	5.8	-	6.2
G	0	-	0.1
Н	15.5	-	15.9
h	-	-	1.1
L	0.8	-	1.1
Ν		8° (typ.)	1
S		8° (max.)	
Т	-	10	-

Table 7. PowerSO20 package mechanical data

"D" and "E1" do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed 0.15 mm (0.006").



# 9 Revision history

Date	Revision	Changes
15-Nov-2011	10	Updated Features in coverpage and Table 4.
15-Mar-2017	11	Removed PowerDIP 20-pin package and all references throughout document. Updated <i>Figure 1 on page 3</i> (replaced by new figure). Added note <i>1</i> . below <i>Table 7 on page 13</i> . Minor modifications throughout document.



#### IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved

