Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	17 10.6	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	45	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	43	mJ	I_D=2.2A; V_{DD}=50V
Avalanche energy, repetitive	E_{AR}	-	-	0.36	mJ	I_D=2.2A; V_{DD}=50V
Avalanche current, repetitive	I_{AR}	-	-	2.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0 to 400V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	101	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-
Continuous diode forward current	I_S	-	-	12	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	45	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	1	V/ns	V_{DS}=0 to 400V, I_{SD}<=3.6A, T_j=25°C
Maximum diode commutation speed[3]	di_f/dt	-	-	50	A/µs	V_{DS}=0 to 400V, I_{SD}<=3.6A, T_j=25°C

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.2	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	Device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.5
[2] Pulse width t_p limited by $T_{j,max}$
[3] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G; t_{cond}<2µs

3 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	V_{DS}=V_{GS}, I_D=0.36mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=800V, V_{GS}=0V, T_j=25°C V_{DS}=800V, V_{GS}=0V, T_j=150°C
Gate-source leakage curent incl. zener diode	I_{GSS}	-	-	1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.24 0.62	0.28 -	Ω	V_{GS}=10V, I_D=7.2A, T_j=25°C V_{GS}=10V, I_D=7.2A, T_j=150°C
Gate resistance	R_G	-	1	-	Ω	f=250kHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1200	-	pF	V_{GS}=0V, V_{DS}=500V, f=250kHz
Output capacitance	C_{oss}	-	20	-	pF	V_{GS}=0V, V_{DS}=500V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	38	-	pF	V_{GS}=0V, V_{DS}=0 to 500V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	490	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0 to 500V
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=7.2A, R_G=4.7Ω
Rise time	t_r	-	6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=7.2A, R_G=4.7Ω
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=7.2A, R_G=4.7Ω
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=7.2A, R_G=4.7Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=640V, I_D=7.2A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	15	-	nC	V_{DD}=640V, I_D=7.2A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	36	-	nC	V_{DD}=640V, I_D=7.2A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	V_{DD}=640V, I_D=7.2A, V_{GS}=0 to 10V

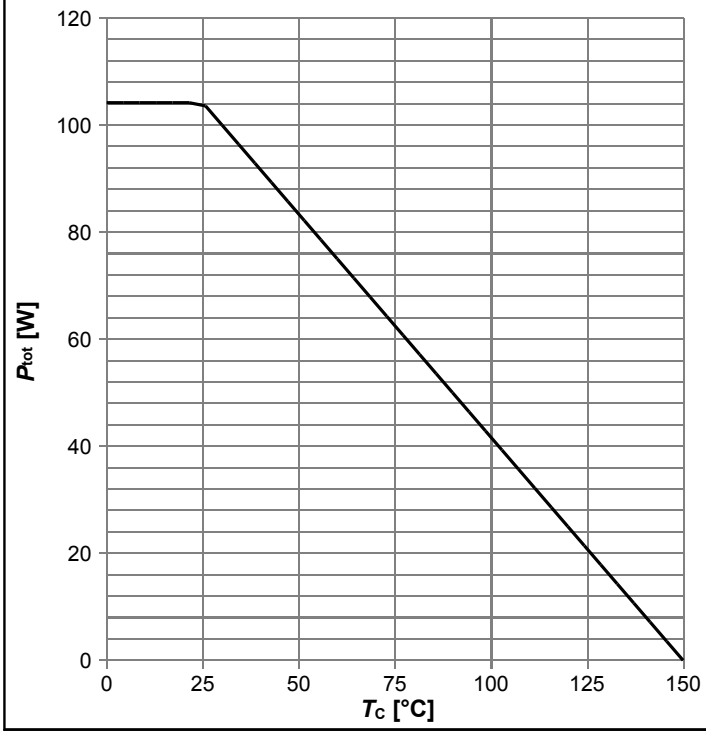
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=7.2A, T_f=25°C
Reverse recovery time	t_{rr}	-	1200	-	ns	V_R=400V, I_F=3.6A, di_F/dt=50A/µs
Reverse recovery charge	Q_{rr}	-	15	-	µC	V_R=400V, I_F=3.6A, di_F/dt=50A/µs
Peak reverse recovery current	I_{rrm}	-	24	-	A	V_R=400V, I_F=3.6A, di_F/dt=50A/µs

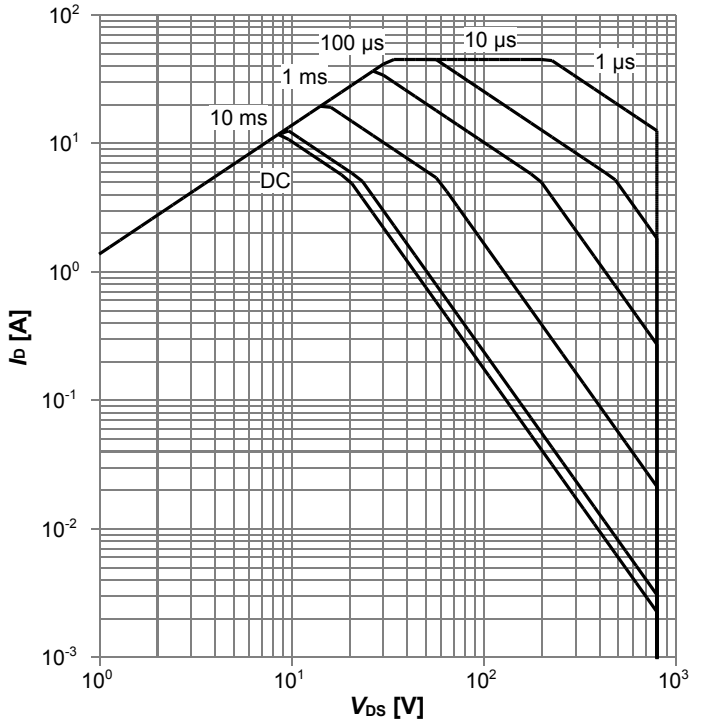
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



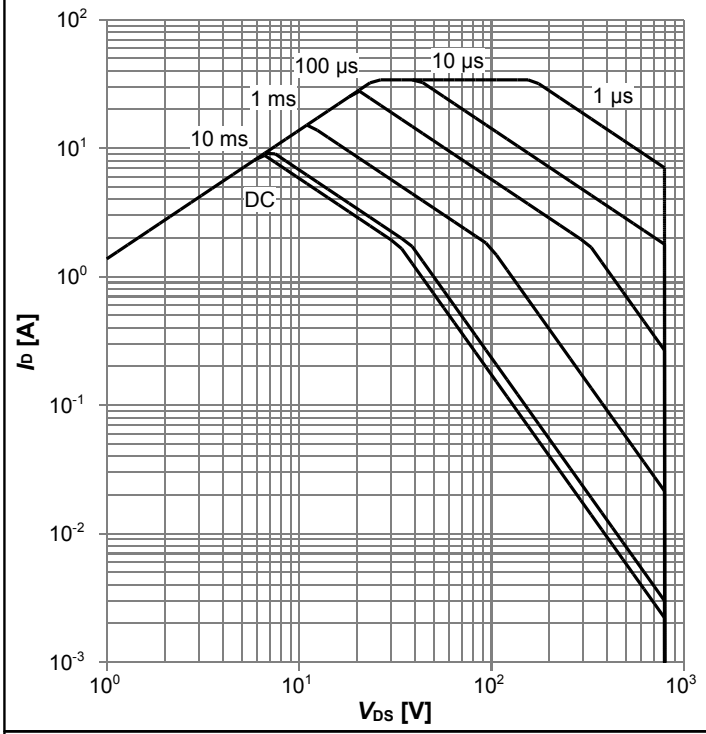
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



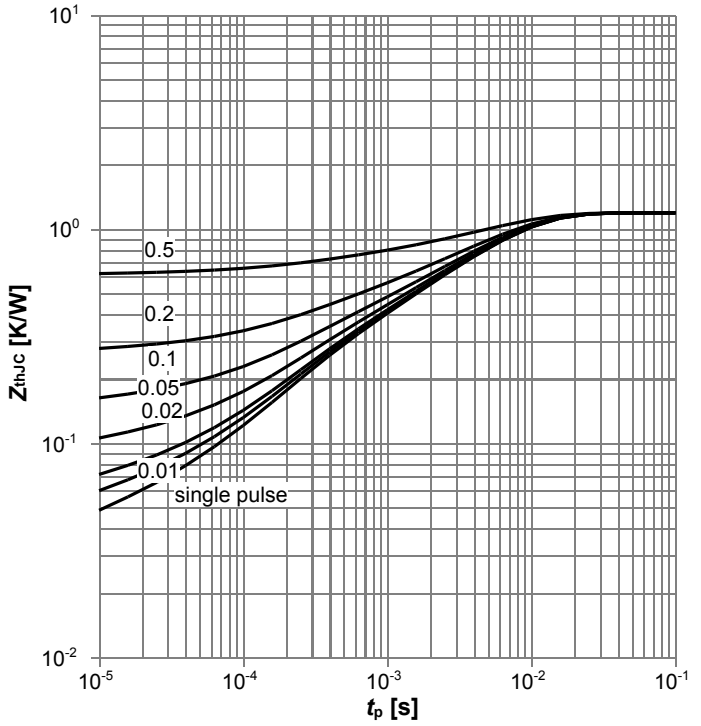
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 3: Safe operating area



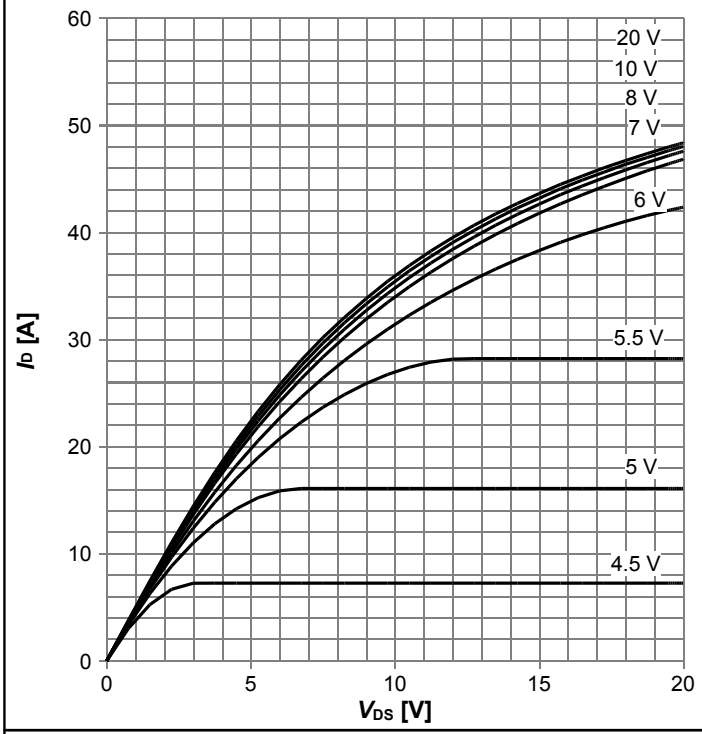
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



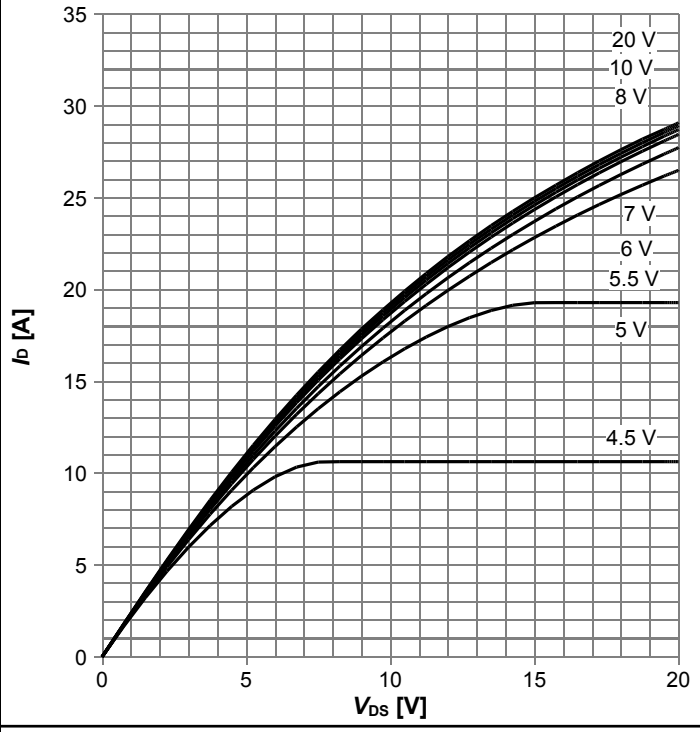
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



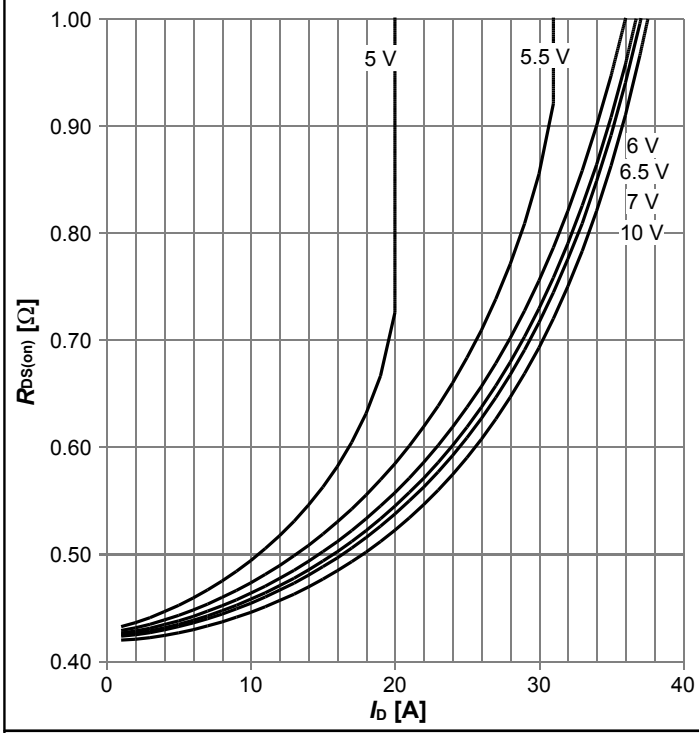
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



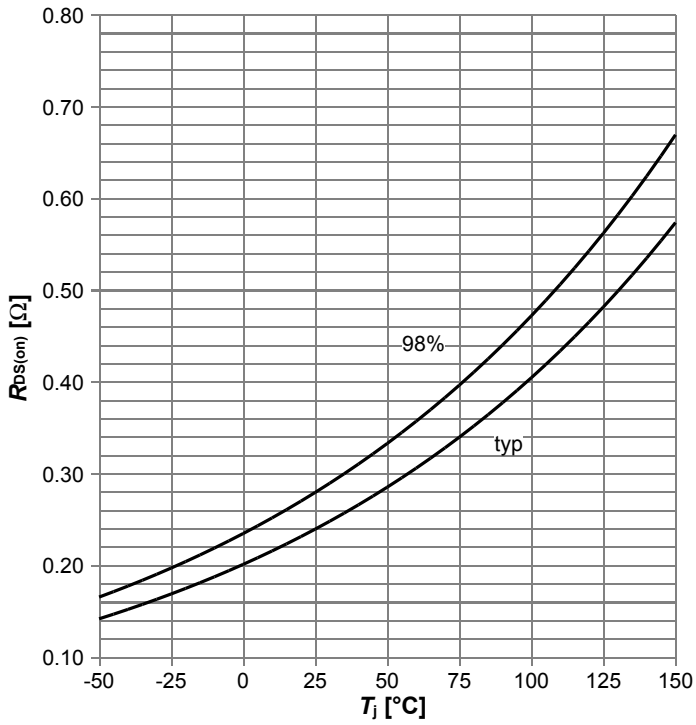
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



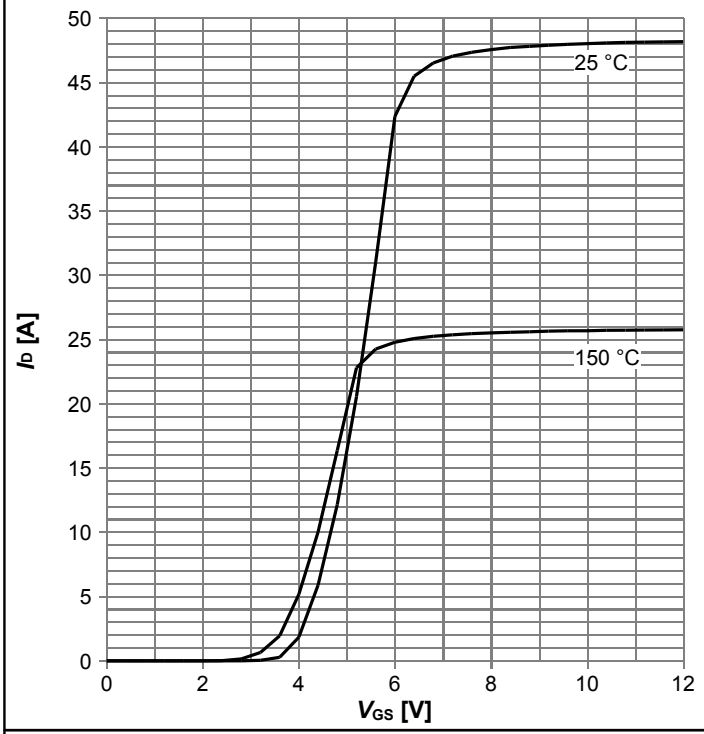
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



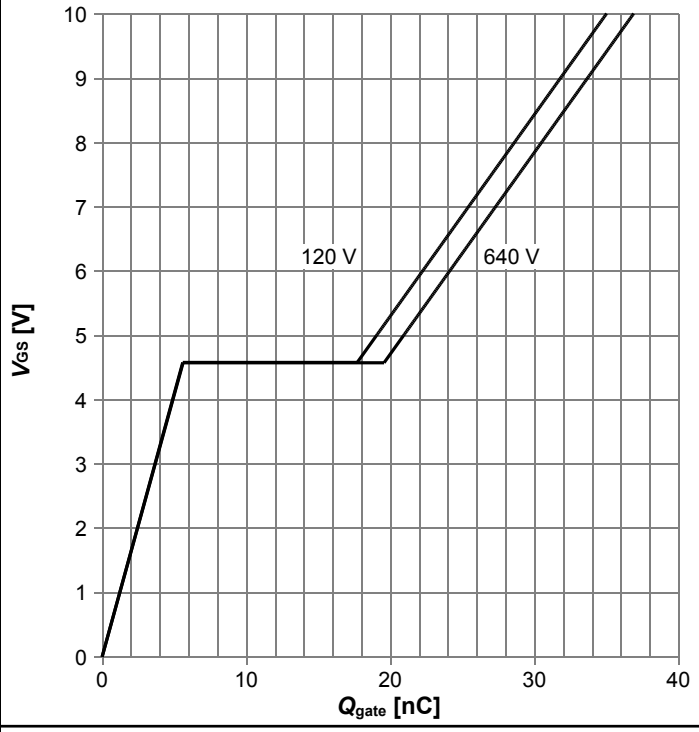
$R_{DS(on)}=f(T_j)$; $I_D=7.2$ A; $V_{GS}=10$ V

Diagram 9: Typ. transfer characteristics



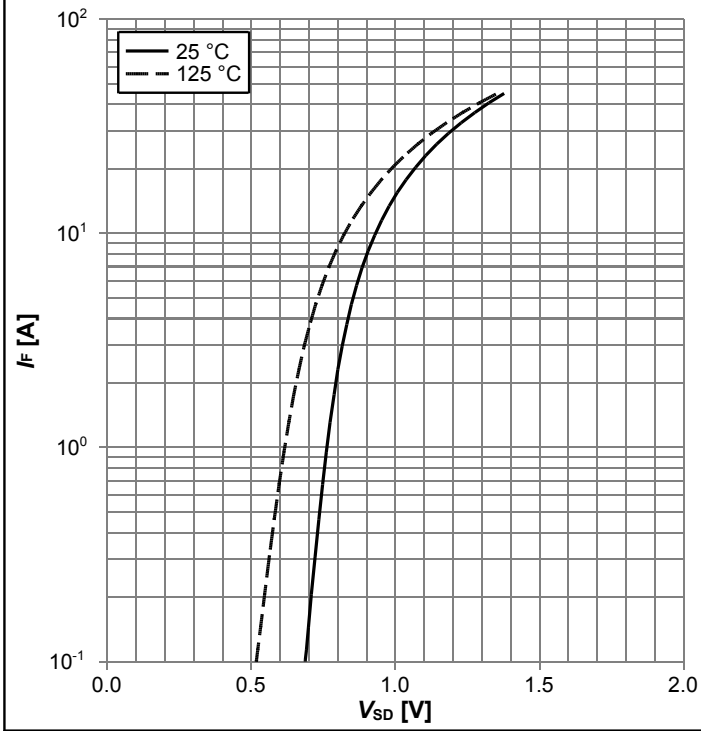
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



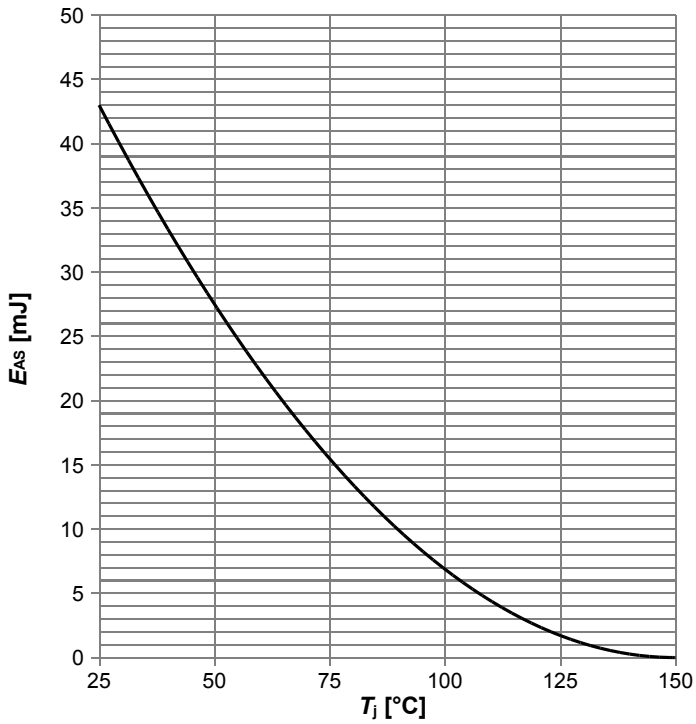
$V_{GS}=f(Q_{gate})$; I_D=7.2 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



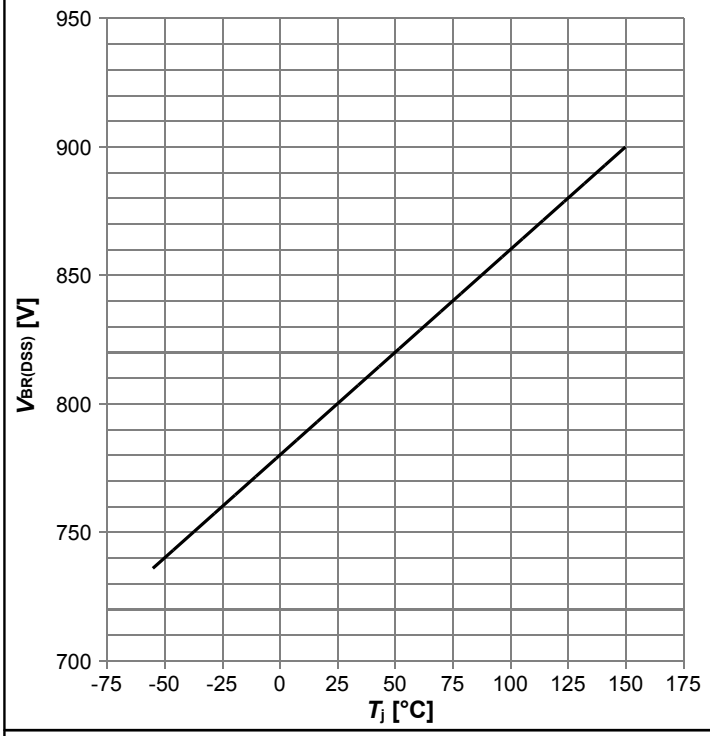
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



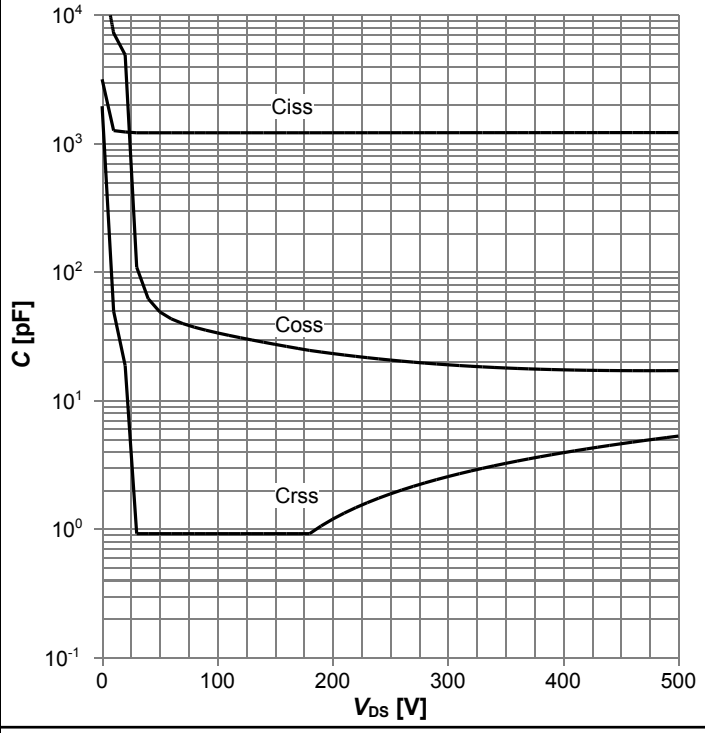
$E_{AS}=f(T_j)$; I_D=2.2 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



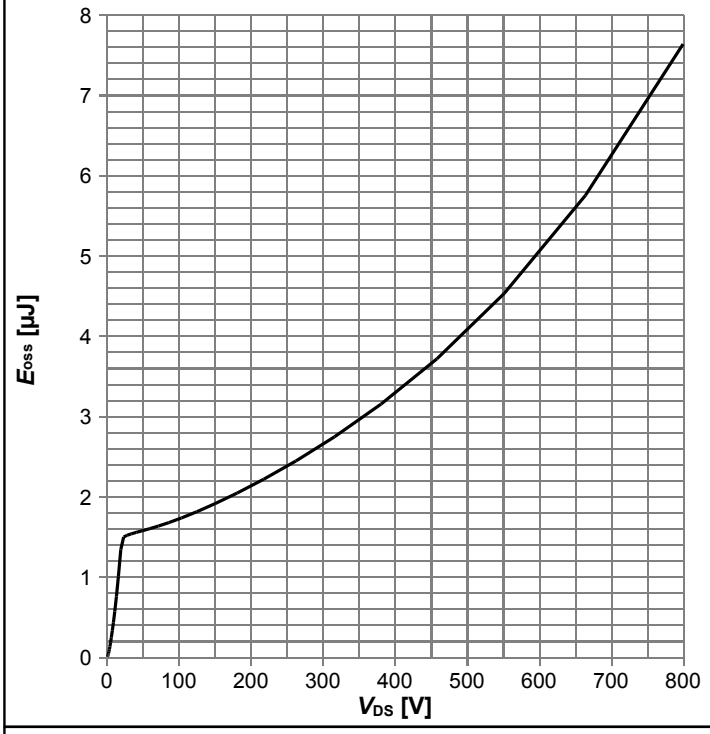
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

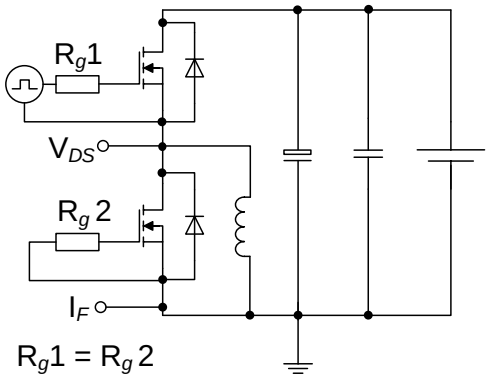
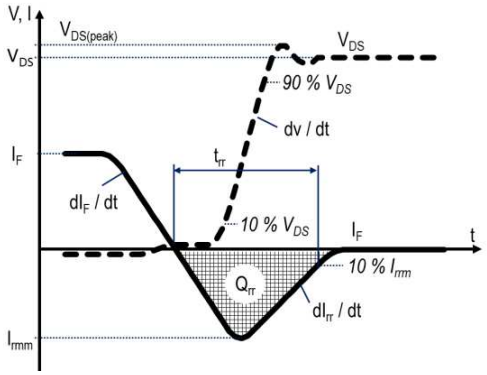
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

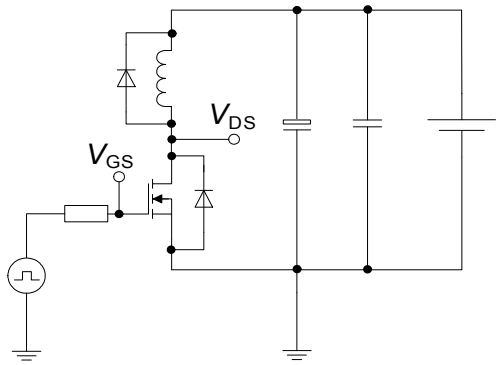
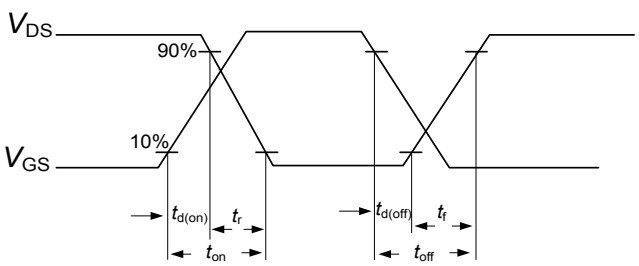
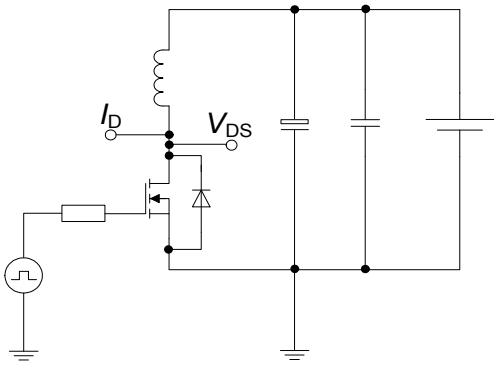
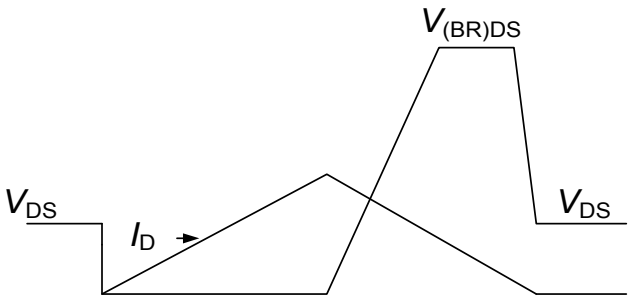
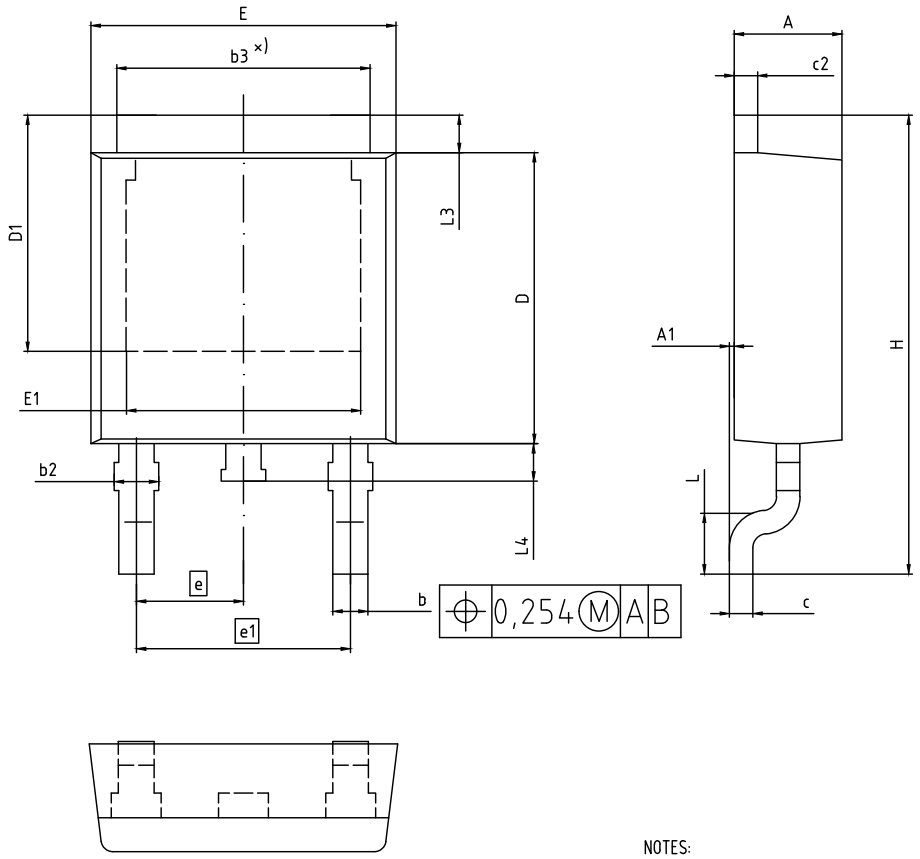
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	4,95	5.50	0.195	0.217
c	0.46	0.61	0.018	0.024
c2	0.40	0.98	0.016	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.78	0.046	0.070
L3	0.89	1.27	0.035	0.050
L4	0.51	1.02	0.020	0.040

DOCUMENT NO.
Z8B00003328

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-02-2016

REVISION
06

Figure 1 Outline PG-TO 252-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPD80R280P7

Revision: 2018-02-09, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-05	Release of final version
2.1	2018-02-09	Corrected front page text

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