TABLE OF CONTENTS

REVISION HISTORY

5/2018—Rev. C to Rev. D

Changed + 27 V to 27 dBm in Rating Column, Table 2 ... 4
Change to Ordering Guide ... 11
Added Theory of Operation Section, RF Input and Output Section, and Power Supply Section ... 9
Changes to Figure 22 ... 10
Changes to Ordering Guide ... 11

8/2017—Rev. 02.0417 to Rev. C

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changed N/C to NIC ... Throughout
Changes to Features Section, Applications Section, and General Description Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 and Added Thermal Resistance Section ... 4
Added Table 3; Renumbered Sequentially ... 4
Changes to Table 4 ... 5
Changes to Figure 5 Caption through Figure 10 Caption ... 6
Changes to Figure 11 Caption through Figure 14 Caption ... 7
Changes to Figure 15 Caption through Figure 20 Caption ... 8

SPECIFICATIONS

VDD = 5 V, VSS = −5 V, V_{CTL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		33	GHz
INSERTION LOSS		0.1 GHz to 18 GHz		4.5	5.5	dB
		18 GHz to 26.5 GHz		5.5	7.0	dB
		26.5 GHz to 33 GHz		6.0	8.0	dB
ATTENUATION						
Range		Between minimum and maximum attenuation states, 0.1 GHz to 33 GHz		31		dB
Step Size		Between any successive attenuation states, 0.1 GHz to 33 GHz		1		dB
Step Error		Between any successive attenuation states, 0.1 GHz to 33 GHz		0.5		dB
State Error		Referenced to insertion loss state				
		1 dB to 15 dB attenuation states, 0.1 GHz to 33 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 0.1 GHz to 20 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 20 GHz to 33 GHz	−(0.6 + 8% of attenuation state)		+(0.6 + 8% of attenuation state)	dB
RETURN LOSS		RF1 and RF2 pins, all attenuation states, 0.1 GHz to 33 GHz		10		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		0.1 GHz to 18 GHz		45		Degrees
		18 GHz to 26.5 GHz		60		Degrees
		26.5 GHz to 33 GHz		80		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		45		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		60		ns
INPUT LINEARITY		All attenuation states				
0.1 dB Compression	P0.1dB	0.1 GHz to 0.5 GHz		20		dBm
		0.5 GHz to 33 GHz		24		dBm
Third-Order Intercept	IP3	8 dBm per tone, 1 MHz spacing				
		0.1 GHz to 0.5 GHz		43		dBm
		0.5 GHz to 33 GHz		40		dBm
SUPPLY CURRENT						
Positive	I_{DD}		2.5	4.5	6.5	mA
Negative	I_{SS}		−7.0	−5.5	−3.0	mA
DIGITAL CONTROL INPUTS		P0 to P5 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		2.0		5.0	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
Positive	+7 V
Negative	−7 V
Digital Control Input Voltage	V_{DD} + 0.5 V
RF Input Power (All Attenuation States, f = 0.1 GHz to 33 GHz, T_{CASE} = 85°C)	27 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 85°C)	0.453 W
Temperature	
Junction, T_J	150°C
Storage	−65°C to +150°C
Reflow[1] ((Moisture Sensitivity Level 3 (MSL3) Rating)	260°C
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-24-16[1]	143.5[2]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

[2] The device is set to maximum attenuation state.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

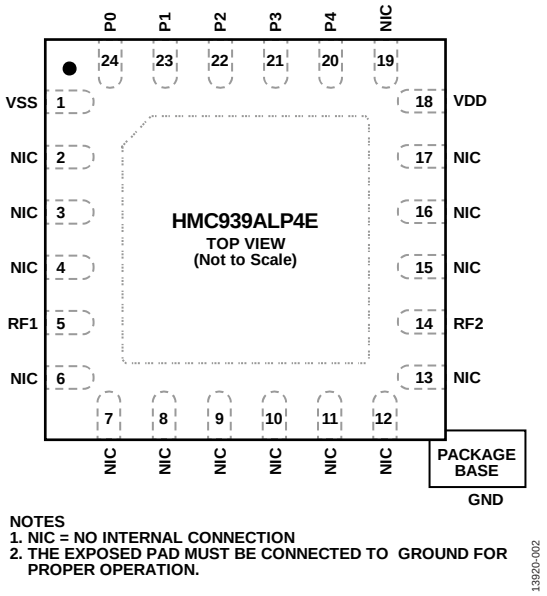


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VSS	Negative Supply Voltage.
2 to 4, 6 to 13, 15 to 17, 19	NIC	These pins are not internally connected; however, all data shown herein was measured when these pins connected to the RF/DC ground of evaluation board.
5	RF1	This pin can be used as RF input or output of attenuator. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
14	RF2	This pin can be used as RF input or output of attenuator. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
18	VDD	Positive Supply Voltage.
20 to 24	P4 to P0	Parallel Control Voltage Inputs. These pins select the required attenuation (see Table 6). There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (VIH or VIL) and not be left floating.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

INTERFACE SCHEMATICS

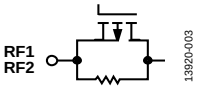


Figure 3. RF1, RF2 Interface Schematic

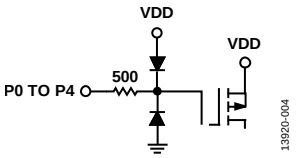


Figure 4. Digital Control Input Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

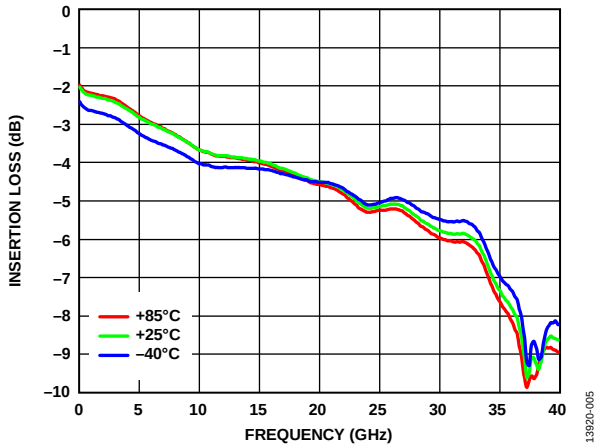


Figure 5. Insertion Loss vs. Frequency over Temperature

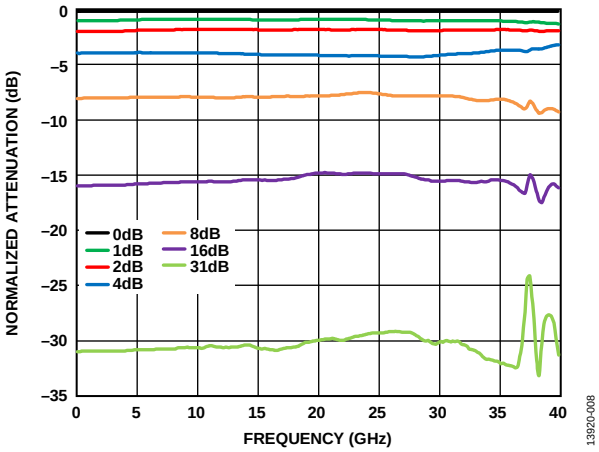


Figure 8. Normalized Attenuation vs. Frequency over Major Attenuation States

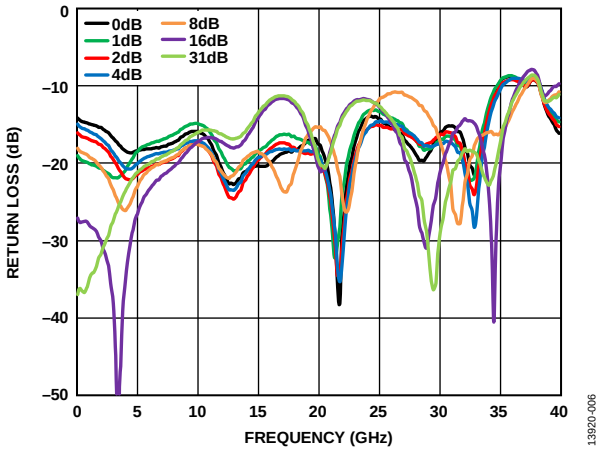


Figure 6. RF1 Return Loss vs. Frequency over Major Attenuation States

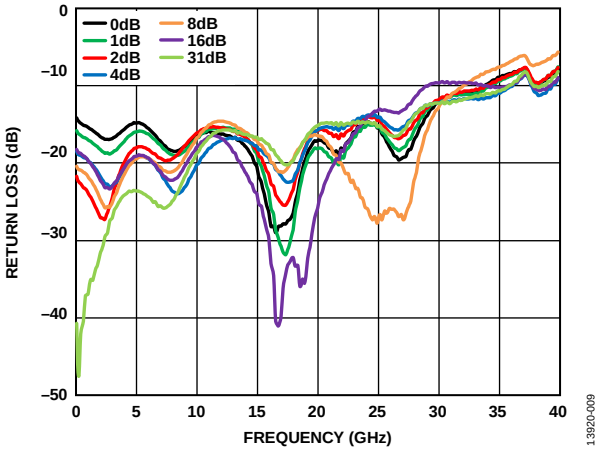


Figure 9. RF2 Return Loss vs. Frequency over Major Attenuation States

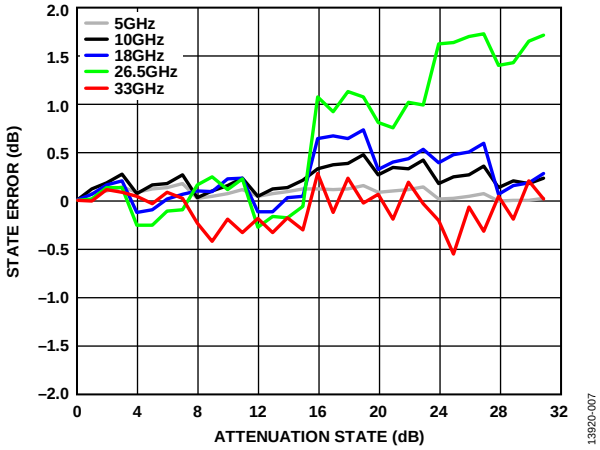


Figure 7. State Error vs. Attenuation State over Frequency

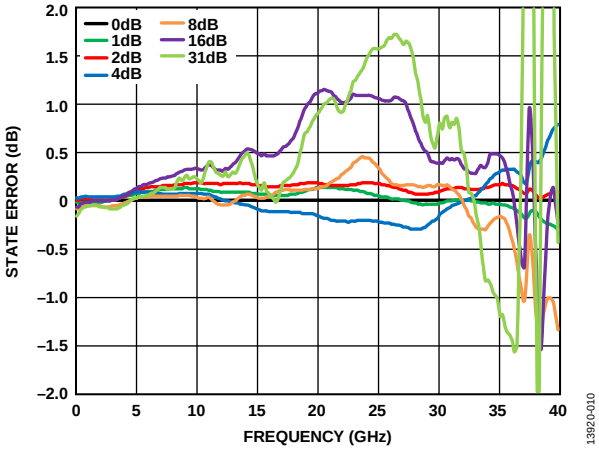


Figure 10. State Error vs. Frequency over Major Attenuation States

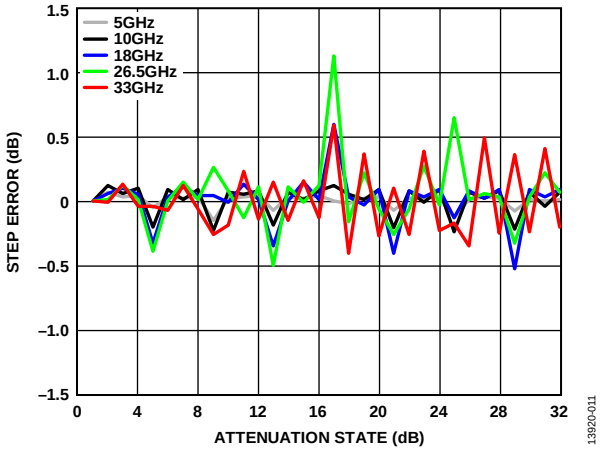


Figure 11. Step Error vs. Attenuation State over Frequency

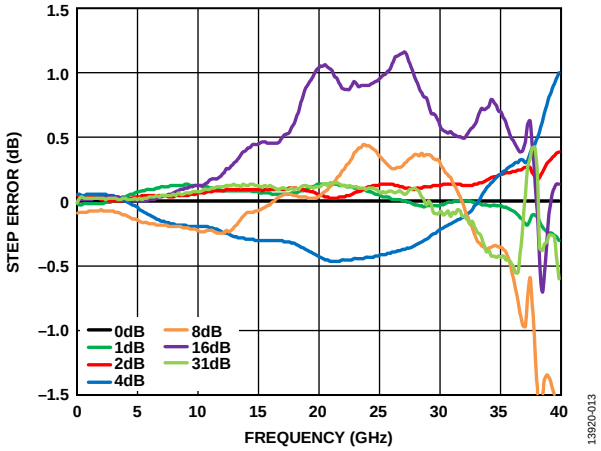


Figure 13. Step Error vs. Frequency over Major Attenuation States

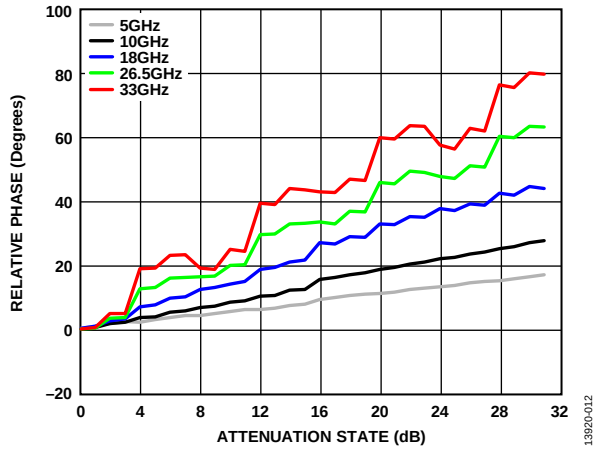


Figure 12. Relative Phase vs. Attenuation State over Frequency

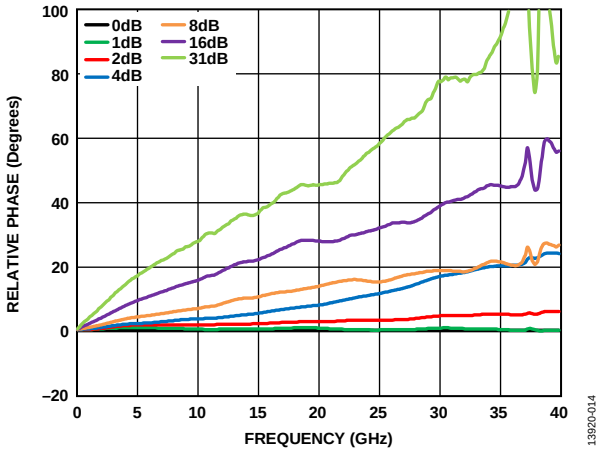


Figure 14. Relative Phase vs. Frequency over Major Attenuation States

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

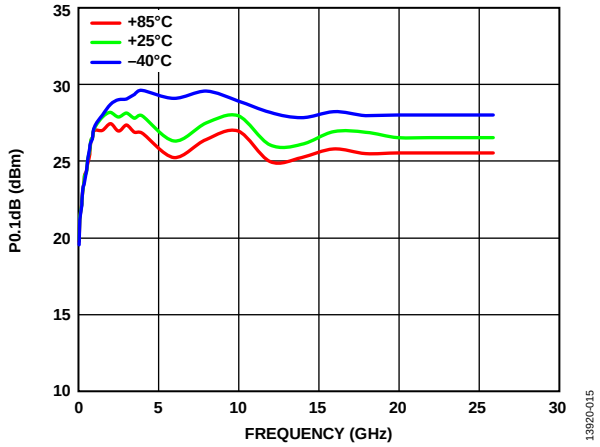


Figure 15. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature

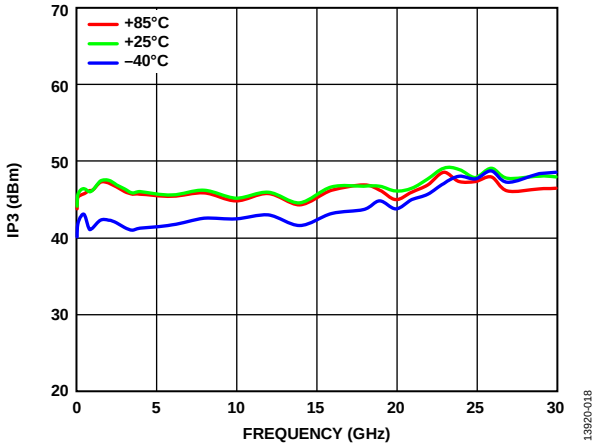


Figure 18. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature

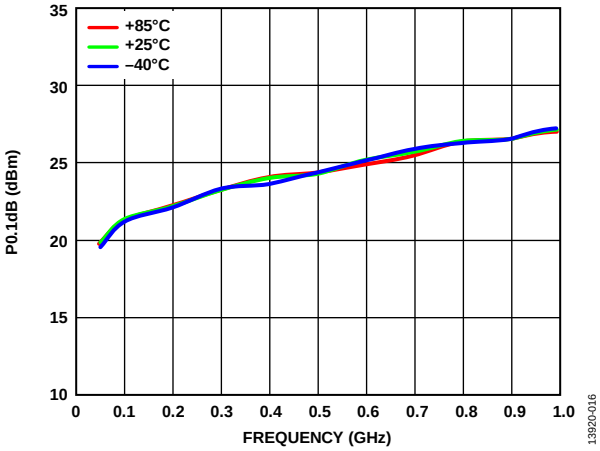


Figure 16. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature (Low Frequency Detail)

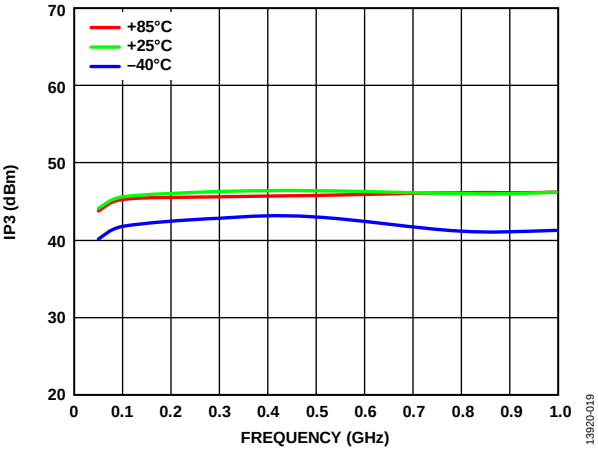


Figure 19. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature (Low Frequency Detail)

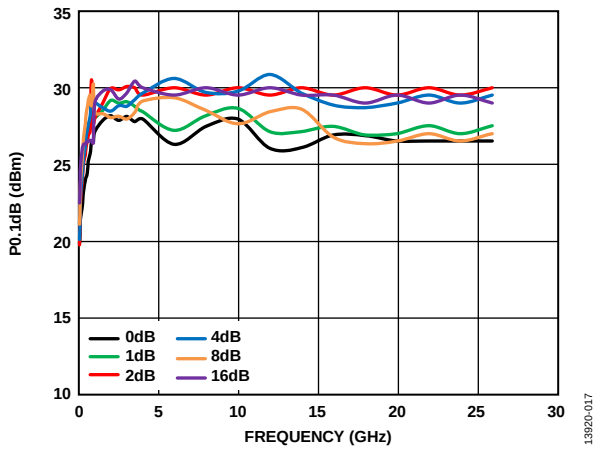


Figure 17. Input P0.1dB vs. Frequency over Major Attenuation States

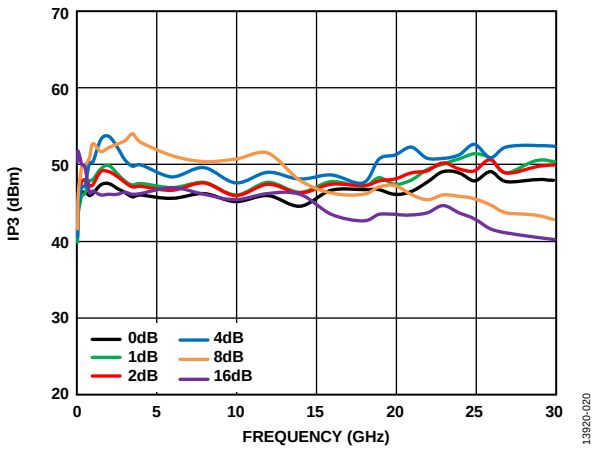


Figure 20. Input IP3 vs. Frequency over Major Attenuation States

THEORY OF OPERATION

The HMC939ALP4E incorporates a 5-bit attenuator die that offers an attenuation range of 31 dB in 1 dB steps and a driver for CMOS-/TTL-compatible parallel control of the 5-bit attenuator. See Table 5 for the truth table.

Table 5. P4 to P0 Truth Table

Digital Control Input[1]					Attenuation
P4	P3	P2	P1	P0	State (dB)
High	High	High	High	High	0 dB (reference)
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

[1] Any combination of the control voltage input states shown in Table 5 provides an attenuation equal to the sum of the bits selected.

POWER SUPPLY

The HMC939ALP4E requires dual supply voltages, VDD = +5 V and VSS = −5 V, and CMOS/TTL-compatible control voltages applied to the P0 to P4 pins. The ideal power-up sequence is as follows:

1. Connect the ground reference.
2. Power up VDD and VSS. The relative order is not important.
3. Apply the digital control inputs. The relative order of the digital control inputs is not important.
4. Apply an RF input signal to RF1 or RF2.

The power-down sequence is the reverse of the power-up sequence.

RF INPUT AND OUTPUT

The HMC939ALP4E is bidirectional. The RF1 and RF2 pins are internally matched to 50 Ω and dc-coupled to 0 V; therefore, they do not require external matching components and dc blocking capacitors when the RF line potential is equal to 0 V.

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC939ALP4E uses a 4-layer evaluation board. The copper thickness is 0.5 oz (0.7 mil) on each layer. The top dielectric material is 10 mil Rogers RO4350 for optimal high frequency performance. The middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil. RF traces are routed on the top copper layer and the bottom layer is grounded plane that provide a solid ground for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 16 mil and ground spacing of 13 mil to have a characteristic impedance of 50 Ω. For enhanced RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 21 shows the top view of the populated HMC939ALP4E evaluation board, available from Analog Devices, Inc., upon request (see the Ordering Guide section).

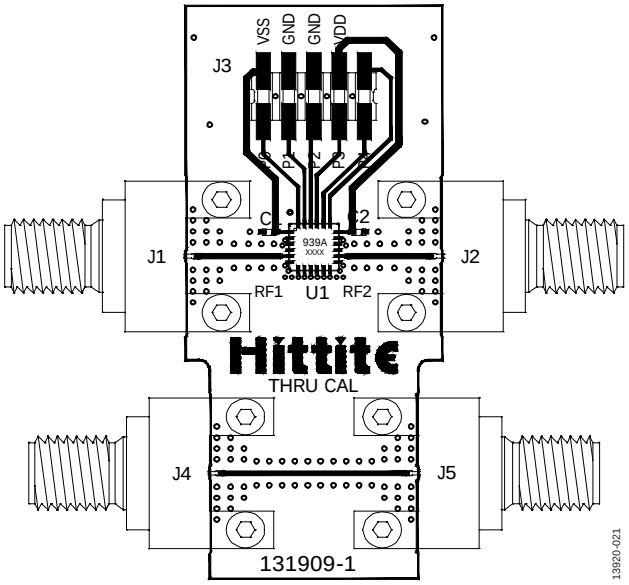


Figure 21. Populated Evaluation Board—Top View

The evaluation board is grounded from the 2 × 5-pin header, J3. All the supply and digital control pins are also connected to the J3. A 1 nF decoupling capacitors are placed on the supply traces to filter high frequency noise.

The RF1 and RF2 ports are connected through 50 Ω transmission lines to the RF connectors, J1 and J2, respectively. A thru calibration line connects J4 and J5; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

Figure 22 and Table 6 show the evaluation board schematic and bill of materials, respectively.

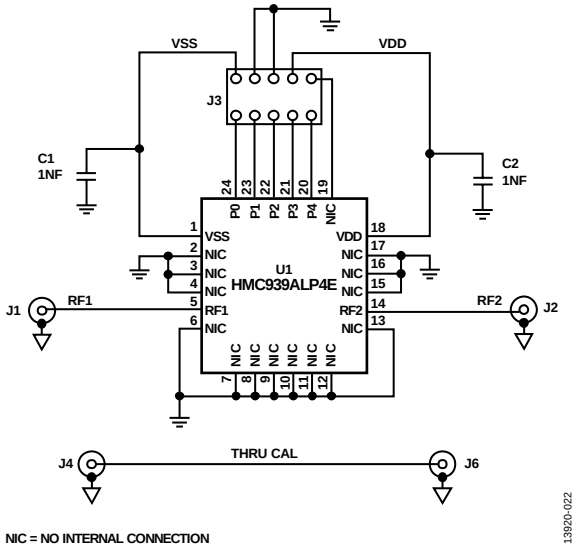
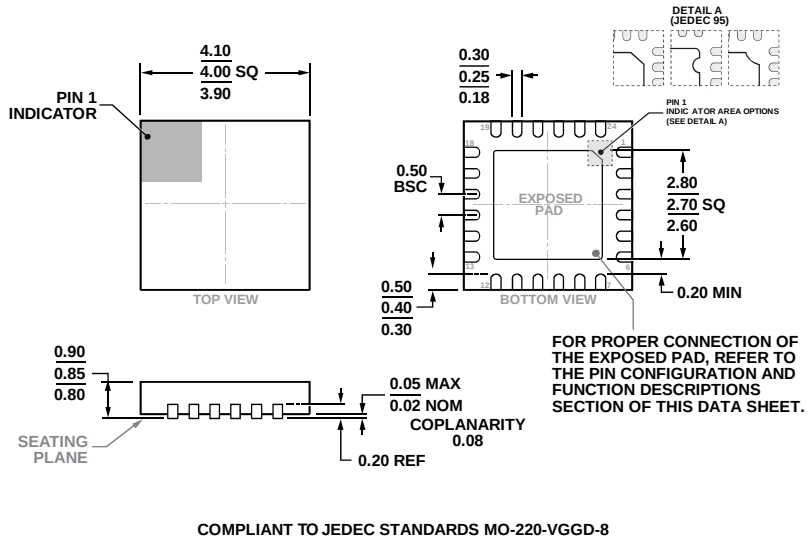


Figure 22. Evaluation Board Schematic

Table 6. List of Materials for EV1HMC939ALP4

Item	Description
J1, J2	PCB mount, 2.9 mm RF connector
J3,	2 × 5-pin header
J4, J5	PCB mount, 2.9 mm RF connector, do not insert
C1, C2	1 nF capacitor, 0402 package
U1	HMC939ALP4E digital attenuator
PCB	131909-1 evaluation PCB

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 23. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC939ALP4E	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16
HMC939ALP4ETR	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16
EV1HMC939ALP4			Evaluation Board	

[1] All models are RoHS compliant.
[2] See the Absolute Maximum Ratings section.

D13920-0-5/18(D)