ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+ to V-		44	V
GND to V-		25	
V_L		(GND - 0.3) to (V+) +0.3	
Digital Inputs [a], V_S, V_D		(V-) -2 to (V+) +2 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle)		100	
Storage Temperature		-65 to 125	°C
Power Dissipation (Package) [b]	16-Pin Plastic DIP [c]	450	mW
	16-Pin Narrow Body SOIC [d]	640	

Notes
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 8 mW/°C above 75 °C.

SPECIFICATIONS for Dual Supplies

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [e]		TEMP. [a]	D SUFFIX -40 °C TO 85 °C			UNIT
					MIN. [b]	TYP. [c]	MAX. [b]	
Analog Switch								
Analog Signal Range [d]	V_{ANALOG}			Full	-15	-	15	V
Drain-Source On-Resistanc [e]	$R_{DS(on)}$	I_S = -10 mA, V_D = ± 8.5 V V+ = 13.5 V, V- = -13.5 V		Room	-	50	85	Ω
				Full	-	-	100	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V- = -16.5 V V_D = ± 15.5 V, V_S = ± 15.5 V		Room	-0.5	± 0.01	0.5	nA
				Full	-5	± 0.01	5	
	$I_{D(off)}$			Room	-0.5	± 0.01	0.5	
				Full	-5	± 0.01	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = -16.5 V V_S = V_D = ± 15.5 V		Room	-0.5	± 0.08	0.5	
				Full	-10	± 0.08	10	
Digital Control								
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V		Full	-500	-0.01	500	nA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V		Full	-500	0.01	500	
Dynamic Characteristics								
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ± 10 V, See Figure 2		Room	-	120	250	ns
Turn-Off Time	t_{OFF}		DG444	Room	-	110	140	
			DG445	Room	-	160	210	
Charge Injection [e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω		Room	-	-1	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω , C_L = 5 pF, f =1 MHz		Room	-	60	-	dB
Crosstalk (Channel-to-Channel) [d]	X_{TALK}			Room	-	100	-	
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz		Room	-	4	-	pF
Drain Off Capacitance	$C_{D(off)}$			Room	-	4	-	
Channel On Capacitance	$C_{D(on)}$	V_{ANALOG} = 0 V		Room	-	16	-	

SPECIFICATIONS for Dual Supplies

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [e]	TEMP. [a]	D SUFFIX -40 °C TO 85 °C			UNIT
				MIN. [b]	TYP. [c]	MAX. [b]	
Power Supplies							
Positive Supply Current	I+		Room	-	0.001	1	
			Full	-	-	5	
Negative Supply Current	I-	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 V or 5 V	Room	-1	-0.0001	-	
			Full	-5	-	-	µA
Logic Supply Current	I_L		Room	-	0.001	1	
			Full	-	0.001	5	
Ground Current	I_{GND}		Room	-1	-0.001	-	
			Full	-5	-0.001	-	

SPECIFICATIONS for Unipolar Supplies

| PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [e]	TEMP. [a]	LIMITS -40 °C °C TO 85 °C			UNIT
				MIN. [b]	TYP. [c]	MAX. [b]	
Analog Switch							
Analog Signal Range [d]	V_{ANALOG}		Full	0	-	12	V
Drain-Source On-Resistance [d]	$R_{DS(on)}$	I_S = -10 mA, V_D = 3 V, 8 V V+ = 10.8 V, V_L = 5.25 V	Room	-	100	160	Ω
			Full	-	-	200	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V See Figure 2	Room	-	300	450	ns
Turn-Off Time	t_{OFF}		Room	-	60	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	-	2	-	pC
Power Supplies							
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 V or 5 V	Room	-	0.001	1	
			Full	-	-	5	
Negative Supply Current	I-	V_{IN} = 0 V or 5 V	Room	-1	-0.0001	-	
			Full	-5	-	-	µA
Logic Supply Current	I_L	V_L = 5.25 V, V_{IN} = 0 V or 5 V	Room	-	0.001	1	
			Full	-	-	5	
Ground Current	I_{GND}	V_{IN} = 0 V or 5 V	Room	-1	-0.001	-	
			Full	-5	-	-	

Notes

a. Room = 25 °C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
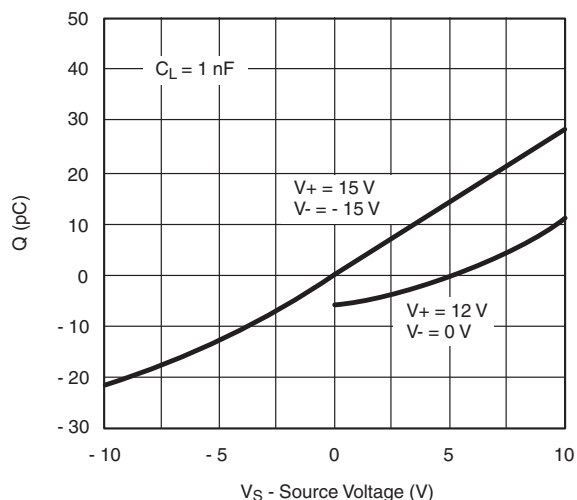
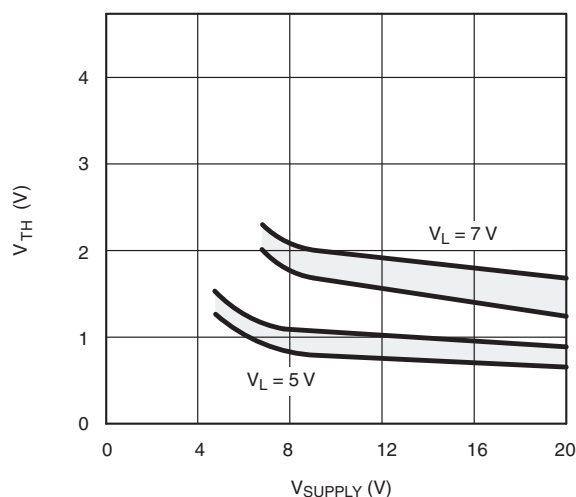## TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)
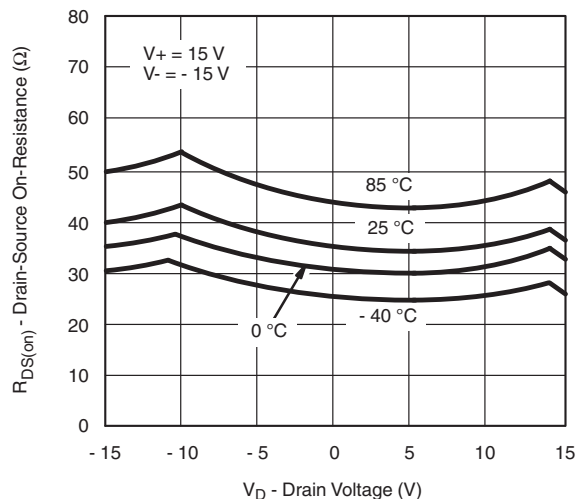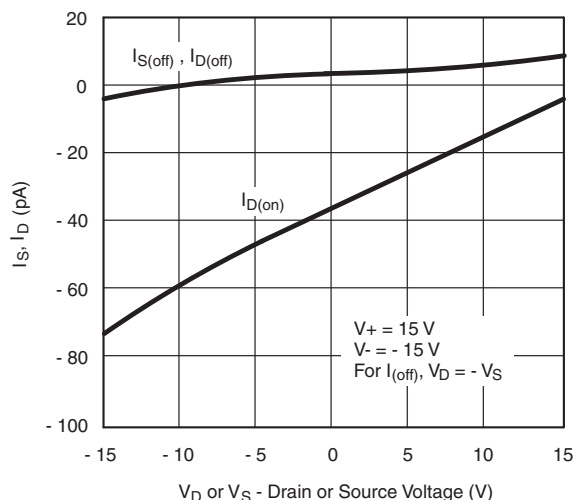

$R_{DS(on)}$ vs. V_D and Temperature
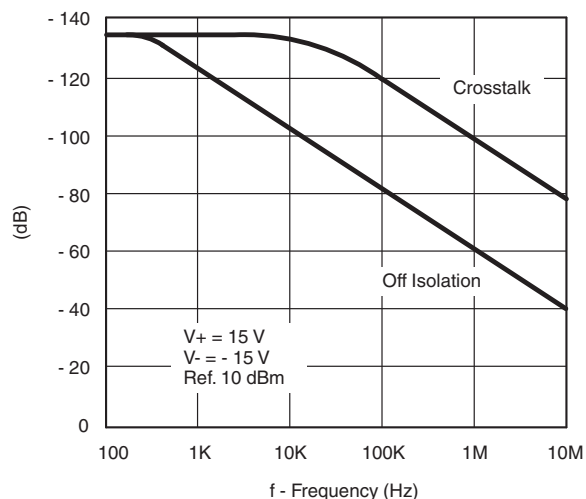
Crosstalk and Off Isolation vs. Frequency
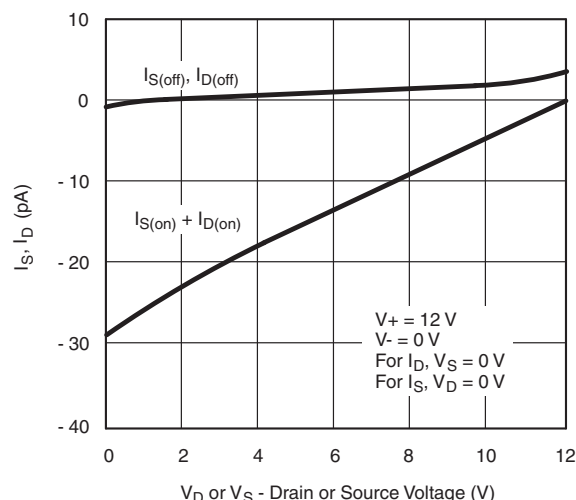

Charge Injection vs. Source Voltage

Switching Threshold vs. Supply Voltage

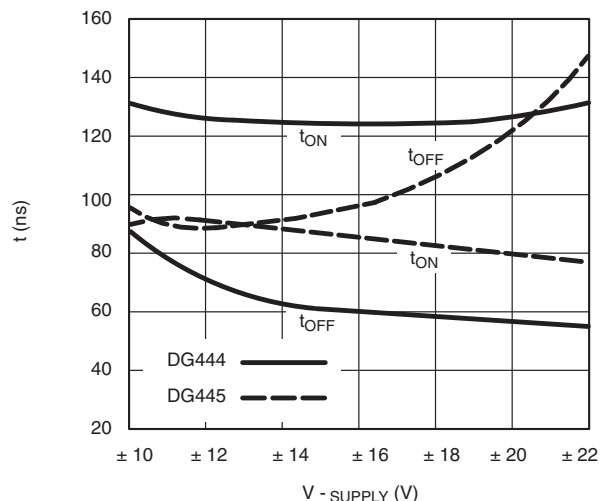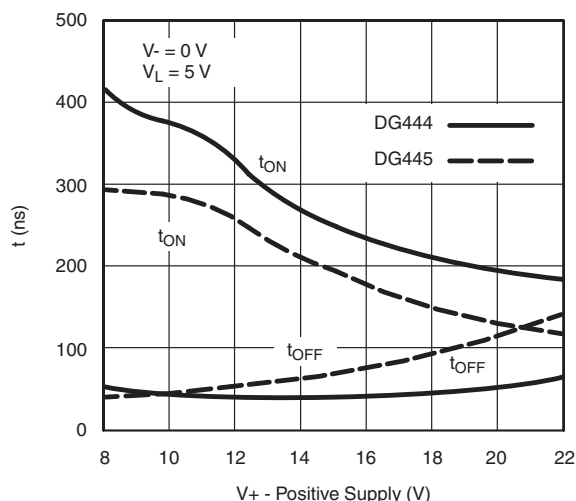Source/Drain Leakage Currents
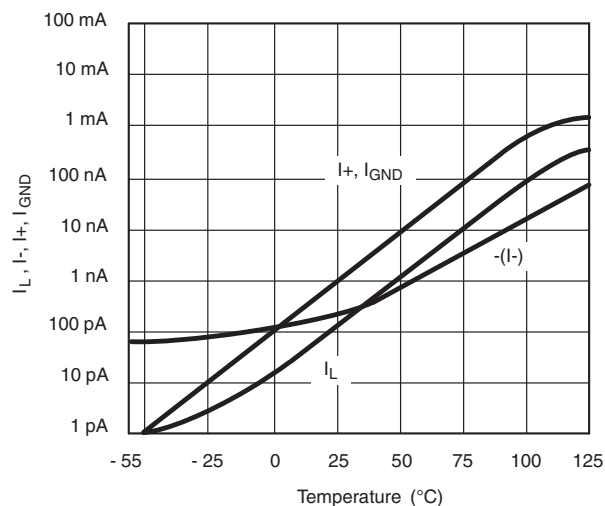

Source/Drain Leakage Currents (Single 12-V Supply)

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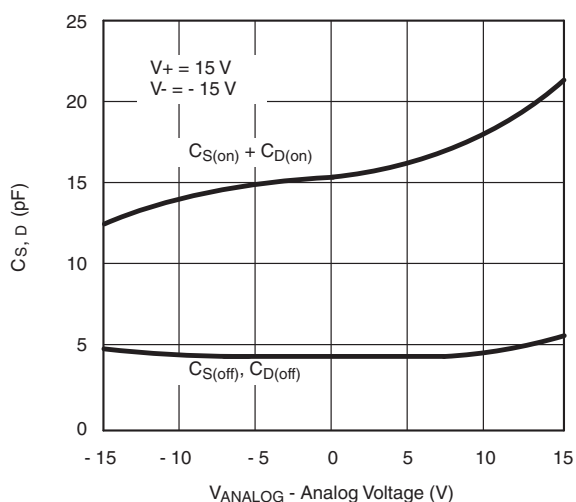## TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)
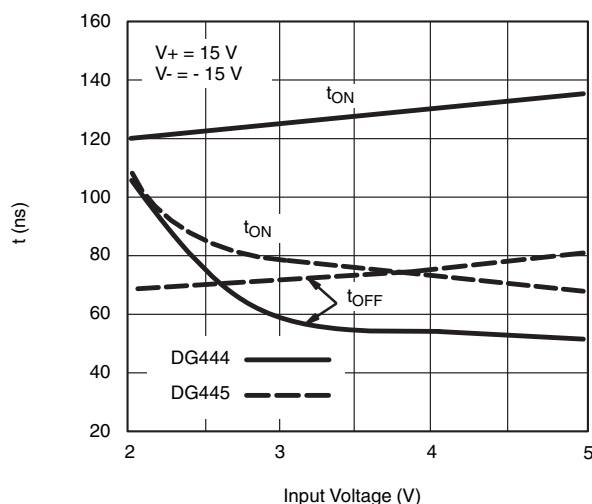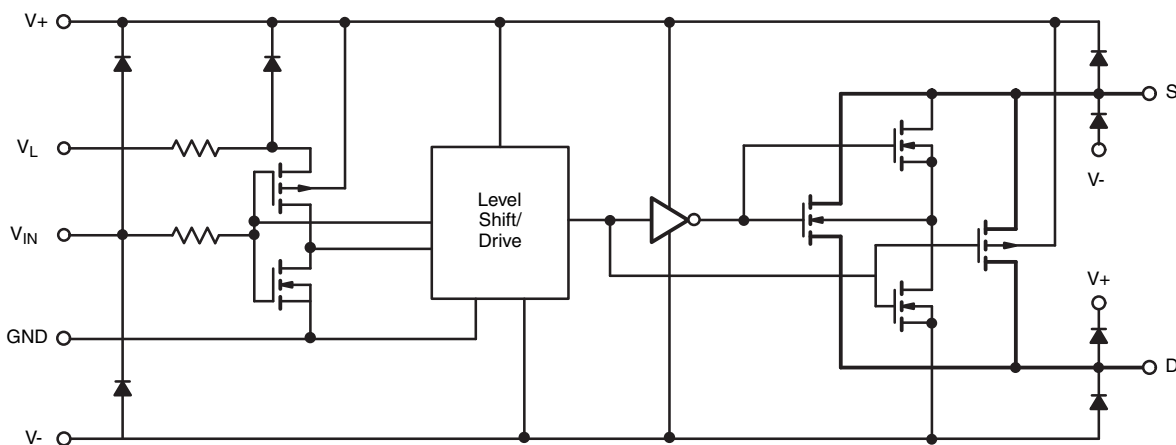

Switching Time vs. Power Supply Voltage

Switching Times vs. Power Supply Voltage
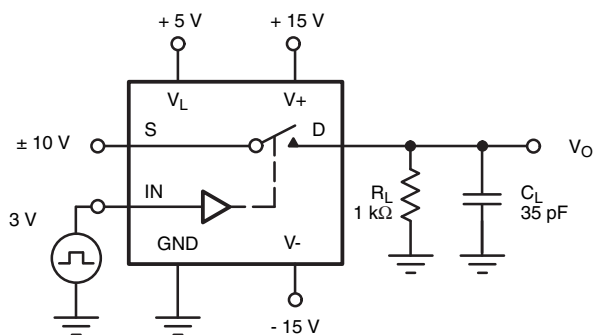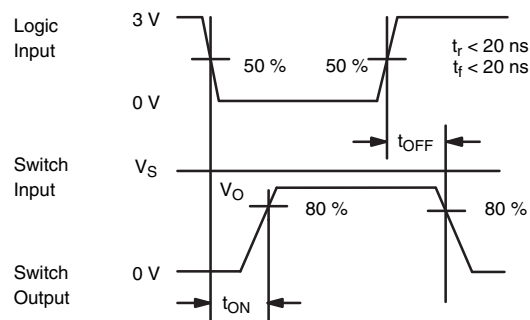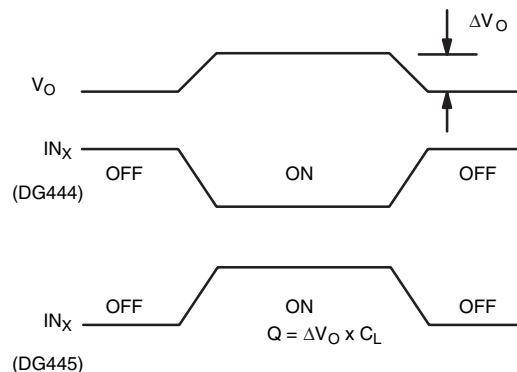

Supply Current vs. Temperature
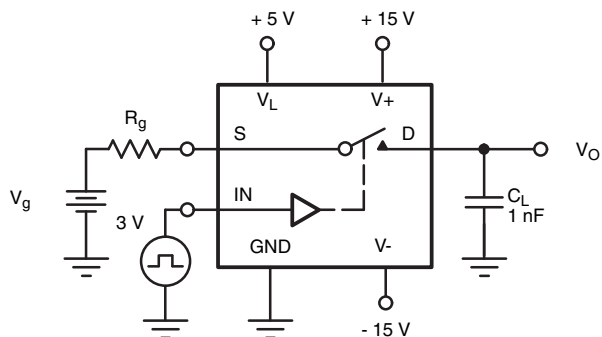

Source/Drain Capacitance vs. Analog Voltage

Switching Time vs. Input Voltage

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SCHEMATIC DIAGRAM TYPICAL CHANNEL

Fig. 1

TEST CIRCUITS

C_L (includes fixture and stray capacitance)

Note: Logic input waveform is inverted for DG445.

Fig. 2 - Switching Time

$Q = \Delta V_O \times C_L$

Fig. 3 - Charge Injection

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TEST CIRCUITS

C = 1 mF tantalum in parallel with 0.01 mF ceramic

$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Fig. 4 - Crosstalk
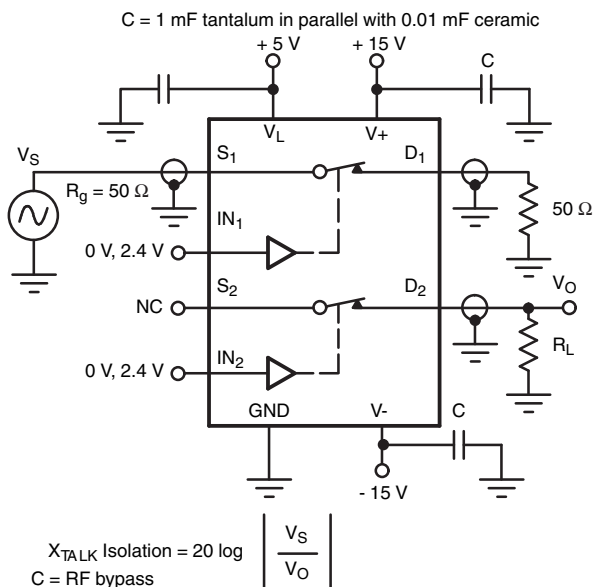
$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$
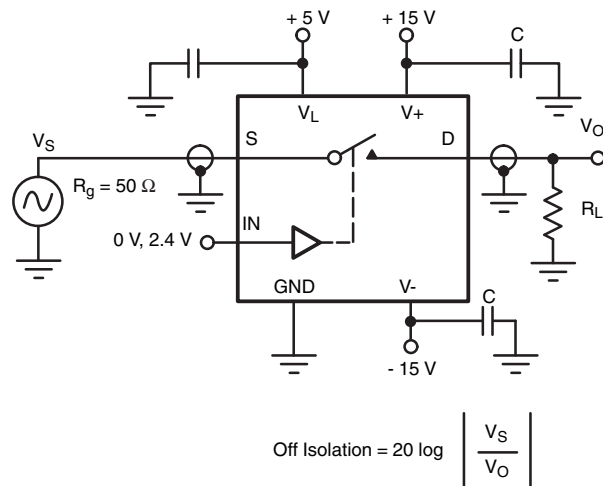
Fig. 5 - Off Isolation
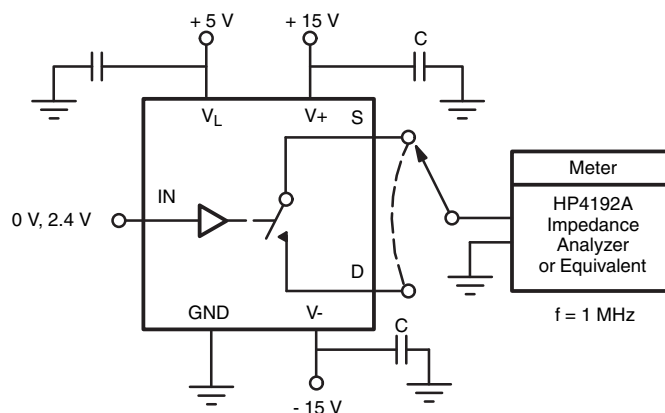
Fig. 6 - Source/Drain Capacitances

APPLICATIONS

Fig. 7 - Level Shifter

7

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APPLICATIONS

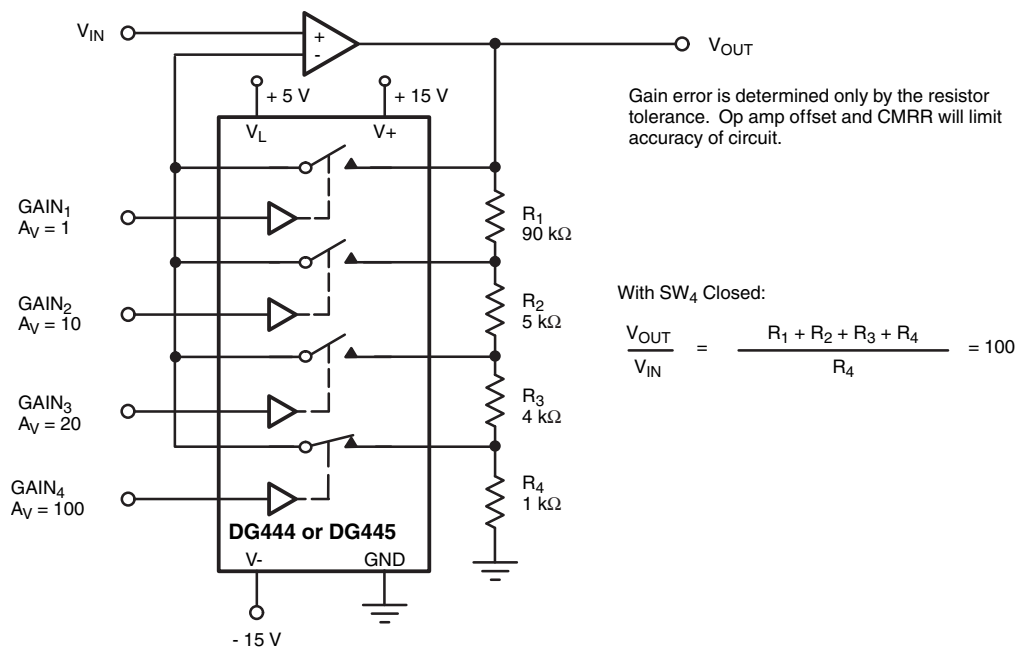Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW_4 Closed:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

Fig. 8 - Precision-Weighted Resistor Programmable-Gain Amplifier
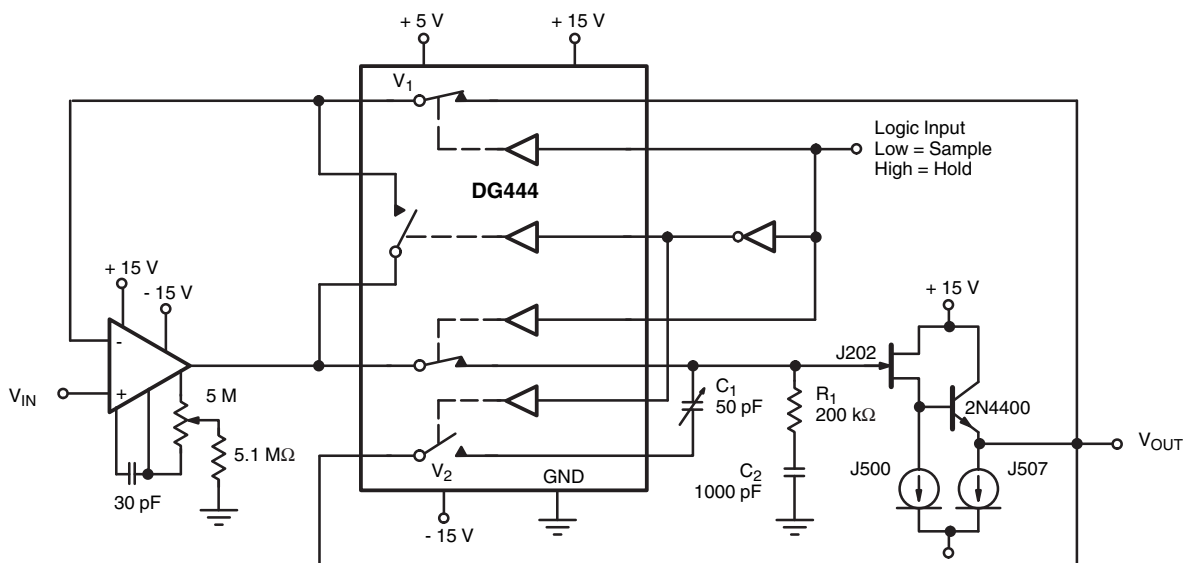
Fig. 9 - Precision Sample-and-Hold

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SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012
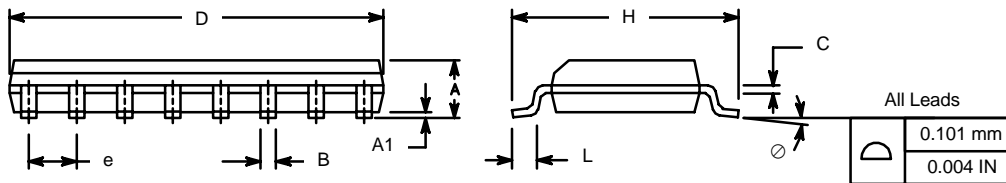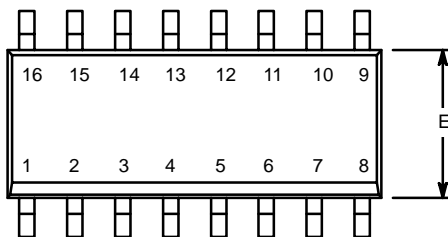
Dim	MILLIMETERS		INCHES	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A$_1$	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
$\oslash$	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

All Leads	
0.101 mm	
0.004 IN	

PDIP: 16-LEAD
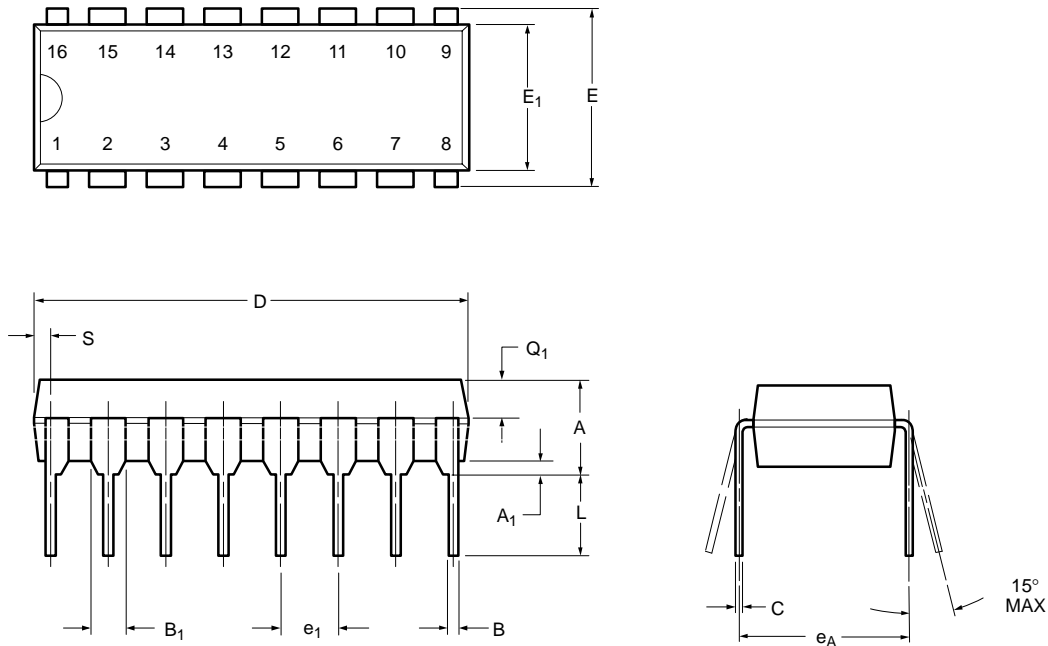
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

RECOMMENDED MINIMUM PADS FOR SO-16

0.372
(9.449)

0.047
(1.194)

0.246
(6.248)

0.152
(3.861)

0.022
(0.559)

0.050
(1.270)

0.028
(0.711)
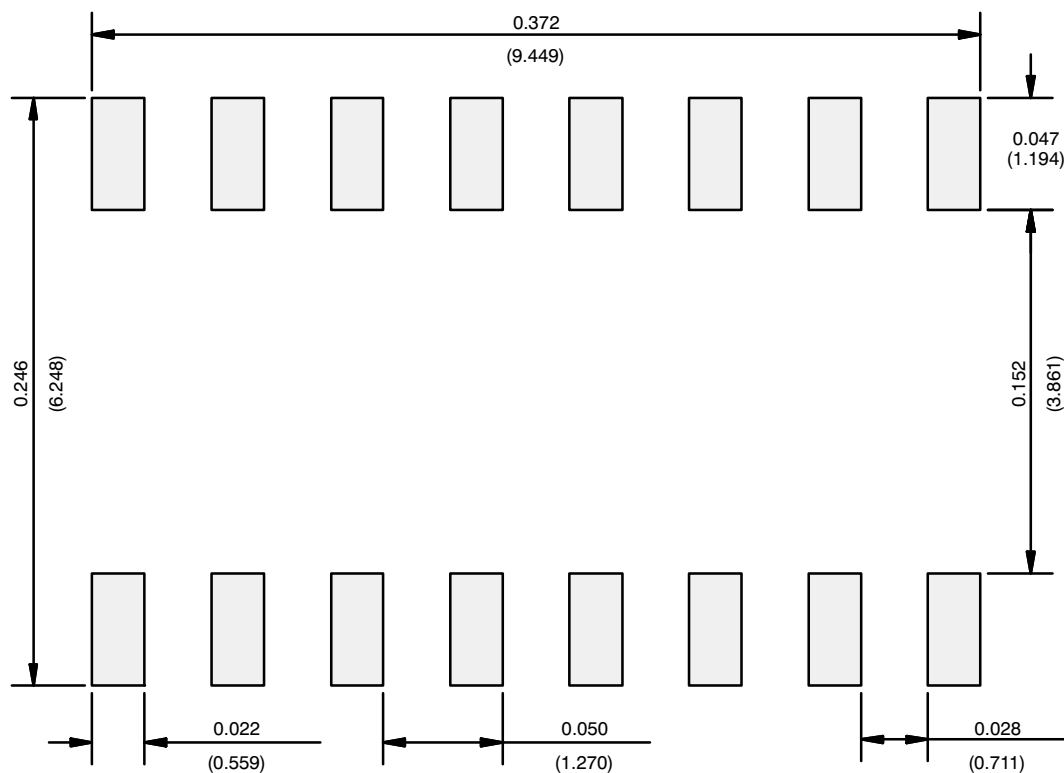
Recommended Minimum Pads
Dimensions in Inches/(mm)

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