Logic Block Diagram

Pin Configuration

TQFP
Top View

Selection Guide

	7C48X1-10	7C48X1-15	7C48X1-25	7C48X1-35
Maximum Frequency (MHz)	100	66.7	40	28.6
Maximum Access Time (ns)	8	10	15	20
Minimum Cycle Time (ns)	10	15	25	35
Minimum Data or Enable Set-Up (ns)	3	4	6	7
Minimum Data or Enable Hold (ns)	0.5	1	1	2
Maximum Flag Delay (ns)	8	10	15	20
Active Power Supply Current (I_{CC1}) (mA) — Commercial	60	60	60	60
Active Power Supply Current (I_{CC1}) (mA) — Industrial	70	70	70	70

	CY7C4801	CY7C4811	CY7C4821	CY7C4831	CY7C4841	CY7C4851
Density	Double 256 x 9	Double 512 x 9	Double 1K x 9	Double 2K x 9	Double 4K x 9	Double 8K x 9
Package	64-pin TQFP	64-pin TQFP	64-pin TQFP	64-pin TQFP	64-pin TQFP	64-pin TQFP

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied..−55°C to +125°C

Supply Voltage to Ground Potential ....−0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State ....−0.5V to +7.0V

DC Input Voltage ....−0.5V to +7.0V

Output Current into Outputs (LOW) ....20 mA

Static Discharge Voltage.. >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current... >200 mA

Operating Range[1]

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%

Notes:
1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
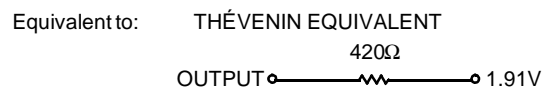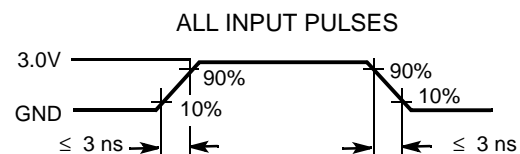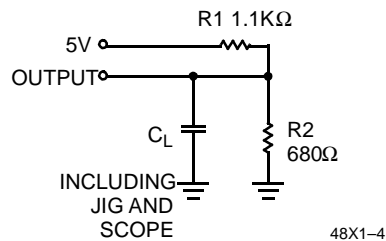2. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	Description	I/O	Description
DA$_{0-8}$	Data Inputs	I	Data Inputs for 9-bit bus
DB$_{0-8}$	Data Inputs	I	Data Inputs for 9-bit bus
QA$_{0-8}$	Data Outputs	O	Data Outputs for 9-bit bus
QB$_{0-8}$	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{\text{WENA1}}$ $\overline{\text{WENB1}}$	Write Enable 1	I	WENA1 and WENB1 become the only write enables when the device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when (WENA1,WENB1) is LOW and (FFA,FFB) is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when (WENA1,WENB1) is LOW and (WENA2/LDA,WENB2/LDB) and (FFA,FFB) are HIGH.
WENA2/$\overline{\text{LDA}}$ WENB2/$\overline{\text{LDB}}$ Dual Mode Pin	Write Enable 2	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. (WENA1,WENB1) must be LOW and (WENA2/LDA,WENB2/LDB) must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the (FFA,FFB) is LOW. If the FIFO is configured to have programmable flags, (WENA2/LDA,WENB2/LDB) is held LOW to write or read the program-mable flag offsets.
	Load	I	
$\overline{\text{RENA1}}$ $\overline{\text{RENA2}}$ $\overline{\text{RENB1}}$ $\overline{\text{RENB2}}$	Read Enable Inputs	I	Enables the device for Read operation.
WCLKA WCKLB	Write Clock	I	The rising edge clocks data into the FIFO when (WENA1,WENB1) is LOW and (WENA2/LDA,WENB2/LDB) is HIGH and the FIFO is not Full. When (WENA2/LDA,WENB2/LDB) is asserted, WCLK writes data into the programmable flag-offset register.
RCLKA RCLKB	Read Clock	I	The rising edge clocks data out of the FIFO when (RENA1,RENB1) and (RENA2,RENB2) are LOW and the FIFO is not Empty. When (WENA2/LDA,WENB2/LDB) is LOW, (RCLKA,RCLKB) reads data out of the programmable flag-offset register.
$\overline{\text{EFA}}$,$\overline{\text{EFB}}$	Empty Flag	O	When (EFA,EFB) is LOW, the FIFO is empty. (EFA,EFB) is synchronized to (RCLKA,RCLKB).
$\overline{\text{FFA}}$,$\overline{\text{FFB}}$	Full Flag	O	When (FFA,FFB) is LOW, the FIFO is full. (FFA,FFB) is synchronized to (WCLKA,WCLKB).
$\overline{\text{PAEA}}$ $\overline{\text{PAEB}}$	Programmable Almost Empty	O	When (PAEA,PAEB) is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. PAE is synchronized to RCLK.
$\overline{\text{PAFA}}$ $\overline{\text{PAFB}}$	Programmable Almost Full	O	When (PAFA,PAFB) is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. PAF is synchronized to WCLK.
$\overline{\text{RSA}}$ $\overline{\text{RSB}}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{\text{OEA}}$ $\overline{\text{OEB}}$	Output Enable	I	When (OEA,OEB) is LOW, the FIFO's data outputs drive the bus to which they are connected. If (OEA,OEB) is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

[+] Feedback

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C48X1-10 Min.	7C48X1-10 Max.	7C48X1-15 Min.	7C48X1-15 Max.	7C48X1-25 Min.	7C48X1-25 Max.	7C48X1-35 Min.	7C48X1-35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $I_{OH} = -2.0$ mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $I_{OL} = 8.0$ mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC1}[5]	Active Power Supply Current		Com'l		60		60		60		60	mA
			Ind		70		70		70		70	mA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7, 8]

R1 1.1KΩ
5V
OUTPUT
C_L
R2 680Ω
INCLUDING JIG AND SCOPE
48X1–4

ALL INPUT PULSES
3.0V
90%
GND
10%
90%
10%
≤ 3 ns
≤ 3 ns
48X1–5

Equivalent to: THÉVENIN EQUIVALENT
420Ω
OUTPUT
1.91V

Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. Test no more than one output at a time for not more than one second.
5. Outputs open. Tested at Frequency = 20 MHz.
6. Tested initially and after any design or process changes that may affect these parameters.
7. C_L = 30 pF for all AC parameters except for t_{OHZ}.
8. C_L = 5 pF for t_{OHZ}.

**Switching Characteristics** Over the Operating Range

| Parameter	Description	7C48X1-10 Min.	7C48X1-10 Max.	7C48X1-15 Min.	7C48X1-15 Max.	7C48X1-25 Min.	7C48X1-25 Max.	7C48X1-35 Min.	7C48X1-35 Max.	Unit
f_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3.5		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3.5		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[9]	10		15		25		35		ns
t_{RSS}	Reset Set-Up Time	8		10		15		20		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{OLZ}	Output Enable to Output in Low Z[10]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[10]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	15		15		18		20		ns

Notes:
9. Pulse widths less than minimum values are not allowed.
10. Values guaranteed by design, not currently tested.

## Switching Waveforms

Write Cycle Timing

48X1–6

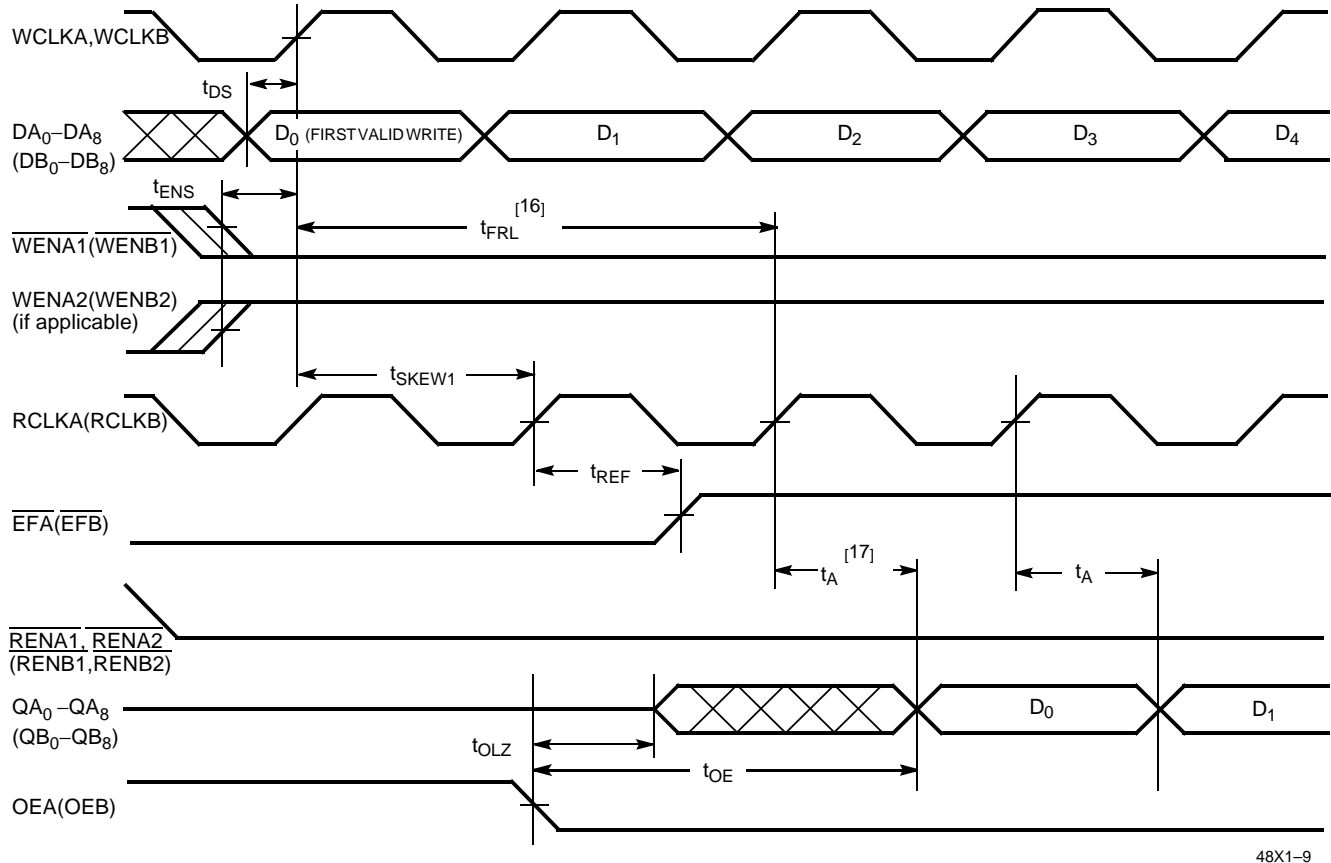### Read Cycle Timing

48X1–7
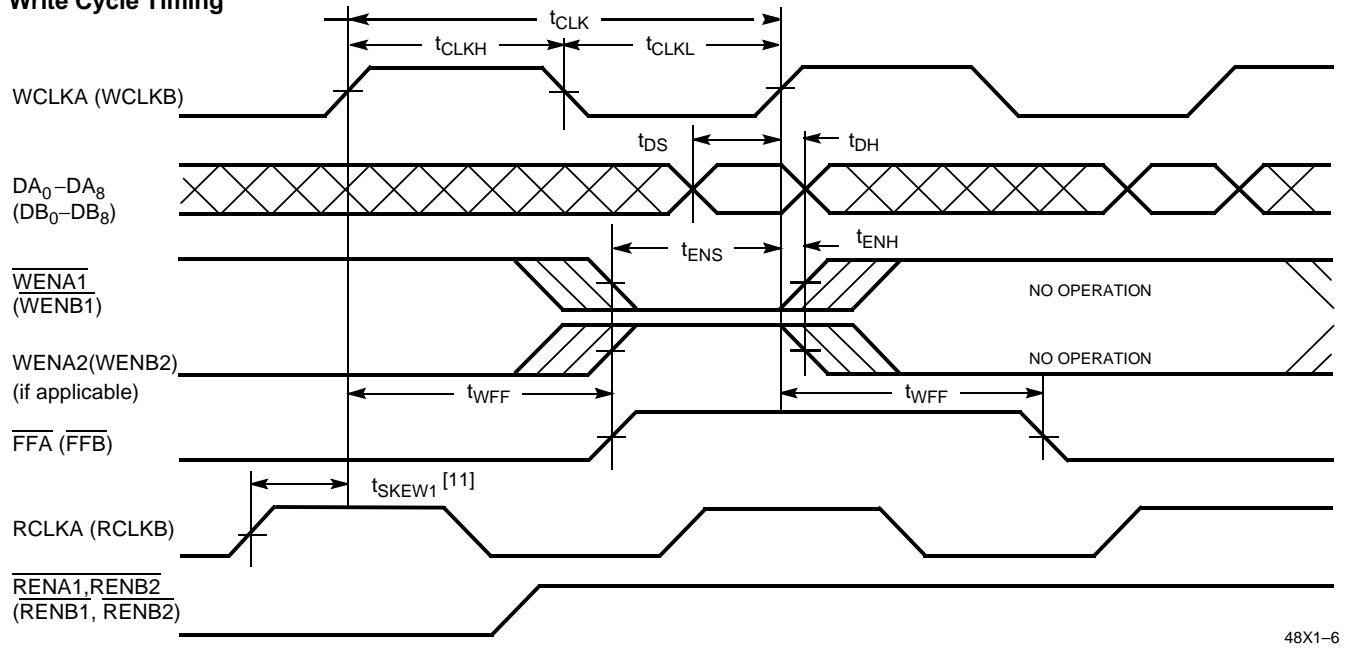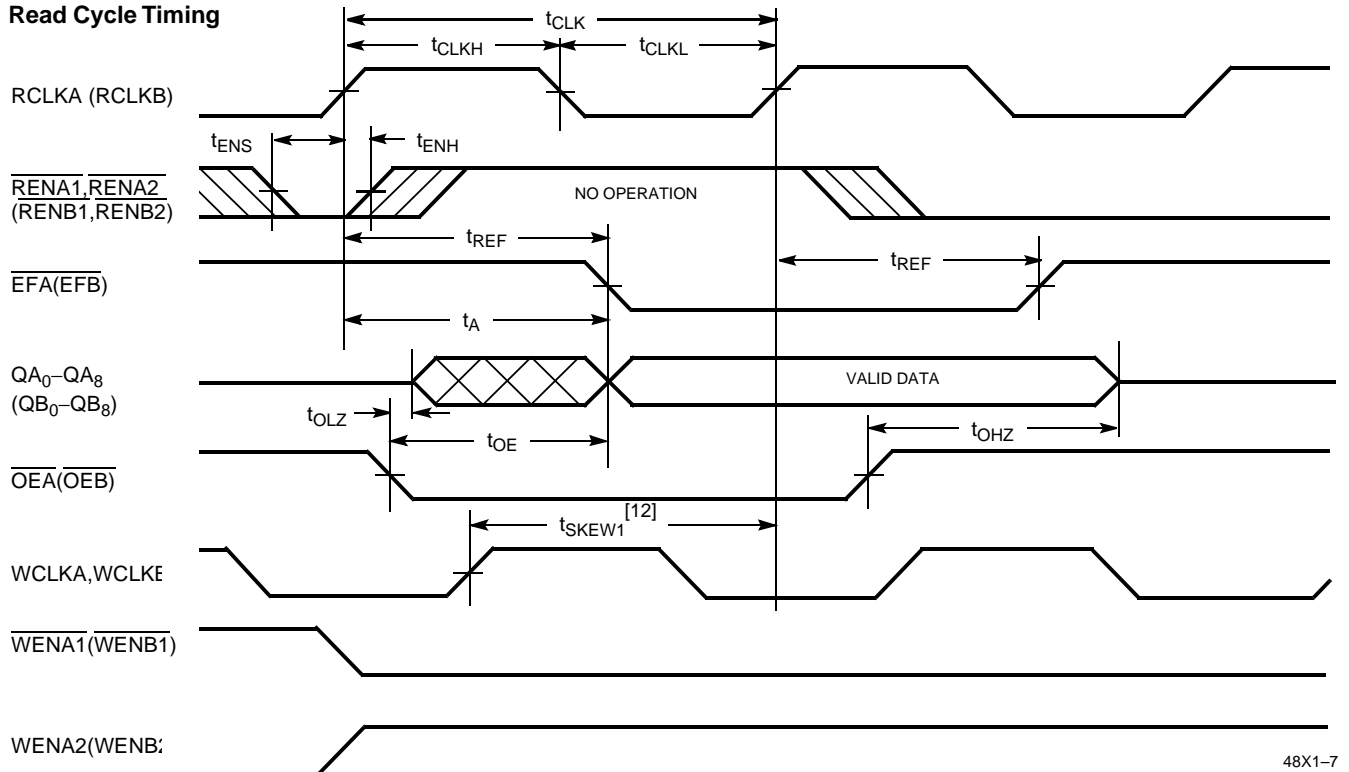
Notes:
11. t_{SKEW1} is the minimum time between a rising (RCLKA,RCLKB) edge and a rising (WCLKA,WCLKB) edge to guarantee that ($\overline{FFA}$,$\overline{FFB}$) will go HIGH during the current clock cycle. If the time between the rising edge of (RCLKA,RCLKB) and the rising edge of (WCLKA,WCLKB) is less than t_{SKEW1}, then ($\overline{FFA}$,$\overline{FFB}$) may not change state until the next (WCLKA,WCLKB) rising edge.
12. t_{SKEW1} is the minimum time between a rising (WCLKA,WCLKB) edge and a rising (RCLKA,RCLKB) edge to guarantee that ($\overline{EFA}$,$\overline{EFB}$) will go HIGH during the current clock cycle. It the time between the rising edge of (WCLKA,WCLKB) and the rising edge of RCLK is less than t_{SKEW1}, then ($\overline{EFA}$,$\overline{EFB}$) may not change state until the next (RCLKA,RCLKB) rising edge.

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[+] Feedback

Switching Waveforms (continued)

Reset Timing[13]
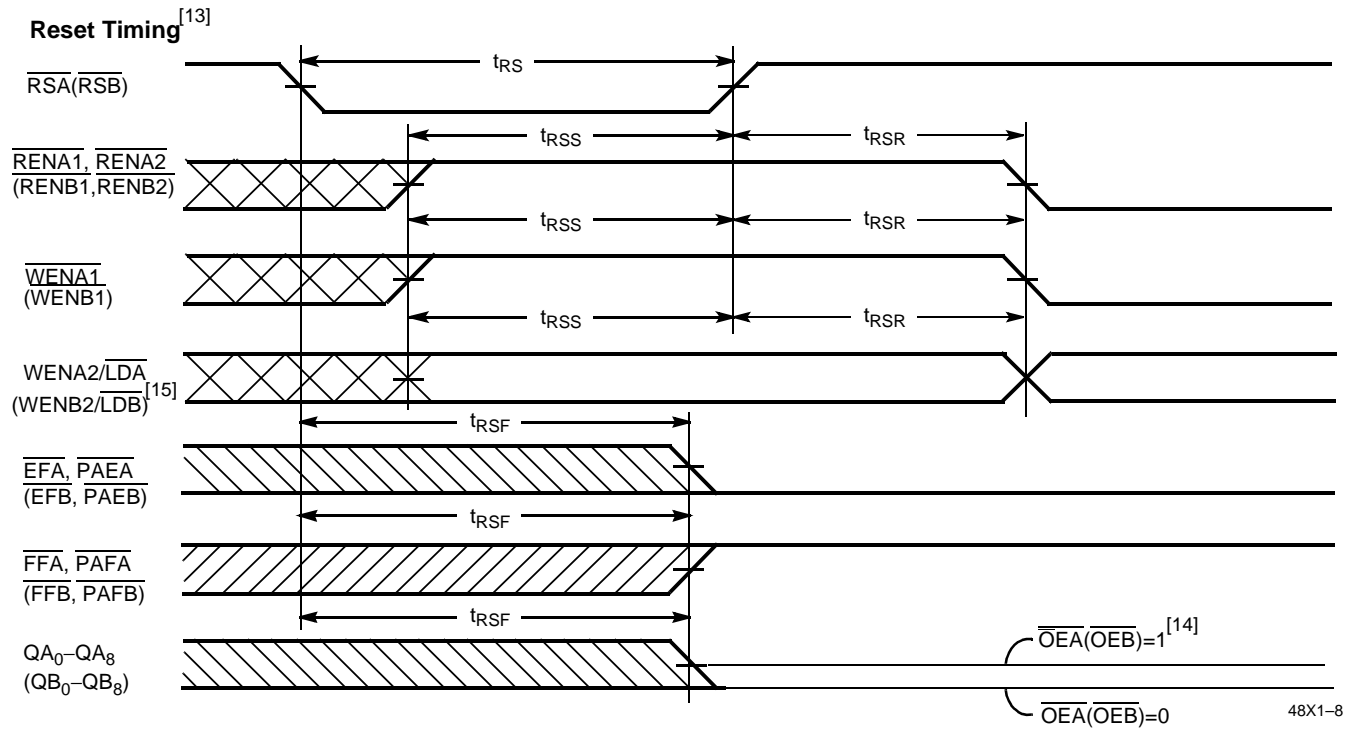
Notes:
13. The clocks (RCLKA,RCLKB, WCLKA,WCLKB) can be free-running during reset.
14. After reset, the outputs will be LOW if (OEA,OEB) = 0 and three-state if (OEA,OEB)=1.
15. Holding (WENA2/LDA,WENB2/LDB) HIGH during reset will make the pin act as a second enable pin. Holding(WENA2/LDA,WENB2/LDB) LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

[+] Feedback

Switching Waveforms (continued)

### First Data Word Latency after Reset with Simultaneous Read and Write

WCLKA, WCLKB

t_{DS}

DA_0–DA_8
$(DB_0$–$DB_8)$ — D_0 (FIRST VALID WRITE) D_1 D_2 D_3 D_4

t_{ENS}

$\overline{WENA1}(\overline{WENB1})$

t_{FRL} [16]

WENA2(WENB2)
(if applicable)

t_{SKEW1}

RCLKA(RCLKB)

t_{REF}

$\overline{EFA}(\overline{EFB})$

t_A [17] t_A

$\overline{RENA1}, \overline{RENA2}$
$(\overline{RENB1}, \overline{RENB2})$

QA_0–QA_8
$(QB_0$–$QB_8)$ — D_0 D_1

t_{OLZ}

t_{OE}

OEA(OEB)

48X1–9

Notes:
16. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW1}$. When $t_{SKEW1} <$ minimum specification, t_{FRL} (maximum) = either $2 \ast t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary (EFA, EFB= LOW).
17. The first word is available the cycle after (EFA, EFB) goes HIGH, always.

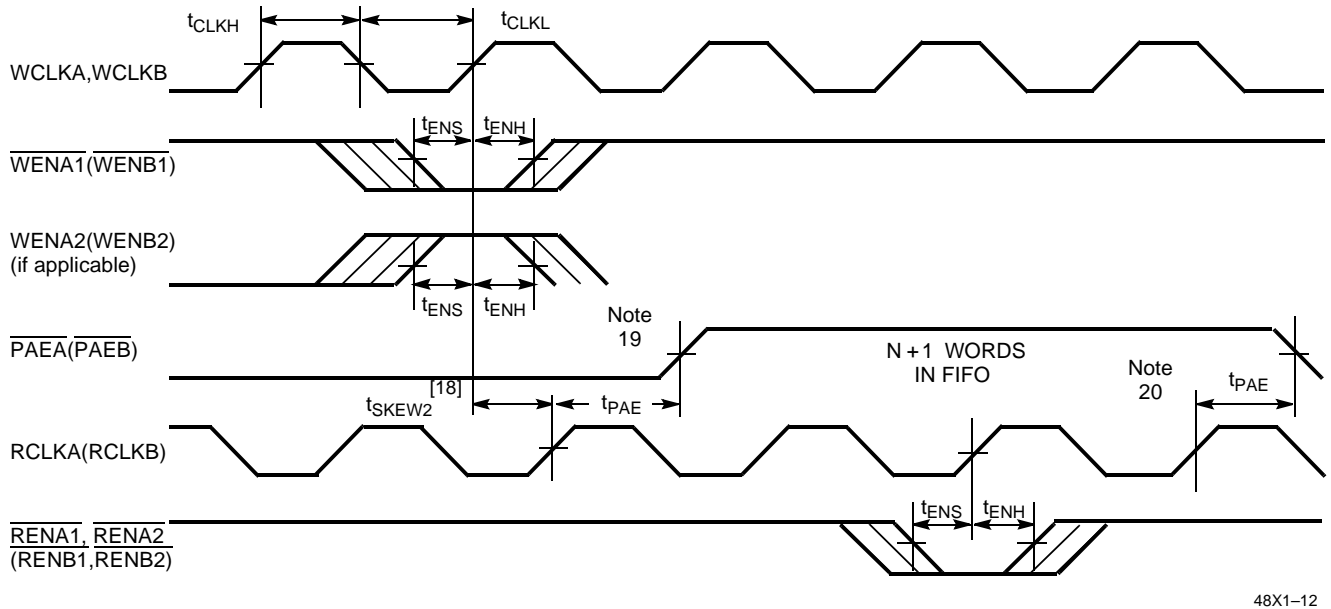## Switching Waveforms (continued)

Empty Flag Timing

48X1–10

[+] Feedback
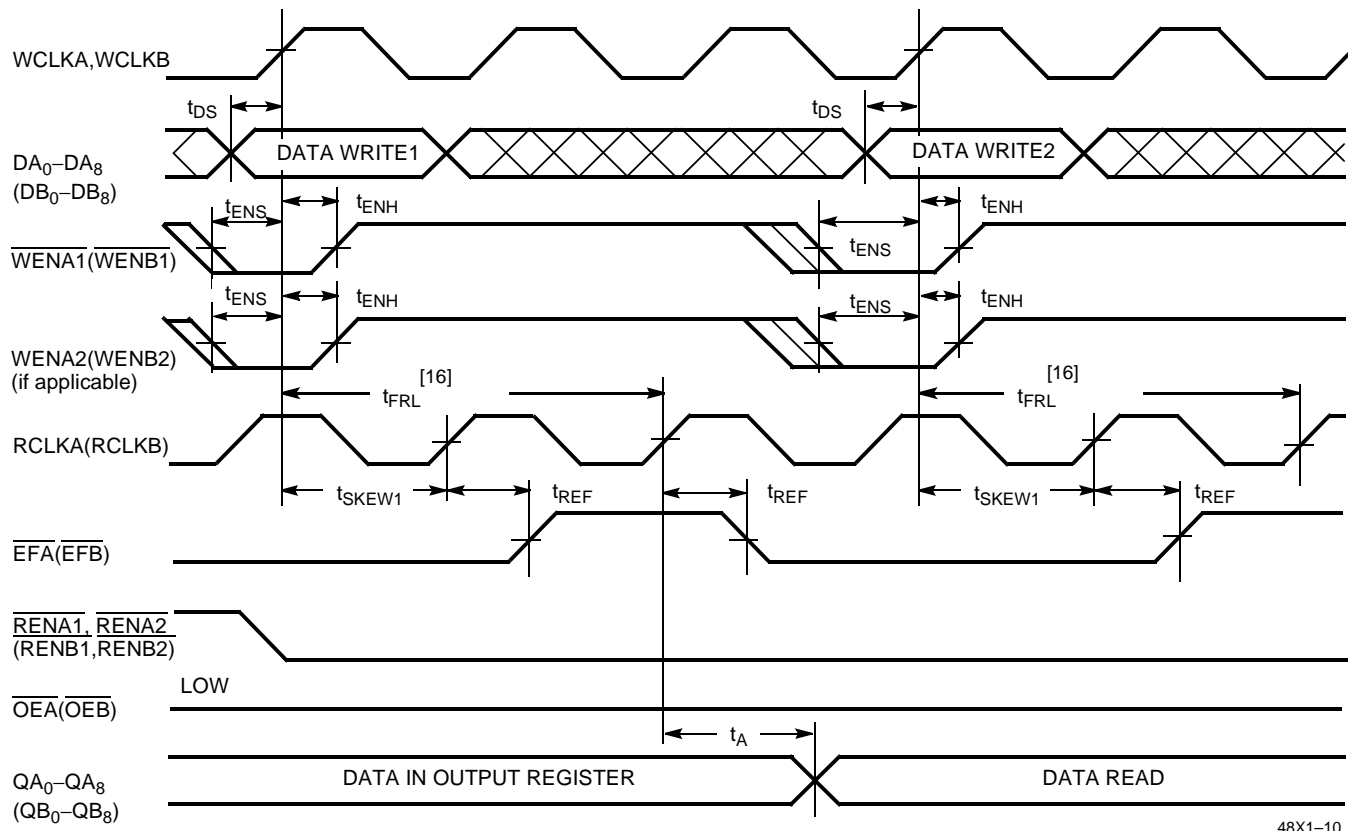
Switching Waveforms (continued)

Full Flag Timing
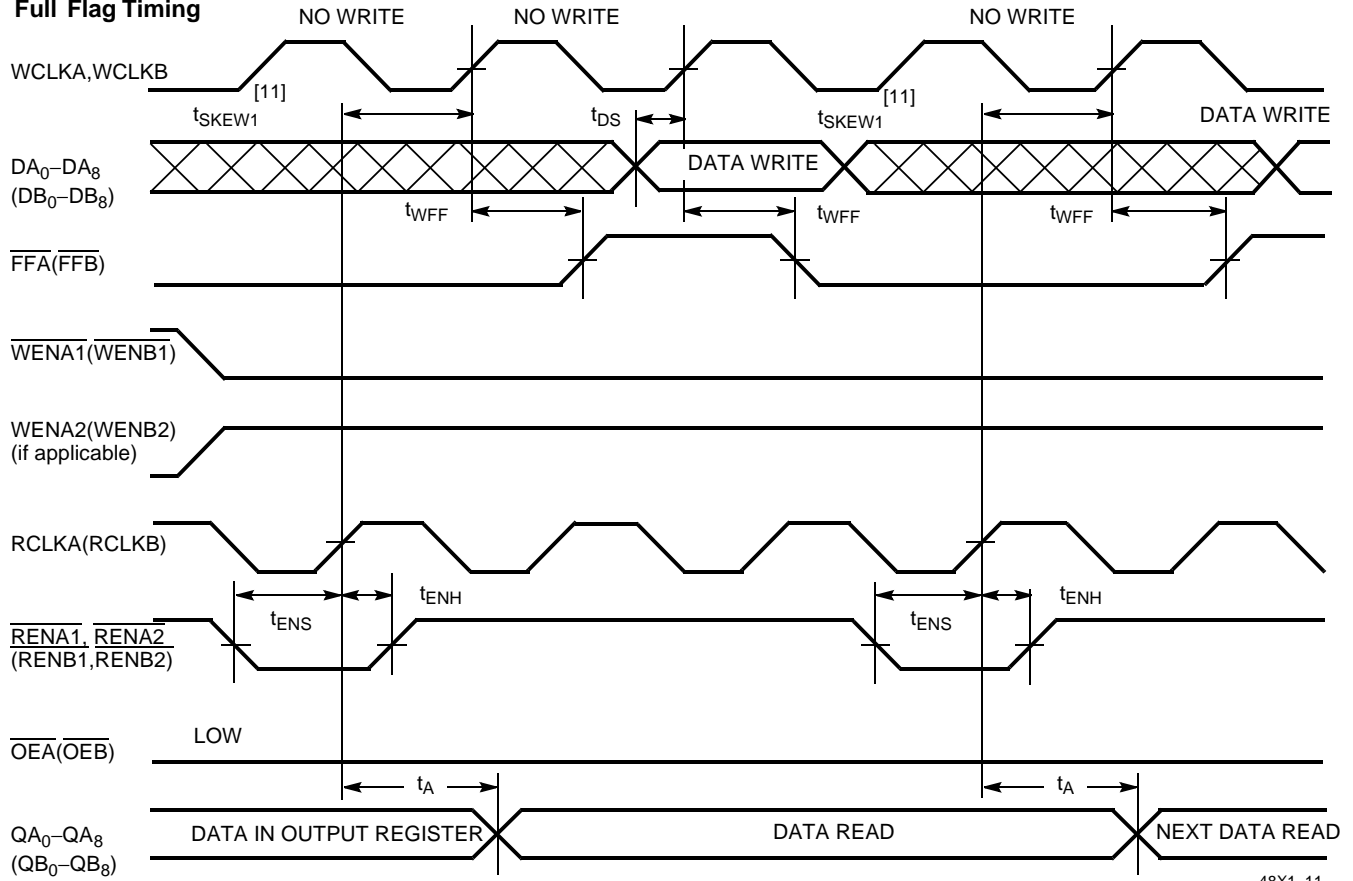
48X1–11

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing

t_{CLKH} t_{CLKL}

WCLKA,WCLKB

t_{ENS} t_{ENH}

$\overline{WENA1}(\overline{WENB1})$

WENA2(WENB2)
(if applicable)

t_{ENS} t_{ENH}

$\overline{PAEA}(\overline{PAEB})$ Note 19   N + 1 WORDS IN FIFO   Note 20 t_{PAE}

[18] t_{SKEW2} t_{PAE}

RCLKA(RCLKB)

t_{ENS} t_{ENH}

$\overline{RENA1}, \overline{RENA2}$
$(\overline{RENB1},\overline{RENB2})$

48X1–12

Programmable Almost Full Flag Timing

t_{CLKH} t_{CLKL} Note 21

WCLKA,WCLKB

t_{ENS} t_{ENH}

$\overline{WENA1}(\overline{WENB1})$

WENA2(WENB2)
(if applicable)   Note 22

t_{ENS} t_{ENH} t_{PAF}

$\overline{PAFA}(\overline{PAFB})$ FULL– M+1 WORDS IN FIFO   FULL– M WORDS IN FIFO [23]

t_{SKEW2} [24] t_{PAF}

RCLKA(RCLKB)

t_{ENS} t_{ENS} t_{ENH}

$\overline{RENA1}, \overline{RENA2}$
$(\overline{RENB1},\overline{RENB2})$

48X1–13
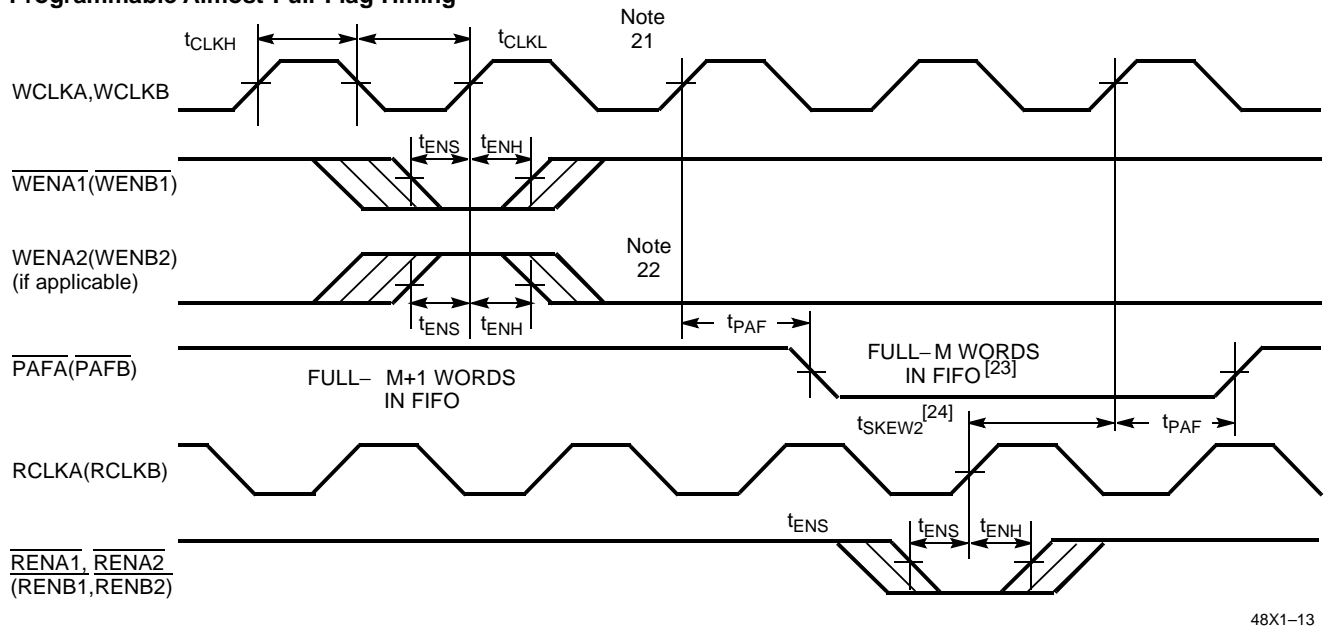
Notes:
18. t_{SKEW2} is the minimum time between a rising (WCLKA,WCLKB) and a rising (RCLKA,RCLKB) edge for ($\overline{PAEA}$,$\overline{PAEB}$) to change state during that clock cycle. If the time between the edge of (WCLKA,WCLKB) and the rising (RCLKA,RCLKB) is less than t_{SKEW2}, then (PAEA,PAEB) may not change state until the next RCLK.
19. (PAEA,PAEB) offset = n.
20. If a read is preformed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when ($\overline{PAEA}$,$\overline{PAFB}$) goes LOW.
21. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words of the FIFO when (PAFA,PAFB) goes LOW.
22. (PAFA,PAFB) offset = m.
23. 256-m words in FIFO for CY7C4801, 512-m words for CY7C4811, 1024-m words for CY7C4821, 2048-m words for CY7C4831, 4096-m words for CY7C4841, 8192-m words for CY7C4851.
24. t_{SKEW2} is the minimum time between a rising (RCLKA,RCLKB) edge and a rising (WCLKA,WCLKB) edge for ($\overline{PAFA}$,$\overline{PAFB}$) to change during that clock cycle. If the time between the rising edge of (RCLKA,RCLKB) and the rising edge of (WCLKA,WCLKB) is less than t_{SKEW2}, then (PAFA,PAFB) may not change state until the next (WCLKA,WCLKB).
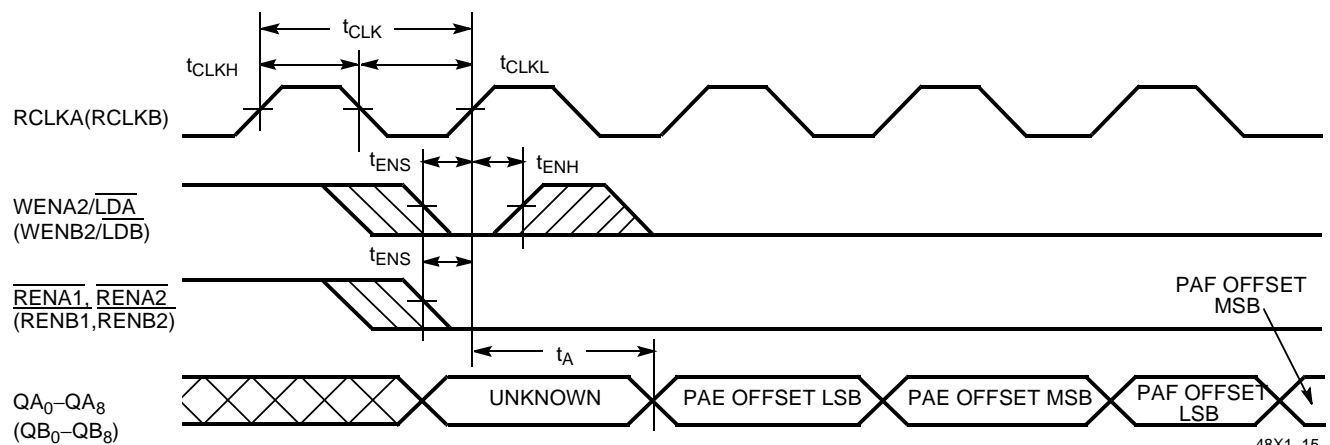
[+] Feedback

Switching Waveforms (continued)

Write Programmable Registers
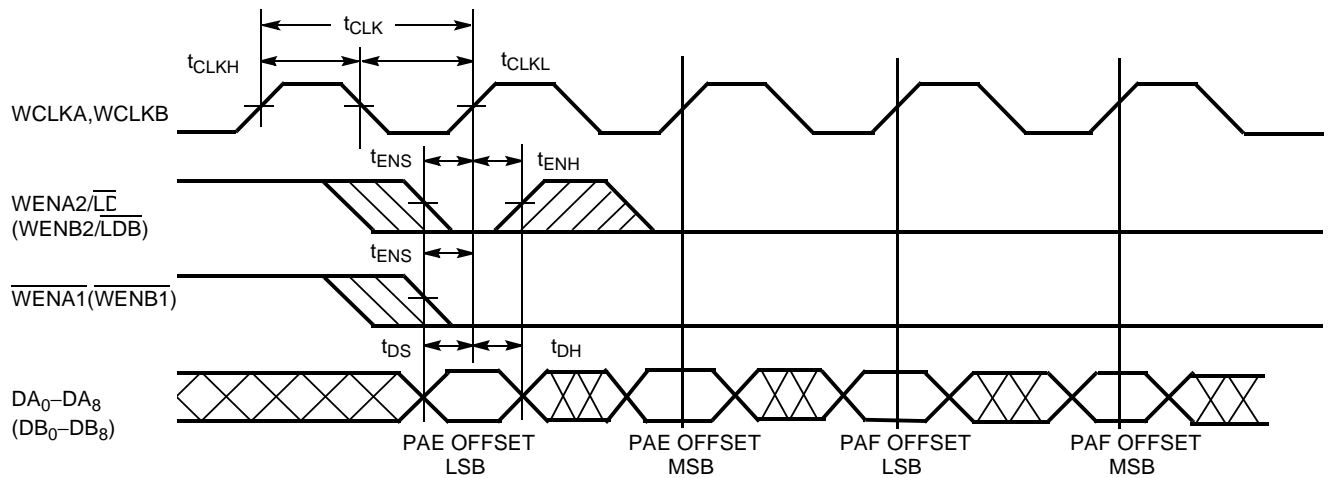
48X1–14

Read Programmable Registers

48X1–15

Architecture

The CY7C48X1 functions as two independent FIFOs in a single package, each with its own separate set of controls. The device consists of two arrays of 256 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), two read pointers, two write pointers, control signals (RCLKA, RCLKB, WCLKA, WCLKB, RENA1, RENB1, RENA2, RENB2, WENA1, WENB1, WENA2, WENB2, RSA, RSB), and flags (EFA,EFB, PAEA,PAEB, PAFA,PAFB, FFA,FFB).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset (RSA, RSB) cycle. This causes the FIFO to enter the Empty condition signified by (EFA,EFB) being LOW. All data outputs (QA$_{0-8}$,QB$_{0-8}$) go LOW t$_{RSF}$ after the rising edge of RSA, RSB. In order for the FIFO to reset to its default state, a falling edge must occur on (RSA,RSB) and the user must not read or write while (RSA,RSB) is LOW. All flags are guaranteed to be valid t$_{RSF}$ after (RSA,RSB) is taken LOW.

FIFO Operation

When the (WENA1,WENB1) signal is active LOW and (WENA2,WENB2) is active HIGH, data present on the (DA$_{0-8}$, DB$_{0-8}$) pins is written into the FIFO on each rising edge (WCLKA,WCLKB) of the (WCLKA,WCLKB) signal. Similarly, when the (RENA1,RENB1) and (RENA2,RENB2) signals are active LOW, data in the FIFO memory will be presented on the (QA$_{0-8}$,QB$_{0-8}$) outputs. New data will be presented on each rising edge of (RCLKA,RCLKB) while (RENA1,RENB1) and (RENA2,RENB2) are active. (RENA1,RENB1) and (RENA2,RENB2) must set up t$_{ENS}$ before (RCLKA,RCLKB) for it to be a valid read function. (WENA1,WENB1) and (WENA2,WENB2) must occur t$_{ENS}$ before (WCLKA,WCLKB) for it to be a valid write function.

An output enable (OEA,OEB) pin is provided to three-state the (QA$_{0-8}$,QB$_{0-8}$) outputs when (OEA,OEB) is asserted. When (OEA,OEB) is enabled (LOW), data in the output register will be available to the (QA$_{0-8}$,QB$_{0-8}$) outputs after tOE.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its (QA$_{0-8}$,QB$_{0-8}$) outputs even after additional reads occur.

Write Enable 1 (WENA1,WENB1) - If the FIFO is configured for programmable flags, Write Enable 1 (WENA1,WENB1) is the only write enable control pin. In this configuration, when Write Enable 1 (WENA1,WENB1) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH

transition of every write clock (WCLKA,WCLKB). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WENA2/LDA, WENB2/LDB) - This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WENA2/LDA, WENB2/LDB) is set active HIGH at Reset (RSA,RSB=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable 1 (WENA1,WENB1) is LOW and Write Enable 2/Load (WENA2/LDA, WENB2/LDB) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLKA,WCLKB). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When (WENA2/LDA, WENB2/LDB) is held LOW during Reset, this pin is the load (LDA,LDB) enable for flag offset programming. In this configuration, (WENA2/LDA, WENB2/LDB) can be used to access the four 8-bit offset registers contained in the CY7C48X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both (WENA2/LDA, WENB2/LDB) and (WENA1,WENB1) are LOW, the first LOW-to-HIGH transition of (WCLKA,WCLKB) writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of (WCLKA,WCLKB) store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when (WENA2/LDA, WENB2/LDB) and (WENA1,WENB1) are LOW. The fifth LOW-to-HIGH transition of (WCLKA,WCLKB) while (WENA2/LDA, WENB2/LDB) and (WENA1,WENB1) are LOW writes data to the empty LSB register again. *Figure 1* shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the (WENA2/LDA, WENB2/LDB) input HIGH, the FIFO is returned to normal read and write operation. The next time (WENA2/LDA, WENB2/LDB) is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when (WENA2/LDA, WENB2/LDB) is LOW and both (RENA1,RENB1) and (RENA2,RENB2) are LOW. LOW-to-HIGH transitions of (RCLKA,RCLKB) read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.
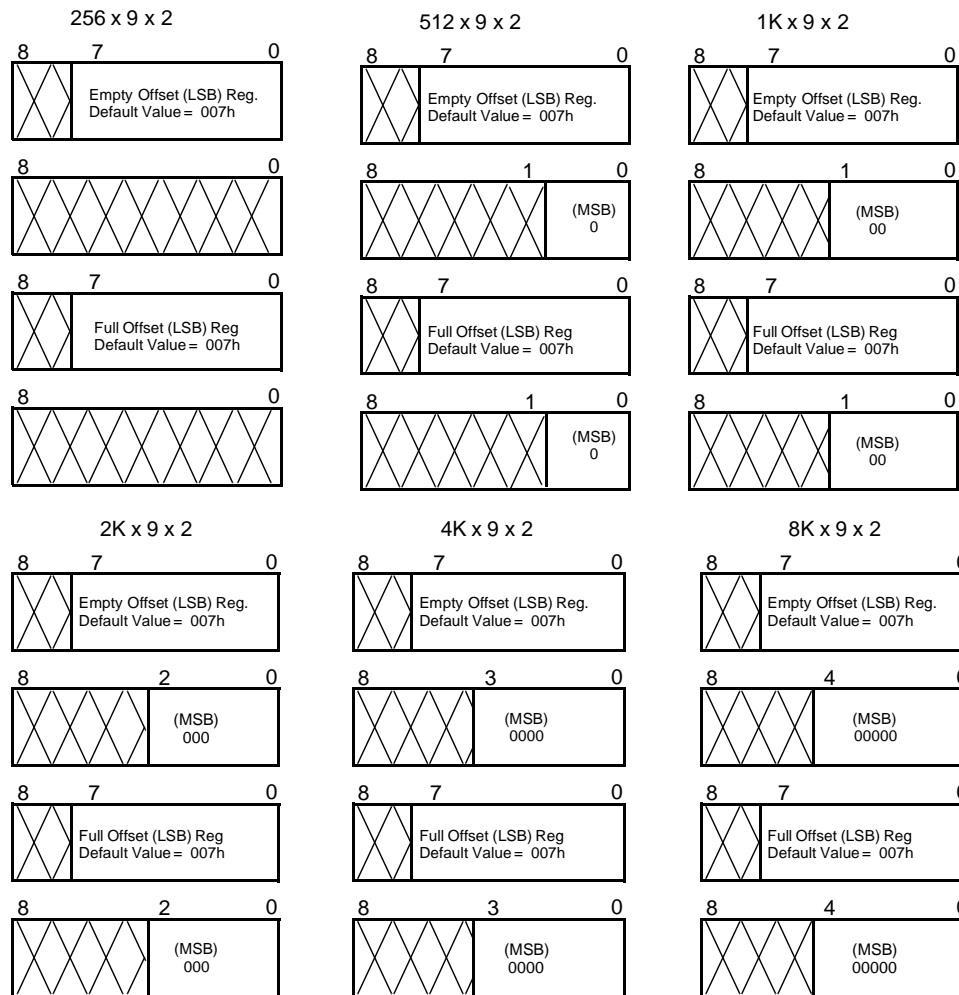
256 x 9 x 2

512 x 9 x 2

1K x 9 x 2

2K x 9 x 2

4K x 9 x 2

8K x 9 x 2

Figure 1. Offset Register Location and Default Values.

Programmable Flag (PAEA, PAEB, PAFA, PAFB) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag (PAEA, PAEB) and programmable almost-full flag (PAFA, PAFB) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers.

LD	WEN	WCLK[25]	Selection
0	0	⌐	Empty Offset (LSB) / Empty Offset (MSB) / Full Offset (LSB) / Full Offset (MSB)
0	1	⌐	No Operation
1	0	⌐	Write Into FIFO
1	1	⌐	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of (PAEA, PAEB). (PAEA, PAEB) is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. (PAEA, PAEB) is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of (PAFA, PAFB). (PAEA, PAEB) is synchronized to the LOW-to-HIGH transition of (WCLKA, WCLKB) by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4801 (256–m), CY7C4811 (512–m), CY7C4821 (1K–m), CY7C4831 (2K–m), CY7C4841 (4K–m), and CY7C4851 (8K–m). (PAFA, PAFB) is set HIGH by the LOW-to-HIGH transition of (WCLKA, WCLKB) when the number of available memory locations is greater than m.

Notes:
25. The same selection sequence applies to reading form the registers. REN1 and REN2 are enabled and a read is performed on the LOW- to-HIGH transition of RCLK.

[+] Feedback

Flag Operation

The CY7C48X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, (PAEA,PAEB), and (PAFA,PAFB) are synchronous.

Full Flag

The Full Flag ($\overline{FFA},\overline{FFB}$) will go LOW when the device is full. Write operations are inhibited whenever ($\overline{FFA},\overline{FFB}$) is LOW regardless of the state of ($\overline{WENA1},\overline{WENB1}$) and ($\overline{WENA2/LDA},\overline{WENB2/LDB}$).

($\overline{FFA},\overline{FFB}$) is synchronized to (WCLKA,WCLKB), i.e., it is exclusively updated by each rising edge of (WCLKA,WCLKB).

Empty Flag

The Empty Flag ($\overline{EFA},\overline{EFB}$) will go LOW when the device is empty. Read operations are inhibited whenever ($\overline{EFA},\overline{EFB}$) is LOW, regardless of the state of ($\overline{RENA1},\overline{RENB1}$) and ($\overline{RENA2},\overline{RENB2}$. ($\overline{EFA},\overline{EFB}$) is synchronized to (RCLKA,RCLKB), i.e., it is exclusively Full Flag.

Table 2. Status Flags.

Number of Words in FIFO			$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
CY7C4801	CY7C4811	CY7C4821				
0	0	0	H	H	L	L
1 to n[26]	1 to n[26]	1 to n[26]	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (1024 –(m+1))	H	H	H	H
(256–m)[27] to 255	(512–m)[27] to 511	(1024–m)[27] to 1023	H	L	H	H
256	512	1024	L	L	H	H

Number of Words in FIFO			$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
CY7C4831	CY7C4841	CY7C4851				
0	0	0	H	H	L	L
1 to n[26]	1 to n[26]	1 to n[26]	H	H	L	H
(n+1) to (2048 –(m+1))	(n+1) to (4096 –(m+1))	(n+1) to (8192 –(m+1))	H	H	H	H
(2048–m)[27] to 2047	(4096–m)[27] to 4095	(8192–m)[27] to 8191	H	L	H	H
2048	4096	8192	L	L	H	H

Notes:
26. n =Empty Offset (n=7 default value).
27. m = Full Offset (m=7 default value).

[+] Feedback

Single Device Configuration

When FIFO A(B) is in a Single Device Configuration, the Read Enable 2 RENA2(RENB2) control input can be grounded (see *Figure 2*). in this configuration, the Write Enable2/Load (WENA2/$\overline{\text{LDA}}$,WENB2/$\overline{\text{LDB}}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Figure 2. Block Diagram of 256 x 9,512 x 9,1024 x 9,2048 x 9,4096 x 9,8192 x 9 Double Sync FIFO Used in a Single Device Configuration.

[+] Feedback

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags EFA and EFB, also FFA and FFB. The partial status flags PAEA, PAFB, PAFA, PAFB can be detected from any one device. *Figure 3* demonstrates an 18-bit word width using the two FIFOs contained in one CY7C4801/4811/4821/4831/4841 /4851. Any word width can be attained by adding additional CY7C4801/4811/4821/4831/4841/4851s.

When the CY7C4801/4811/4821/4831/4841/4851 is in a Width Expansion Configuration, the Read Enable 2 (RENA2 and RENB2) control unputs can be grounded (see *Figure 3*). In this configuration, the Write Enable 2/Load (WENA2/LDA,WENB2/LDB) pins are set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

48X1–17

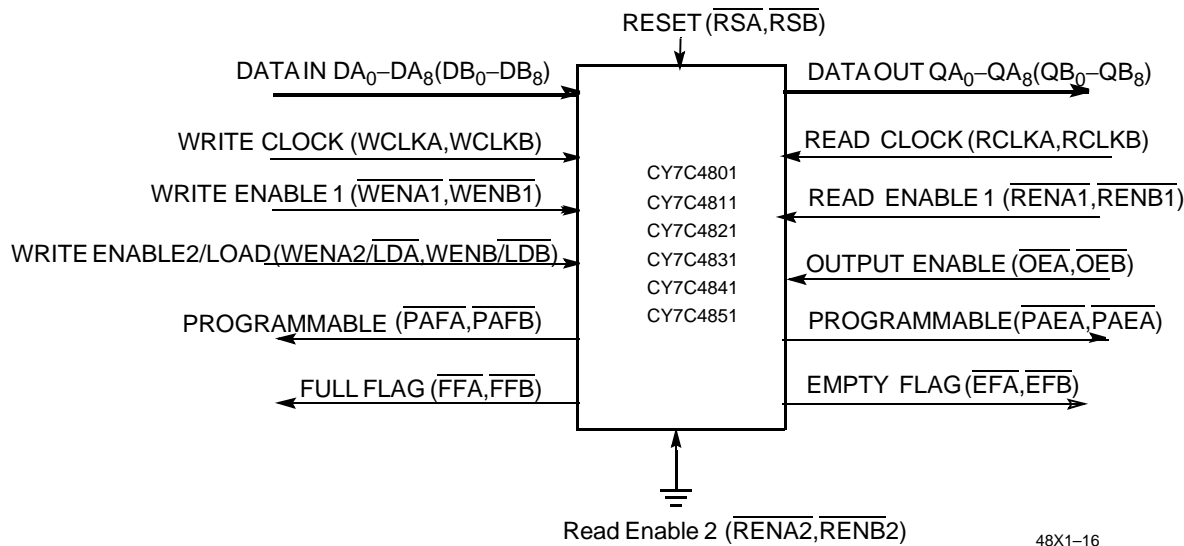**Figure 3. Block Diagram of two FIFOs contained in one CY7C4801/4811/4821/4831/4841/4851 configured for an 18-bit width-expansion.**

Bidirectional Configuration

The two FIFOs of the CY7C4801/4811/4821/4831/4841/4851 can be used to buffer data flow in two directions. In the example that follows, processor A can write data to processor B via

FIFO A, and, in turn, processor B can write processor A via FIFO B.
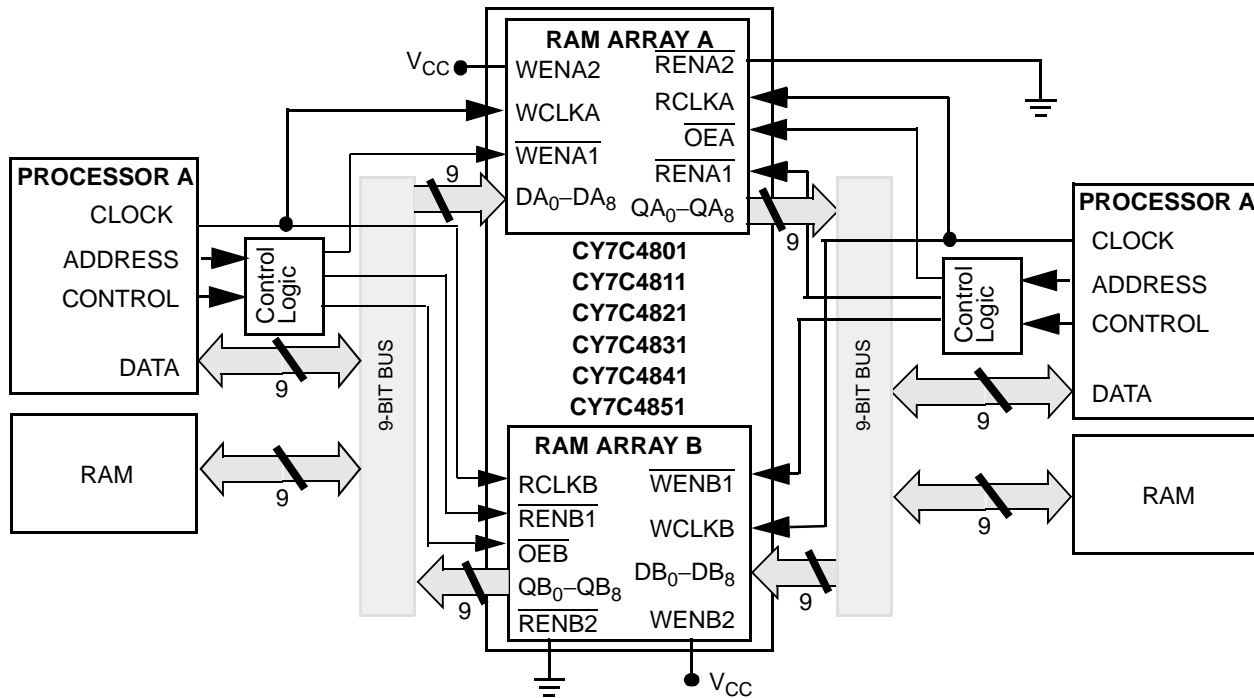
Figure 4. Block Diagram of Bidirectional Configuration.

Depth Expansion

CY7C4801/4811/4821/4831/4841/4851can be adapted to applications that require greater than 256/512/1024/2048/4096/8192 words. The existence of dual enable pins on the read and write ports allow depth expansion. The Write Enable 2/Load (WENA2, WENB2) pins are used as a second write enables in a depth expansion configuration, thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of

data. a typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The CY7C4801/4811/4821/4831/4841/ 4851 operates in the Depth Expansion configuration when the following conditions are met:

1. WENA2/$\overline{\text{LDA}}$ and WENB2/$\overline{\text{LDB}}$ pins are held HIGH during Reset so that these pins operate as second Write Enables.

2. External logic is used to control the flow of data.

[+] Feedback

Ordering Information

Double 256x9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4801-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4801-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4801-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4801-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4801-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4801-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4801-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4801-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

Double 512x9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4811-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4811-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4811-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4811-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4811-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4811-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4811-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4811-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

Double 1Kx9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4821-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4821-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4821-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4821-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4821-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4821-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4821-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4821-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

[+] Feedback

Ordering Information (continued)

Double 2Kx9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4831-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4831-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4831-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4831-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4831-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4831-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4831-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4831-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

Double 4Kx9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4841-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4841-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4841-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4841-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4841-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4841-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4841-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4841-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

Double 8Kx9 FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4851-10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4851-10AI	A65	64-Lead Thin Quad Flatpack	Industrial
15	CY7C4851-15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4851-15AI	A65	64-Lead Thin Quad Flatpack	Industrial
25	CY7C4851-25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4851-25AI	A65	64-Lead Thin Quad Flatpack	Industrial
35	CY7C4851-35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4851-35AI	A65	64-Lead Thin Quad Flatpack	Industrial

[+] Feedback

Package Diagram

64-Lead Thin Plastic Quad Flat Pack A65
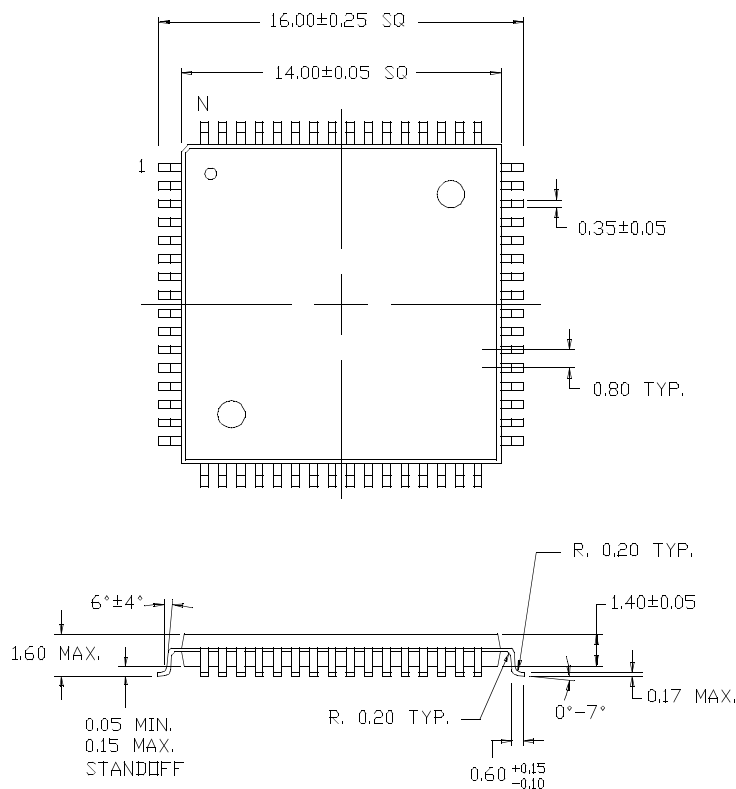
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.100 MAX.

16.00±0.25 SQ

14.00±0.05 SQ

N

1

0.35±0.05

0.80 TYP.

R. 0.20 TYP.

6°±4°

1.40±0.05

1.60 MAX.

0.05 MIN.
0.15 MAX.
STANDOFF

R. 0.20 TYP.

0°–7°

0.17 MAX.

0.60 +0.15 −0.10

Document Title: CY7C4801/4811/4821/CY7C4831.4841/4851 256/512/1K/2K/4K/8K x9 x2 Double Sync (TM) Fifos
Document Number: 38-06005

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106466	07/11/01	SZV	Change from Spec Number: 38-00538 to 38-06005
*A	122258	12/26/02	RBI	Power up requirements added to Operating Conditions Information

[+] Feedback