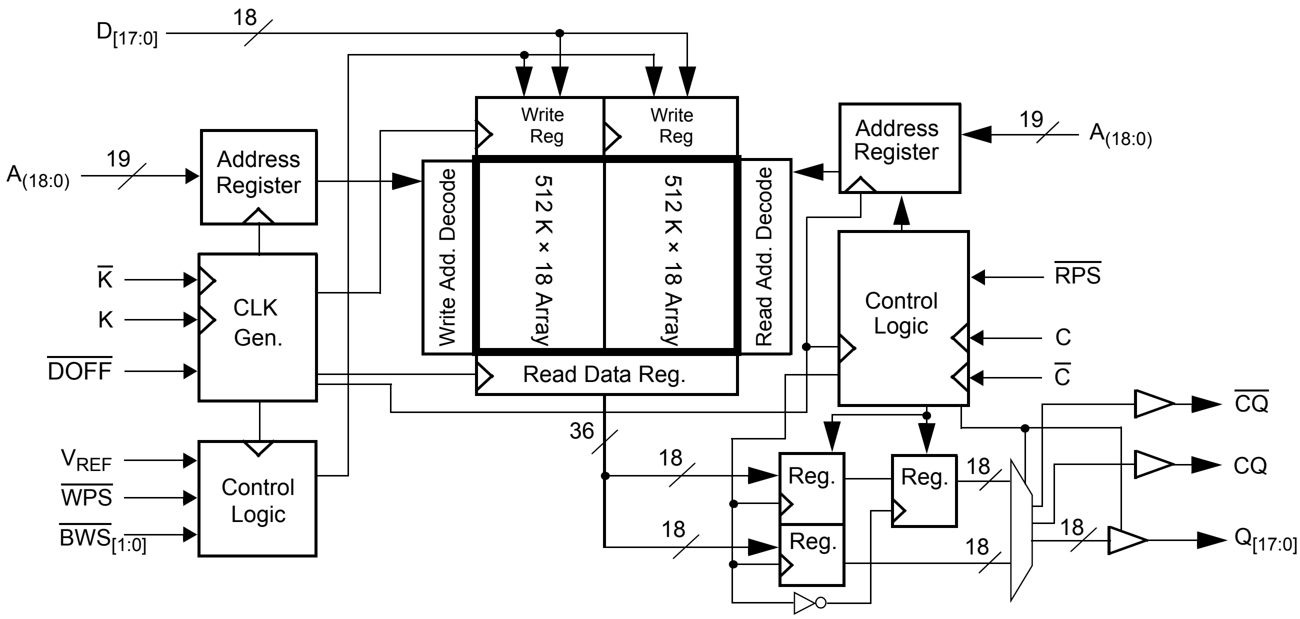
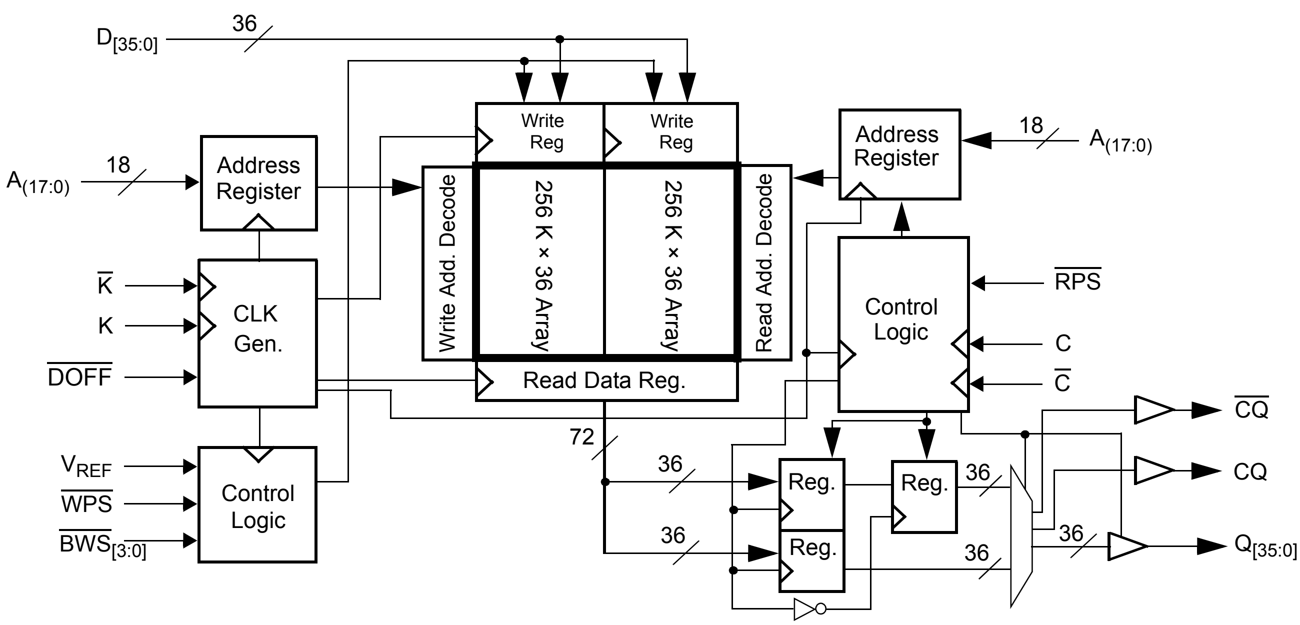
Logic Block Diagram (CY7C1312BV18)



Logic Block Diagram (CY7C1314BV18)



Contents

Pin Configuration

The pin configuration for CY7C1312BV18, and CY7C1314BV18 follow. [1]

165-ball FBGA (13 × 15 × 1.4 mm) Pinout

Table 1. CY7C1312BV18 (1 M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144 M	NC/36 M	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288 M	$\overline{RPS}$	A	NC/72 M	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	A	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Table 2. CY7C1314BV18 (512 K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/288 M	NC/72 M	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	NC/36 M	NC/144 M	CQ
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	A	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Note
1. NC/36 M, NC/72 M, NC/144 M, and NC/288 M are not connected to the die and can be tied to any voltage level.

Pin Definitions

Pin Name	I/O	Pin Description
$D_{[x:0]}$	Input-Synchronous	**Data Input Signals.** Sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. CY7C1312BV18 - $D_{[17:0]}$ CY7C1314BV18 - $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	**Write Port Select** – **Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	**Byte Write Select 0, 1, 2 and 3** – **Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1312BV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$. CY7C1314BV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address Inputs.** Sampled on the rising edge of the K (Read address) and $\overline{K}$ (Write address) clocks during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 1 M × 18 (2 arrays each of 512 K × 18) for CY7C1312BV18 and 512 K × 36 (2 arrays each of 256 K × 36) for CY7C1314BV18. Therefore, only 19 address inputs are needed to access the entire memory array of CY7C1312BV18 and 18 address inputs for CY7C1314BV18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-Synchronous	**Data Output Signals**. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during read operations, or K and $\overline{K}$ when in single clock mode. When the read port is deselected, $Q_{[x:0]}$ are automatically tri-stated. CY7C1312BV18 – $Q_{[17:0]}$ CY7C1314BV18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	**Read Port Select** – **Active LOW**. Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the C clock. Each read access consists of a burst of two sequential transfers.
C	Input Clock	**Positive Input Clock for Output Data**. C is used in conjunction with $\overline{C}$ to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See Application Example on page 8 for further details.
$\overline{C}$	Input Clock	**Negative Input Clock for Output Data**. $\overline{C}$ is used in conjunction with C to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See Application Example on page 8 for further details.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Echo Clock	**CQ Referenced with Respect to C**. This is a free - running clock and is synchronized to the Input clock for output data (C) of the QDR II. In the single clock mode, CQ is generated with respect to K. The timings for the echo clocks is shown in the Switching Characteristics on page 22.
$\overline{CQ}$	Echo Clock	**$\overline{CQ}$ Referenced with Respect to $\overline{C}$**. This is a free - running clock and is synchronized to the Input clock for output data ($\overline{C}$) of the QDR II. In the single clock mode, $\overline{CQ}$ is generated with respect to $\overline{K}$. The timings for the echo clocks is shown in the Switching Characteristics on page 22.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
$\overline{DOFF}$	Input	**DLL Turn Off** – **Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timing in the DLL turned off operation differs from those listed in this data sheet.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK Pin for JTAG**.
TDI	Input	**TDI Pin for JTAG**.
TMS	Input	**TMS Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/36M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, Outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

Functional Overview

The CY7C1312BV18, and CY7C1314BV18 are synchronous pipelined Burst SRAMs equipped with a read port and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and flows out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR II completely eliminates the need to turn around the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of two 18-bit data transfers in the case of CY7C1312BV18, and two 36-bit data transfers in the case of CY7C1314BV18 in one clock cycle.

Accesses for both ports are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the rising edge of the output clocks (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode).

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

CY7C1312BV18 is described in the following sections. The same basic descriptions apply to CY7C1314BV18.

Read Operations

The CY7C1312BV18 is organized internally as two arrays of 512K x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address is latched on the rising edge of the K clock. The address presented to the address inputs is stored in the read address register. Following the next K clock rise the corresponding lowest order 18-bit word of data is driven onto the $Q_{[17:0]}$ using C as the output timing reference. On the subsequent rising edge of C, the next 18-bit data word is driven onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the output clock (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the output clocks (C/$\overline{C}$). This allows for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the same K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$), the address is latched and the information presented to $D_{[17:0]}$ is stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36-bits of data are then written into the memory array at the specified location. When deselected, the write port ignores all inputs after completion of pending write operations.

Byte Write Operations

Byte write operations are supported by the CY7C1312BV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each 18-bit data word. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write allows the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

Single Clock Mode

The CY7C1312BV18 can be used with a single clock that controls both the input and output registers. In this mode, the device recognizes only a single pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ HIGH at power on. This function is a strap option and not alterable during device operation.

Concurrent Transactions

The read and write ports on the CY7C1312BV18 operate independently of one another. As each port latches the address inputs on different clock edges, the user can read or write to any location, regardless of the transaction on the other port. The user can start reads and writes in the same clock cycle. If the ports access the same location at the same time, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Depth Expansion

The CY7C1312BV18 has a port select input for each port. This enables for easy depth expansion. Both port selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting a port does not affect the other port. All pending transactions (read and write) are completed prior to the device being deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the QDR II to simplify data capture on high-speed systems. Two echo clocks are generated by the QDR II. CQ is referenced with respect to C and $\overline{CQ}$ is referenced with respect to $\overline{C}$. These are free-running clocks and are synchronized to the output clock (C/$\overline{C}$) of the QDR II. In single clock mode, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$. The timing for the echo clocks is shown in the Switching Characteristics on page 22.

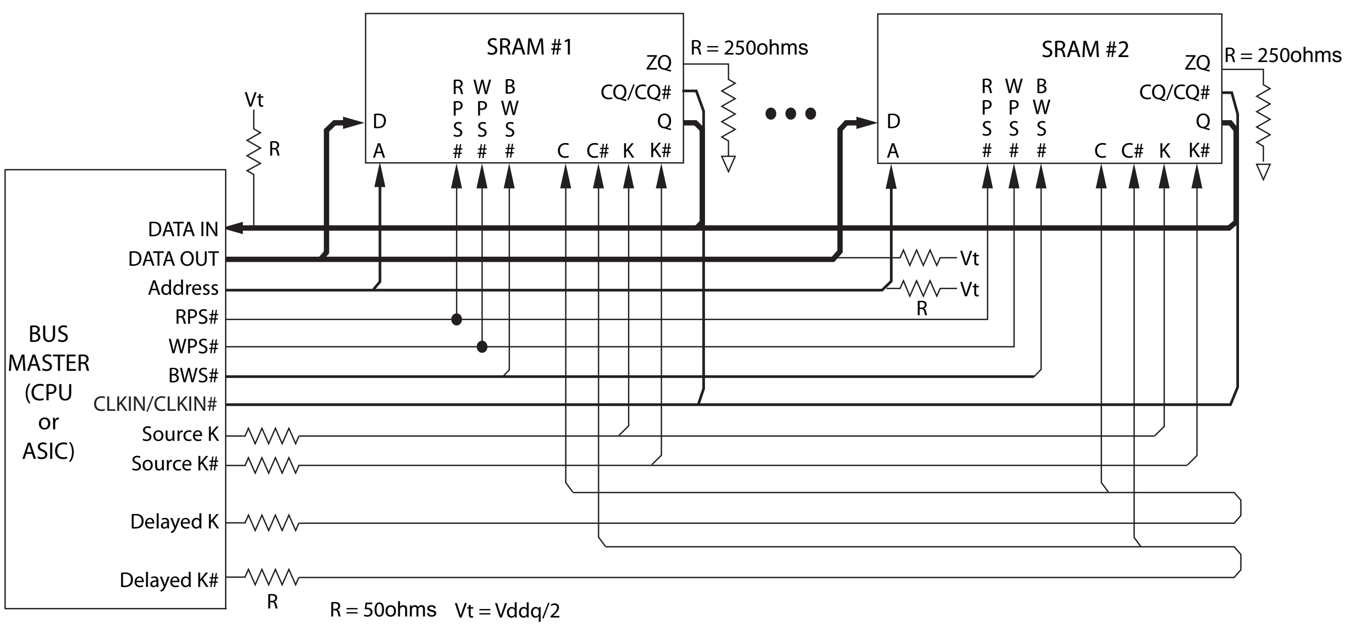
DLL

These chips use a DLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power-up, when the $\overline{DOFF}$ is tied HIGH, the DLL is locked after 1024 cycles of stable clock. The DLL can also be reset by slowing or stopping the input clock K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the DLL to lock to the desired frequency. The DLL automatically locks 1024 clock cycles after a stable clock is presented. The DLL may be disabled by applying ground to the $\overline{DOFF}$ pin. For information refer to the application note, DLL Considerations in QDRII/DDRII/QDRII+/DDRII+ – AN5062.

Application Example

Figure 1 shows two QDR II used in an application.

Figure 1. Application Example



Truth Table

The truth table for CY7C1312BV18, and CY7C1314BV18 follows. [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ
Write cycle: Load address on the rising edge of $\overline{K}$; input write data on K and $\overline{K}$ rising edges.	L-H	X	L	D(A + 0) at K(t) $\uparrow$	D(A + 1) at $\overline{K}$(t) $\uparrow$
Read Cycle: Load address on the rising edge of K; wait one and a half cycle; read data on $\overline{C}$ and C rising edges.	L-H	L	X	Q(A + 0) at $\overline{C}$(t + 1) $\uparrow$	Q(A + 1) at C(t + 2) $\uparrow$
NOP: No operation	L-H	H	H	D = X Q = High Z	D = X Q = High Z
Standby: Clock stopped	Stopped	X	X	Previous state	Previous state

Write Cycle Descriptions

The write cycle description table for CY7C1312BV18 follows. [2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: Both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the data portion of a write sequence: Both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes
2. X = "Do not Care," H = Logic HIGH, L = Logic LOW, $\uparrow$represents rising edge.
3. Device powers up deselected with the outputs in a tri-state condition.
4. "A" represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represents the internal address sequence in the burst.
5. "t" represents the cycle at which a Read/Write operation is started. t + 1, and t + 2 are the first, and second clock cycles respectively succeeding the "t" clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
7. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

Write Cycle Descriptions

The write cycle description table for CY7C1314BV18 follows. [9, 10]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes
9. X = "Do not Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.
10. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-1900. The TAP operates using JEDEC standard 1.8 V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull-up resistor. TDO must be left unconnected. Upon power-up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 13. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 16). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in on page 14. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 17 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 16.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 16. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the "extest output bus tri-state," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

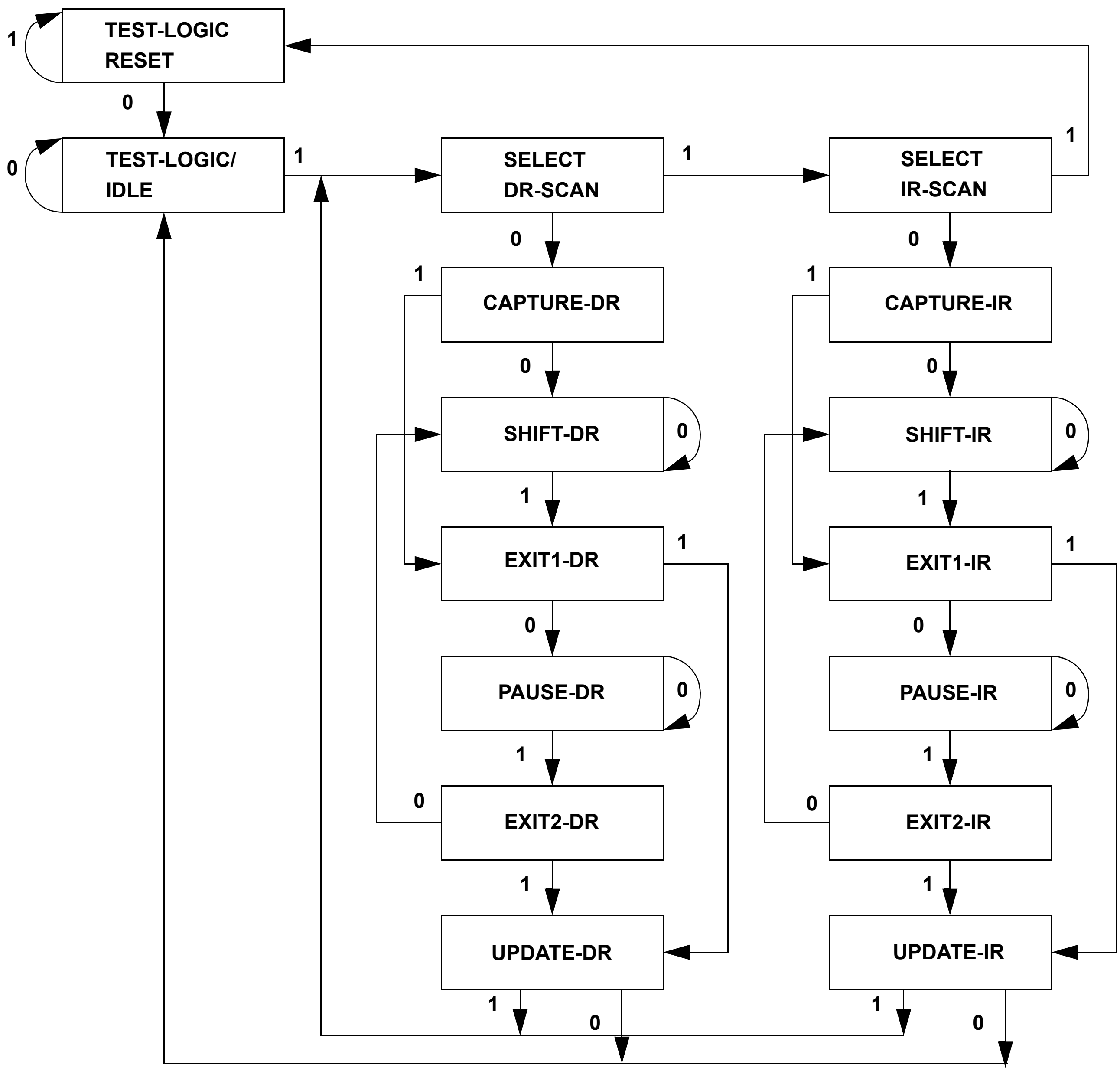
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set LOW to enable the output when the device is powered-up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

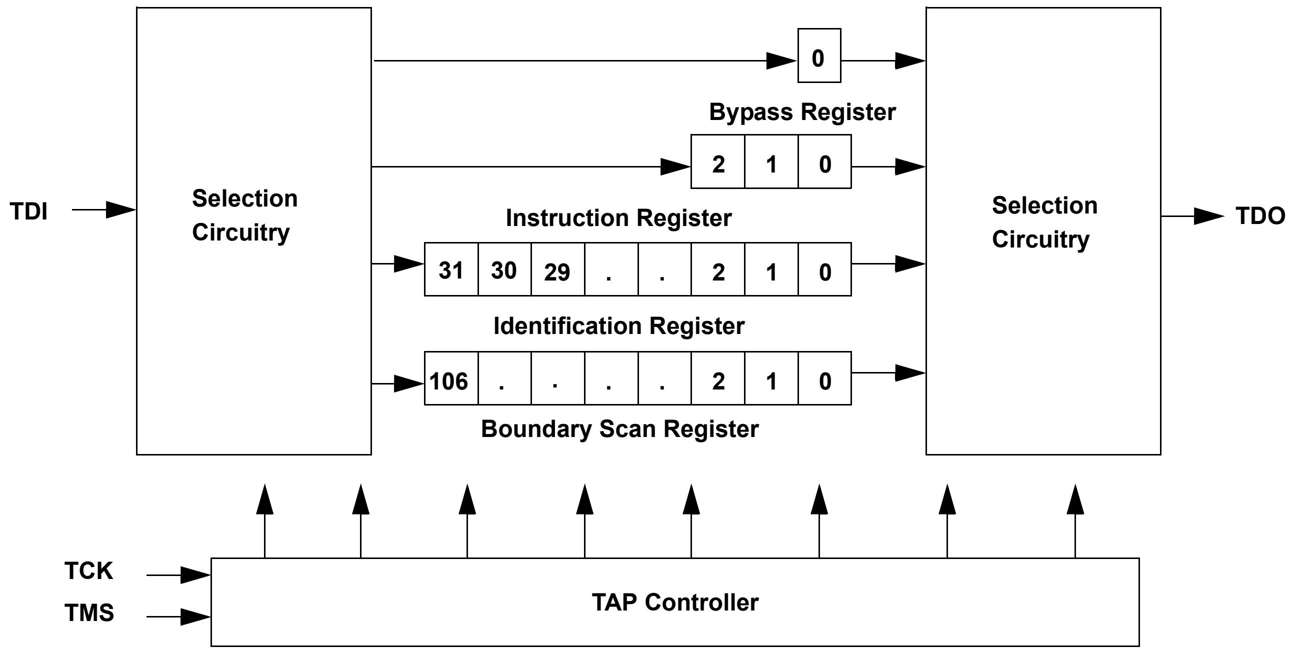
The state diagram for the TAP controller follows. [11]



Note

11. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range [12, 13, 14]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH voltage	$I_{OH} = -2.0$ mA	1.4	–	V
V_{OH2}	Output HIGH voltage	$I_{OH} = -100\ \mu A$	1.6	–	V
V_{OL1}	Output LOW voltage	$I_{OL} = 2.0$ mA	–	0.4	V
V_{OL2}	Output LOW voltage	$I_{OL} = 100\ \mu A$	–	0.2	V
V_{IH}	Input HIGH voltage		0.65 V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	0.35 V_{DD}	V
I_X	Input and output load current	$GND \le V_I \le V_{DD}$	–5	5	µA

Notes

12. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics table.
13. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -1.5$ V (Pulse width less than $t_{CYC}/2$).
14. All Voltage referenced to Ground.

TAP AC Switching Characteristics

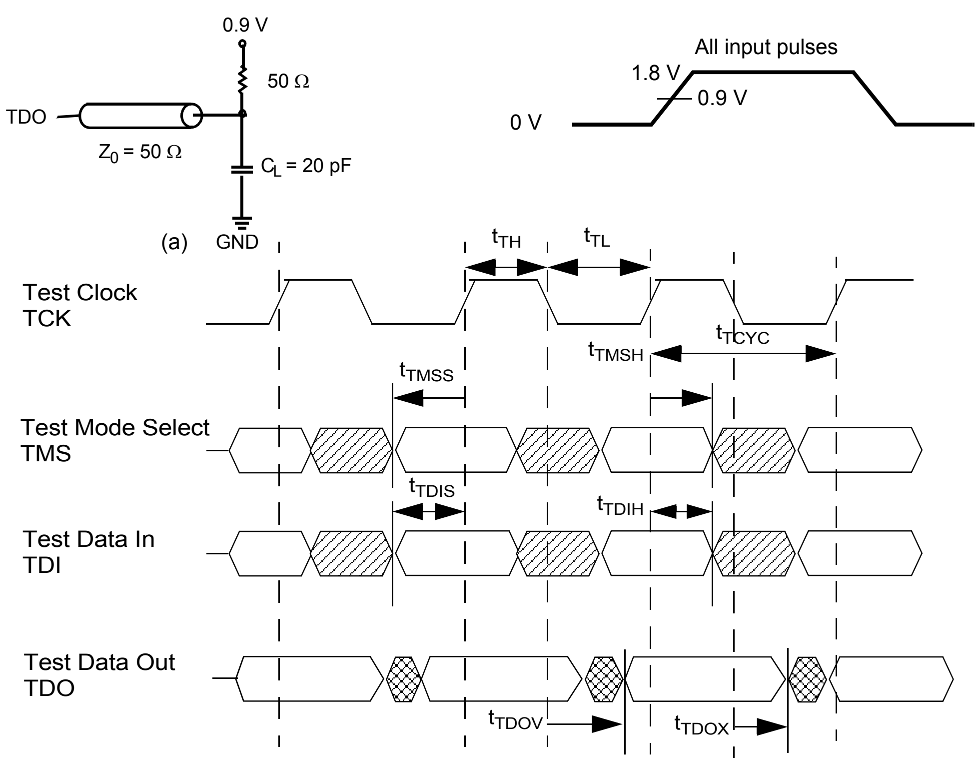
Over the Operating Range [15, 16]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

TAP Timing and Test Conditions

Figure 2 shows the TAP timing and test conditions. [16]

Figure 2. TAP Timing and Test Conditions



Notes

15. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
16. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value		Description
	CY7C1312BV18	CY7C1314BV18	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	11010011010010101	11010011010100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do not use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do not use: This instruction is reserved for future use.
RESERVED	110	Do not use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J

Bit #	Bump ID
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	Internal
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A

Bit #	Bump ID
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	1H
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F

Bit #	Bump ID
81	3G
82	2G
83	1J
84	2J
85	3K
86	3J
87	2K
88	1K
89	2L
90	3L
91	1M
92	1L
93	3N
94	3M
95	1N
96	2M
97	3P
98	2N
99	2P
100	1P
101	3R
102	4R
103	4P
104	5P
105	5N
106	5R

Power-up Sequence in QDR II SRAM

QDR II SRAMs must be powered-up and initialized in a predefined manner to prevent undefined operations.

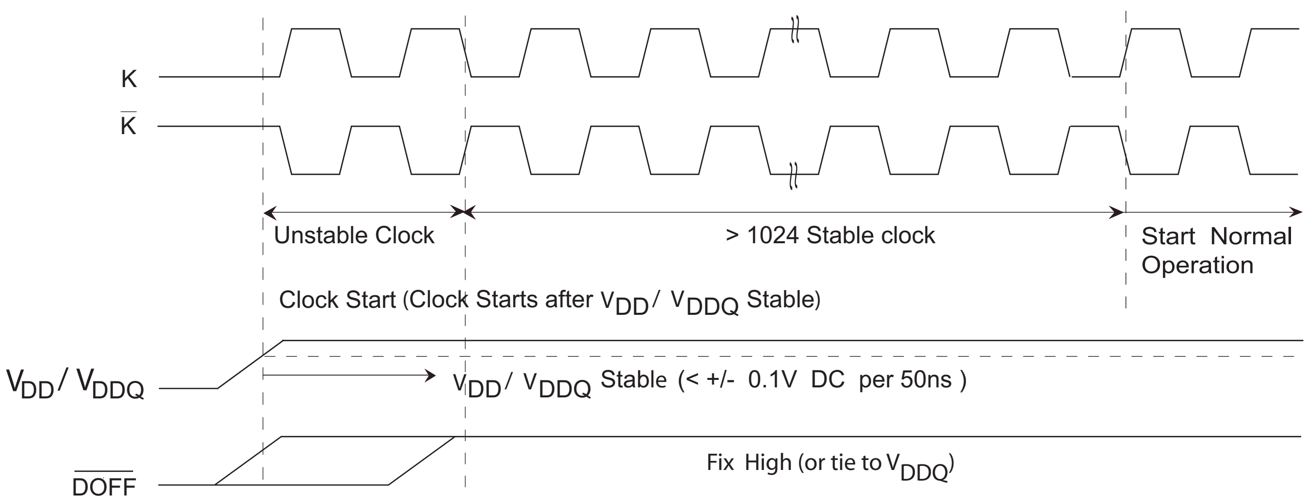
Power-up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (all other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 1024 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide1024 cycles stable clock to relock to the desired clock frequency.

Figure 3. Power-up Waveforms



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +2.9 V

Supply voltage on V_{DDQ} relative to GND....... –0.5 V to $+V_{DD}$

DC applied to outputs in high Z ....–0.5 V to V_{DDQ} + 0.3 V

DC input voltage [17] ....–0.5 V to V_{DD} + 0.3 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, M. 3015).. > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD} [18]	V_{DDQ} [18]
Commercial	0 °C to +70 °C	1.8 ± 0.1 V	1.4 V to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	320	368	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates – AN54908.

Electrical Characteristics

DC Electrical Characteristics

Over the Operating Range [19]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O supply voltage		1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH voltage	Note 20	$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW voltage	Note 21	$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH voltage	I_{OH} = –0.1 mA, nominal impedance	$V_{DDQ} – 0.2$	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW voltage	I_{OL} = 0.1 mA, nominal impedance	V_{SS}	–	0.2	V
V_{IH}	Input HIGH voltage		V_{REF} + 0.1	–	V_{DDQ} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	–	V_{REF} – 0.1	V
I_X	Input leakage current	GND ≤ V_I ≤ V_{DDQ}	–5	–	5	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ output disabled	–5	–	5	µA
V_{REF}	Input reference voltage [22]	Typical Value = 0.75 V	0.68	0.75	0.95	V

Notes
17. Overshoot: $V_{IH}(AC) < V_{DDQ}$ + 0.85 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > –1.5$ V (Pulse width less than $t_{CYC}/2$).
18. Power-up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
19. All Voltage referenced to Ground.
20. Output are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175 ohms ≤ RQ ≤ 350 ohms.
21. Output are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 ohms ≤ RQ ≤ 350 ohms.
22. V_{REF} (min) = 0.68 V or 0.46 V_{DDQ}, whichever is larger, V_{REF} (max) = 0.95 V or 0.54 V_{DDQ}, whichever is smaller.

Electrical Characteristics (continued)

DC Electrical Characteristics

Over the Operating Range [19]

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
I_{DD} [23]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	250 MHz	(x18)	–	–	800	mA
				(x36)	–	–	900	
			200 MHz	(x18)	–	–	675	
				(x36)	–	–	750	
			167 MHz	(x18)	–	–	600	
				(x36)	–	–	650	
I_{SB1}	Automatic power-down current	Max V_{DD}, both ports deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = 1/t_{CYC}, inputs static	250 MHz	(x18)	–	–	400	mA
				(x36)	–	–	450	
			200 MHz	(x18)	–	–	380	
				(x36)	–	–	400	
			167 MHz	(x18)	–	–	360	
				(x36)	–	–	370	

AC Electrical Characteristics

Over the Operating Range [24]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage		V_{REF} + 0.2	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{REF} – 0.2	V

Notes

23. The operation current is calculated with 50% read cycle and 50% write cycle.
24. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -1.5$ V (Pulse width less than $t_{CYC}/2$).

Capacitance

Tested initially and after any design or process change that may affect these parameters.

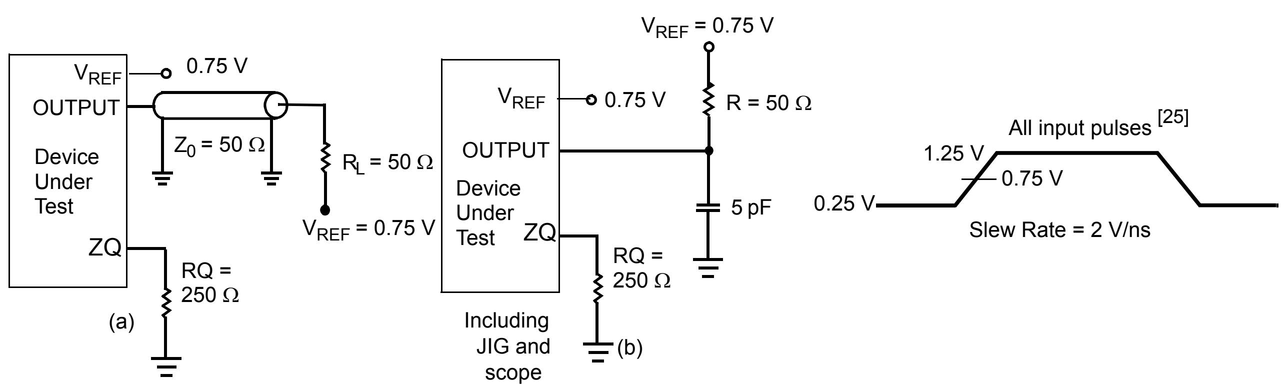
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	5	pF
C_{CLK}	Clock input capacitance		6	pF
C_O	Output capacitance		7	pF

Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	18.7	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.5	°C/W

Figure 4. AC Test Loads and Waveforms



Note

25. Unless otherwise noted, test conditions are based on signal transition time of 2V/ns, timing reference levels of 0.75 V, Vref = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

Switching Characteristics

Over the Operating Range [26, 27]

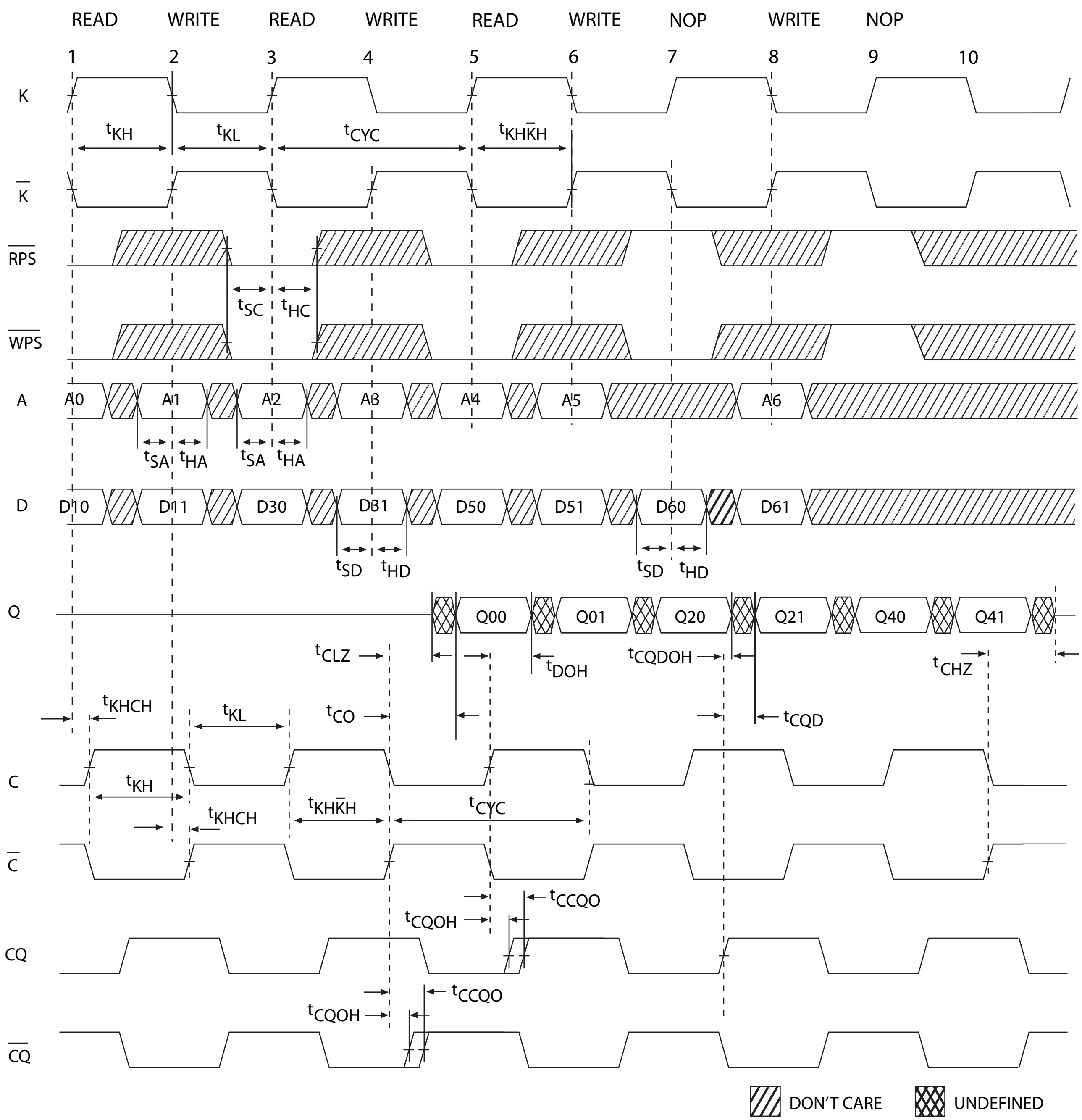
Cypress Parameter	Consortium Parameter	Description	250 MHz		200 MHz		167 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the first access [28]	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K clock and C clock cycle time	4.0	8.4	5.0	8.4	6.0	8.4	ns
t_{KH}	t_{KHKL}	Input clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	1.6	–	2.0	–	2.4	–	ns
t_{KL}	t_{KLKH}	Input clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	1.6	–	2.0	–	2.4	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K clock rise to $\overline{K}$ clock rise and C to $\overline{C}$ rise (rising edge to rising edge)	1.8	–	2.2	–	2.7	–	ns
t_{KHCH}	t_{KHCH}	K/$\overline{K}$ clock rise to C/$\overline{C}$ clock rise (rising edge to rising edge)	0	1.8	0	2.2	0	2.7	ns
Setup Times									
t_{SA}	t_{AVKH}	Address setup to K clock rise	0.35	–	0.4	–	0.5	–	ns
t_{SC}	t_{IVKH}	Control setup to K clock rise ($\overline{RPS}$, $\overline{WPS}$)	0.35	–	0.4	–	0.5	–	ns
t_{SCDDR}	t_{IVKH}	DDR control setup to clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_3}$, $\overline{BWS_4}$)	0.35	–	0.4	–	0.5	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ setup to clock (K/$\overline{K}$) rise	0.35	–	0.4	–	0.5	–	ns
Hold Times									
t_{HA}	t_{KHAX}	Address hold after K clock rise	0.35	–	0.4	–	0.5	–	ns
t_{HC}	t_{KHIX}	Control hold after K clock rise ($\overline{RPS}$, $\overline{WPS}$)	0.35	–	0.4	–	0.5	–	ns
t_{HCDDR}	t_{KHIX}	DDR control hold after clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_3}$, $\overline{BWS_4}$)	0.35	–	0.4	–	0.5	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ hold after clock (K/$\overline{K}$) rise	0.35	–	0.4	–	0.5	–	ns
Output Times									
t_{CO}	t_{CHQV}	C/$\overline{C}$ clock rise (or K/$\overline{K}$ in single clock mode) to data valid	–	0.45	–	0.45	–	0.50	ns
t_{DOH}	t_{CHQX}	Data output hold after output C/$\overline{C}$ clock rise (active to active)	–0.45	–	–0.45	–	–0.50	–	ns
t_{CCQO}	t_{CHCQV}	C/$\overline{C}$ clock rise to echo clock valid	–	0.45	–	0.45	–	0.50	ns
t_{CQOH}	t_{CHCQX}	Echo clock hold after C/$\overline{C}$ clock rise	–0.45	–	–0.45	–	–0.50	–	ns
t_{CQD}	t_{CQHQV}	Echo clock high to data valid	–	0.30	–	0.35	–	0.40	ns
t_{CQDOH}	t_{CQHQX}	Echo clock high to data invalid	–0.30	–	–0.35	–	–0.40	–	ns
t_{CHZ}	t_{CHQZ}	Clock (C/$\overline{C}$) rise to high Z (active to high Z) [29, 30]	–	0.45	–	0.45	–	0.50	ns
t_{CLZ}	t_{CHQX1}	Clock (C/$\overline{C}$) rise to low Z [29, 30]	–0.45	–	–0.45	–	–0.50	–	ns
DLL Timing									
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock phase jitter	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL lock time (K, C)	1024	–	1024	–	1024	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K static to DLL reset	30	–	30	–	30	–	ns

Notes

26. Unless otherwise noted, test conditions are based on signal transition time of 2V/ns, timing reference levels of 0.75 V, Vref = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.
27. When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timing of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
28. This part has a voltage regulator internally; t_{POWER} is the time that the power is supplied above V_{DD} minimum initially before a read or write operation is initiated.
29. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±100 mV from steady state voltage.
30. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.

Switching Waveforms

Figure 5. Read/Write/Deselect Sequence [31, 32, 33]



Notes

31. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0+1.
32. Outputs are disabled (High Z) one clock cycle after a NOP.
33. In this example, if address A0 = A1, then data Q00 = D10 and Q01 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
250	CY7C1312BV18-250BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Commercial
	CY7C1314BV18-250BZC			
	CY7C1314BV18-250BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm) Pb-free	
200	CY7C1312BV18-200BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Commercial
	CY7C1314BV18-200BZC			
	CY7C1312BV18-200BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm) Pb-free	
	CY7C1312BV18-200BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Industrial
167	CY7C1312BV18-167BZC	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Commercial
	CY7C1314BV18-167BZC			
	CY7C1312BV18-167BZI	51-85180	165-ball Fine Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Industrial

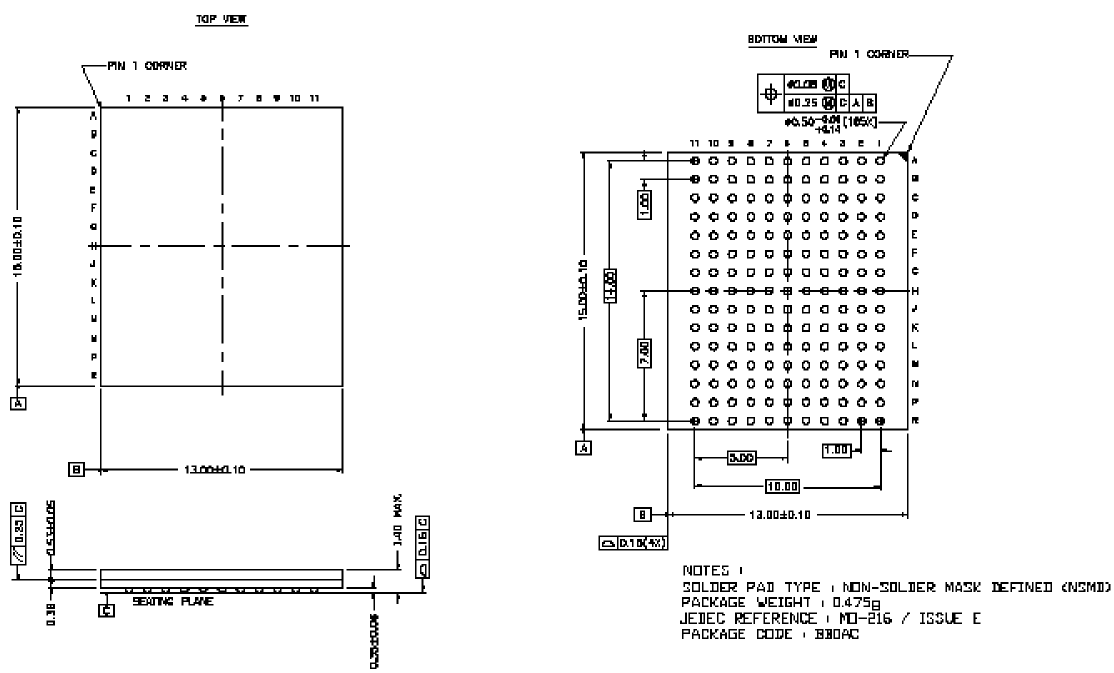
Ordering Code Definitions

CY 7C 13XX B V18 - XXX XXX X

- Temperature Range: X = C or I
  C = Commercial; I = Industrial
- Package Type: XXX = BZ or BZX
  BZ = 165-ball FPBGA
  BZX = 165-ball FPBGA (Pb-free)
- Speed: 250 MHz / 200 MHz / 167 MHz
- V18 = 1.8 V V_{DD}
- Process Technology: 90 nm errata affected
- Part Identifier: 13XX = 1312 or 1314
- Marketing Code: 7C = SRAMs
- Company ID: CY = Cypress

Package Diagram

Figure 6. 165-ball FPBGA (13 × 15 × 1.4 mm)



51-85180 *C

[+] Feedback

Acronyms

Acronym	Description
DDR	double data rate
FPBGA	fine-pitch ball grid array
HSTL	high-speed transceiver logic
JEDEC	joint electron device engineering council
JTAG	joint test action group
ODT	on-die termination
PLL	phase-locked loop
QDR	quad data rate
TAP	test access port
TCK	test clock
TDO	test data out
TDI	test data in
TMS	test mode select

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mm	milli meter
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title: CY7C1312BV18/CY7C1314BV18, 18-Mbit QDR® II SRAM Two-Word Burst Architecture Document Number: 38-05619				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	252474	SYT	See ECN	New datasheet
*A	325581	SYT	See ECN	Removed CY7C1910BV18 from the title Included 300 MHz Speed Bin Added Industrial Temperature Grade Replaced TBDs for I_{DD} and I_{SB1} specifications Replaced the TBDs on the Thermal Characteristics Table to Θ_{JA} = 28.51 °C/W and Θ_{JC} = 5.91 °C/W Replaced TBDs in the Capacitance Table for the 165 FBGA Package Changed the package diagram from BB165E (15 × 17 × 1.4 mm) to BB165D (13 × 15 × 1.4 mm) Added Pb-Free Product Information Updated the Ordering Information by Shading and Unshading MPNs as per availability
*B	413997	NXR	See ECN	Converted from Preliminary to Final Added CY7C1910BV18 part number to the title Removed 300 MHz Speed Bin Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed $C/\overline{C}$ Pin Description in the features section and Pin Description Corrected Typo in Identification Register Definitions for CY7C1910BV18 on page# 16 Added power-up sequence details and waveforms Added foot notes #15, 16, and 17 on page# 18 Replaced Three state with Tri-state Changed the description of I_X from Input Load Current to Input Leakage Current on page# 13 Modified the I_{DD} and I_{SB} values Modified test condition in Footnote #20 on page# 19 from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Replaced Package Name column with Package Diagram in the Ordering Information table Updated Ordering Information Table
*C	423334	NXR	See ECN	Changed the IEEE Standard # 1149.1-1900 to 1149.1-2001 Changed the Minimum Value of t_{SC} and t_{HC} from 0.5ns to 0.35ns for 250 MHz and 0.6 ns to 0.4 ns for 200 MHz speed bins Changed the description of t_{SA} from K Clock Rise to Clock $(K/\overline{K})$ Rise Changed the description of t_{SC} and t_{HC} from Clock (K and $\overline{K}$) Rise to K Clock Rise
*D	472384	NXR	See ECN	Modified the ZQ Definition from Alternately, this pin is connected directly to V_{DD} to Alternately, this pin is connected directly to V_{DDQ} Changed the IEEE Standard # from 1149.1-2001 to 1149.1-1900 Included Maximum Ratings for Supply Voltage on V_{DDQ} Relative to GND Changed the Maximum Ratings for DC Input Voltage from V_{DDQ} to V_{DD} Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in Tap Switching Characteristics. Modified power-up waveform Changed the Maximum rating of Ambient Temperature with Power Applied from –10 □C to +85 □C to –55 □C to +125 □C Added additional notes in the AC parameter section Modified AC Switching Waveform Corrected the typo In the Tap Switching Characteristics. Updated the Ordering Information Table

Document History Page (continued)

Document Title: CY7C1312BV18/CY7C1314BV18, 18-Mbit QDR® II SRAM Two-Word Burst Architecture Document Number: 38-05619				
*E	1274723	VKN	See ECN	Corrected typo in the JTAG ID code for CY7C1910BV18
*F	2511674	VKN/ PYRS	06/03/08	Updated Logic Block diagrams Updated I_{DD}/I_{SB} specs Added footnote# 19 related to I_{DD} Updated power-up sequence waveform and its description Changed DLL minimum operating frequency from 80 MHz to 120 MHz Changed Θ_{JA} spec from 28.51 to 18.7 Changed Θ_{JC} spec from 5.91 to 4.5 Changed t_{CYC} maximum spec to 8.4 ns for all speed bins Modified footnotes 21 and 28
*G	2755901	VKN	08/25/09	Removed x8 and x9 part number details Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information. Updated Package Diagram.
*H	2998771	NJY	08/02/10	Template update. Package diagram update: 51-85180 – *B to *C
*I	3088678	NJY	11/25/2010	Updated Ordering Information. Added Units of Measure.

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