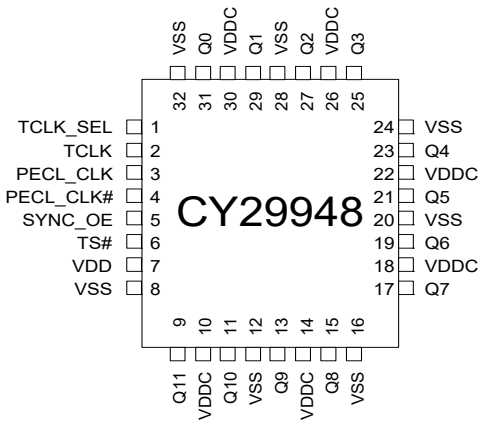
Contents

Pin Configuration

Figure 1. 32-pin TQFP pinout



Pin Description

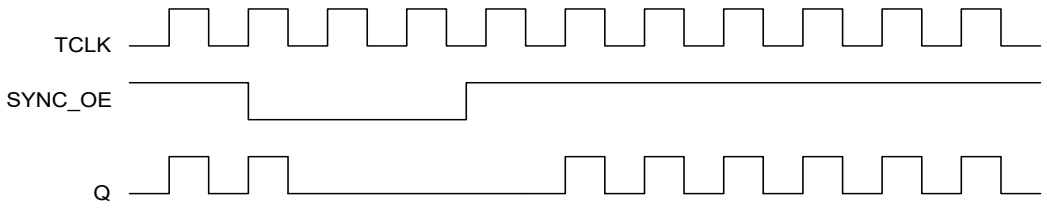
Pin	Name	PWR	I/O [1]	Description
3	PECL_CLK	–	I, PU	**PECL Input Clock**
4	PECL_CLK#	–	I, PD	**PECL Input Clock**
2	TCLK	–	I, PU	**External Reference/Test Clock Input**
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q(11:0)	VDDC	O	**Clock Outputs**
1	TCLK_SEL	–	I, PU	**Clock Select Input**. When LOW, PECL clock is selected. When HIGH TCLK is selected.
5	SYNC_OE	–	I, PU	**Output Enable Input**. When asserted HIGH, the outputs are enabled. When set LOW the outputs are disabled in a LOW state.
6	TS#	–	I, PU	**Three-state Control Input**. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 26, 30	VDDC	–	–	**2.5 V or 3.3 V Power Supply for Output Clock Buffers**
7	VDD	–	–	**2.5 V or 3.3 V Power Supply**
8, 12, 16, 20, 24, 28, 32	VSS	–	–	**Common Ground**

Note
1. PD = Internal pull-down, PU = Internal pull-up.

Output Enable/Disable

The CY29948 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in Figure 2.

Figure 2. SYNC_OE Timing Diagram



Maximum Ratings

Exceeding maximum ratings [2] may shorten the useful life of the device. User guidelines are not tested.

Maximum Input Voltage Relative to V_{SS} ..... V_{SS} – 0.3 V

Maximum Input Voltage Relative to V_{DD} ..... V_{DD} + 0.3 V

Storage Temperature ..... –65 °C to + 150 °C

Operating Temperature ..... –40 °C to +85 °C

Maximum ESD protection ..... 2 kV

Maximum Power Supply ..... 5.5 V

Maximum Input Current ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters

$V_{DD} = V_{DDC}$ = 3.3 V ± 10% or 2.5 V ± 5%, over the specified temperature range.

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	V_{DD} = 3.3 V, PECL_CLK single ended	1.49	–	1.825	V
		V_{DD} = 2.5 V, PECL_CLK single ended	1.10	–	1.45	
		All other inputs	V_{SS}	–	0.8	
V_{IH}	Input High Voltage	V_{DD} = 3.3 V, PECL_CLK single ended	2.135	–	2.42	V
		V_{DD} = 2.5 V, PECL_CLK single ended	1.75	–	2.0	
		All other inputs	2.0	–	V_{DD}	
I_{IL}	Input Low Current [3]		–	–	–100	µA
I_{IH}	Input High Current [3]		–	–	100	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300	–	1000	mV
V_{CMR}	Common Mode Range [4] PECL_CLK	V_{DD} = 3.3 V	V_{DD} – 2.0	–	V_{DD} – 0.6	V
		V_{DD} = 2.5 V	V_{DD} – 1.2	–	V_{DD} – 0.6	
V_{OL}	Output Low Voltage [5]	I_{OL} = 20 mA	–	–	0.4	V
V_{OH}	Output High Voltage [5]	I_{OH} = –20 mA, V_{DD} = 3.3 V	2.5	–	–	V
		I_{OH} = –20 mA, V_{DD} = 2.5 V	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3 V, Outputs @ 100 MHz, C_L = 30 pF	–	180	–	mA
		V_{DD} = 3.3 V, Outputs @ 160 MHz, C_L = 30 pF	–	270	–	
		V_{DD} = 2.5 V, Outputs @ 100 MHz, C_L = 30 pF	–	125	–	
		V_{DD} = 2.5 V, Outputs @ 160 MHz, C_L = 30 pF	–	190	–	
Z_{out}	Output Impedance	V_{DD} = 3.3 V	12	15	18	Ω
		V_{DD} = 2.5 V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Notes

2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Driving series or parallel terminated 50 Ω (or 50 Ω to V_{DD}/2) transmission lines.

Thermal Resistance

Parameter [6]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

AC Parameters

$V_{DD} = V_{DDC}$ = 3.3 V ± 10% or 2.5 V ± 5%, over the specified operating range.

Parameter [7]	Description	Conditions	Min	Typ	Max	Unit
F_{max}	Input Frequency [8]	V_{DD} = 3.3 V	–	–	200	MHz
		V_{DD} = 2.5 V	–	–	170	
T_{pd}	PECL_CLK to Q Delay [8]	V_{DD} = 3.3 V	4.0	–	8.0	ns
	TCLK to Q Delay [8]		4.4	–	8.9	
	PECL_CLK to Q Delay [8]	V_{DD} = 2.5 V	6.0	–	10.0	
	TCLK to Q Delay [8]		6.4	–	10.9	
F_{outDC}	Output Duty Cycle [8, 9, 10]	Measured at $V_{DD}/2$	45	–	55	%
t_{pZL}, t_{pZH}	Output Enable Time (all outputs)		2	–	10	ns
t_{pLZ}, t_{pHZ}	Output Disable Time (all outputs)		2	–	10	ns
T_{skew}	Output-to-Output Skew [8, 10]		–	150	250	ps
$T_{skew(pp)}$	Part-to-Part Skew [11]	PECL_CLK to Q	–	–	1.5	ns
		TCLK to Q	–	–	2.0	
T_s	Set-up Time [8, 12]	SYNC_OE to PECL_CLK	1.0	–	–	ns
		SYNC_OE to TCLK	0.0	–	–	
T_h	Hold Time [8, 12]	PECL_CLK to SYNC_OE	0.0	–	–	ns
		TCLK to SYNC_OE	1.0	–	–	
T_r/T_f	Output Clocks Rise/Fall Time [10]	0.8 V to 2.0 V, V_{DD} = 3.3 V	0.20	–	1.0	ns
		0.6 V to 1.8 V, V_{DD} = 2.5 V	0.20	–	1.3	

Notes
6. These parameters are guaranteed by design and are not tested.
7. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
8. Outputs driving 50Ω transmission lines.
9. 50% input duty cycle.
10. See Figure 3 on page 7 and Figure 4 on page 7.
11. Part-to-Part skew at a given temperature and voltage.
12. Setup and hold times are relative to the falling edge of the input clock.

Figure 3. LVCMOS_CLK CY29948 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

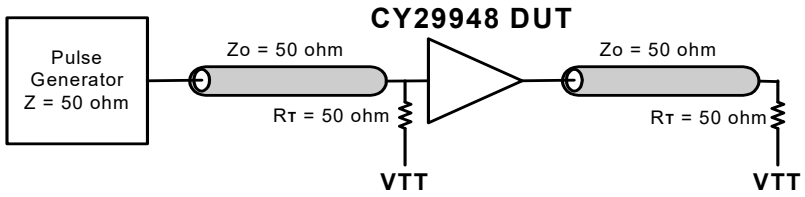


Figure 4. PECL_CLK CY29948 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

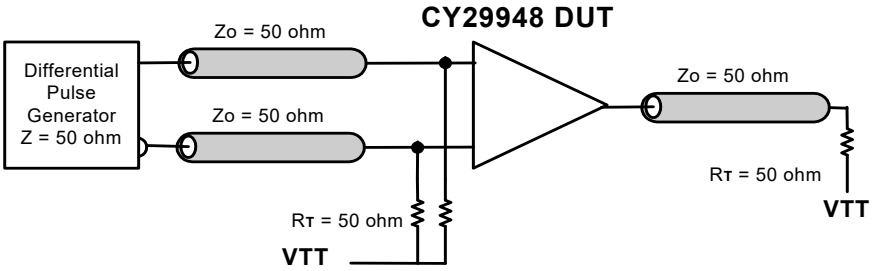


Figure 5. Propagation Delay (t_{PD}) Test Reference

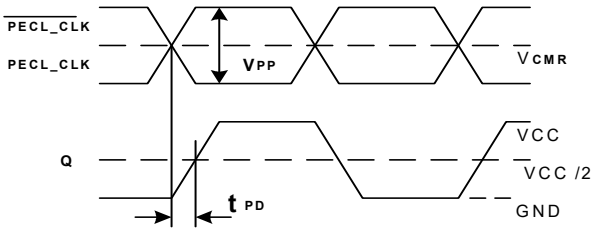


Figure 6. LVCMOS Propagation Delay (t_{PD}) Test Reference

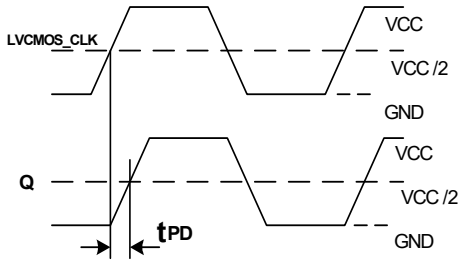


Figure 7. Output Duty Cycle (F_{outDC})

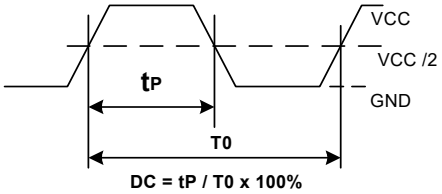
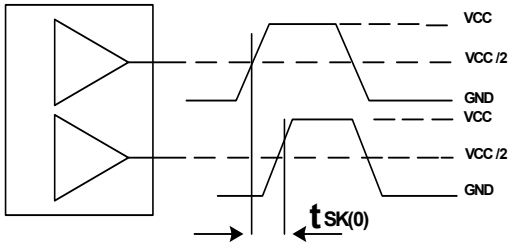


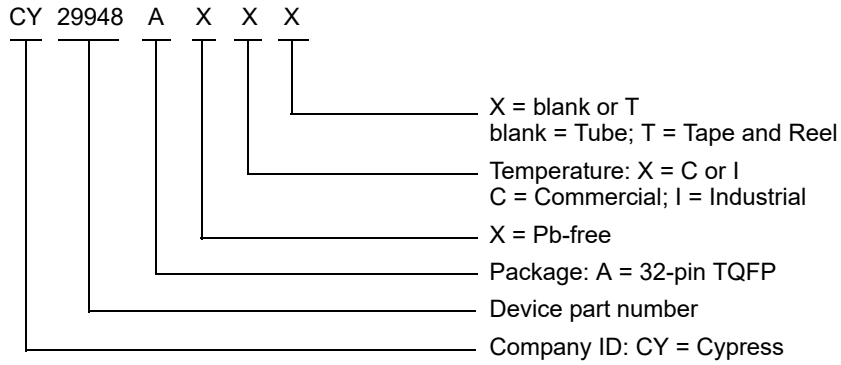
Figure 8. Output-to-Output Skew tsk(0)



Ordering Information

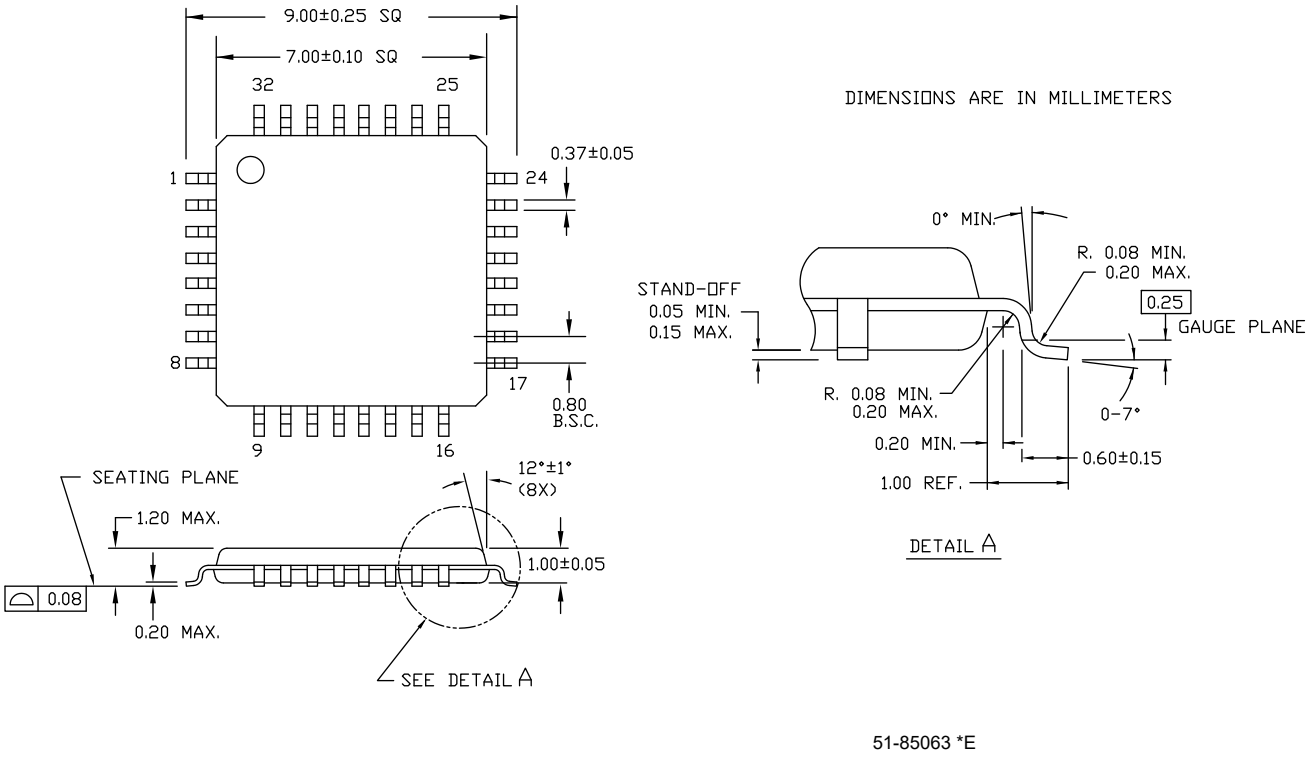
Part Number	Package Type	Production Flow
Pb-free		
CY29948AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29948AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to +70 °C
CY29948AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29948AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin TQFP (7 × 7 × 1.0 mm) Package Outline, 51-85063



51-85063 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
I/O	Input/Output
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document Revision History

Document Title: CY29948, 2.5 V or 3.3 V, 200 MHz, 1:12 Clock Distribution Buffer Document Number: 38-07288				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	111099	BRK	02/13/2002	New data sheet.
*A	116782	HWT	08/14/2002	Added Commercial Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*B	122880	RBI	12/22/2002	Updated Maximum Ratings: Added Note 2 and referred the same note in “maximum ratings”.
*C	428221	RGL	02/21/2006	Updated Ordering Information: Updated part numbers. Updated to new template.
*D	2904731	CXQ	04/05/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85063 – Changed revision from *B to *C. Updated to new template.
*E	3246222	CXQ	05/02/2011	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*F	3859773	AJU	01/07/2013	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85063 – Changed revision from *C to *D.
*G	4345036	XHT	04/14/2014	Updated to new template. Completing Sunset Review.
*H	4586288	XHT	12/03/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*I	5275785	PSR	05/18/2016	Added Thermal Resistance. Updated Package Diagrams: spec 51-85063 – Changed revision from *D to *E. Updated to new template.
*J	6142409	XHT	04/17/2018	Updated to new template. Completing Sunset Review.

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