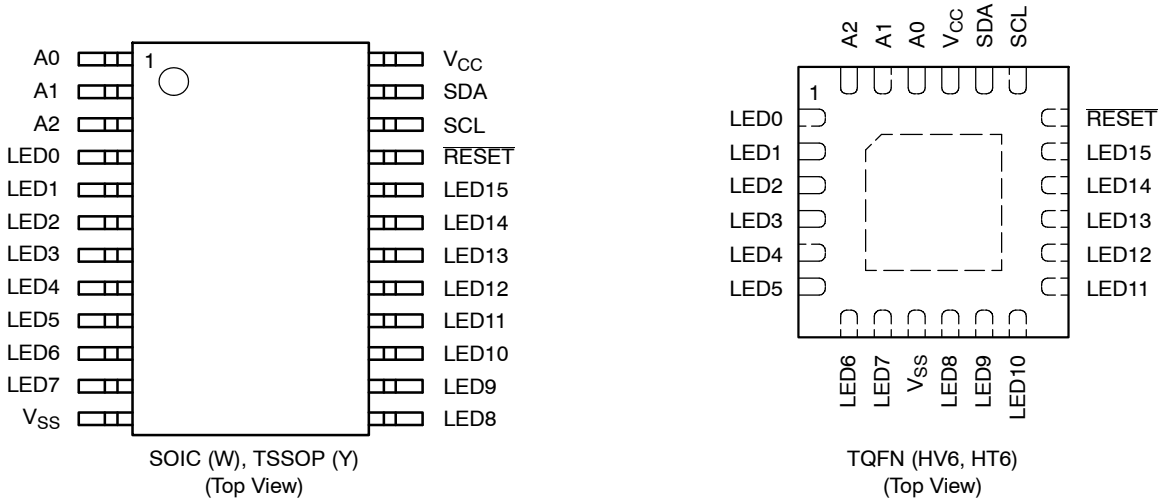


Figure 1. Pin Configurations

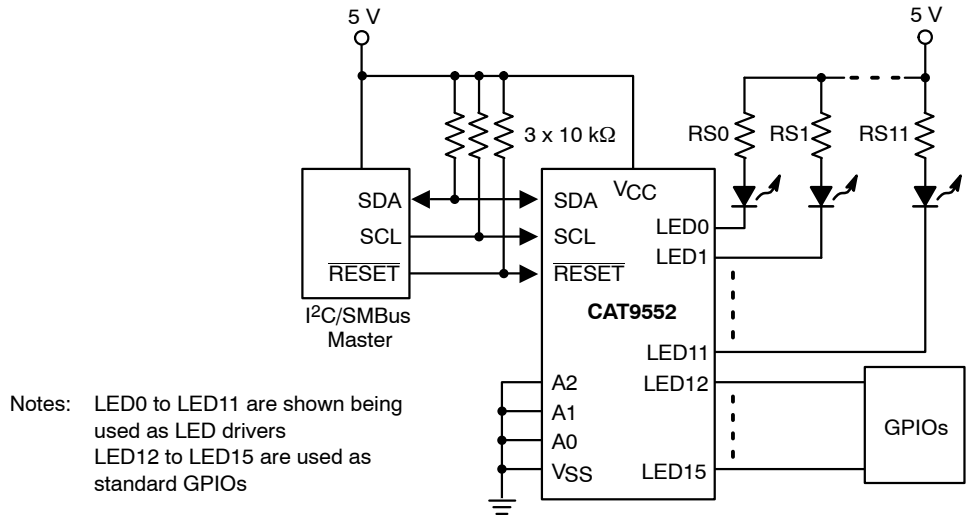


Figure 2. Typical Application Circuit

Table 1. PIN DESCRIPTION

SOIC / TSSOP	TQFN	Pin Name	Function
1	22	A0	Address Input 0
2	23	A1	Address Input 1
3	24	A2	Address Input 2
4–11	1–8	LED0 – LED7	LED Driver Output 0 to 7, I/O Port 0 to 7
12	9	V_{SS}	Ground
13–20	10–17	LED8 – LED15	LED Driver Output 8 to 15, I/O Port 8 to 15
21	18	$\overline{\text{RESET}}$	Reset Input
22	19	SCL	Serial Clock
23	20	SDA	Serial Data
24	21	V_{CC}	Power Supply
–	Pad	Backside pad	For enhanced heat dissipation. Electrically this pad must be at ground potential.

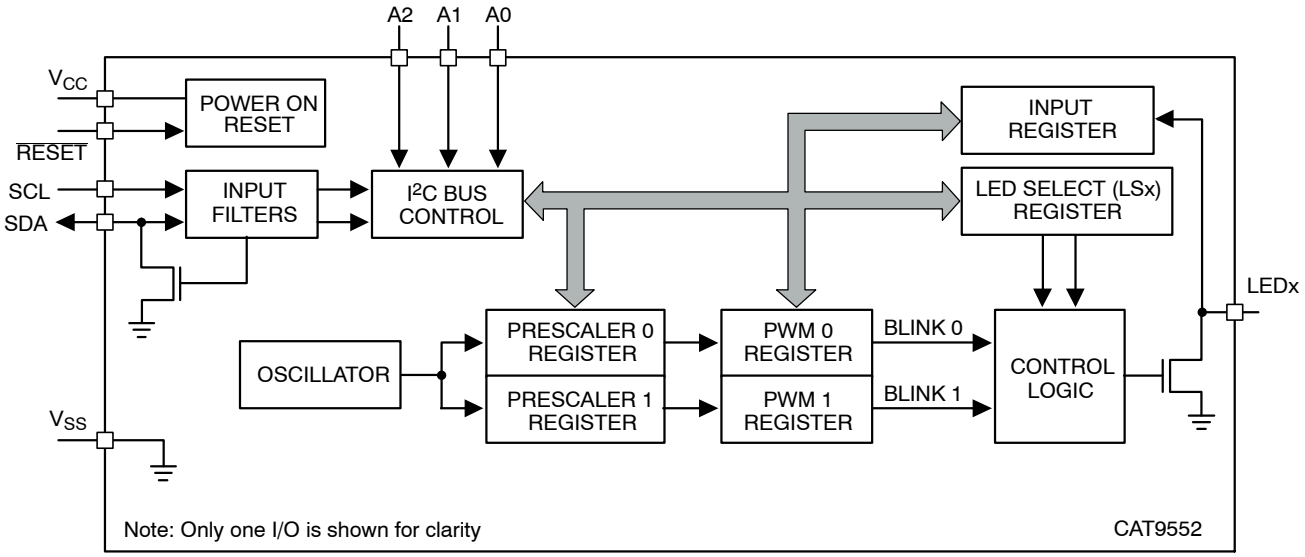


Figure 3. Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	−2.0 to +7.0	V
Voltage on Any Pin with Respect to Ground	−0.5 to +5.5	V
DC Current on I/Os	±25	mA
Supply Current	200	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C
Lead Soldering Temperature (10 seconds)	300	°C
Operating Ambient Temperature	−40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V, V_{SS} = 0 V; T_A = −40°C to +85°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply Voltage		2.3	–	5.5	V
I_{CC}	Supply Current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	–	250	550	μA
I_{stb}	Standby Current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{SS} or V_{CC}, f_{SCL} = 0 kHz	–	2.1	5.0	μA
ΔI_{stb}	Additional Standby Current	Standby mode; V_{CC} = 5.5 V; every LED I/O = V_{IN} = 4.3 V, f_{SCL} = 0 kHz	–	–	2	mA
V_{POR} (Note 1)	Power−on Reset Voltage	V_{CC} = 3.3 V, No load; V_I = V_{CC} or V_{SS}	–	1.5	2.2	V
SCL, SDA, $\overline{\text{RESET}}$						
V_{IL} (Note 2)	Low Level Input Voltage		−0.5	–	0.3 V_{CC}	V
V_{IH} (Note 2)	High Level Input Voltage		0.7 V_{CC}	–	5.5	V
I_{OL}	Low Level Output Current	V_{OL} = 0.4 V	3	–	–	mA
I_{IL}	Leakage Current	V_I = V_{CC} = V_{SS}	−1	–	+1	μA
C_I (Note 3)	Input Capacitance	V_I = V_{SS}	–	–	6	pF
C_O (Note 3)	Output Capacitance	V_O = V_{SS}	–	–	8	pF
A0, A1, A2						
V_{IL} (Note 2)	Low Level Input Voltage		−0.5	–	0.8	V
V_{IH} (Note 2)	High Level Input Voltage		2.0	–	5.5	V
I_{IL}	Input Leakage Current		−1	–	1	μA
I/Os						
V_{IL} (Note 2)	Low Level Input Voltage		−0.5	–	0.8	V
V_{IH} (Note 2)	High Level Input Voltage		2.0	–	5.5	V
I_{OL} (Note 4)	Low Level Output Current	V_{OL} = 0.4 V; V_{CC} = 2.3 V	9	–	–	mA
		V_{OL} = 0.4 V; V_{CC} = 3.0 V	12	–	–	
		V_{OL} = 0.4 V; V_{CC} = 5.0 V	15	–	–	
		V_{OL} = 0.7 V; V_{CC} = 2.3 V	15	–	–	
		V_{OL} = 0.7 V; V_{CC} = 3.0 V	20	–	–	
		V_{OL} = 0.7 V; V_{CC} = 5.0 V	25	–	–	
I_{IL}	Input Leakage Current	V_{CC} = 3.6 V; V_I = V_{SS} or V_{CC}	−1	–	1	μA
$C_{I/O}$ (Note 3)	Input/Output Capacitance		–	–	8	pF

1. V_{DD} must be lowered to 0.2 V in order to reset the device.
2. V_{IL} min and V_{IH} max are reference values only and are not tested.
3. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
4. The output current must be limited to a maximum 25 mA per each I/O; the total current sunk by all I/O must be limited to 200 mA (or 100 mA for eight I/Os)

Table 4. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified) (Note 5)

Symbol	Parameter	Standard I²C		Fast I²C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 6)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 6)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
PORT TIMING						
t_{PV}	Output Data Valid				200	ns
t_{PS}	Input Data Setup Time			100		ns
t_{PH}	Input Data Hold Time			1		μs
RESET						
t_W (Note 6)	Reset Pulse Width			10		ns
t_{REC}	Reset Recovery Time			0		ns
t_{RESET} (Note 7)	Time to Reset			400		ns

5. Test conditions according to “AC Test Conditions” table.
6. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
7. The full delay to reset the part will be the sum of t_{RESET} and the RC time constant of the SDA line.

Table 5. AC TEST CONDITIONS

Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}
Input Rise and Fall Times	≤5 ns
Input Reference Voltage	0.3 V_{CC}, 0.7 V_{CC}
Output Reference Voltage	0.5 V_{CC}
Output Load	Current source: I_{OL} = 3 mA; 400 pF for $f_{SCL(max)}$ = 400 kHz

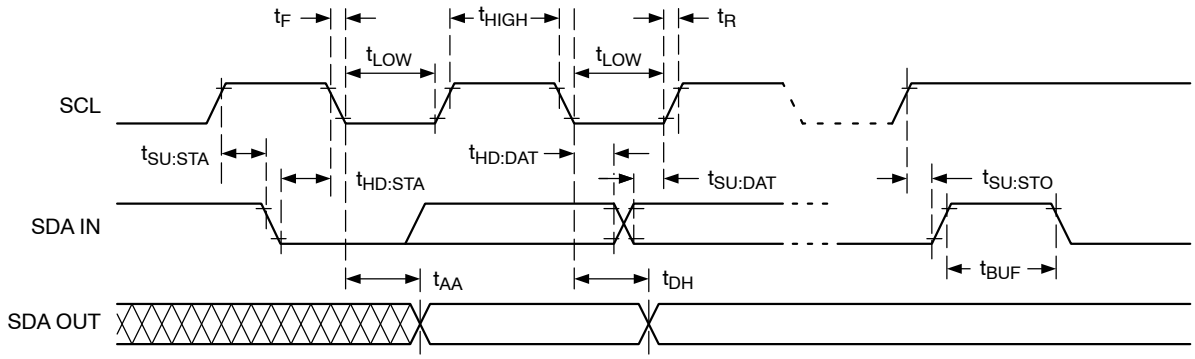


Figure 4. 2−Wire Serial Interface Timing

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{CC}.

LED0−LED15: LED Driver Outputs/General Purpose I/Os

These pins are open drain outputs used to directly drive LEDs. Any of these pins can be programmed to drive the LED ON, OFF, or to Blink Rate1 or Blink Rate2. A current limiting resistor should be placed in series with each LED to control the maximum LED current. When not used for controlling the LEDs, these pins may be used as general purpose parallel input/output.

$\overline{\text{RESET}}$: External Reset Input

Active low Reset input is used to initialize the CAT9552 internal registers and the I^2C state machine. The internal registers are held in their default state while Reset input is active. An external pull−up resistor of maximum 25 kΩ is required when this pin is not actively driven.

Functional Description

The CAT9552 is a 16−channel I/O bus expander that provides a pair of programmable LED blinkers, controlled through an I^2C compatible serial interface.

The CAT9552 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9552 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 5).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9552 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9552 for a read or write operation. The four most significant bits of the slave address are fixed as binary 1100 (Figure 6). The CAT9552 uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7−bit slave address is the R/W bit that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the CAT9552 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9552 then performs a read or a write operation depending on the state of the R/W bit.

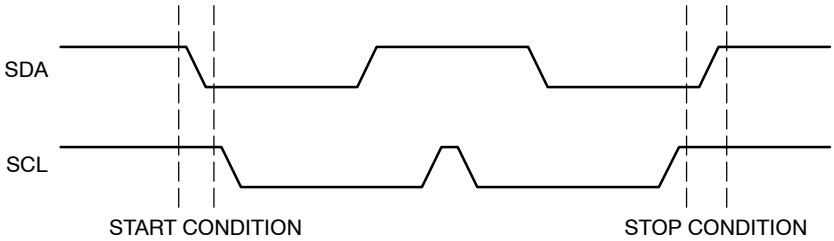


Figure 5. Start/Stop Timing

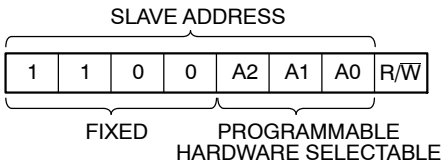


Figure 6. CAT9552 Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 7).

The CAT9552 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8− bit byte.

When the CAT9552 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9552 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT9552 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

After the successful acknowledgement of the slave address, the bus master will send a command byte to the CAT9552 which will be stored in the Control Register. The format of the Control Register is shown in Figure 8.

The Control Register acts as a pointer to determine which register will be written or read. The four least significant bits, B0, B1, B2, B3, are used to select which internal register is accessed, according to the Table 6.

If the auto increment flag is set (AI = 1), the four least significant bits of the Control Register are automatically incremented after a read or write operation. This allows the user to access the CAT9552 internal registers sequentially. The content of these bits will rollover to “0000” after the last register is accessed.

Table 6. INTERNAL REGISTERS SELECTION

B3	B2	B1	B0	Register Name	Type	Register Function
0	0	0	0	INPUT0	READ	Input Register 0
0	0	0	1	INPUT1	READ	Input Register 1
0	0	1	0	PSC0	READ/WRITE	Frequency Prescaler 0
0	0	1	1	PWM0	READ/WRITE	PWM Register 0
0	1	0	0	PSC1	READ/WRITE	Frequency Prescaler 1
0	1	0	1	PWM1	READ/WRITE	PWM Register 1
0	1	1	0	LS0	READ/WRITE	LED 0−3 Selector
0	1	1	1	LS1	READ/WRITE	LED 4−7 Selector
1	0	0	0	LS2	READ/WRITE	LED 8−11 Selector
1	0	0	1	LS3	READ/WRITE	LED 12−15 Selector

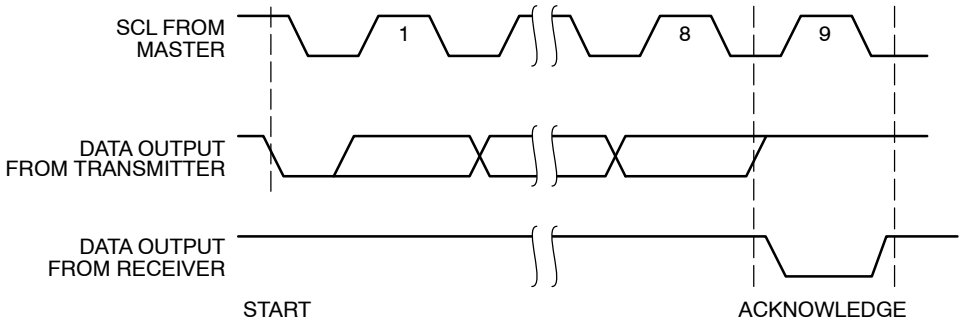


Figure 7. Acknowledge Timing

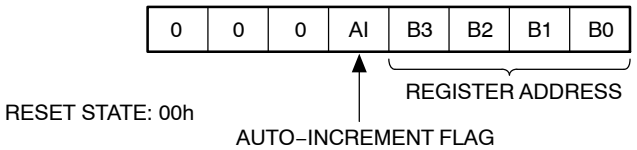


Figure 8. Control Register

Input Register 0 and Input Register 1 reflect the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output. These registers are read only ports. Writes to the input registers will be acknowledged but will have no effect.

Table 7. INPUT REGISTER 0 AND INPUT REGISTER 1

INPUT0								
	LED 7	**LED 6**	**LED 5**	**LED 4**	**LED 3**	**LED 2**	**LED 1**	**LED 0**
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X
INPUT1								
	LED 15	**LED 14**	**LED 13**	**LED 12**	**LED 11**	**LED 10**	**LED 9**	**LED 8**
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The Frequency Prescaler 0 and Frequency Prescaler 1 registers (PSC0, PSC1) are used to program the period of the pulse width modulated signals BLINK0 and BLINK1 respectively:

T_BLINK0 = (PSC0 + 1) / 44;
T_BLINK1 = (PSC1 + 1) / 44

Table 8. FREQUENCY PRESCALER 0 AND FREQUENCY PRESCALER 1 REGISTERS

PSC0								
bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1
PSC1								
bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

The PWM Register 0 and PWM Register 1 (PWM0, PWM1) are used to program the duty cycle of BLINK0 and BLINK1 respectively:

Duty Cycle_BLINK0 = (256 − PWM0) / 256;
Duty Cycle_BLINK1 = (256 − PWM1) / 256

After writing to the PWM0/1 register an 8−bit internal counter starts to count from 0 to 255. The outputs are low (LED on) when the counter value is less than the value programmed into PWM register. The LED is off when the counter value is higher than the value written into PWM register.

Table 9. PWM REGISTER 0 AND PWM REGISTER 1

PWM0								
bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0
PWM1								
bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

Every LED driver output can be programmed to one of four states, LED OFF, LED ON, LED blinks at BLINK0 rate and LED blinks at BLINK1 rate using the LED Selector Registers (Table 10).

Table 10. LED SELECTOR REGISTERS

LS0								
	LED 3		**LED 2**		**LED 1**		**LED 0**	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1
LS1								
	LED 7		**LED 6**		**LED 5**		**LED 4**	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1
LS2								
	LED 11		**LED 10**		**LED 9**		**LED 8**	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1
LS3								
	LED 15		**LED 14**		**LED 13**		**LED 12**	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

The LED output (LED0 to LED15) is set by the 2 bit value from the corresponding LSx Register (x = 0 to 3):

00 = LED Output set LOW (LED On)
01 = LED Output set Hi−Z (LED Off – Default)
10 = LED Output blinks at BLINK0 Rate
11 = LED Output blinks at BLINK1 Rate

Write Operations

Data is transmitted to the CAT9552 registers using the write sequence shown in Figure 9.

If the AI bit from the command byte is set to “1”, the CAT9552 internal registers can be written sequentially. After sending data to one register, the next data byte will be sent to the next register sequentially addressed.

Read Operations

The CAT9552 registers are read according to the timing diagrams shown in Figure 10 and Figure 11. Data from the register, defined by the command byte, will be sent serially on the SDA line.

After the first byte is read, additional data bytes may be read when the auto−increment flag, AI, is set. The additional data byte will reflect the data read from the next register sequentially addressed by the (B3, B2, B1, B0) bits of the command byte.

When reading Input Port Registers (Figure 11), data is clocked into the register on the failing edge of the acknowledge clock pulse. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

LED Pins Used as General Purpose I/O

Any LED pins not used to drive LEDs can be used as general purpose input/output, GPIO.

When used as input, the user should program the corresponding LED pin to Hi−Z (“01” for the LSx register bits). The pin state can be read via the Input Register according to the sequence shown in Figure 11.

For use as a logic output, an external pull−up resistor should be connected to the pin. The value of the pull−up resistor is calculated according to the DC operating characteristics. To set the output high, the user has to program the output Hi−Z writing “01” into the corresponding LED Selector (LSx) register bits. The output pin is set low when the output is programmed low through the LSx register bits (“00” in LSx register bits).

GPIO can also be used as PWM outputs by setting the LED Selector (LSx) register to “10” or “11” to output either the BLINK0 or BLINK1 waveform.

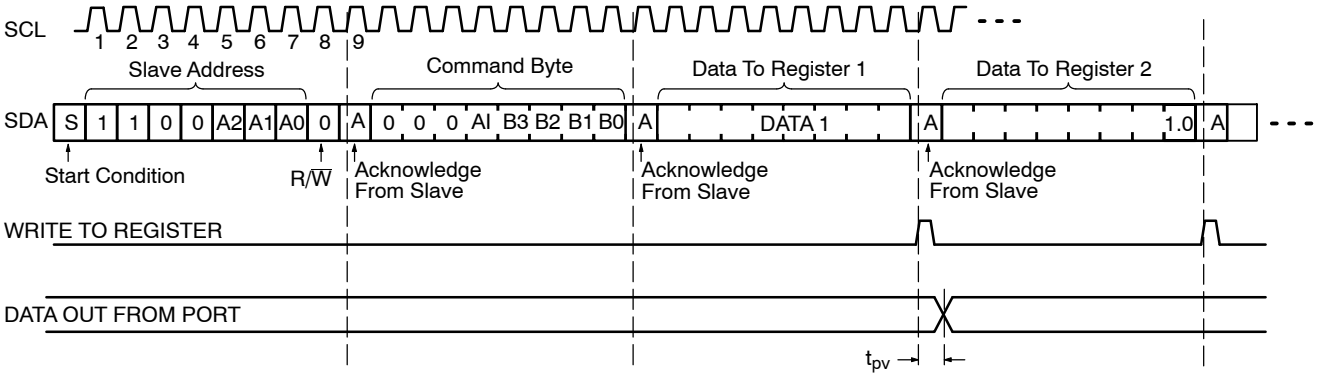


Figure 9. Write to Register Timing Diagram

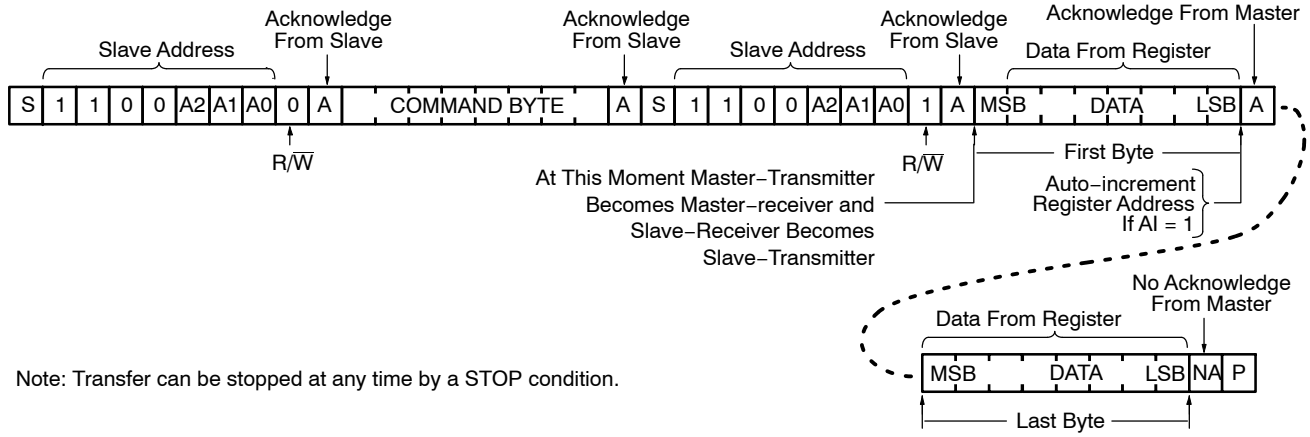


Figure 10. Read from Register Timing Diagram

External Reset Operation

The CAT9552 registers and the I^2C state machine are initialized to their default state when the RESET input is held low for a minimum of t_W. CAT9552's registers will be held in their default state until RESET returns to a logic HIGH state. The external Reset timing is shown in Figure 12.

Power−On Reset Operation

The CAT9552 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device is in a reset state for V_{CC} less than the internal POR threshold level (V_{POR}). When V_{CC} exceeds the V_{POR} level, the reset state is released and the CAT9552 internal state machine and registers are initialized to their default state. Thereafter V_{CC} must be taken below 0.2 V to reset the device.

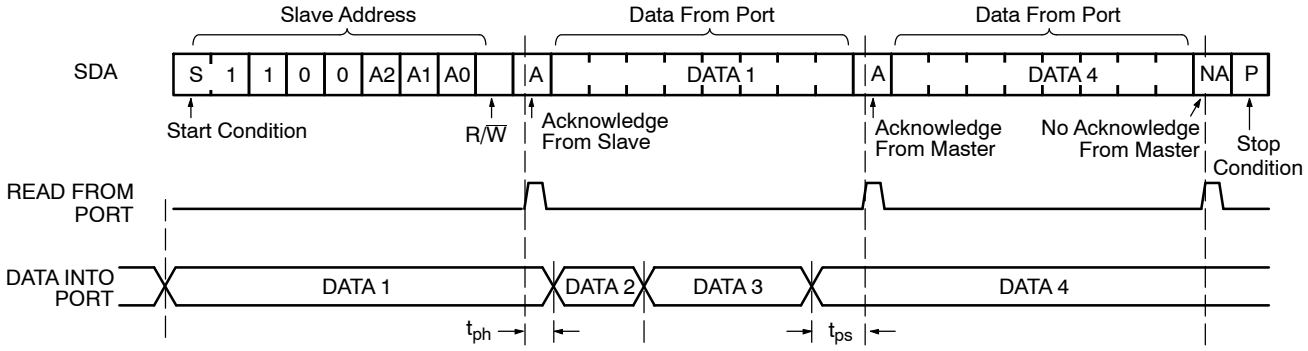


Figure 11. Read Input Port Register Timing Diagram

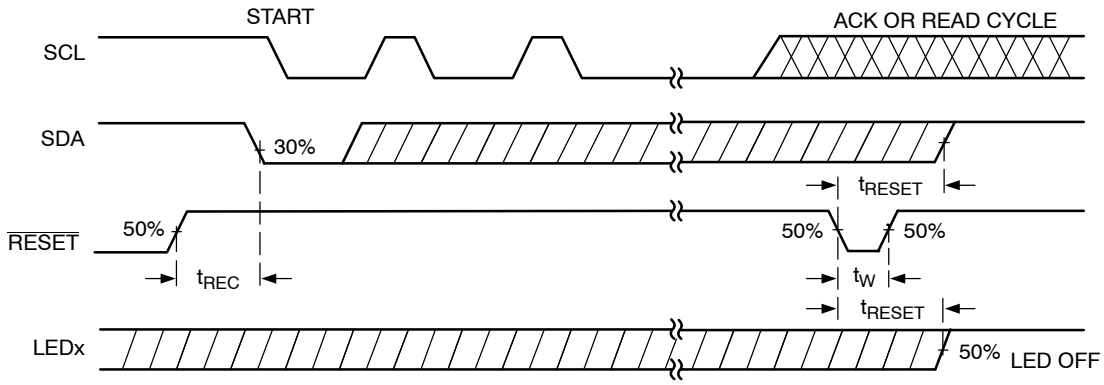


Figure 12. $\overline{\text{RESET}}$ Timing Diagram

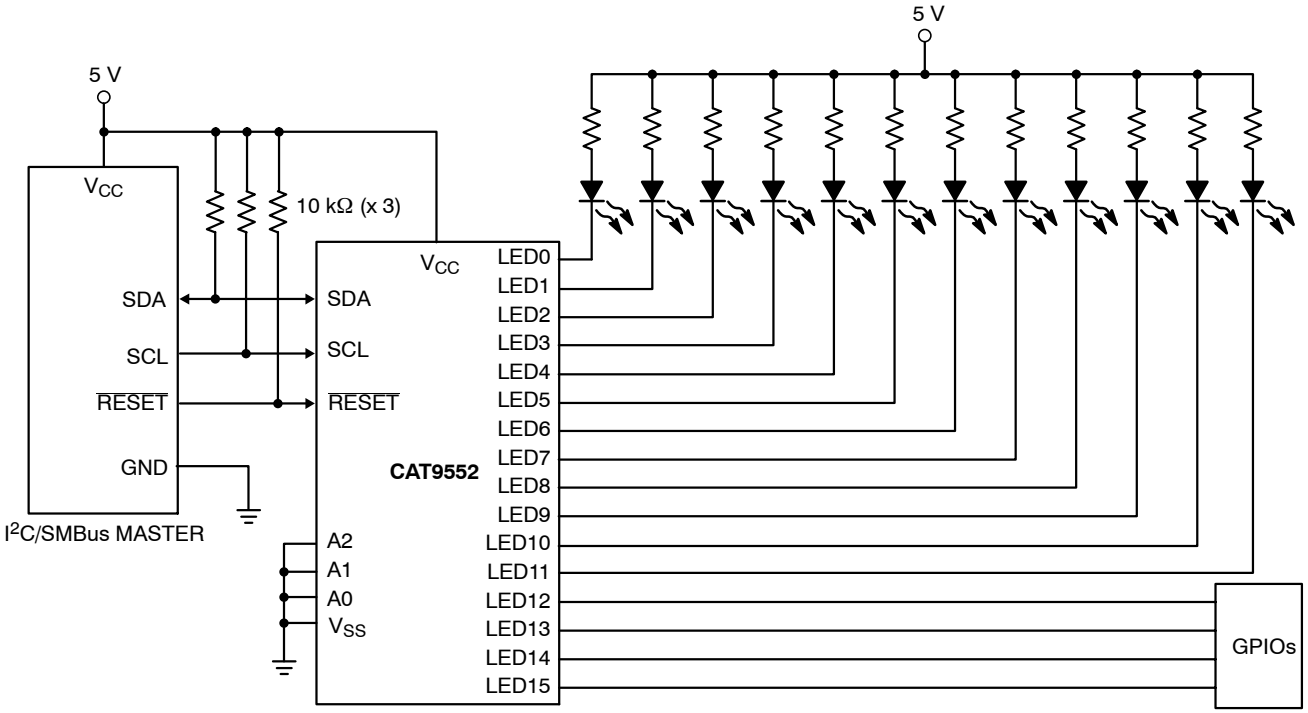
Application Information

Programming Example

The following programming sequence is an example how to set:

- LED0 to LED3: ON
- LED4 to LED7: Blink at 1 Hz with a 50% duty cycle (Blink 0)
- LED8 to LED11: Blink at 4 Hz with a 20% duty cycle (Blink 1)
- LED12 to LED15: OFF

	Command Description	I²C Data
1	START	
2	Send Slave address, A0−A2 = low	C0h
3	Command Byte: AI=”1”; PSC0 Addr	12h
4	Set Blink 0 at 1 Hz, T_Blink1 = (PSC0+1)/44 = 1 Write PSC0 = 43	2Bh
5	Set PWM0 duty cycle to 50% (256−PWM0) / 256 = 0.5 Write PWM0=128	80h
6	Set Blink 1 at 4 Hz, T_Blink1 = (PSC1+1)/44 = 0.25 Write PSC1 = 10	0Ah
7	Set PWM1 duty cycle to 25% (256−PWM1) / 256 = 0.25 Write PWM1=192	C0h
8	Write LS0: LED0 to LED3 = ON	00h
9	Write LS1: LED4 to LED7 at Blink0	AAh
10	Write LS2: LED8 to LED11 at Blink1	FFh
11	Write LS3: LED12 to LED15 = OFF	55h
12	STOP	

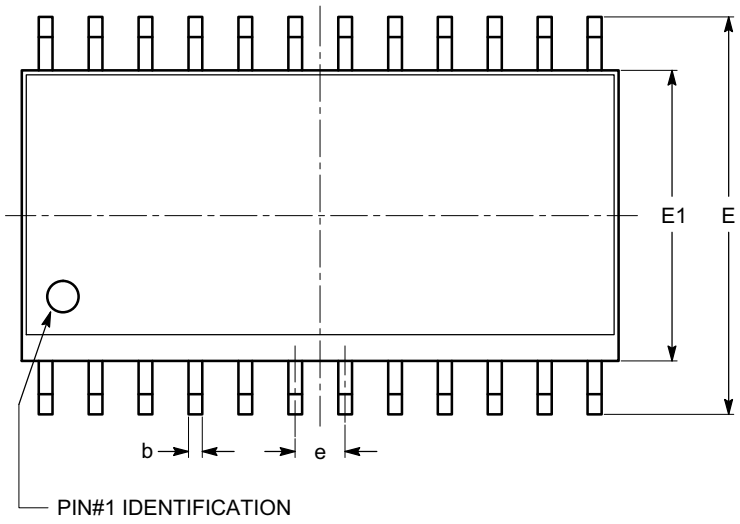


Note: LED0 to LED11 are used as LED drivers and LED12 to LED15 are used as regular GPIOs.

Figure 13. Typical Application

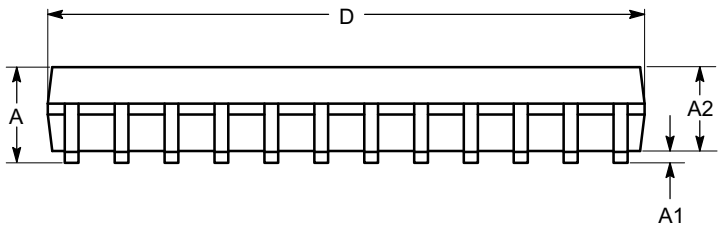
PACKAGE DIMENSIONS

SOIC−24, 300 mils
CASE 751BK−01
ISSUE O

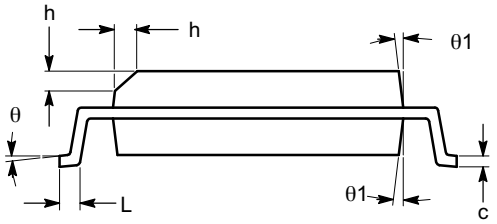


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW

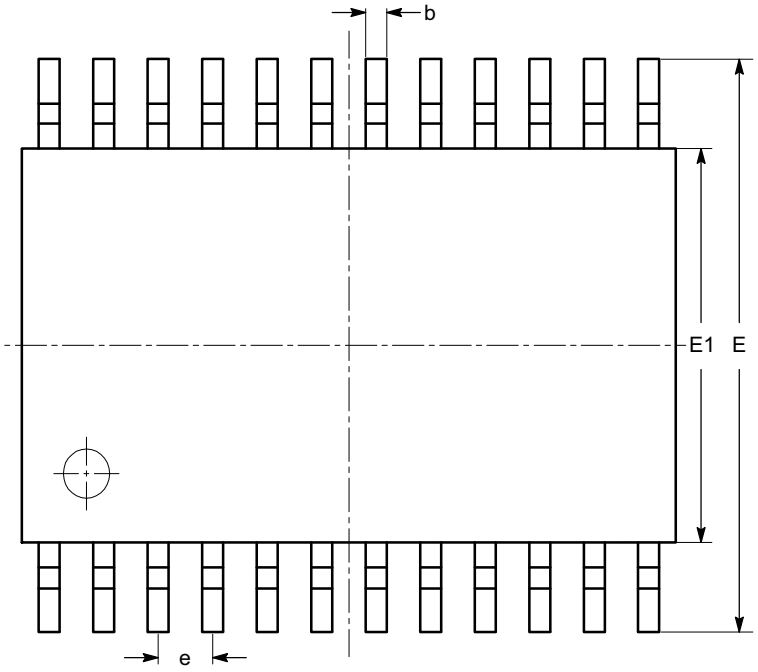


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

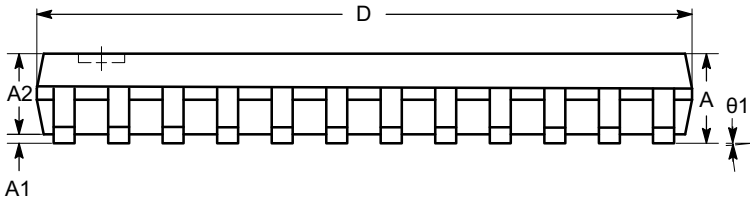
PACKAGE DIMENSIONS

TSSOP24, 4.4x7.8
CASE 948AR−01
ISSUE A

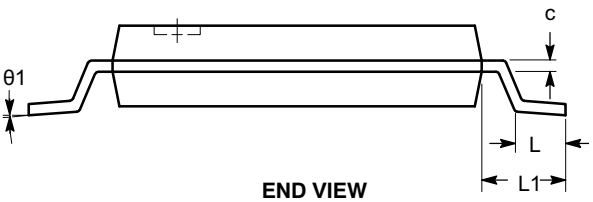


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.70
L1		1.00 REF	
θ	0°		8°



SIDE VIEW

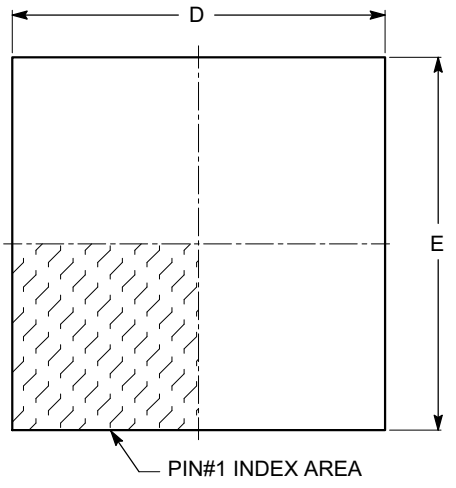


END VIEW

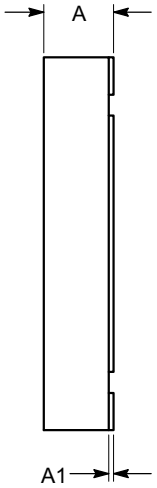
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PACKAGE DIMENSIONS

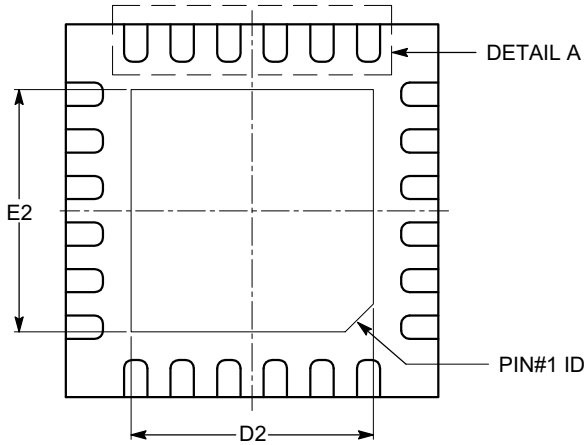
TQFN24, 4x4
CASE 510AG−01
ISSUE B



TOP VIEW

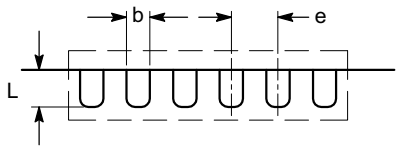


SIDE VIEW

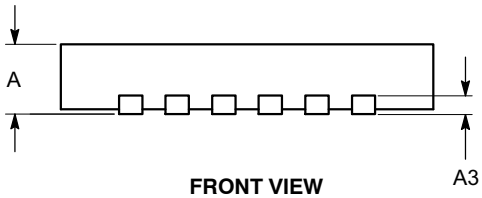


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00		0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.70	2.80	2.90
E		4.00 BSC	
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30		0.50



DETAIL A

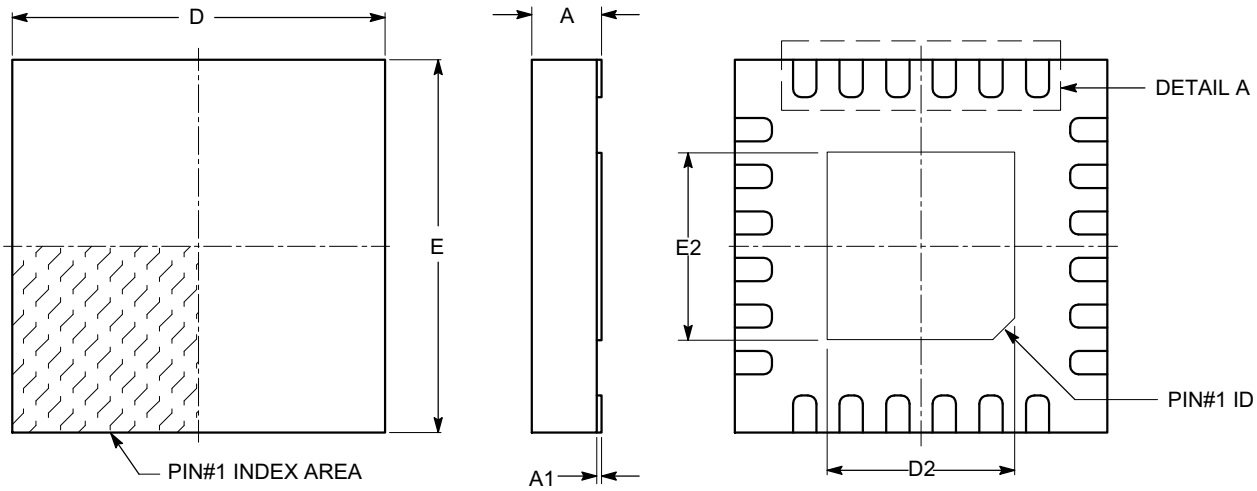


FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-220.
(3) Minimum space between leads and flag cannot be smaller than 0.15 mm.

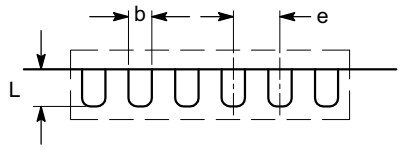
PACKAGE DIMENSIONS

TQFN24, 4x4 TA
CASE 510AN−01
ISSUE O

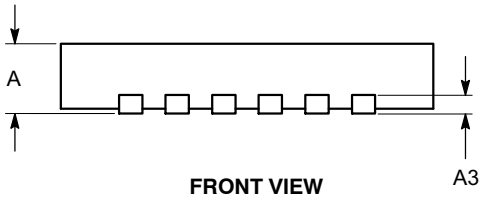


TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.00	–	2.20
E		4.00 BSC	
E2	2.00	–	2.20
e		0.50 BSC	
L	0.30	–	0.50



DETAIL A



FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-220.
(3) Minimum space between leads and flag cannot be smaller than 0.15 mm.

Table 11. ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping
CAT9552HT6I−GT2	MAAE	TQFN−24	−40°C to +85°C	NiPdAu	Tape & Reel, 2,000 Units / Reel
CAT9552HV6I−GT2	LAAE	TQFN−24	−40°C to +85°C	NiPdAu	Tape & Reel, 2,000 Units / Reel
CAT9552WI−T1	9552W	SOIC−24, JEDEC	−40°C to +85°C	Matte−Tin	Tape & Reel, 1,000 Units / Reel
CAT9552YI−T2	CAT9552Y	TSSOP−24	−40°C to +85°C	Matte−Tin	Tape & Reel, 2,000 Units / Reel

8. All packages are RoHS−compliant (Lead−free, Halogen−free).
9. For additional temperature options, please contact your nearest ON Semiconductor Sales office.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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