Typical Application Circuit

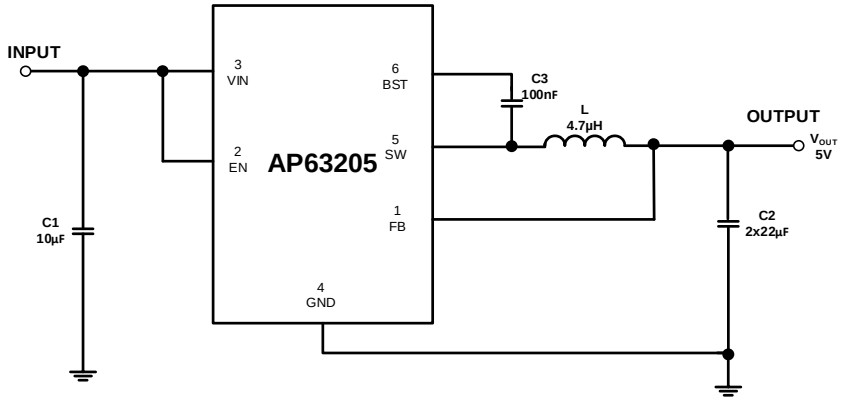


Figure 1. Typical Application Circuit

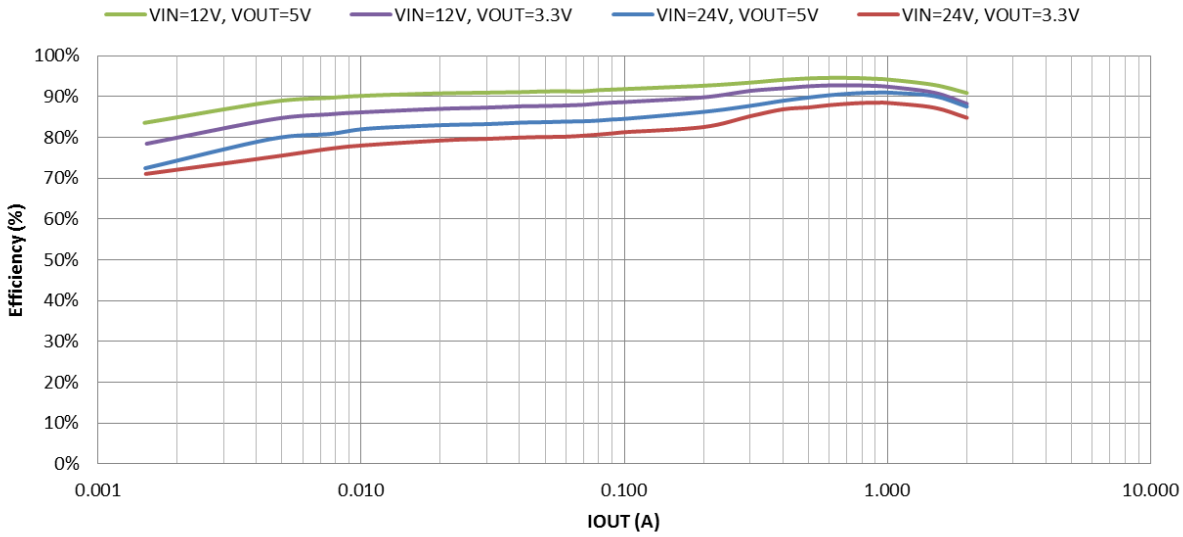


Figure 2. Efficiency vs. Output Current

Pin Descriptions

Pin Number	Pin Name	Function
1	FB	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
2	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Attach to VIN or leave open for automatic startup. The EN has a precision threshold of 1.18V for programing the UVLO. See **Enable** section for more details.
3	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 3.8V to 32V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
4	GND	Power Ground.
5	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
6	BST	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET. A 100nF capacitor is recommended from SW to BST to power the high-side switch.

Functional Block Diagram

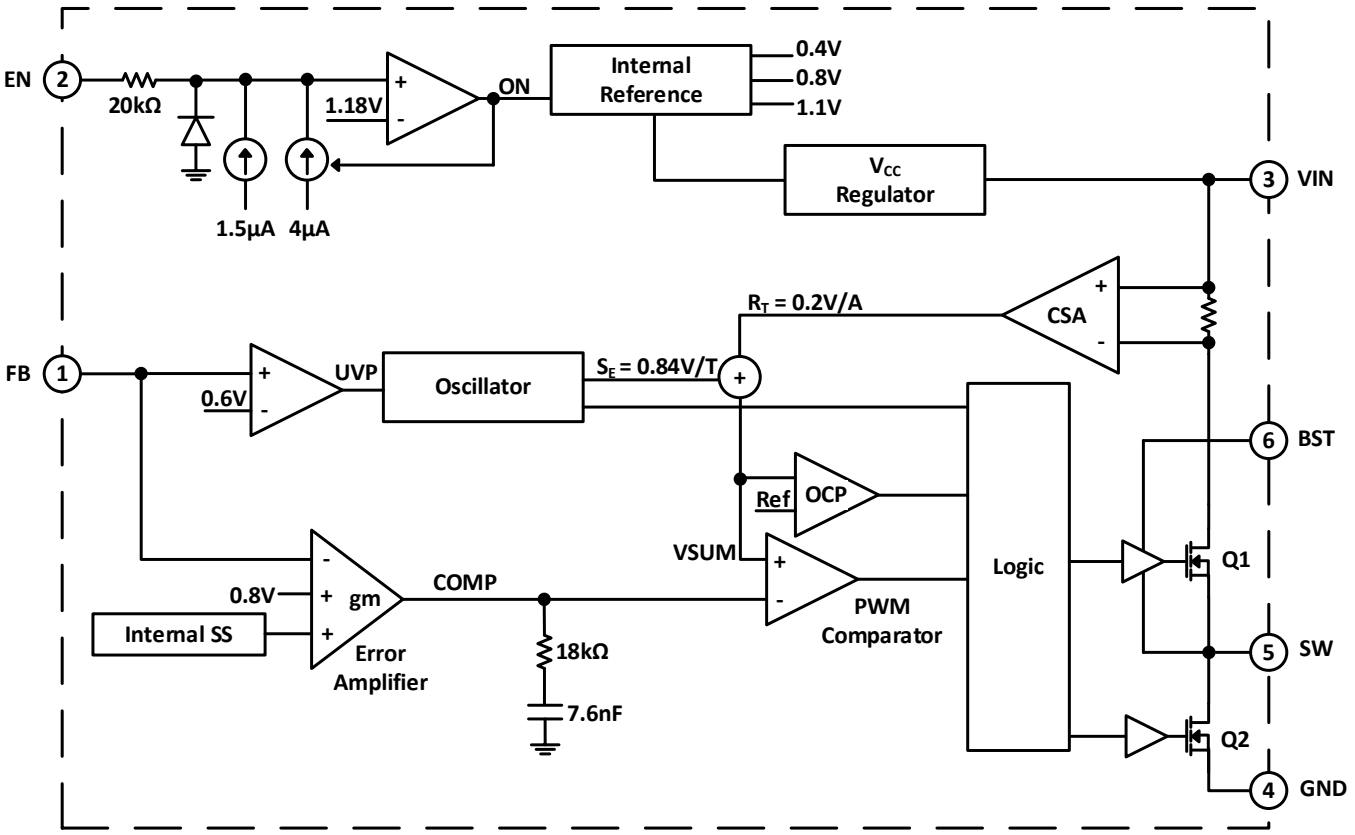


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +35.0 (DC)	V
		-0.3 to +40.0 (400ms)	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} + 0.3	V
V_{BST}	Bootstrap Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +35.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	1000	V

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	TSOT26	89	°C/W
θ_{JC}	Junction to Case	TSOT26	39	°C/W

Note: 6. Test condition for TSOT26: Device mounted on FR-4 substrate, single-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3.8	32	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics

(T_A = +25°C, V_{IN} = 12V, unless otherwise specified. Min/Max limits apply across the recommended ambient temperature range, -40°C to +85°C, and input voltage range, 3.8V to 32V).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	3	μA
I_Q	Supply Current (Quiescent)	AP63201: V_{EN} = OPEN, V_{FB} = 1.0V	—	258	—	μA
		AP63200/AP63203/AP63205: V_{EN} = OPEN, V_{FB} = 1.0V	—	22	—	μA
UVLO	V_{IN} Under Voltage Threshold (Rising)	—	3.30	3.50	3.70	V
	V_{IN} Under Voltage Threshold Hysteresis	—	—	440	—	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 8)	—	—	125	—	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 8)	—	—	68	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	—	2.5	2.8	3.1	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	—	2.5	3.2	3.9	A
f_{SW}	Oscillator Frequency	AP63200/AP63201	—	500	—	kHz
		AP63203/AP63205	—	1100	—	kHz
FSS	Frequency Spread Spectrum	—	—	±6	—	%
t_{ON}	Minimum On Time	—	—	80	—	ns
V_{FB}	Feedback Voltage	CCM, AP63200/AP63201	792	800	808	mV
		CCM, AP63203	3.27	3.30	3.33	V
		CCM, AP63205	4.95	5.00	5.05	V
V_{EN_H}	EN Logic High	—	1.15	1.18	1.23	V
V_{EN_L}	EN Logic Low	—	1.05	1.10	1.15	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.5	—	μA
		V_{EN} = 1V	—	1.5	—	μA
t_{SS}	Soft-Start Period	—	—	4	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{HYS}	Thermal Hysteresis (Note 8)	—	—	+25	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP63200 @T_A = +25°C, V_{IN} = 12V, V_{OUT} = 5V, unless otherwise specified.)

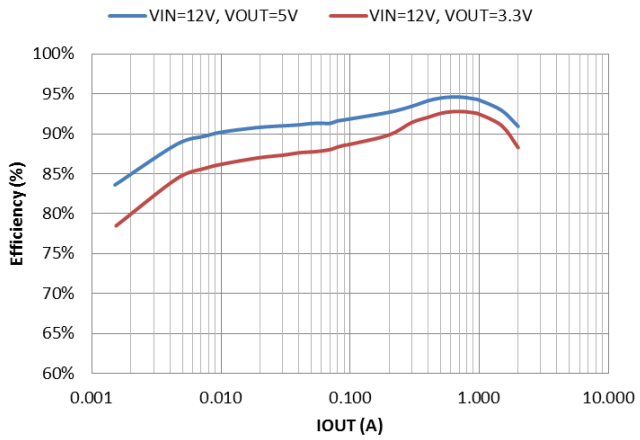


Figure 4. Efficiency vs. Output Current, VIN = 12V

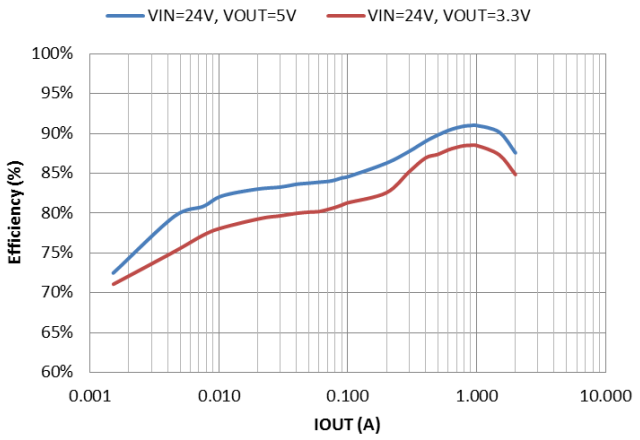


Figure 5. Efficiency vs. Output Current, VIN = 24V

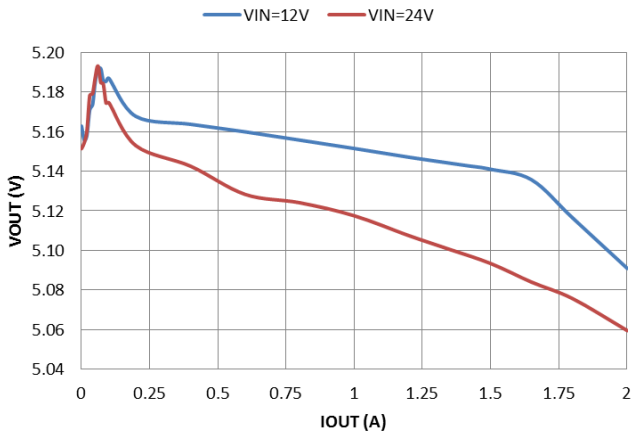


Figure 6. Load Regulation, VOUT = 5V

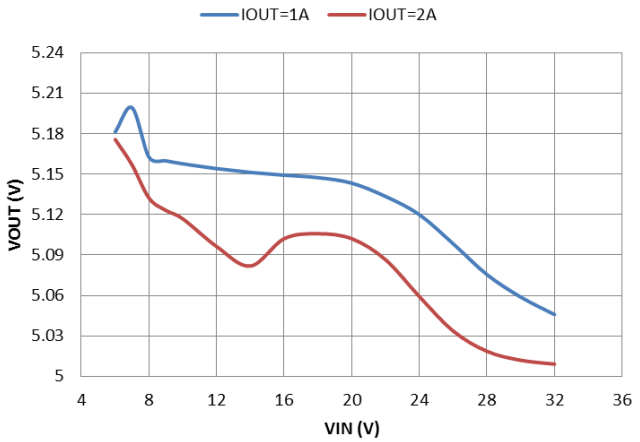


Figure 7. Line Regulation, VOUT = 5V

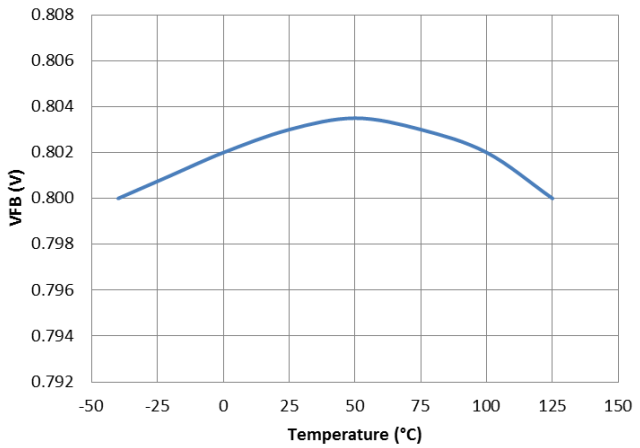


Figure 8. Feedback Voltage vs. Temperature

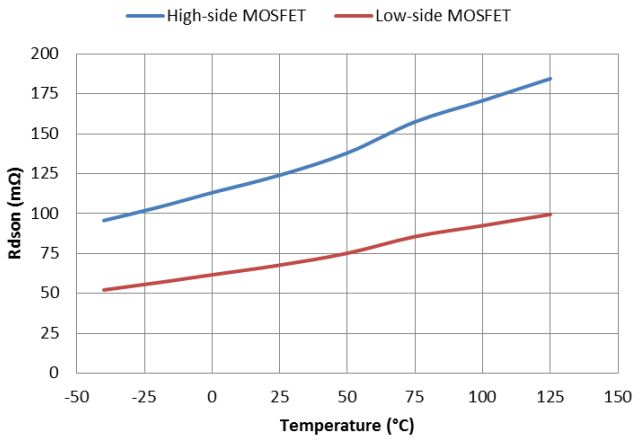


Figure 9. Power Switch $R_{DS(ON)}$ vs. Temperature

Typical Performance Characteristics (continued)

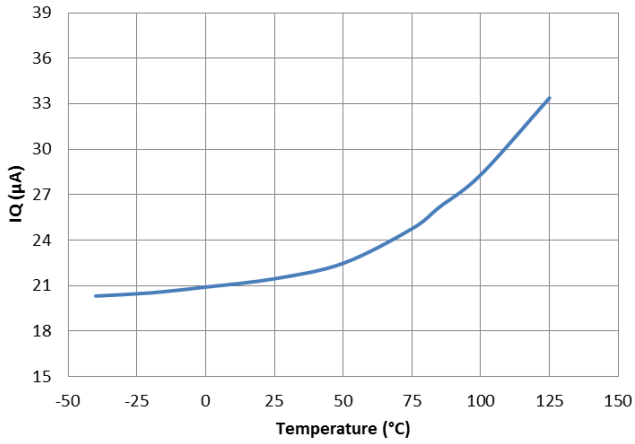


Figure 10. I_Q vs. Temperature

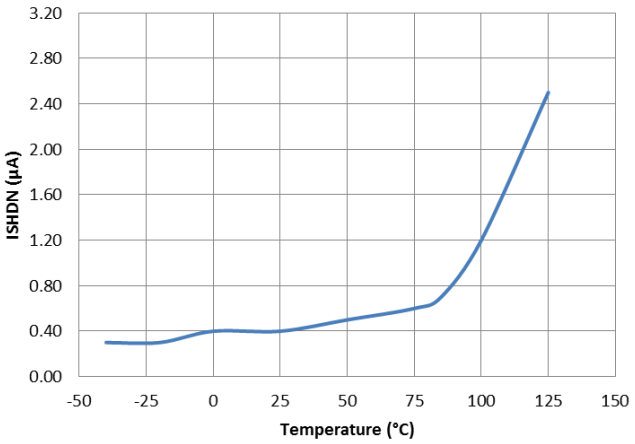


Figure 11. I_{SHDN} vs. Temperature

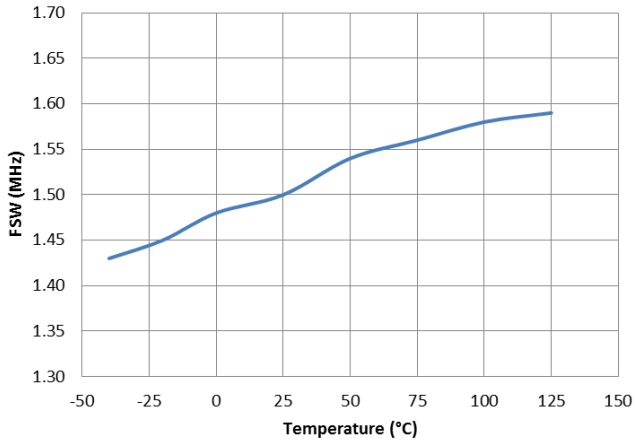


Figure 12. F_{SW} vs. Temperature

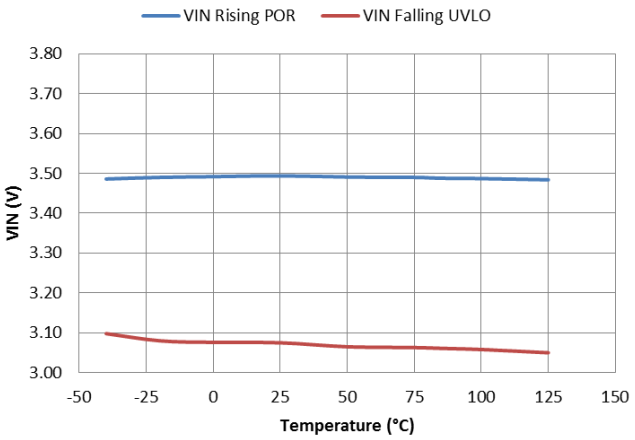


Figure 13. VIN POR and UVLO vs. Temperature

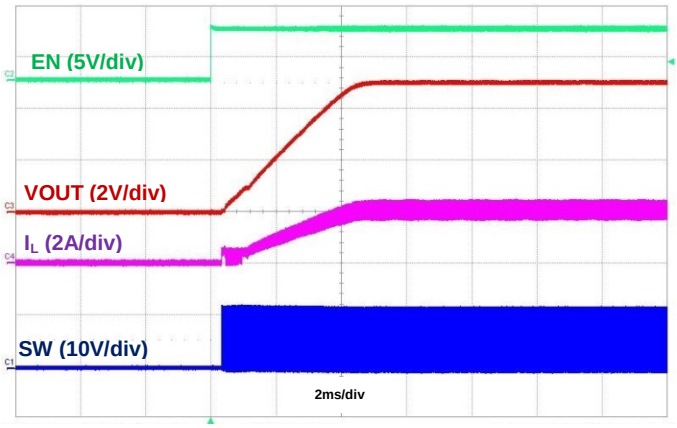


Figure 14. Startup using EN, Iout = 2A

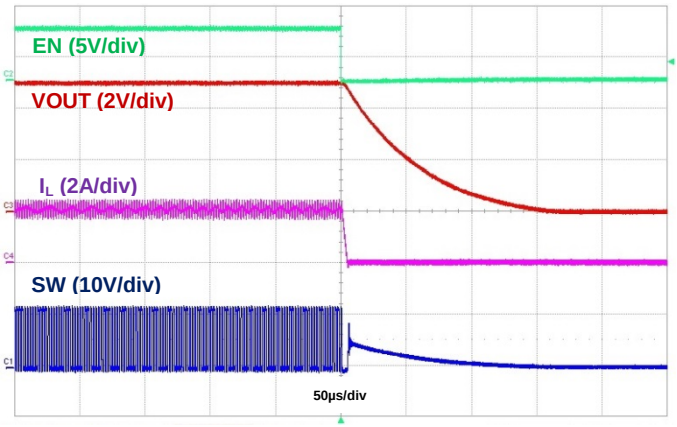


Figure 15. Shutdown using EN, Iout = 2A

Typical Performance Characteristics (continued)

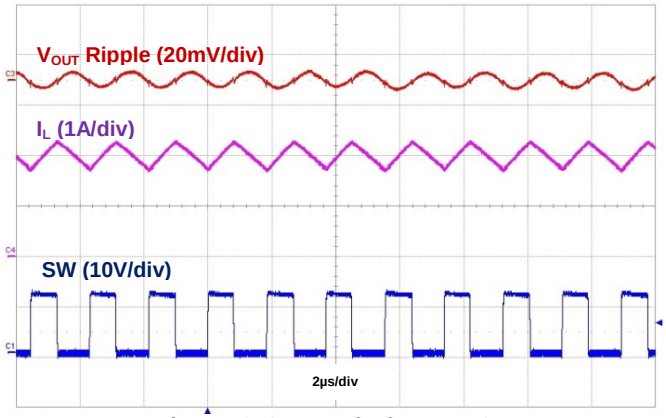


Figure 16. Output Ripple, Iout = 2A

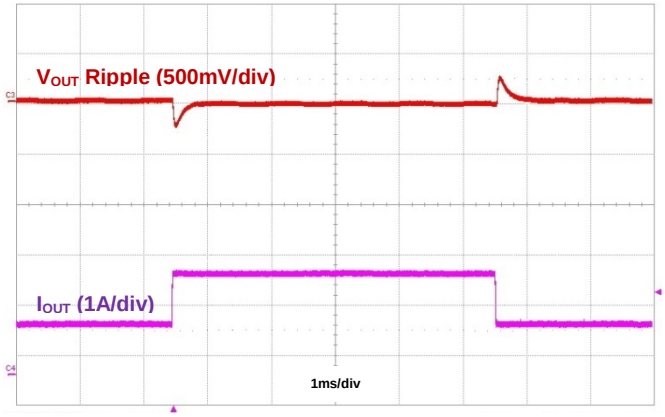


Figure 17. Load Transient, Iout = 1A to 2A

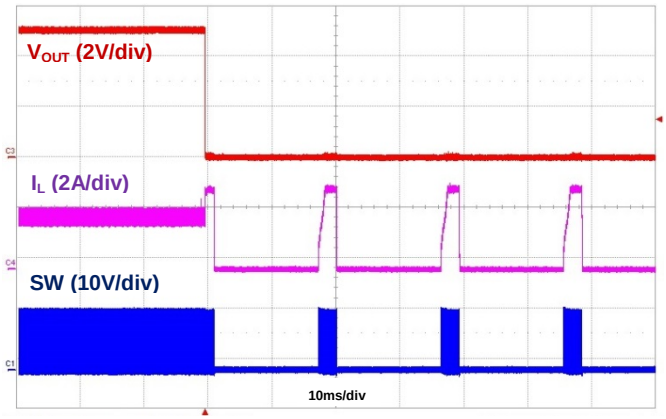


Figure 18. Output Short Protection, Iout = 2A

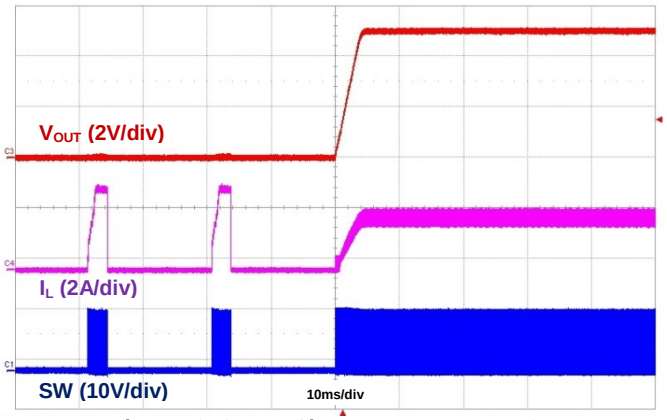


Figure 19. Output Short Recovery, Iout = 2A

Application Information

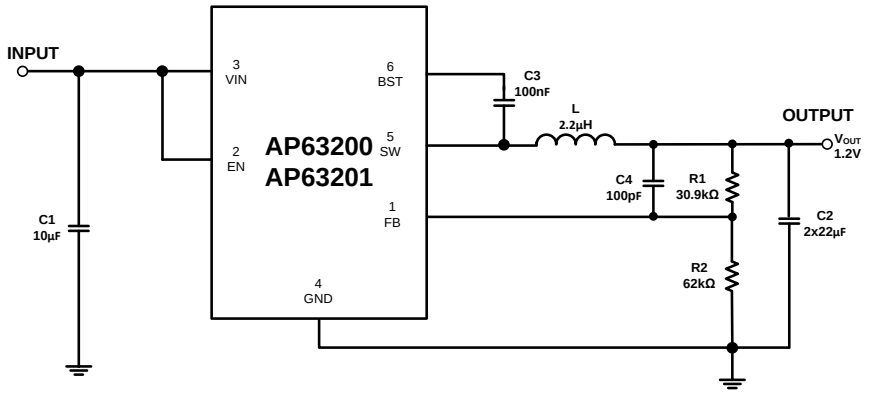


Figure 20. Typical Application Circuit of AP63200/AP63201

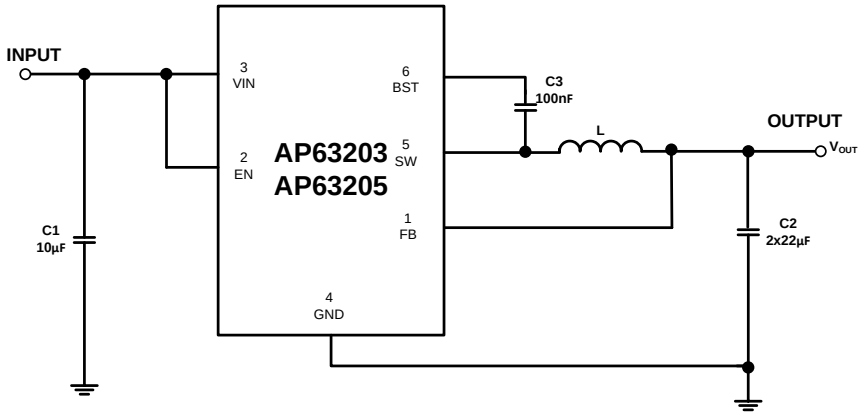


Figure 21. Typical Application Circuit of AP63203/AP63205

1 PWM Operation Control

The AP63200/AP63201/AP63203/AP63205 device is a 3.8V-to-32V input, 2A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 3. The device employs fixed-frequency peak current mode control. The internal clock's rising edge (500kHz for AP6300 and AP63201, 1.1MHz for AP63203 and AP63205) initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly, and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the internal COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off, and Q1 turns on. This sequence repeats every clock cycle.

The peak current mode control with the internal loop compensation network and built-in 4ms soft-start simplifies the AP63200/AP63201/AP63203/AP63205 footprint as well as minimizes the external component count.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The device also integrates internal slope compensation circuitry to prevent subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The AP63200/AP63201/AP63203/AP63205 device implements Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%. FSS reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. The converter further dampens high frequency radiated EMI noise through the use of its proprietary gate driver scheme to achieve a ringing-free switching node voltage without sacrificing the MOSFET switching times.

Application Information (continued)

In order to provide a small output ripple in light load conditions, the AP63201 offers a fixed 500kHz switching frequency with FSS and Pulse Width Modulation (PWM).

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The AP63200/AP63201/AP63203/AP63205 also features full protections including cycle-by-cycle high-side MOSFET peak current limit, overvoltage protection, and overtemperature protection.

2 Pulse Frequency Modulation

In heavy load conditions, the AP63200, AP63203, and AP63205 operate at forced PWM mode. The internal COMP node voltage decreases as the load current decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 450mA peak inductor current. As the load current approaches zero, the AP63200, AP63203, and AP63205 enter Pulse Frequency Modulation (PFM) to increase the converter power efficiency at light load conditions. The AP63201 remains in continuous conduction mode at light load conditions. When the inductor current decreases to zero, zero-cross detection circuitry on the low-side power MOSFET, Q2, forces it off until the beginning of the next switching cycle. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP63200, AP63203, and AP63205 work in PFM during light load conditions, they can achieve power efficiency of up to 88% at a 5mA load condition.

The quiescent current of AP63200, AP63203 and AP63205 is 22μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1μA. When applying a voltage higher than the EN upper threshold (typical 1.18V, rising), the AP63200/AP63201/AP63203/AP63205 enables all functions, and the device initiates the soft-start phase. The AP63200/AP63201/AP63203/AP63205 has a built-in 4ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its lower threshold (typical 1.1V, falling), the internal SS voltage is discharged to ground and device operation is disabled.

An internal 1.5μA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that a high on the EN pin automatically enables the device. For applications requiring a higher VIN UVLO voltage than is provided by the default setup, there is a 4μA hysteresis pull-up current source on the EN pin that configures the VIN UVLO voltage with an external resistive divider (R5 and R6) shown in Figure 22. The resistive divider resistor values are calculated by equations Eq.1 and Eq.2.

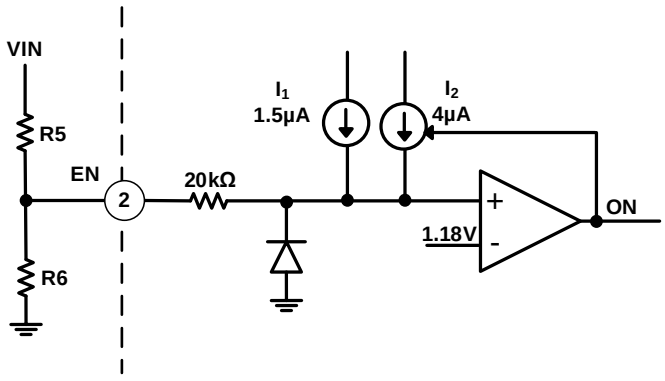


Figure 22. Programming UVLO

$$R_5 = \frac{0.932 \cdot V_{ON} - V_{OFF}}{4.1\mu A} \quad \text{Eq. 1}$$

$$R_6 = \frac{1.1R_5}{V_{OFF} - 1.1V + 5.5\mu A \cdot R_5} \quad \text{Eq. 2}$$

Where:

- V_{ON} is the rising edge voltage to enable the regulator
- V_{OFF} is the falling edge voltage to disable the regulator

Application Information (continued)

Alternatively, a small ceramic capacitor can be added from EN to GND. This delays the output startup voltage, which is useful when sequencing multiple power rails to minimize input inrush current. The amount of capacitance is calculated by equation Eq.3.

$$C_d[\mathrm{nF}] = 1.27 \cdot t_S[ms] \quad \text{Eq. 3}$$

Where:

- C_d is the time delay capacitance in nF
- t_S is the delay time in ms

The EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases.

4 Undervoltage Lockout

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP63200/AP63201/AP63203/AP63205 device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. If the input voltage falls below 3.1V, the AP63200/AP63201/AP63203/AP63205 is disabled. In this event, both the high-side and low-side power MOSFETs are turned off.

5 EMI Reduction with Frequency Spread Spectrum and Ringing-free Switching Node

In the some applications, the system must meet EMI standards. To improve EMI reduction, the AP63200/AP63201/AP63203/AP63205 adopts FSS to spread the switching noise over a wider frequency band and therefore reduces conducted and radiated interference at a particular frequency.

In buck converters, the switching node's (SW's) ringing amplitude and cycles are critical, especially in relation to the high frequency radiation EMI noise. The AP63200/AP63201/AP63203/AP63205 device implements a multi-level gate driver scheme to achieve a ringing-free switching node without sacrificing neither the switching node's rise and fall slew rates nor the converter's power efficiency. The AP63203 and AP63205 also have the feature to remove the resonance ringing of the SW pin when the inductor current is 0A and the device operates in PFM. The zoomed in waveform for SW is shown in Figure 23.

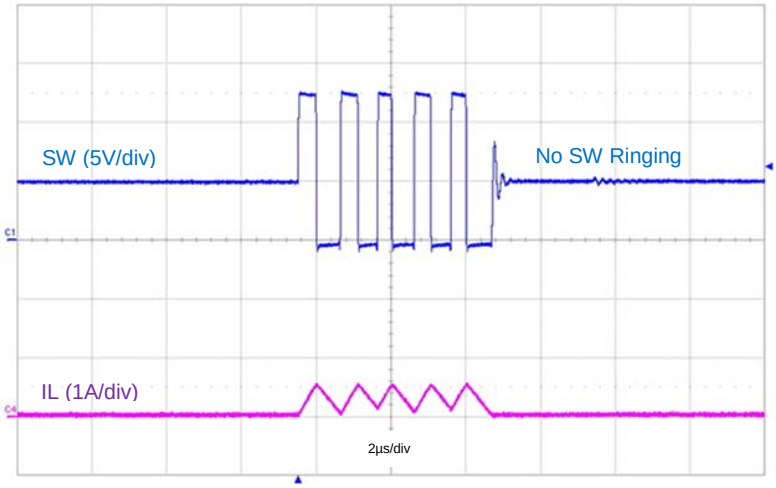


Figure 23. AP63203/AP63205 SW Node Waveform

6 Overcurrent Protection

The AP63200/AP63201/AP63203/AP63205 has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET Q1. While Q1 is on, its conduction current is monitored by the internal sensing circuitry. Once the current through Q1 exceeds the current peak limit, Q1 immediately turns off. If Q1 consistently hits the peak current limit for 2ms, the buck converter enters hiccup mode and shuts down. After 16ms of off time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

7 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +150°C, the AP63200/AP63201/AP63203/AP63205 shuts down both their high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+130°C nominal), the device initiates a normal power-up cycle with soft-start.

Application Information (continued)

8 Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$\mathbf{T_{RISE}} = \mathbf{PD} \cdot (\boldsymbol{\theta_{JA}}) \quad \textbf{Eq. 4}$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$\mathbf{T_J} = \mathbf{T_A} + \mathbf{T_{RISE}} \quad \textbf{Eq. 5}$$

Where T_A is the ambient temperature of the environment. For the TSOT26 package, the θ_{JA} is 89°C/W. The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design. A typical derating curve versus ambient temperature is shown in Figure 24.

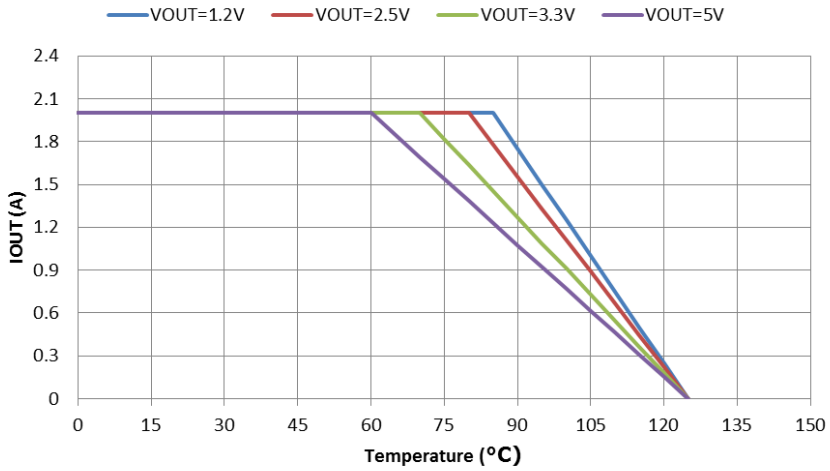


Figure 24. Output Current Derating Curve vs. Temperature, VIN = 12V

9 Setting the Output Voltage

The AP63203 and AP63205 have fixed output voltages of 3.3V and 5V, respectively. The AP63200 and AP63201 have adjustable output voltages starting from 0.8V using an external resistive divider. An optional in Figure 20, of 10pF to 220pF is used to improve the transient response. Resistor R2 is selected based on a design tradeoff between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high values of R2. R1 can be determined by the following equation:

$$\mathbf{R_1} = \boldsymbol{R_2} \cdot (\frac{\boldsymbol{V_{OUT}}}{\mathbf{0.8V}} - \mathbf{1}) \quad \textbf{Eq. 6}$$

Application Information (continued)

Table 1 shows a list of recommended component selections for common output voltages for AP6300 and AP63201 referencing Figure 20.

AP63200/AP63201							
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (μH)**	**C1 (μF)**	**C2 (μF)**	**C3 (nF)**	**C4 (pF)**
1.2	30.9	62	2.2	10	2 x 22	100	100
1.5	54.2	62	2.2	10	2 x 22	100	100
1.8	77.5	62	3.3	10	2 x 22	100	100
2.5	131	62	3.3	10	2 x 22	100	100
3.3	182	62	6.8	10	2 x 22	100	100
5	157	30	10	10	2 x 22	100	100
12	249	18	10	10	2 x 22	100	56

Table 1. Recommended Component Selections for AP63200/AP63201

Tables 2 and 3 show recommended component selections for AP63203 and AP63205 referencing Figure 21.

AP63203				
Output Voltage (V)	**L (μH)**	**C1 (μF)**	**C2 (μF)**	**C3 (nF)**
3.3	3.9	10	2 x 22	100

Table 2. Recommended Component Selections for AP63203

AP63205				
Output Voltage (V)	**L (μH)**	**C1 (μF)**	**C2 (μF)**	**C3 (nF)**
5	4.7	10	2 x 22	100

Table 3. Recommended Component Selections for AP63205

10 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{sw}} \quad \text{Eq. 7}$$

Where ΔI_L is the inductor ripple current, and f_{SW} is the buck converter switching frequency. For AP63200/AP63201/AP63203/AP63205, choose ΔI_L to be 30% to 50% of the maximum load current of 2A.

The inductor peak current is calculated by:

$$I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2} \quad \text{Eq. 8}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 2.2μH to 10μH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 100mΩ. Use a larger inductance for improved efficiency under light load conditions.

11 Input Capacitor

The input capacitor reduces the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time of Q1. It must have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMS rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic, or ceramics with low ESR should be used. If a tantalum capacitor is used it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor greater than 10μF is sufficient for most applications.

Application Information (continued)

12 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces the overshoot/undershoot of the output voltage during load transients. During the first few milliseconds of a load transient, the output capacitor supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum but the current slope is limited by the inductor value.

The output capacitor, C_{OUT}, requirements can be calculated from equations Eq. 9 and Eq. 10.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from Eq. 9:

$$V_{OUT_{Ripple}} = \Delta I_L \cdot ESR \quad \text{Eq. 9}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirement, C_{OUT} should be greater than the following calculated from Eq. 10:

$$C_{OUT} > \frac{L \cdot \left(I_{OUT} + \frac{\Delta I_L}{2}\right)^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2} \quad \text{Eq. 10}$$

Where ΔV is the maximum output overshoot voltage.

13 Bootstrap Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the BST and SW pins. A 100nF ceramic capacitor is sufficient. If the BST capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 220ns to refresh the BST capacitor and raise its voltage back above 2.85V. The BST capacitor voltage threshold is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event requires the refreshing of the BST capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low dropout mode by holding Q1 on for multiple clock cycles. To prevent the BST capacitor from discharging, Q2 is forced to refresh. The effective duty cycle is approximately 100% so that it acts as an LDO to maintain the output voltage regulation.

Layout

PCB Layout

1. The AP63200/AP63201/AP63203/AP63205 device works at 2A current load, so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Provide sufficient vias for the input and output capacitors' GND side to dissipate heat to the bottom layer.
3. Make the bottom layer under the device as the GND layer for heat dissipation. The GND layer should be as large as possible to provide better thermal effect.
4. Place the VIN capacitors as close to the device as possible.
5. Place the feedback components as close to FB as possible.
6. See Figure 25 for reference.

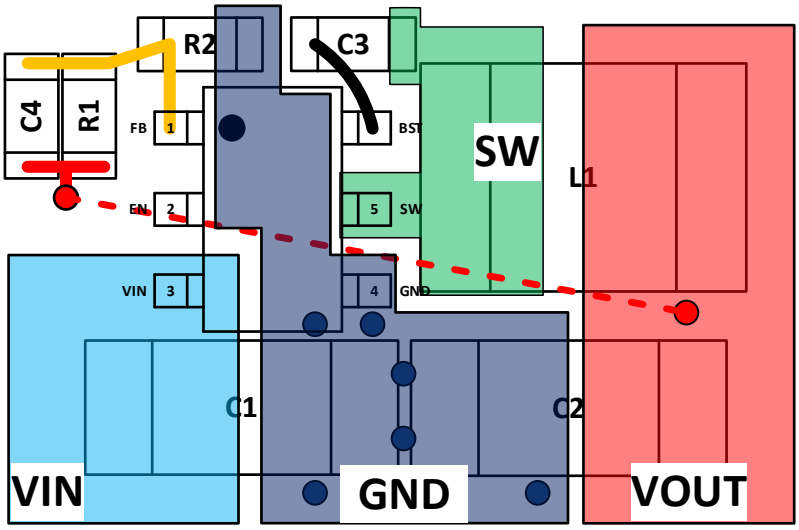


Figure 25. Recommended Layout

Ordering Information

Please see http://www.diodes.com/package-outlines.html for additional latest information such as Mechanical Data and Device Tape Orientation.

AP6320X XX - X

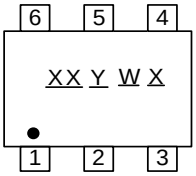
Product Version	Package	Packing
0: AP63200 1: AP63201 3: AP63203 5: AP63205	WU : TSOT26	7 : Tape & Reel

Part Number	Mode	Frequency	V_{OUT}	Package Code	Tape and Reel	
					Quantity	Part Number Suffix
AP63200WU-7	PWM/PFM	500kHz	Adjustable	WU	3000	-7
AP63201WU-7	PWM Only	500kHz	Adjustable	WU	3000	-7
AP63203WU-7	PWM/PFM	1100kHz	3.3V	WU	3000	-7
AP63205WU-7	PWM/PFM	1100kHz	5V	WU	3000	-7

Marking Information

TSOT26

(Top View)



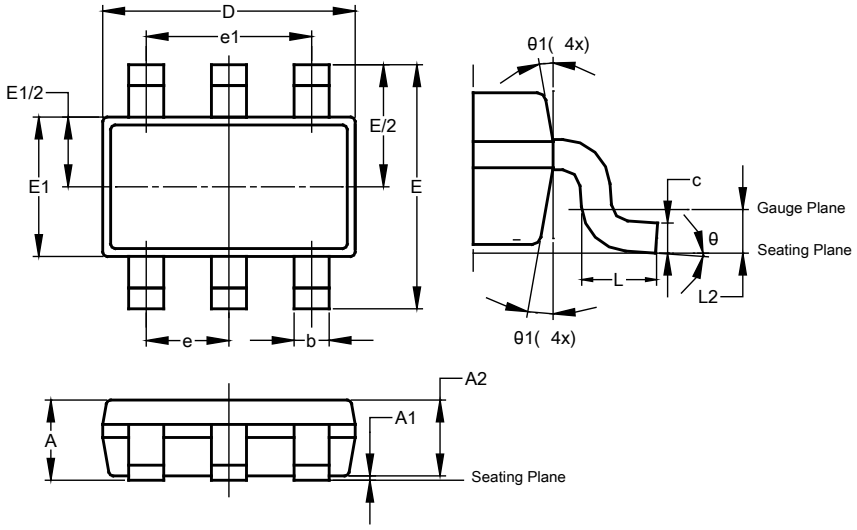
XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP63200WU-7	TSOT26	T2
AP63201WU-7	TSOT26	T3
AP63203WU-7	TSOT26	T4
AP63205WU-7	TSOT26	T5

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26

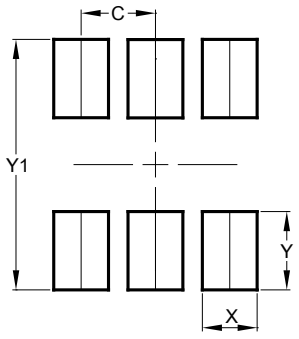


TSOT26			
Dim	**Min**	**Max**	**Typ**
A	□	1.00	—
A1	0.010	0.100	—
A2	0.840	0.900	—
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	—
c	0.120	0.200	—
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	—
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	—
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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