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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 1.

		AD9211-200			AD9211-250			AD9211-300			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			10			10			10		Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	25°C		4.3			4.6			4.4		mV
	Full	−12		+12	−13		+13	−13		+13	mV
Gain Error	25°C		1.0			1.3			1.1		% FS
	Full	−2.2		+4.3	−2.2		+4.3	−2.2		+4.3	% FS
Differential Nonlinearity (DNL)	25°C		±0.1			±0.1			±0.1		LSB
	Full	−0.5		+0.5	−0.5		+0.5	−0.5		+0.5	LSB
Integral Nonlinearity (INL)	25°C		±0.2			±0.2			±0.2		LSB
	Full	−0.35		0.35	−0.45		0.45	−0.7		+0.7	LSB
TEMPERATURE DRIFT											
Offset Error	Full		±8			±7			±6		µV/°C
Gain Error	Full		0.018			0.018			0.018		%/°C
ANALOG INPUTS (VIN+, VIN−)											
Differential Input Voltage Range[2]	Full	0.98	1.25	1.5	0.98	1.25	1.5	0.98	1.25	1.5	V p-p
Input Common-Mode Voltage	Full		1.4			1.4			1.4		V
Input Resistance (Differential)	Full		4.3			4.3			4.3		kΩ
Input Capacitance	25°C		2			2			2		pF
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Currents											
I_{AVDD}[3]	Full		134	144		158	169		189	203	mA
I_{DRVDD}[3]/SDR Mode[4]	Full		51	54		53	55		54	57	mA
I_{DRVDD}[3]/DDR Mode[5]	Full		35			38			39		mA
Power Dissipation[3]	Full										mW
SDR Mode[4]	Full		333	356		380	403		437	468	mW
DDR Mode[5]	Full		304			353			410		mW

[1] See the AN-835 application note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

[2] The input range is programmable through the SPI, and the range specified reflects the nominal values of each setting. See the Memory Map section.

[3] I_{AVDD} and I_{DRVDD} are measured with a −1 dBFS, 10.3 MHz sine input at rated sample rate.

[4] Single data rate mode; this is the default mode of the AD9211.

[5] Double data rate mode; user-programmable feature. See the Memory Map section.

AC SPECIFICATIONS[1]

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 2.

Parameter[2]	Temp	AD9211-200 Min	AD9211-200 Typ	AD9211-200 Max	AD9211-250 Min	AD9211-250 Typ	AD9211-250 Max	AD9211-300 Min	AD9211-300 Typ	AD9211-300 Max	Unit
SNR											
f_{IN} = 10 MHz	25°C	59.0	59.5		58.9	59.4		58.6	59.2		dB
	Full	58.9			58.7			57.5			dB
f_{IN} = 70 MHz	25°C	58.9	59.3		58.8	59.3		58.5	59.1		dB
	Full	58.8			58.7			57.0			dB
f_{IN} = 170 MHz	25°C	58.5	59.0		58.5	59.0		58.3	58.7		dB
	Full	58.4			58.4			57.0			dB
SINAD											
f_{IN} = 10 MHz	25°C	59.0	59.5		58.9	59.4		58.6	59.1		dB
	Full	58.9			58.7			57.3			dB
f_{IN} = 70 MHz	25°C	58.8	59.2		58.8	59.2		58.4	59.0		dB
	Full	58.7			58.6			57.0			dB
f_{IN} = 170 MHz	25°C	58.2	58.8		58.2	59.0		58.2	58.8		dB
	Full	58.1			58.1			56.7			dB
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 10 MHz	25°C		9.8			9.7			9.7		Bits
f_{IN} = 70 MHz	25°C		9.7			9.7			9.7		Bits
f_{IN} = 170 MHz	25°C		9.6			9.7			9.6		Bits
WORST HARMONIC (Second or Third)											
f_{IN} = 10 MHz	25°C		−85	−78		−86	−79		−80	−75	dBc
	Full			−78			−77			−70	dBc
f_{IN} = 70 MHz	25°C		−77	−75		−80	−76		−80	−74	dBc
	Full			−75			−74			−67	dBc
f_{IN} = 170 MHz	25°C		−77	−72		−79	−70		−80	−73	dBc
	Full			−72			−70			−67	dBc
WORST OTHER (SFDR Excluding Second and Third)											
f_{IN} = 10 MHz	25°C		−86	−82		−82	−80		−82	−75	dBc
	Full			−82			−77			−70	dBc
f_{IN} = 70 MHz	25°C		−83	−81		−82	−79		−80	−75	dBc
	Full			−81			−77			−71	dBc
f_{IN} = 170 MHz	25°C		−81	−74		−79	−77		−80	−75	dBc
	Full			−74			−75			−70	dBc
TWO-TONE IMD											
140.2 MHz/141.3 MHz @ −7 dBFS	25°C		−78			−87			−81		dBc
170.2 MHz/171.3 MHz @ −7 dBFS	25°C		−86			−82			−82		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

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[1] All ac specifications tested by driving CLK+ and CLK− differentially.

[2] See the AN-835 application note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 3.

		AD9211-200			AD9211-250			AD9211-300			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS											
Logic Compliance	Full	CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			
Internal Common-Mode Bias	Full		1.2			1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V_{IH})	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V_{IL})	Full	0		0.8	0		0.8	0		0.8	V
High Level Input Current (I_{IH})	Full	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current (I_{IL})	Full	−10		+10	−10		+10	−10		+10	µA
Input Resistance (Differential)	Full	16	20	24	16	20	24	16	20	24	kΩ
Input Capacitance	Full		4			4			4		pF
LOGIC INPUTS											
Logic 1 Voltage	Full	0.8 × VDD			0.8 × VDD			0.8 × VDD			V
Logic 0 Voltage	Full			0.2 × AVDD			0.2 × AVDD			0.2 × AVDD	V
Logic 1 Input Current (SDIO)	Full		0			0			0		µA
Logic 0 Input Current (SDIO)	Full		−60			−60			−60		µA
Logic 1 Input Current (SCLK, PWDN, CSB, RESET)	Full		55			55			50		µA
Logic 0 Input Current (SCLK, PWDN, CSB, RESET)	Full		0			0			0		µA
Input Capacitance	25°C		4			4			4		pF
LOGIC OUTPUTS[2]											
V_{OD} Differential Output Voltage	Full	247		454	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	1.125		1.375	1.125		1.375	1.125		1.375	V
Output Coding		Twos complement, Gray code, or offset binary (default)									

[1] See the AN-835 application note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] LVDS $R_{TERMINATION}$ = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 4.

		AD9211-200			AD9211-250			AD921-300			
Parameter (Conditions)	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Maximum Conversion Rate	Full	200			250			300			MSPS
Minimum Conversion Rate	Full			40			40			40	MSPS
CLK+ Pulse Width High (t_{CH})	Full	2.25	2.5		1.8	2.0		1.5	1.7		ns
CLK+ Pulse Width Low (t_{CL})	Full	2.25	2.5		1.8	2.0		1.5	1.7		ns
Output (LVDS – SDR Mode)[1]											
Data Propagation Delay (t_{PD})	Full		3.0			3.0			3.0		ns
Rise Time (t_R) (20% to 80%)	25°C		0.2			0.2			0.2		ns
Fall Time (t_F) (20% to 80%)	25°C		0.2			0.2			0.2		ns
DCO Propagation Delay (t_{CPD})	Full		3.9			3.9			3.9		ns
Data to DCO Skew (t_{SKEW})	Full	−0.3	+0.1	+0.5	−0.3	+0.1	+0.5	−0.3	+0.1	+0.5	ns
Latency	Full		7			7			7		Cycles
Output (LVDS – DDR Mode)[2]											
Data Propagation Delay (t_{PD})	Full		3.8			3.8			3.8		ns
Rise Time (t_R) (20% to 80%)	25°C		0.2			0.2			0.2		ns
Fall Time (t_F) (20% to 80%)	25°C		0.2			0.2			0.2		ns
DCO Propagation Delay (t_{CPD})	Full		3.9			3.9			3.9		ns
Data to DCO Skew (t_{SKEW})	Full	−0.5	+0.1	+0.3	−0.5	+0.1	+0.3	−0.5	+0.1	+0.3	ns
Latency	Full		7			7			7		Cycles
Aperture Uncertainty (Jitter, t_J)	25°C		0.2			0.2					ps rms

[1] See Figure 2.
[2] See Figure 3.

TIMING DIAGRAMS

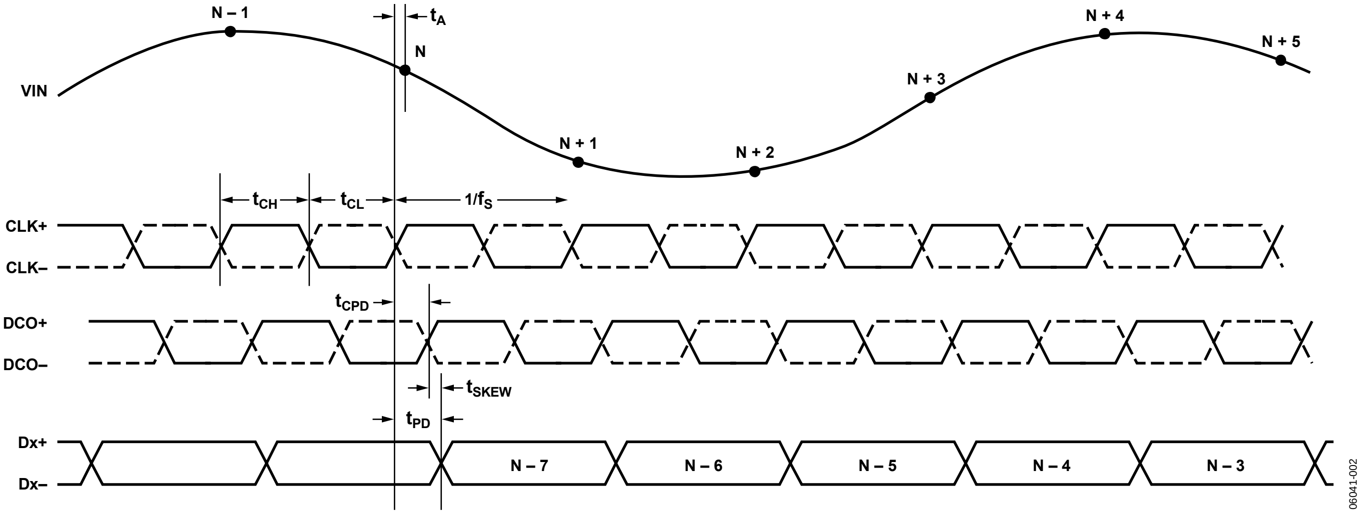


Figure 2. Single Data Rate Mode

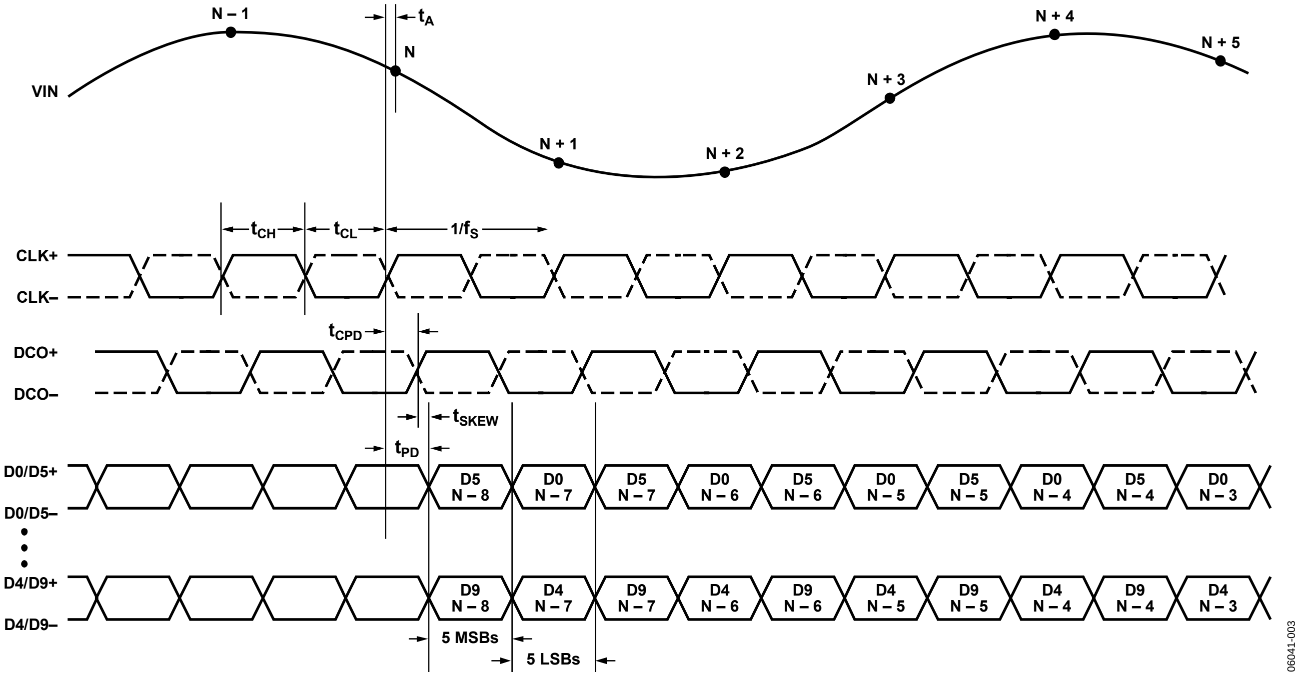


Figure 3. Double Data Rate Mode

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
D0+/D0− through D9+/D9− to DRGND	−0.3 V to DRVDD + 0.3 V
DCO to DRGND	−0.3 V to DRVDD + 0.3 V
OR to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.9 V
CLK− to AGND	−0.3 V to +3.9 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PWDN to AGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to AGND	−0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP (CP-56-2)	30.4	2.9	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

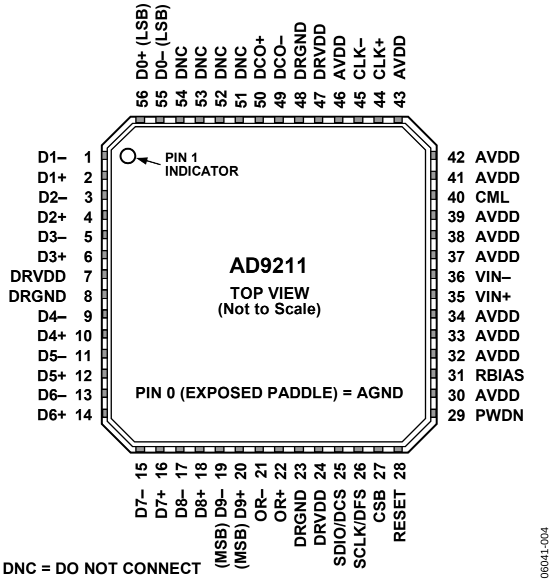


Figure 4. AD9211 Single Data Rate Mode Pin Configuration

Table 7. Single Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51 to 54	DNC	Do Not Connect.
55	D0–	D0 Complement Output Bit (LSB).
56	D0+	D0 True Output Bit (LSB).
1	D1–	D1 Complement Output Bit.
2	D1+	D1 True Output Bit.
3	D2–	D2 Complement Output Bit.
4	D2+	D2 True Output Bit.
5	D3–	D3 Complement Output Bit.
6	D3+	D3 True Output Bit.
9	D4–	D4 Complement Output Bit.
10	D4+	D4 True Output Bit.

Pin No.	Mnemonic	Description
11	D5–	D5 Complement Output Bit.
12	D5+	D5 True Output Bit.
13	D6–	D6 Complement Output Bit.
14	D6+	D6 True Output Bit.
15	D7–	D7 Complement Output Bit.
16	D7+	D7 True Output Bit.
17	D8–	D8 Complement Output Bit.
18	D8+	D8 True Output Bit.
19	D9–	D9 Complement Output Bit (MSB).
20	D9+	D9 True Output Bit (MSB).
21	OR–	Overrange Complement Output Bit.
22	OR+	Overrange True Output Bit.

[1] AGND and DRGND should be tied to a common quiet ground plane.

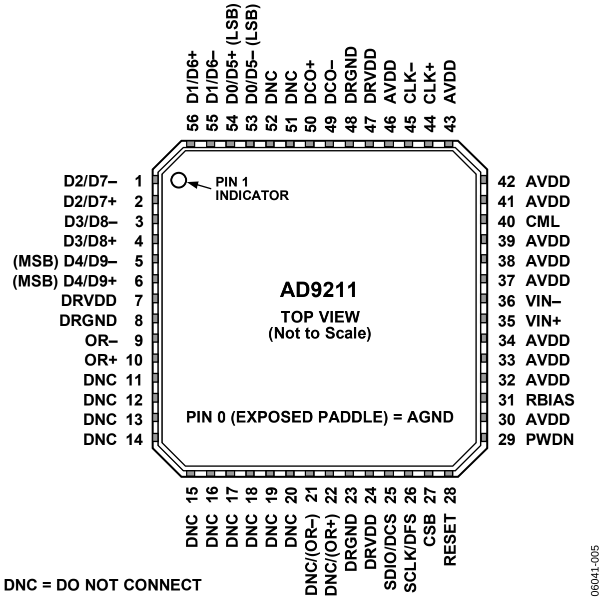


Figure 5. AD9211 Double Data Rate Pin Configuration

Table 8. Double Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
53	D0/D5–	D1/D7 Complement Output Bit (LSB).
54	D0/D5+	D1/D7 True Output Bit (LSB).
55	D1/D6–	D2/D8 Complement Output Bit.
56	D1/D6+	D2/D8 True Output Bit.
1	D2/D7–	D3/D9 Complement Output Bit.
2	D2/D7+	D3/D9 True Output Bit.
3	D3/D8–	D4/D10 Complement Output Bit.
4	D3/D8+	D4/D10 True Output Bit.
5	D4/D9–	D5/D11 Complement Output Bit (MSB).
6	D4/D9+	D5/D11 True Output Bit (MSB).

Pin No.	Mnemonic	Description
9	OR−	D6 Complement Output Bit. (This pin is disabled if Pin 21 is reconfigured through the SPI to be OR−.)
10	OR+	D6 True Output Bit. (This pin is disabled if Pin 22 is reconfigured through the SPI to be OR+.)
11 to 20, 51, 52	DNC	Do Not Connect.
21	DNC/(OR−)	Do Not Connect. (This pin can be reconfigured as the Overrange Complement Output Bit through the serial port register.)
22	DNC/(OR+)	Do Not Connect. (This pin can be reconfigured as the Overrange True Output Bit through the serial port register.)

[1] AGND and DRGND should be tied to a common quiet ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS enabled, T_A = 25°C, 1.25 V p-p differential input, AIN = −1 dBFS, unless otherwise noted.

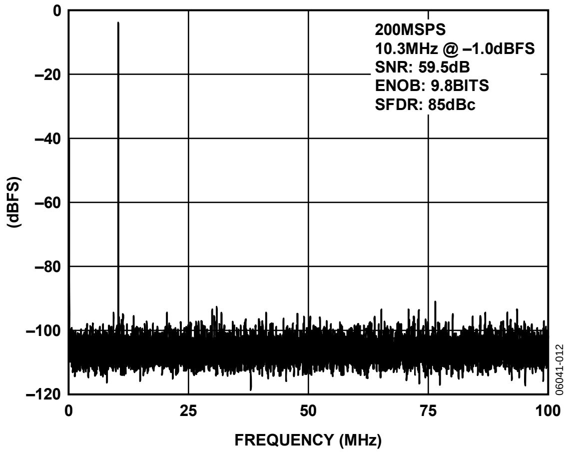


Figure 6. AD9211-200 64k Point Single-Tone FFT; 200 MSPS, 10.3 MHz

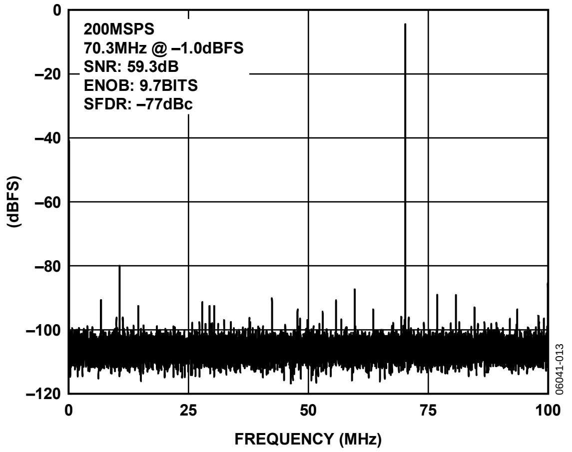


Figure 7. AD9211-200 64k Point Single-Tone FFT; 200 MSPS, 70.3 MHz

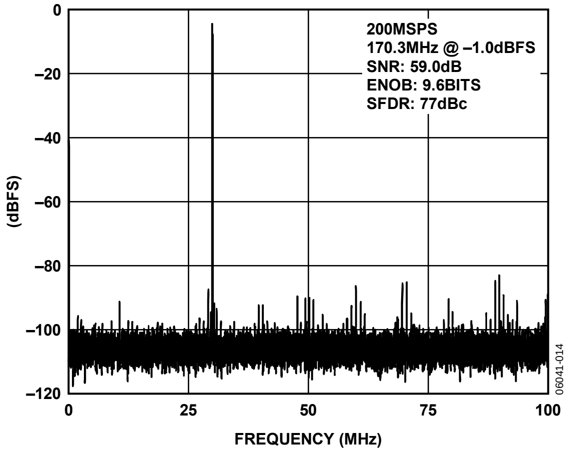


Figure 8. AD9211-200 64k Point Single-Tone FFT; 200 MSPS, 170.3 MHz

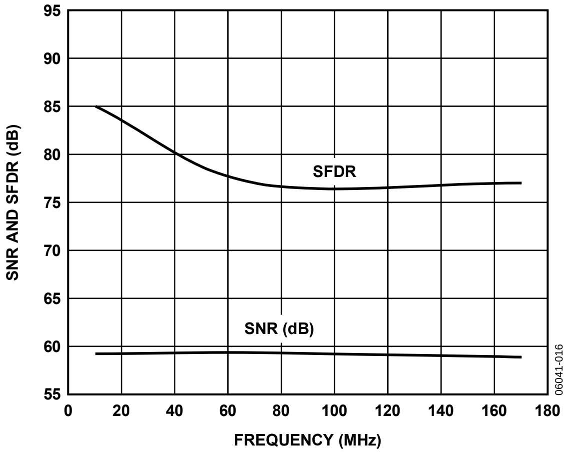


Figure 9. AD9211-200 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 1.25 V p-p Full Scale; 200 MSPS

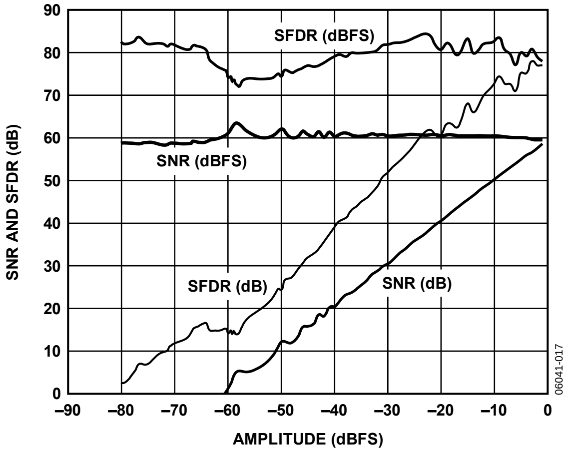


Figure 10. AD9211-200 SNR/SFDR vs. Input Amplitude; 170.3 MHz

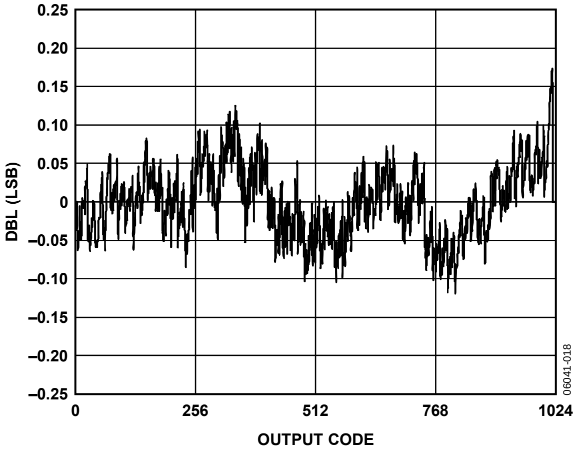


Figure 11. AD9211-200 INL; 200 MSPS

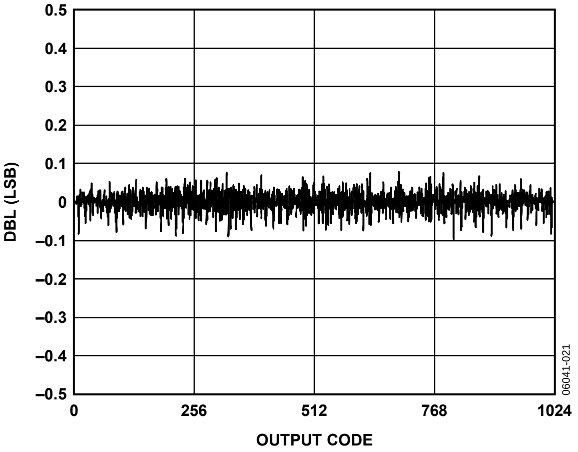


Figure 12. AD9211-200 DNL; 200 MSPS

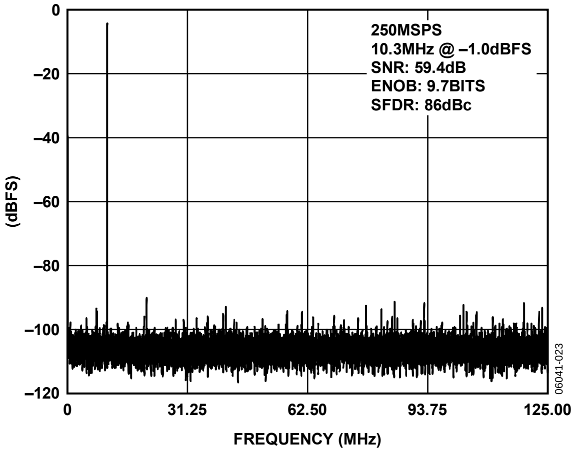


Figure 13. AD9211-250 64k Point Single-Tone FFT; 250 MSPS, 10.3 MHz

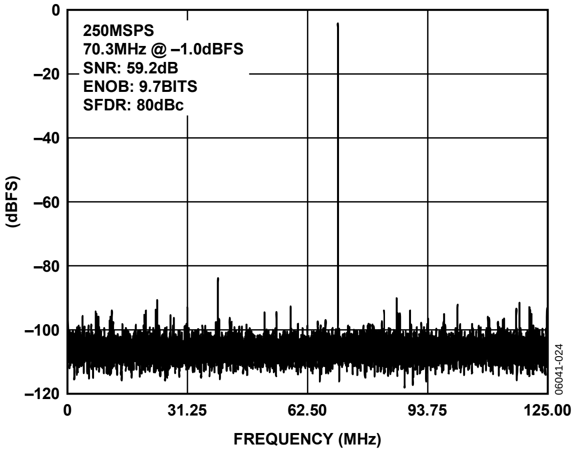


Figure 14. AD9211-250 64k Point Single-Tone FFT; 250 MSPS, 70.3 MHz

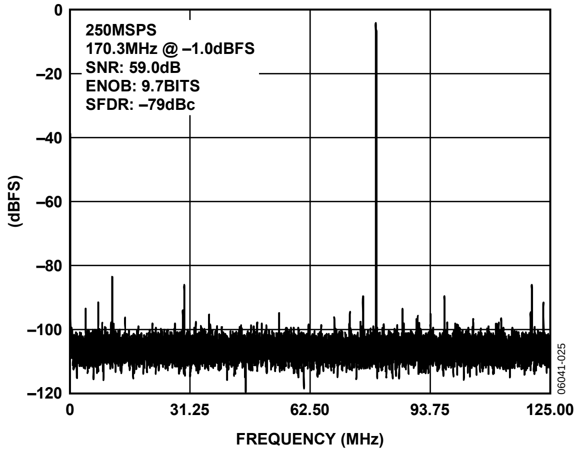


Figure 15. AD9211-250 64k Point Single-Tone FFT; 250 MSPS, 170.3 MHz

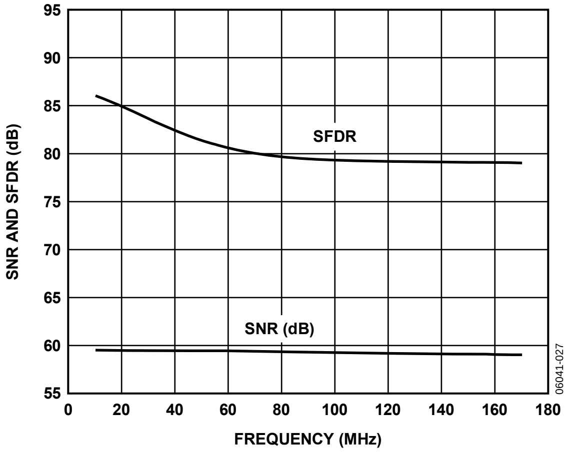


Figure 16. AD9211-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 1.25 V p-p Full Scale; 250 MSPS

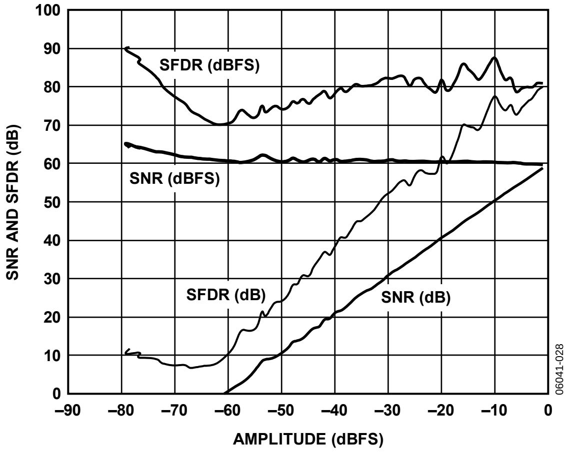


Figure 17. AD9211-250 SNR/SFDR vs. Input Amplitude; 250 MSPS, 170.3 MHz

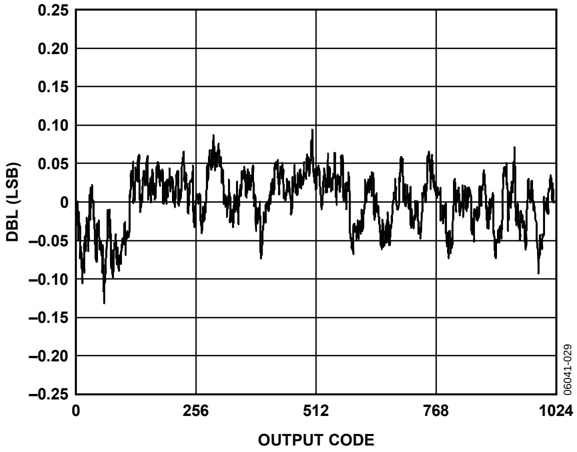


Figure 18. AD9211-250 INL; 250 MSPS

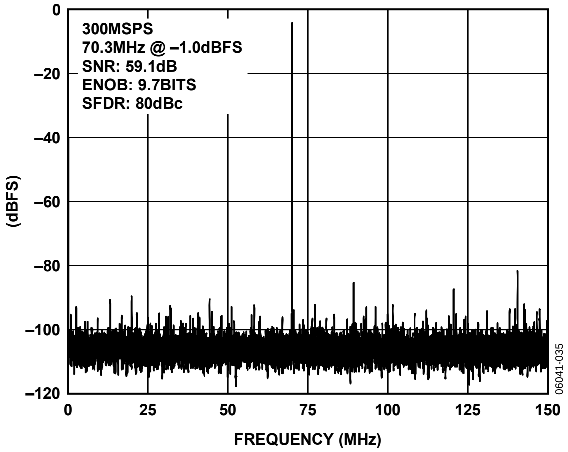


Figure 21. AD9211-300 64k Point Single-Tone FFT; 300 MSPS, 70.3 MHz

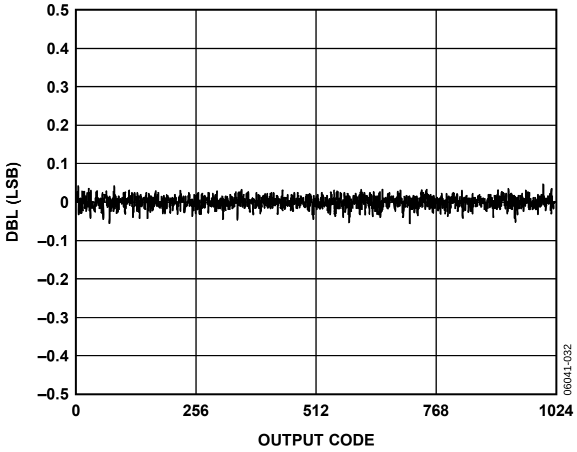


Figure 19. AD9211-250 DNL; 250 MSPS

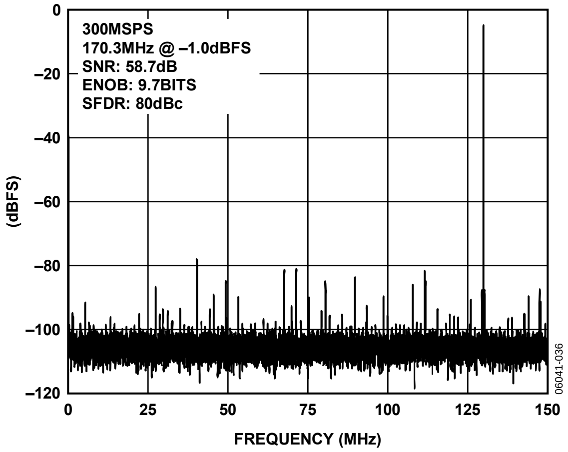


Figure 22. AD9211-300 64k Point Single-Tone FFT; 300 MSPS, 170.3 MHz

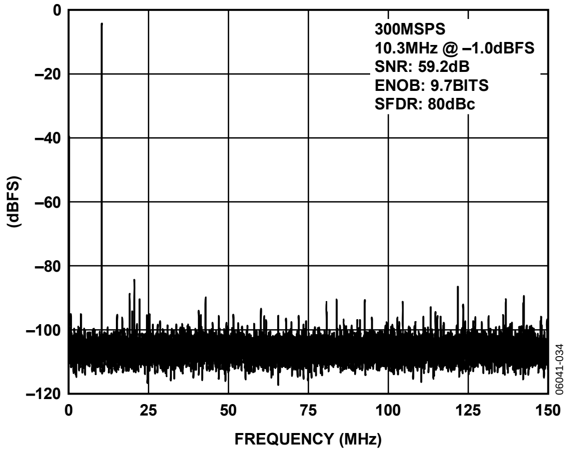


Figure 20. AD9211-300 64k Point Single-Tone FFT; 300 MSPS, 10.3 MHz

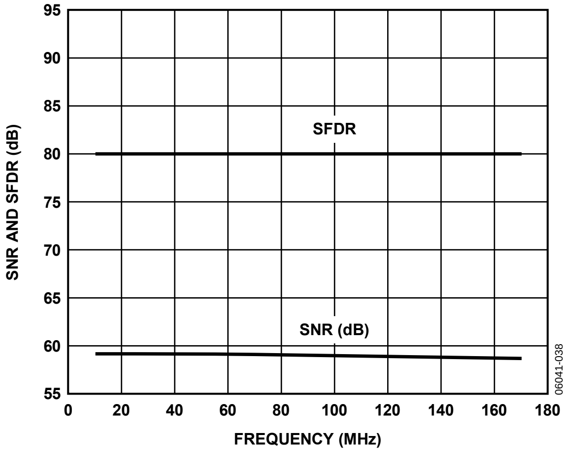


Figure 23. AD9211-300 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 1.25 V p-p Full Scale; 300 MSPS

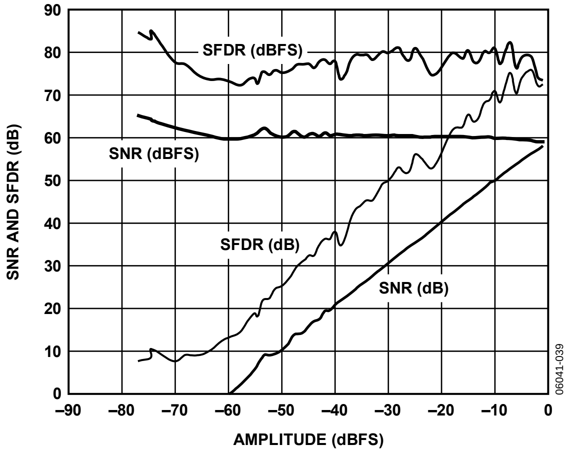


Figure 24. AD9211-300 SNR/SFDR vs. Input Amplitude; 300 MSPS, 170.3 MHz

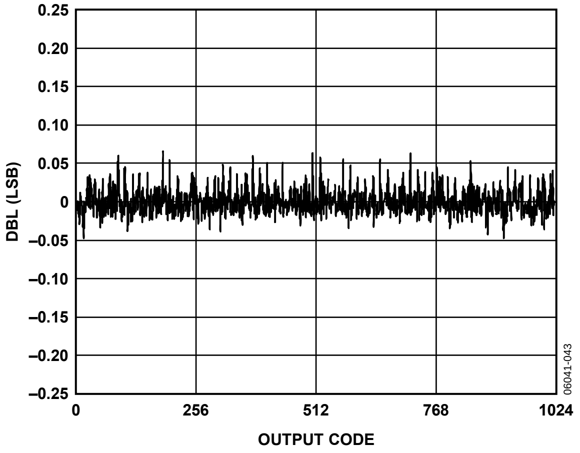


Figure 27. AD9211-300 DNL; 300 MSPS

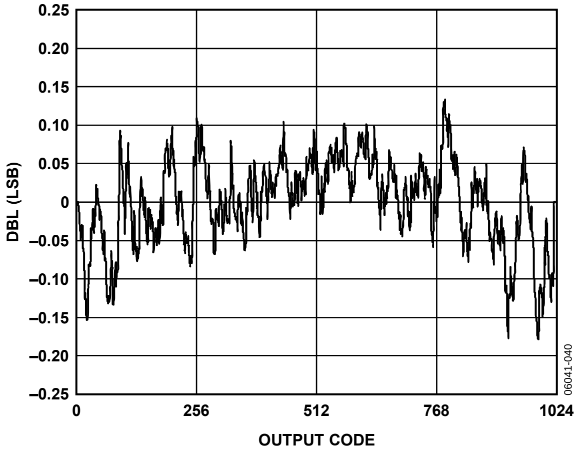


Figure 25. AD9211-300 INL; 300 MSPS

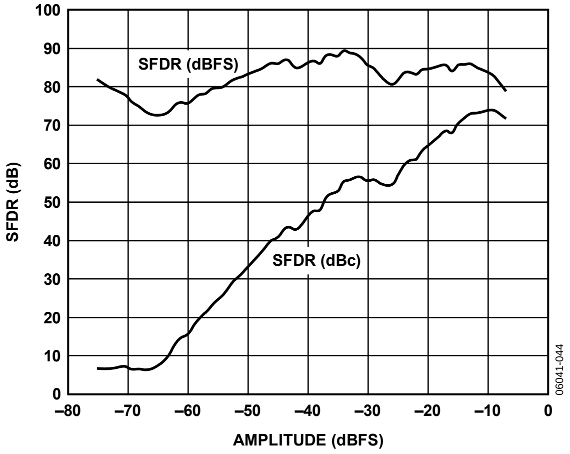


Figure 28. AD9211-300 Two-Tone SFDR vs. Input Amplitude; 300 MSPS, 170.1 MHz, 171.1 MHz

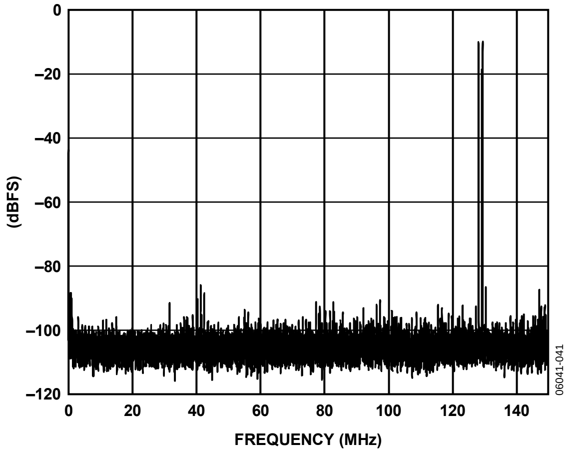


Figure 26. AD9211-300 64k Point, Two-Tone FFT; 300 MSPS, 170.1 MHz, 171.1 MHz

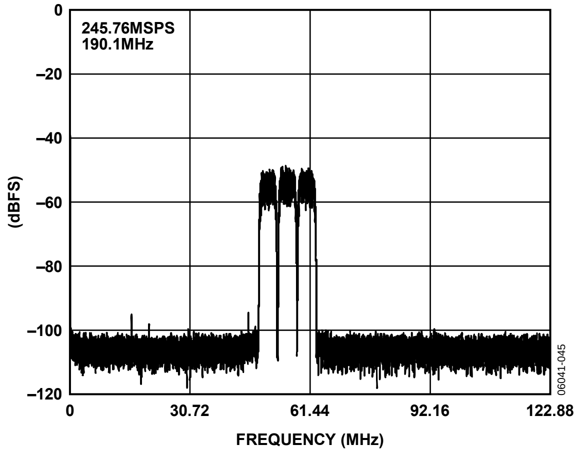


Figure 29. AD9211-300 64k Point FFT; Three W-CDMA Carriers, IF = 190.1 MHz, 245.6 MSPS

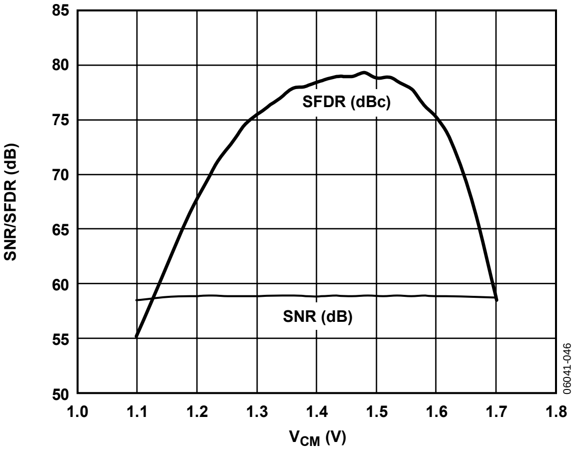


Figure 30. SNR/SFDR vs. Common-Mode Voltage; 300 MSPS, 70.3 MHz @ −1 dBFS

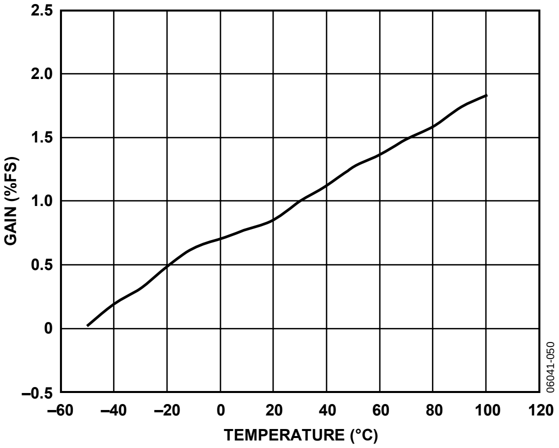


Figure 31. Gain vs. Temperature

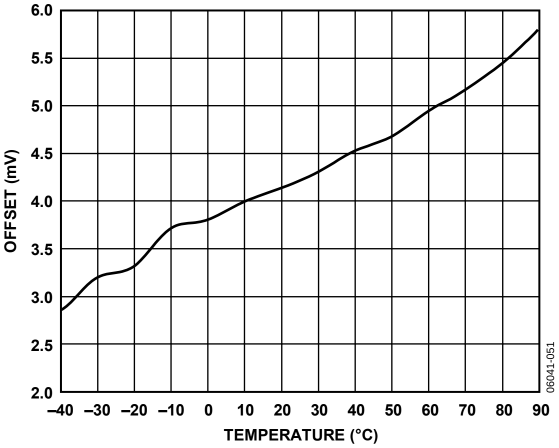


Figure 32. Offset vs. Temperature

EQUIVALENT CIRCUITS

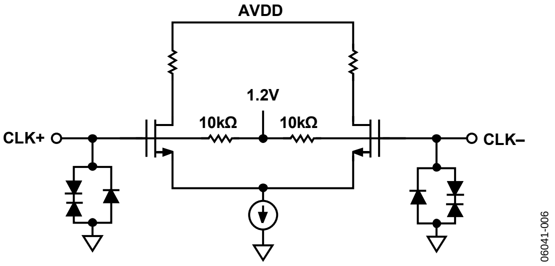


Figure 33. Clock Inputs

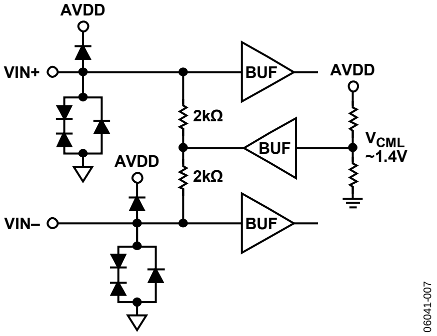


Figure 34. Analog Inputs (V_{CML} = ~1.4 V)

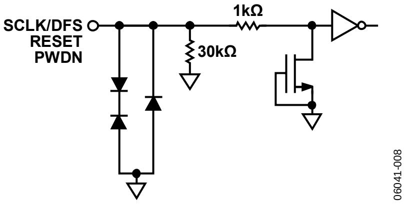


Figure 35. Equivalent SCLK/DFS, RESET, PWDN Input Circuit

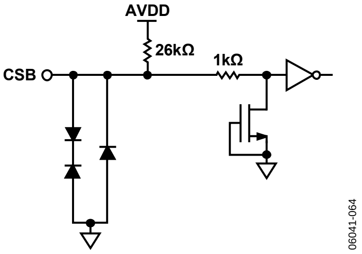


Figure 36. Equivalent CSB Input Circuit

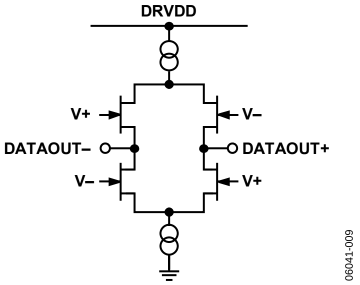


Figure 37. LVDS Outputs (Dx+, Dx–, OR+, OR–, DCO+, DCO–)

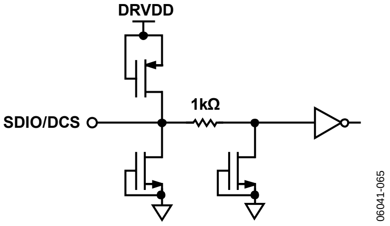


Figure 38. Equivalent SDIO/DCS Input Circuit

THEORY OF OPERATION

The AD9211 architecture consists of a front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended mode. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND VOLTAGE REFERENCE

The analog input to the AD9211 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

A wideband transformer, such as Mini-Circuits® ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 1.3 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.25 V p-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of SPI control. See the AD9211 Configuration Using the SPI section for more details.

Differential Input Configurations

Optimum performance is achieved while driving the AD9211 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2 + 0.5 V, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

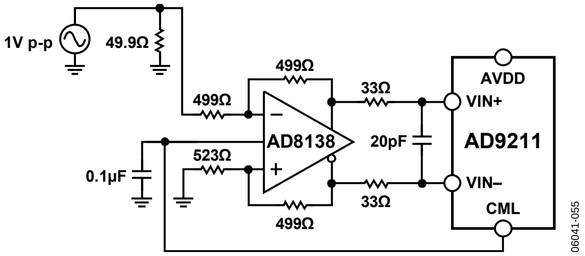


Figure 39. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers may not be adequate to achieve the true performance of the AD9211. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

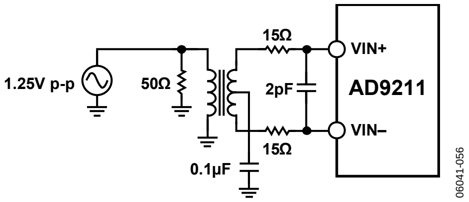


Figure 40. Differential Transformer—Coupled Configuration

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used (see Figure 41).

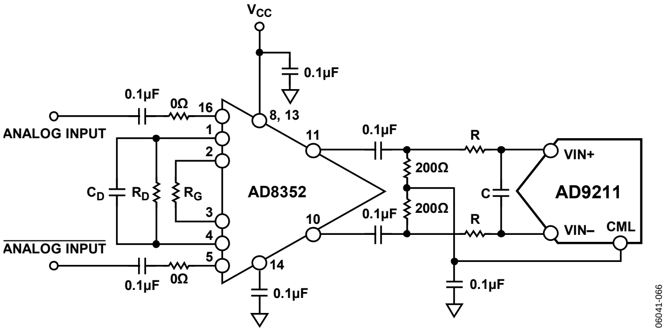


Figure 41. Differential Input Configuration Using the AD8352

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9211 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ pin and CLK− pin via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 42 shows one preferred method for clocking the AD9211. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9211 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9211 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

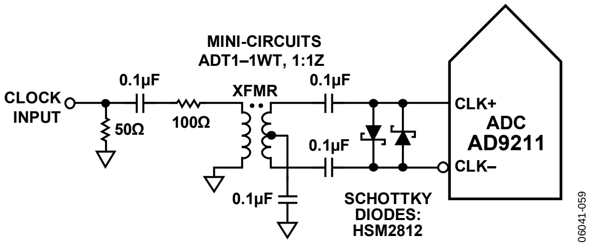
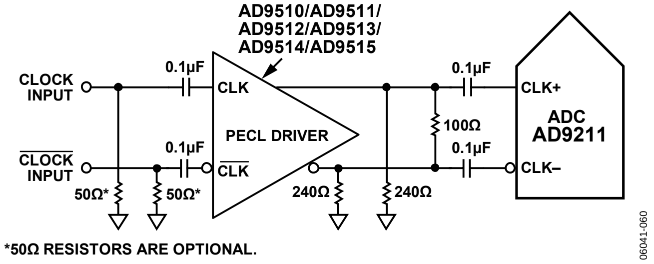


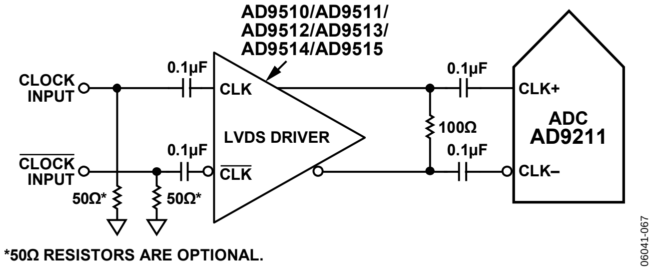
Figure 42. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 43. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.



*50Ω RESISTORS ARE OPTIONAL.

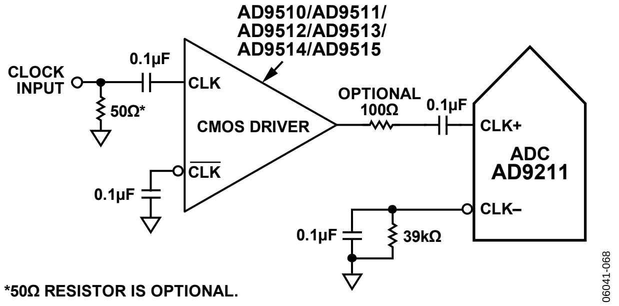
Figure 43. Differential PECL Sample Clock



*50Ω RESISTORS ARE OPTIONAL.

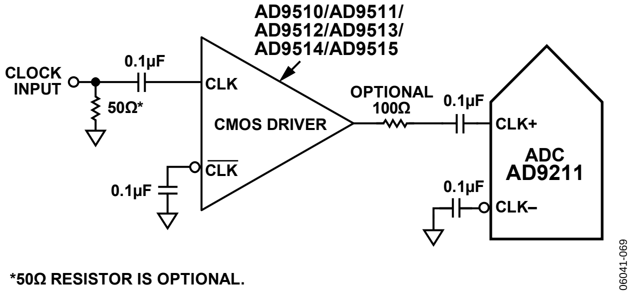
Figure 44. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 45). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.



*50Ω RESISTOR IS OPTIONAL.

Figure 45. Single-Ended 1.8 V CMOS Sample Clock



*50Ω RESISTOR IS OPTIONAL.

Figure 46. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9211 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9211. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the AD9211 Configuration Using the SPI section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log_{10}[½ \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 47).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9211. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 application note and the AN-756 application note for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

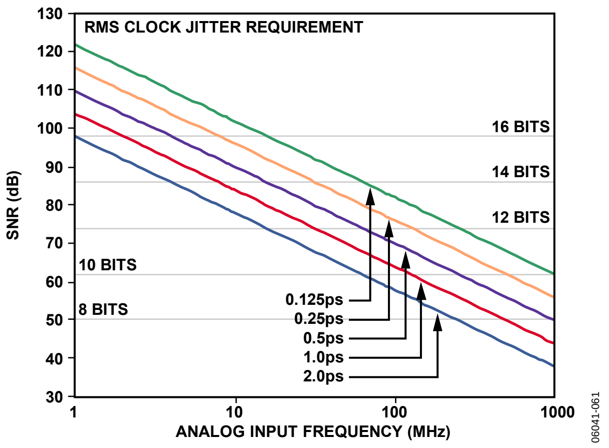


Figure 47. Ideal SNR vs. Input Frequency and Jitter

POWER DISSIPATION AND POWER-DOWN MODE

The power dissipated by the AD9211 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

By asserting PWDN (Pin 29) high, the AD9211 is placed in standby mode or full power-down mode, as determined by the contents of Serial Port Register 08. Reasserting the PWDN pin low returns the AD9211 to its normal operational mode.

An additional standby mode is supported by means of varying the clock input. When the clock rate falls below 20 MHz, the AD9211 assumes a standby state. In this case, the biasing network and internal reference remain on, but digital circuitry is powered down. Upon reactivating the clock, the AD9211 resumes normal operation after allowing for the pipeline latency.

DIGITAL OUTPUTS

Digital Outputs and Timing

The AD9211 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard using the SPI. This LVDS standard can further reduce the overall power dissipation of the device, which reduces the power by ~39 mW. See the Memory Map section for more information. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9211 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length is no longer than 24 inches and that the differential output traces are kept close together and at equal lengths.

An example of the LVDS output using the ANSI standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on regular FR-4 material is shown in Figure 48. Figure 49 shows an example of when the trace lengths exceed 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is up to the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches.

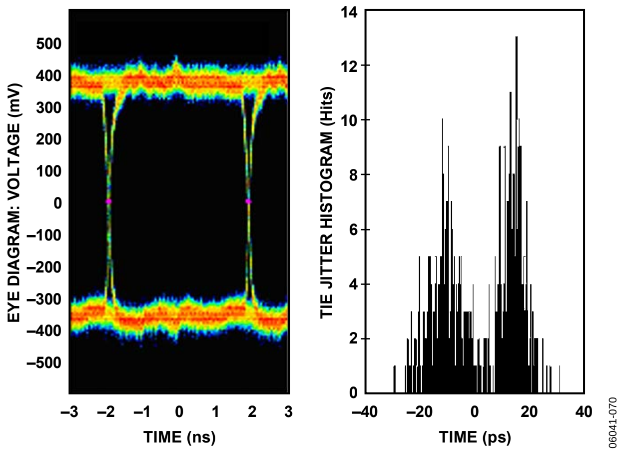


Figure 48. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Less than 24 Inches on Standard FR-4, AD9211-250

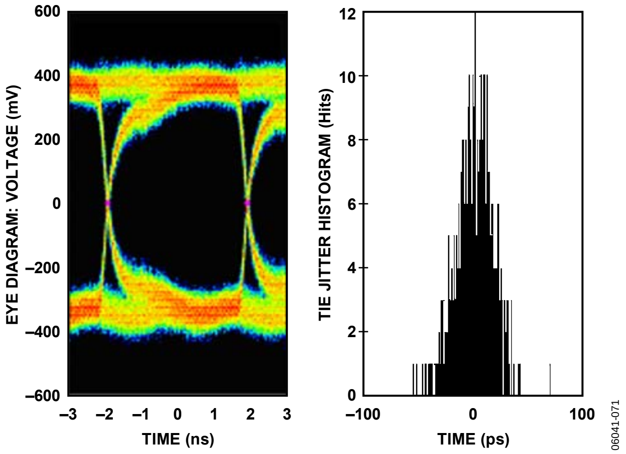


Figure 49. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Greater than 24 Inches on Standard FR-4, AD9211-250

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 12. If it is desired to change the output data format to twos complement, see the AD9211 Configuration Using the SPI section.

An output clock signal is provided to assist in capturing data from the AD9211. The DCO is used to clock the output data and is equal to the sampling clock (CLK) rate. In single data rate mode (SDR), data is clocked out of the AD9211 and must be captured on the rising edge of the DCO. In double data rate mode (DDR), data is clocked out of the AD9211 and must be captured on the rising and falling edges of the DCO. See the timing diagrams shown in Figure 2 and Figure 3 for more information.

Output Data Rate and Pinout Configuration

The output data of the AD9211 can be configured to drive 10 pairs of LVDS outputs at the same rate as the input clock signal (single data rate, or SDR, mode), or five pairs of LVDS outputs at 2× the rate of the input clock signal (double data rate, or DDR, mode). SDR is the default mode; the device may be reconfigured for DDR by setting Bit 3 in Register 14 (see Table 13).

Out-of-Range (OR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OR has the same pipeline latency as the digital data. OR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range, as shown in Figure 50. OR remains high until the analog input returns to within the input range and another conversion is completed. By logically ANDing OR with the MSB and its complement, overrange high or underrange low conditions can be detected.

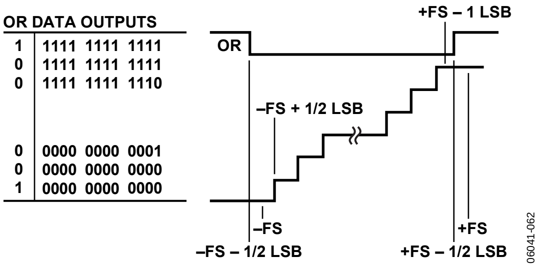


Figure 50. OR Relation to Input Voltage and Output Data

TIMING

The AD9211 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9211. These transients can degrade the converter's dynamic performance. The AD9211 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO.

The lowest typical conversion rate of the AD9211 is 40 MSPS. At clock rates below 1 MSPS, the AD9211 assumes the standby mode.

RBIAS

The AD9211 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This resister should have a 1% tolerance and is used to set the master current reference of the ADC core.

AD9211 CONFIGURATION USING THE SPI

The AD9211 SPI allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or readback) serially in one-byte words. Each byte may be further divided down into fields, which are documented in the Memory Map section.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK/DFS, SPI SDIO/DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB is an active low control that enables or disables the read and write cycles (see Table 9).

Table 9. Serial Port Pins

Mnemonic	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual-purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is an active low control that gates the read and write cycles.
RESET	Master Device Reset. When asserted, device assumes default settings. Active low.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 51 and Table 11.

During an instruction phase, a 16-bit instruction is transmitted. Data then follows the instruction phase and is determined by the W0 and W1 bits, which is 1 or more bytes of data. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether this is a read or write command. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

Data may be sent in MSB or in LSB first mode. MSB first is default on power-up and can be changed by changing the configuration register. For more information about this feature and others, see the AN-877, *Interfacing to High Speed ADCs via SPI.*

HARDWARE INTERFACE

The pins described in Table 9 comprise the physical interface between the user's programming device and the serial port of the AD9211. All serial pins are inputs with an open-drain configuration and should be tied to an external pull-up or pull-down resistor (suggested value of 10 kΩ).

This interface is flexible enough to be controlled by either PROMS or PIC mirocontrollers as well. This provides the user with an alternate method to program the ADC other than a SPI controller.

If the user chooses not to use the SPI interface, some pins serve a dual function and are associated with a specific function when strapped externally to AVDD or ground during device power on. The Configuration Without the SPI section describes the strappable functions supported on the AD9230.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SPI SDIO/DCS and SPI SCLK/DFS pins can alternately serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer. In this mode, the SPI CSB chip select should be connected to ground, which disables the serial port interface.

Table 10. Mode Selection

Mnemonic	External Voltage	Configuration
SPI SDIO/DCS	AVDD	Duty cycle stabilizer enabled
	AGND	Duty cycle stabilizer disabled
SPI SCLK/DFS	AVDD	Twos complement enabled
	AGND	Offset binary enabled

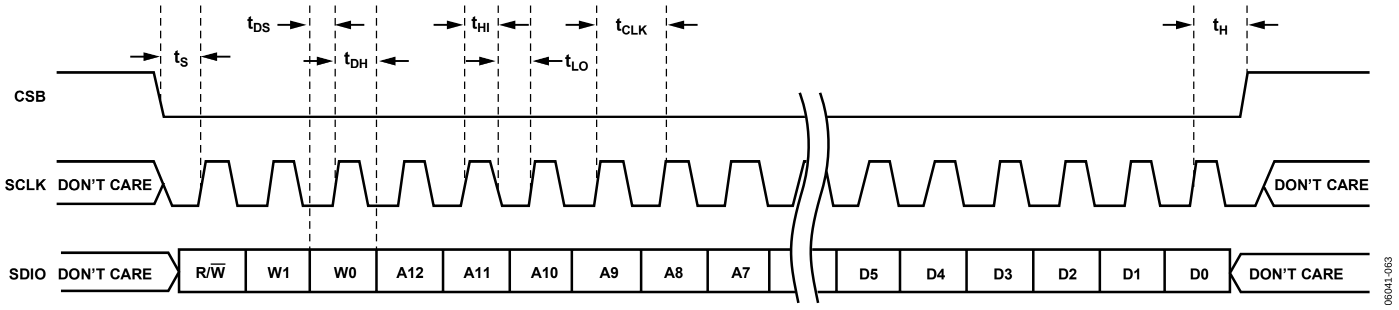


Figure 51. Serial Port Interface Timing Diagram

Table 11. Serial Timing Definitions

Parameter	Timing (minimum, ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	1	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 51)
t_{DIS_SDIO}	5	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 51)

Table 12. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode D11 to D0	Twos Complement Mode D11 to D0	Gray Code Mode (SPI Accessible) D11 to D0	OR
VIN+ – VIN–	< 0.62	0000 0000 00	0000 0000 00	0000 0000 00	1
VIN+ – VIN–	= 0.62	0000 0000 00	0000 0000 00	0000 0000 00	0
VIN+ – VIN–	= 0	0000 0000 00	0000 0000 00	0000 0000 00	0
VIN+ – VIN–	= 0.62	1111 1111 11	1111 1111 11	0000 0000 00	0
VIN+ – VIN–	> 0.62 + 0.5 LSB	1111 1111 11	1111 1111 11	0000 0000 00	1

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: chip configuration register map (Address 0x00 to Address 0x02), transfer register map (Address 0xFF), and program register map (Address 0x08 to Address 0x2A).

The Addr. (Hex) column of the memory map indicates the register address in hexadecimal, and the Default Value (Hex) column shows the default hexadecimal value that is already written into the register. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Hexadecimal Address 0x09, clock, has a hexadecimal default value of 0x01. This means Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. The default value enables the duty cycle stabilizer. Overwriting this default so that Bit 0 = 0 disables the duty cycle stabilizer. For more information on this and other functions, consult the AN-877 application note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to other than their default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

Coming out of reset, critical registers are preloaded with default values. These values are indicated in Table 13. Other registers do not have default values and retain the previous value when exiting reset.

LOGIC LEVELS

An explanation of various registers follows: “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

Table 13. Memory Map Register

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	chip_port_config	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles should be mirrored by the user so that LSB or MSB first mode registers correctly, regardless of shift mode.
01	chip_id	8-bit chip ID, Bits[7:0] AD9211 = 0x06								Read-only	Default is unique chip ID, different for each device. This is a read-only register.
02	chip_grade	0	0	0	Speed grade: 00 = 300 MSPS 01 = 250 MSPS 10 = 200 MSPS		X	X	X	Read-only	Child ID used to differentiate graded devices.
Transfer Register											
FF	device_update	0	0	0	0	0	0	0	SW transfer	0x00	Synchronously transfers data from the master shift register to the slave.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
ADC Functions											
08	modes	0	0	PWDN: 0 = full (default) 1 = standby	0	0	Internal power-down mode: 000 = normal (power-up, default) 001 = full power-down 010 = standby 011 = normal (power-up) Note: External PWDN pin overrides this setting.			0x00	Determines various generic modes of chip operation.
09	clock	0	0	0	0	0	0	0	Duty cycle stabilizer: 0 = disabled 1 = enabled (default)	0x01	
OD	test_io			Reset PN23 gen: 1 = on 0 = off (default)	Reset PN9 gen: 1 = on 0 = off (default)	Output test mode: 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checker board output 0101 = PN 23 sequence 0110 = PN 9 0111 = one/zero word toggle 1000 = unused 1001 = unused 1010 = unused 1011 = unused 1100 = unused (Format determined by output_mode)				0x00	When set, the test data is placed on the output pins in place of normal data.
OF	ain_config	0	0	0	0	0	Analog input disable: 1 = on 0 = off (default)	CML enable: 1 = on 0 = off (default)	0	0x00	
14	output_mode	0		0	Output enable: 0 = enable (default) 1 = disable	DDR: 1 = enabled 0 = disabled (default)	Output invert: 1 = on 0 = off (default)	Data format select: 00 = offset binary (default) 01 = twos complement 10 = Gray code		0x00	0
15	output_adjust	0	0			LVDS course adjust: 0 = 3.5 mA (default) 1 = 2.0 mA	LVDS fine adjust: 001 = 3.50 mA 010 = 3.25 mA 011 = 3.00 mA 100 = 2.75 mA 101 = 2.50 mA 110 = 2.25 mA 111 = 2.00 mA			0x00	0
16	output_phase	Output clock polarity 1 = inverted 0 = normal (default)	0	0	0					0x03	

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
17	flex_output_delay	Output delay enable: 0 = enable 1 = disable			Output clock delay: 00000 = 0.1 ns 00001 = 0.2 ns 00010 = 0.3 ns … 11101 = 3.0 ns 11110 = 3.1 ns 11111 = 3.2 ns					0	
18	flex_vref				Input voltage range setting: 10000 = 0.98 V 10001 = 1.00 V 10010 = 1.02 V 10011 = 1.04 V … 11111 = 1.23 V 00000 = 1.25 V 00001 = 1.27 V … 01110 = 1.48 V 01111 = 1.50 V					0	
2A	ovr_config							OR position (DDR mode only): 0 = Pin 9, Pin 10 1 = Pin 21, Pin 22	OR enable: 1 = on (default) 0 = off		00000001

OUTLINE DIMENSIONS

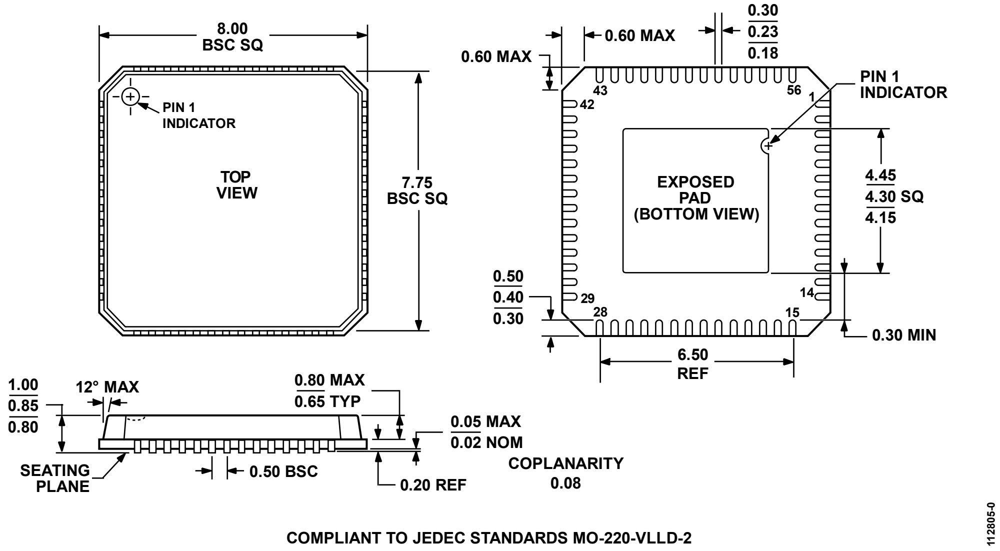


Figure 52. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 mm × 8 mm Body, Very Thin Quad
(CP-56-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9211BCPZ-200[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9211BCPZ-250[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9211BCPZ-300[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9211-200EBZ[1]		LVDS Evaluation Board with AD9211BCPZ-200	
AD9211-250EBZ[1]		LVDS Evaluation Board with AD9211BCPZ-250	
AD9211-300EBZ[1]		LVDS Evaluation Board with AD9211BCPZ-300	

[1] Z = RoHS Compliant Part.

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