TABLE OF CONTENTS

REVISION HISTORY

3/16—Rev. B to Rev. C

Changes to Table 1 ... 1
Change to Endnote 3, Table 1 ... 3
Change to Signal-to-Noise-and-Distortion Ratio Parameter, Table 2 ... 3
Deleted Endnote 4, Table 2 ... 3
Changes to Figure 4 ... 7
Changes to Figure 23 ... 14
Changes to Driver Amplifier Choice Section ... 15
Change to Reference Decoupling Section ... 16
Changes to Reading During Conversion, Fast Host (Turbo or Normal Mode) Section and Split-Reading, Any Speed Host (Turbo or Normal Mode) Section ... 18
Changes to Figure 31 ... 21
Updated Outline Dimensions ... 27
Changes to Ordering Guide ... 27

7/14—Rev. A to Rev. B

Added Patent Endnote ... 1
Changes to Figure 21 ... 13
Changes to Data Reading Options Section ... 18
Updated Outline Dimensions ... 27

8/10—Rev. 0 to Rev. A

Change to Table 4, Conversion Time: CNV Rising Edge to Data Available ... 5

9/09—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 2.5 V, BVDD = 5 V, VIO = 1.8 V to 2.7 V, V_{REF} = 4.096 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	(IN+) − (IN−)	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	V
Leakage Current at 25°C	Acquisition phase		250		nA
Input Impedance			See the Analog Inputs section		
ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity Error, DNL		−0.99	±0.50	+0.99	LSB[1]
Integral Nonlinearity Error, INL		−1.50	±0.7	+1.50	LSB[1]
Transition Noise			0.8		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]		−15	±2	+15	LSB[1]
Gain Error Temperature Drift			±0.8		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]		−0.99	±0.08	+0.99	mV
Zero Temperature Drift			0.55		ppm/°C
Power Supply Sensitivity	AVDD = 2.5 V ± 5%		90		dB[3]
THROUGHPUT					
Conversion Rate		0		2.5	MSPS
Transient Response	Full-scale step			100	ns
AC ACCURACY					
Dynamic Range	V_{REF} = 4.096 V, internal reference	87.5	89		dB[3]
	V_{REF} = 5.0 V, external reference	89.0	90		dB[3]
Signal-to-Noise Ratio, SNR	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal reference	87.0	88.5		dB[3]
	f_{IN} = 20 kHz, V_{REF} = 5.0 V, external reference	89.0	90.0		dB[3]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 20 kHz		103		dB[3]
Total Harmonic Distortion, THD	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal reference		−100		dB[3]
Signal-to-Noise-and-Distortion Ratio, SINAD	f_{IN} = 20 kHz, V_{REF} = 4.096 V		90		dB[3]
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			19		MHz
Aperture Delay			0.7		ns

[1] LSB means least significant bit. With the 4.096 V input range, one LSB is 62.5 µV.
[2] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[3] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE	PDREF is low				
Output Voltage	T_A = 25°C	4.081	4.096	4.111	V
Temperature Drift	−40°C to +85°C		±10		ppm/°C
Line Regulation	AVDD = 2.5 V ± 5%		±50		ppm/V
Turn-On Settling Time	C_{REF} = 10 µF, C_{REFIN} = 0.1 µF		40		ms
REFIN Output Voltage	REFIN at 25°C		1.2		V
REFIN Output Resistance			6		kΩ
EXTERNAL REFERENCE	PDREF is high, REFIN is low				
Voltage Range		2.4		5.1	V
Current Drain			500		µA
REFERENCE BUFFER					
REFIN Input Voltage Range			1.2		V
REFIN Input Current			160		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		0.1 × VIO	V
V_{IH}		0.9 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits, straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
AVDD, DVDD		2.375	2.5	2.625	V
BVDD		4.75	5.0	5.25	V
VIO	Specified performance	1.8	2.5	2.7	V
Standby Current[1, 2]	AVDD = DVDD = VIO = 2.5 V		1.0		µA
Power Dissipation					
With Internal Reference	2.5 MSPS throughput		28	33	mW
	2.0 MSPS throughput		25	30	mW
With External Reference	2.5 MSPS throughput		15.5	17	mW
	2.0 MSPS throughput		12	13	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 2.5 V, BVDD = 5 V, VIO = 1.8 V to 2.7 V, V_{REF} = 4.096 V, T_A = −40°C to +85°C, unless otherwise noted.[1]

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	Turbo mode/normal mode			320/420	ns
Acquisition Time	t_{ACQ}		80			ns
Time Between Conversions	t_{CYC}	Turbo mode/normal mode	400/500			ns
CNV Pulse Width	t_{CNVH}	$\overline{CS}$ mode	10			ns
Data Read During Conversion	t_{DATA}	Turbo mode/normal mode			190/290	ns
Quiet Time During Acquisition from Last SCK Falling Edge to CNV Rising Edge	t_{QUIET}		20			ns
SCK Period	t_{SCK}	$\overline{CS}$ mode	9			ns
	t_{SCK}	Chain mode	11			ns
SCK Low Time	t_{SCKL}		3.5			ns
SCK High Time	t_{SCKH}		3.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}		2			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				4	ns
CNV or SDI Low to SDO D15 MSB Valid	t_{EN}				5	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}	$\overline{CS}$ mode			8	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$		4			ns
SDI Valid Hold Time from CNV Rising Edge	$t_{HSDICNV}$	$\overline{CS}$ mode	0			ns
	$t_{HSDICNV}$	Chain mode	0			ns
SCK Valid Setup Time from CNV Rising Edge	$t_{SSCKCNV}$	Chain mode	5			ns
SCK Valid Hold Time from CNV Rising Edge	$t_{HSCKCNV}$	Chain mode	5			ns
SDI Valid Setup Time from SCK Falling Edge	$t_{SSDISCK}$	Chain mode	2			ns
SDI Valid Hold Time from SCK Falling Edge	$t_{HSDISCK}$	Chain mode	3			ns
SDI High to SDO High	$t_{DSDOSDI}$	Chain mode with busy indicator			15	ns

[1] See Figure 2 and Figure 3 for load conditions.

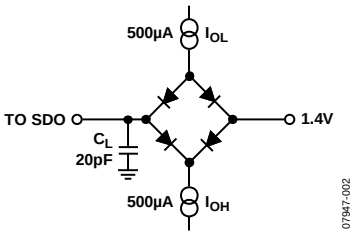

Figure 2. Load Circuit for Digital Interface Timing

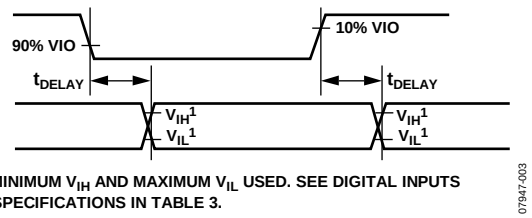

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND[1]	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, BVDD to GND, REFGND	−0.3 V to +6.0 V
AVDD, DVDD, VIO to GND	−0.3 V to +2.7 V
AVDD, DVDD to VIO	−6 V to +3 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
20-Lead LFCSP	30.4°C/W
Lead Temperatures	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Inputs section for an explanation of IN+ and IN−.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

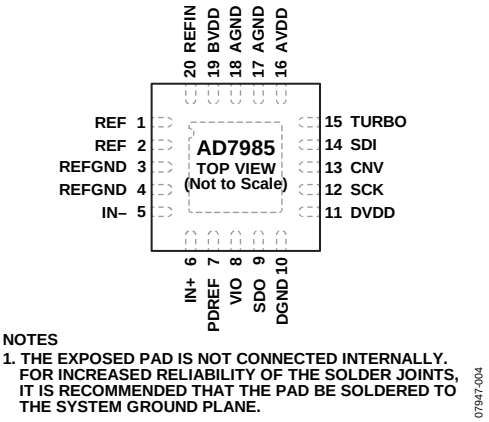

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 2	REF	AI	Reference Output/Input Voltage. When PDREF is low, the internal reference and buffer are enabled, producing 4.096 V on this pin. When PDREF is high, the internal reference and buffer are disabled, allowing an externally supplied voltage reference up to 5.0 V. Decoupling is required with or without the internal reference and buffer. This pin is referred to the REFGND pins and must be decoupled closely to the REFGND pins with a 10 µF capacitor.
3, 4	REFGND	AI	Reference Input Analog Ground.
5	IN–	AI	Analog Input Ground Sense. Connect this pin to the analog ground plane or to a remote ground sense.
6	IN+	AI	Analog Input. This pin is referred to IN–. The voltage range, that is, the difference between IN+ and IN–, is 0 V to V_{REF}.
7	PDREF	DI	Internal Reference Power-Down Input. When this pin is low, the internal reference is enabled. When this pin is high, the internal reference is powered down and an external reference must be used.
8	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply voltage as the host interface (1.8 V, 2.5 V, or 2.7 V).
9	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
10	DGND	P	Digital Power Ground.
11	DVDD	P	Digital Power. Nominally at 2.5 V.
12	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
13	CNV	DI	Convert Input. This input has multiple functions. On the leading edge, it initiates the conversions and selects the interface mode of the device: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data must be read when CNV is high.
14	SDI	DI	Serial Data Input. This input has multiple functions. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In chain mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In $\overline{CS}$ mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
15	TURBO	DI	Conversion Mode Selection. When TURBO is high, the maximum throughput (2.5 MSPS) is achieved, and the ADC does not power down between conversions. When TURBO is low, the maximum throughput is lower (2.0 MSPS), and the ADC powers down between conversions.
16	AVDD	P	Input Analog Power. Nominally at 2.5 V.
17, 18	AGND	P	Analog Power Ground.

Pin No.	Mnemonic	Type[1]	Description
19	BVDD	P	Reference Buffer Power. Nominally at 5.0 V. If an external reference buffer is used to achieve the maximum SNR performance with a 5 V reference, the reference buffer must be powered down by connecting the REFIN pin to ground. The external reference buffer must be connected to the BVDD pin.
20	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. When PDREF is low, the internal band gap reference produces a 1.2 V (typical) voltage on this pin, which needs external decoupling (0.1 µF typical). When PDREF is high, use an external reference to provide 1.2 V (typical) to this pin. When PDREF is high and REFIN is low, the on-chip reference buffer and the band gap reference are powered down. An external reference must be connected to REF and BVDD.
21	Exposed Pad	EP	The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

[1] AI = analog input, AI/O = bidirectional analog, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = DVDD = VIO = 2.5 V, BVDD = 5.0 V, V_{REF} = 5.0 V, external reference (PDREF is high, REFIN is low), unless otherwise noted.

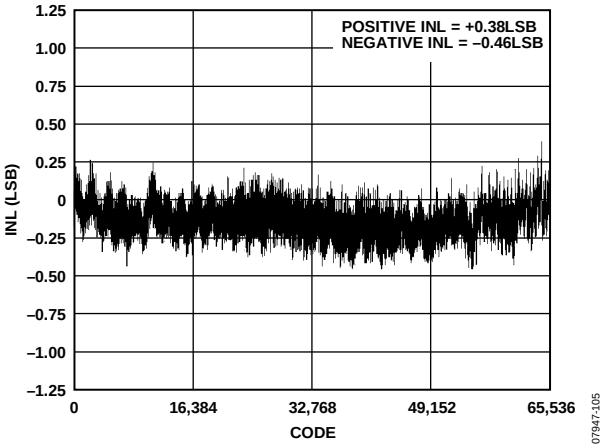

Figure 5. Integral Nonlinearity vs. Code

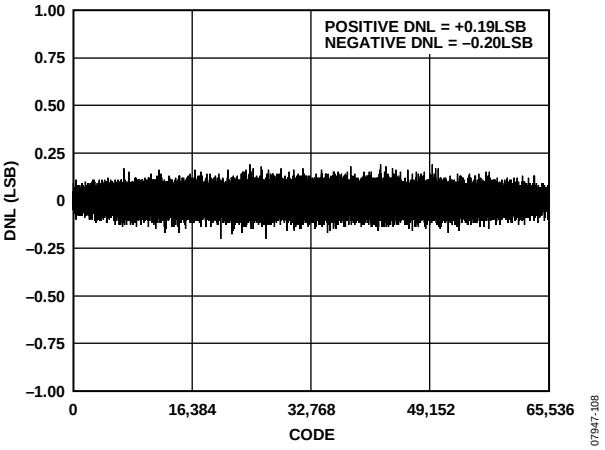

Figure 8. Differential Nonlinearity vs. Code

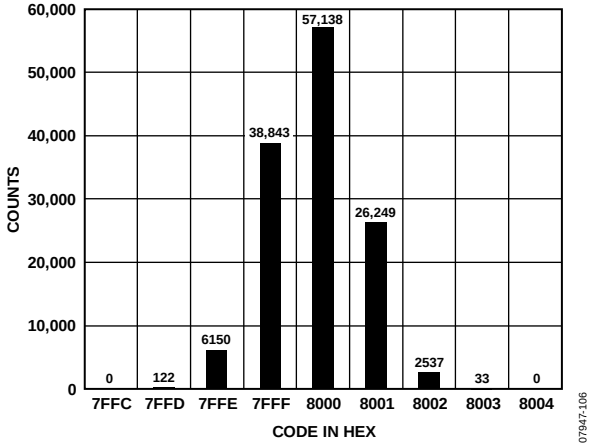

Figure 6. Histogram of DC Input at Code Center (External Reference)

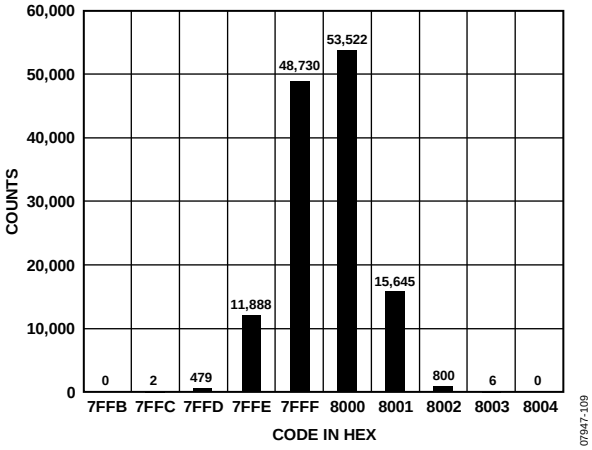

Figure 9. Histogram of DC Input at Code Transition (External Reference)

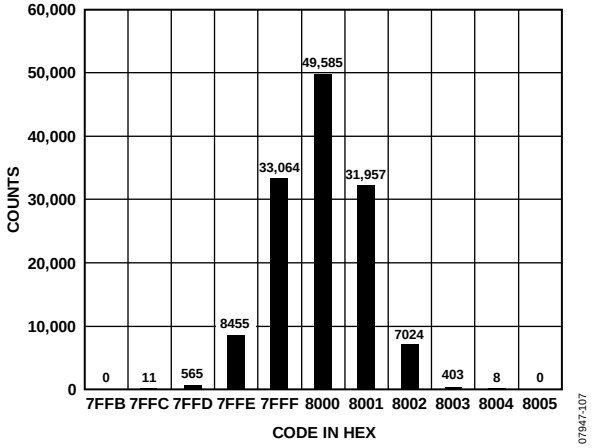

Figure 7. Histogram of DC Input at Code Center (Internal Reference)

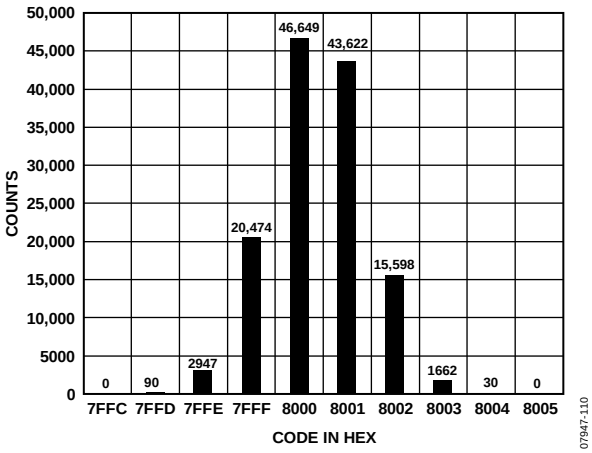

Figure 10. Histogram of DC Input at Code Transition (Internal Reference)

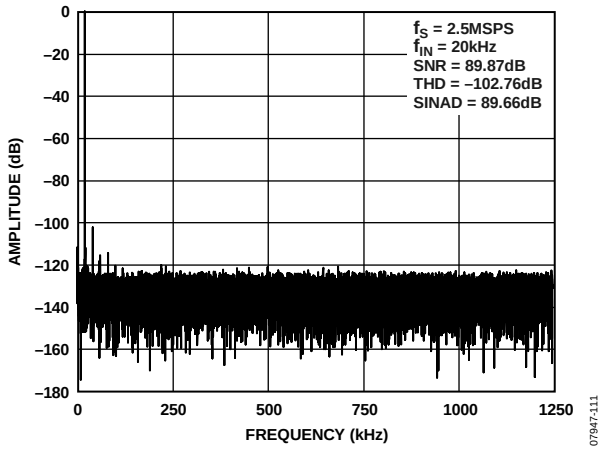

Figure 11. FFT Plot (External Reference)

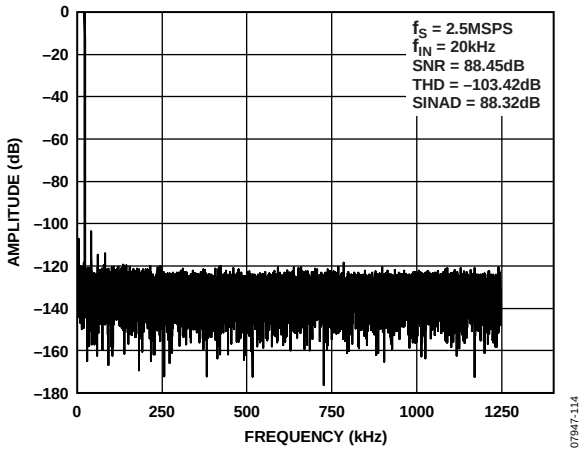

Figure 14. FFT Plot (Internal Reference)

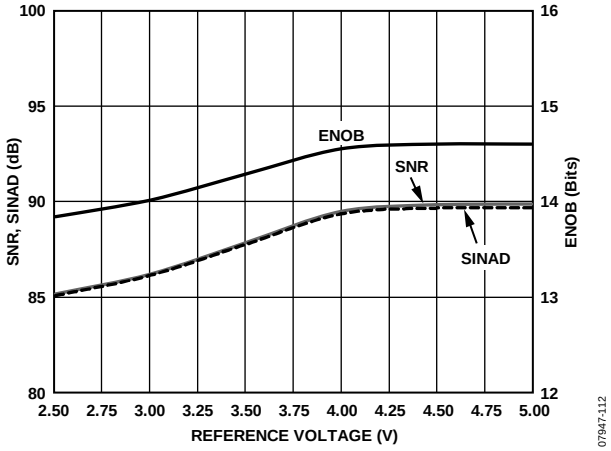

Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

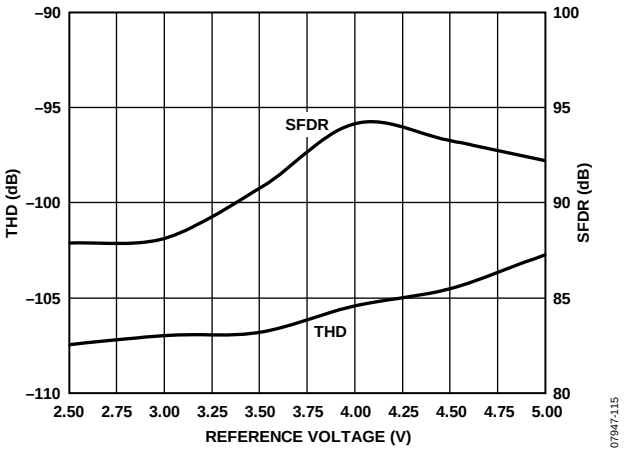

Figure 15. THD and SFDR vs. Reference Voltage

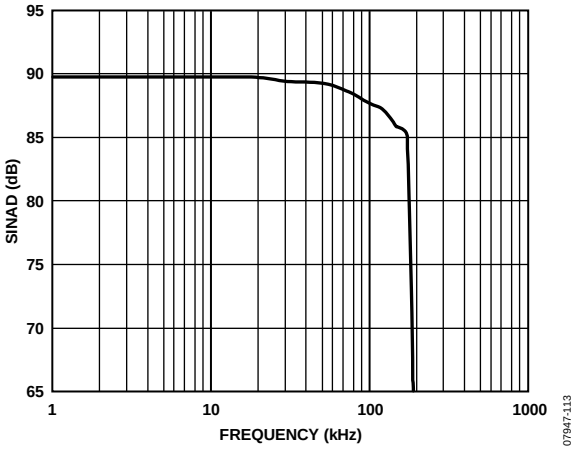

Figure 13. SINAD vs. Frequency

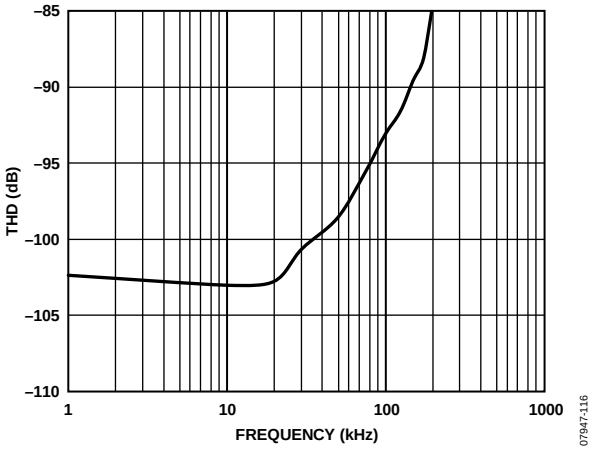

Figure 16. THD vs. Frequency

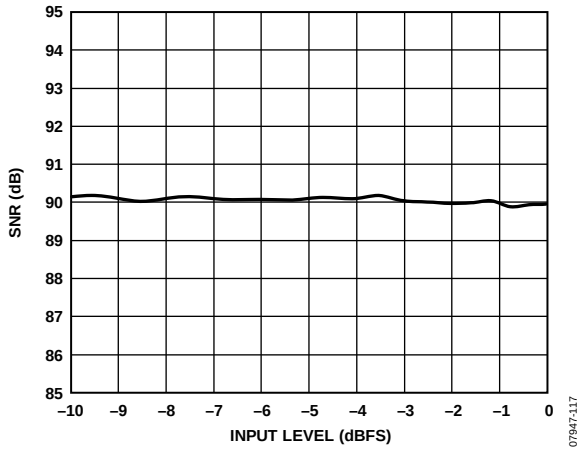

Figure 17. SNR vs. Input Level

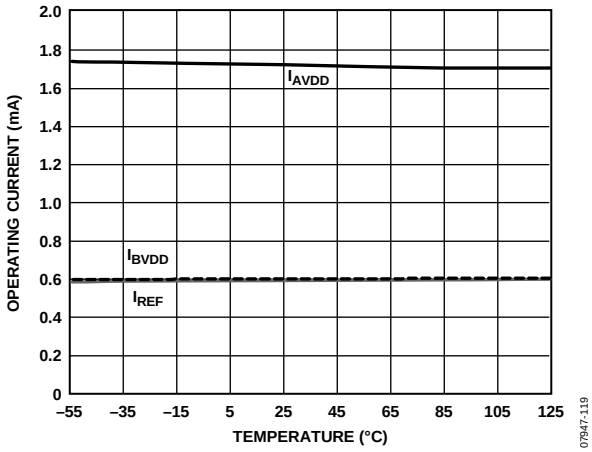

Figure 19. Operating Current vs. Temperature

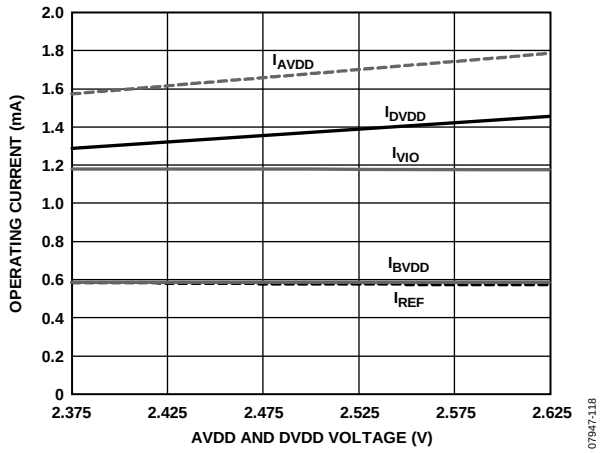

Figure 18. Operating Current vs. Supply Voltage

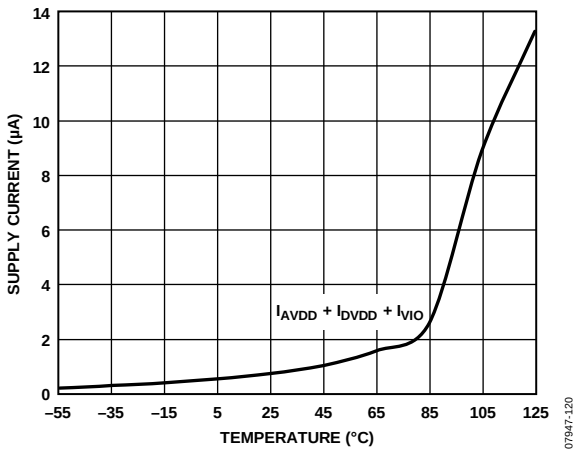

Figure 20. Power-Down Current vs. Temperature

TERMINOLOGY

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is expressed in bits and is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

Effective Resolution
Effective resolution is expressed in bits and is calculated as follows:

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

Gain Error
The last transition (from 111 … 10 to 111 … 11) must occur for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 22).

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is expressed in bits and is calculated as follows:

$$Noise\text{-}Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Transient Response
Transient response is the time required for the ADC to accurately acquire the input after a full-scale step function is applied.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

THEORY OF OPERATION

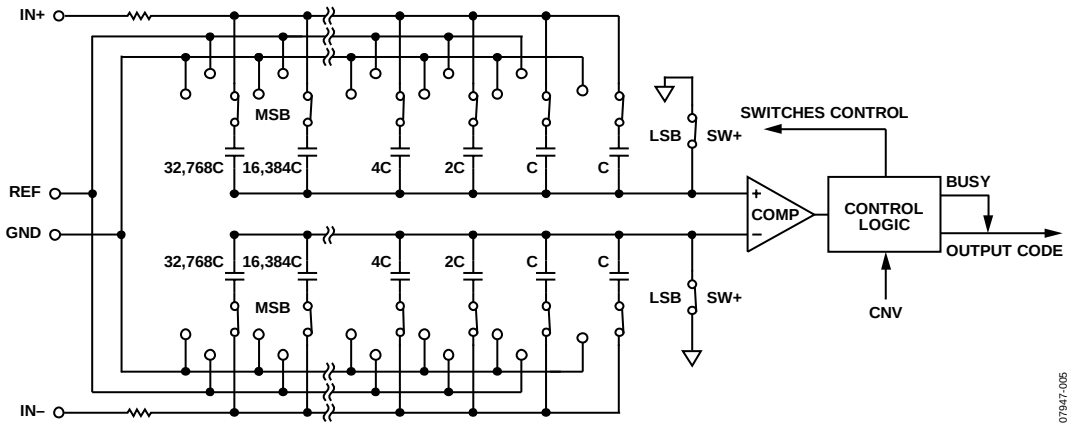

Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7985 is a fast, low power, single-supply, precise, 16-bit ADC using a successive approximation architecture. The AD7985 features different modes to optimize performance according to the application. In turbo mode, the AD7985 is capable of converting 2,500,000 samples per second (2.5 MSPS).

The AD7985 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7985 can be interfaced to any 1.8 V to 2.7 V digital logic family. It is available in a space-saving 20-lead LFCSP that allows flexible configurations. It is pin for pin compatible with the 18-bit AD7986.

CONVERTER OPERATION

The AD7985 is a successive approximation ADC based on a charge redistribution DAC. Figure 21 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array tied to the input of the comparator are connected to AGND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is completed and the CNV input goes high, a conversion phase is initiated.

When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the analog inputs and connected to the REFGND input. Therefore, the differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, … $V_{REF}/65{,}536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7985 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

CONVERSION MODES OF OPERATION

The AD7985 features two conversion modes of operation: turbo and normal. Turbo conversion mode (TURBO is high) allows the fastest conversion rate of up to 2.5 MSPS and does not power down between conversions. The first conversion in turbo mode must be ignored because it contains meaningless data. For applications that require lower power and slightly slower sampling rates, the normal mode (TURBO is low) allows a maximum conversion rate of 2.0 MSPS and powers down between conversions. The first conversion in normal mode contains meaningful data.

Transfer Functions

The ideal transfer function for the AD7985 is shown in Figure 22 and Table 7.

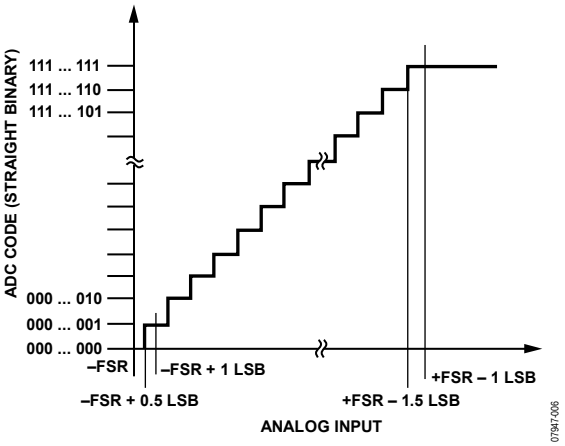

Figure 22. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input, V_{REF} = 4.096 V	Digital Output Code (Hex)
FSR – 1 LSB	4.095938 V	0xFFFF[1]
Midscale + 1 LSB	2.048063 V	0x8001
Midscale	2.048 V	0x8000
Midscale – 1 LSB	2.047938 V	0x7FFF
–FSR + 1 LSB	62.5 µV	0x0001
–FSR	0 V	0x0000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – REFGND).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below REFGND).

TYPICAL CONNECTION DIAGRAM

Figure 23 shows an example of the recommended connection diagram for the AD7985 when multiple supplies are available.

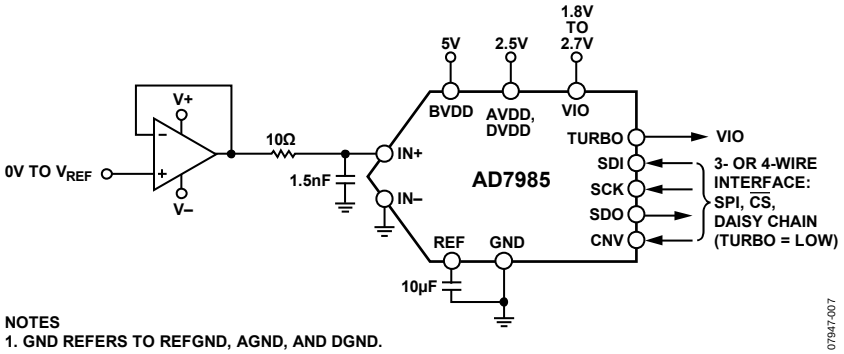

Figure 23. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 24 shows an equivalent circuit of the input structure of the AD7985.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Take care to ensure the analog input signal does not exceed the reference input voltage (REF) by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the V+ and V− supplies of the buffer amplifier in Figure 23) are different from those of REF, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can protect the device.

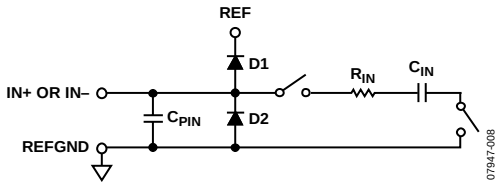

Figure 24. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, the impedance of the analog inputs (IN+ and IN−) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of Resistor R_{IN} and Capacitor C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase, where the switches are closed, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7985 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7985 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7985. The noise from the driver is filtered by the AD7985 analog input circuit one-pole, low-pass filter, made by R_{IN} and C_{IN}, or by the external filter, if one is used. Because the typical noise of the AD7985 is 50 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{50}{\sqrt{50^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

  where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7985 (19 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the operational amplifier in nV/√Hz.
- For ac applications, the driver must have a THD performance commensurate with that of the AD7985.
- For multichannel multiplexed applications, the driver amplifier and the AD7985 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In the data sheet of the driver amplifier, settling at 0.1% to 0.01% is more commonly specified. This value may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
ADA4899-1	Ultralow noise and high frequency
AD8014	Low power and high frequency

VOLTAGE REFERENCE INPUT

The AD7985 allows the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7985 provides excellent performance and can be used in almost all applications.

Internal Reference, REF = 4.096 V (PDREF Low)

To use the internal reference, the PDREF input must be low. This enables the on-chip band gap reference and buffer, resulting in a 4.096 V reference on the REF pin (1.2 V on REFIN).

The internal reference is temperature compensated to 4.096 V ± 15 mV. The reference is trimmed to provide a typical drift of 10 ppm/°C.

The output resistance of REFIN is 6 kΩ when the internal reference is enabled. It is necessary to decouple this pin with a ceramic capacitor of at least 100 nF. The output resistance of REFIN and the decoupling capacitor form an RC filter, which helps to reduce noise.

Because the output impedance of REFIN is typically 6 kΩ, relative humidity (among other industrial contaminants) can directly affect the drift characteristics of the reference. A guard ring typically reduces the effects of drift under such circumstances. However, the fine pitch of the AD7985 makes this difficult to implement. One solution, in these industrial and other types of applications, is to use a conformal coating, such as Dow Corning® 1-2577 or HumiSeal® 1B73.

External 1.2 V Reference and Internal Buffer (PDREF High)

To use an external reference along with the internal buffer, PDREF must be high. This powers down the internal reference and allows the 1.2 V reference to be applied to REFIN, producing 4.096 V (typically) on the REF pin.

External Reference (PDREF High, REFIN Low)

To apply an external reference voltage directly to the REF pin, PDREF must be tied high and REFIN must be tied low. BVDD must also be driven to the same potential as REF. For example, if REF = 2.5 V, BVDD must be tied to 2.5 V.

The advantages of directly using an external voltage reference are as follows:

- SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a larger reference voltage (5 V) instead of a typical 4.096 V reference when the internal reference is used. This is calculated by

$$SNR = 20 \log\left(\frac{4.096}{5.0}\right)$$

- Power savings when the internal reference is powered down (PDREF high).

Reference Decoupling

The AD7985 voltage reference input, REF, has a dynamic input impedance that requires careful decoupling between the REF and REFGND pins. The Layout section describes how this can be done.

When using an external reference, a very low impedance source (for example, a reference buffer using the AD8031 or the AD8605) and a 10 µF (X5R, 0805 size) ceramic chip capacitor are appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For example, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR434 reference.

If desired, a reference decoupling capacitor with a value as small as 2.2 µF can be used with minimal impact on performance, especially DNL.

In any case, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and REFGND pins.

POWER SUPPLY

The AD7985 has four power supply pins: an analog supply (AVDD), a buffer supply (BVDD), a digital supply (DVDD), and a digital input/output interface supply (VIO). VIO allows direct interface with any logic from 1.8 V to 2.7 V. To reduce the number of supplies needed, VIO, DVDD, and AVDD can be tied together. The power supplies do not need to be started in a particular sequence. In addition, the AD7985 is very insensitive to power supply variations over a wide frequency range.

In normal mode, the AD7985 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate. This makes the device ideal for low sampling rates (even a few SPS) and battery-powered applications.

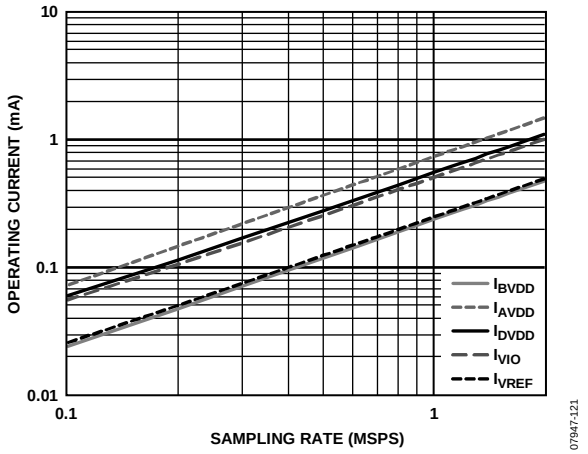

Figure 25. Operating Current vs. Sampling Rate in Normal Mode

DIGITAL INTERFACE

Although the AD7985 has a reduced number of pins, it offers flexibility in the serial interface modes.

In $\overline{CS}$ mode, the AD7985 is compatible with SPI, MICROWIRE, QSPI, and digital hosts. In $\overline{CS}$ mode, the AD7985 can use either a 3-wire or a 4-wire interface. A 3-wire interface that uses the CNV, SCK, and SDO signals minimizes wiring connections, which is useful, for example, in isolated applications. A 4-wire interface that uses the SDI, CNV, SCK, and SDO signals allows CNV, which initiates conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

In chain mode, the AD7985 provides a daisy-chain feature that uses the SDI input for cascading multiple ADCs on a single data line similar to a shift register. Chain mode is available only in normal mode (TURBO is low).

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI is high, and chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, chain mode is always selected.

In normal mode operation, the AD7985 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled in $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 29 and Figure 33). TURBO must be kept low for both digital interfaces.

When CNV is low, readback can occur during conversion or acquisition, or it can be split across acquisition and conversion, as described in the following sections.

A discontinuous SCK is recommended because the device is selected with CNV low, and SCK activity begins to clock out data.

Note that in the following sections, the timing diagrams indicate digital activity (SCK, CNV, SDI, and SDO) during the conversion. However, due to the possibility of performance degradation, digital activity must occur only prior to the safe data reading time, t_{DATA}, because the AD7985 provides error correction circuitry that can correct for an incorrect bit decision during this time. From t_{DATA} to t_{CONV}, there is no error correction, and conversion results may be corrupted.

Similarly, t_{QUIET}, the time from the last falling edge of SCK to the rising edge of CNV, must remain free of digital activity. The user must configure the AD7985 and initiate the busy indicator (if desired in normal mode) prior to t_{DATA}.

It is also possible to corrupt the sample by having SCK near the sampling instant. Therefore, it is recommended that the digital pins be kept quiet for approximately 20 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

DATA READING OPTIONS

There are three different data reading options for the AD7985. There is the option to read during conversion, to split the read across acquisition and conversion (see Figure 26 and Figure 27), and, in normal mode, to read during acquisition. The desired SCK frequency largely determines which reading option to use.

Reading During Conversion, Fast Host (Turbo or Normal Mode)

When reading during conversion (n), conversion results are for the previous (n − 1) conversion. Reading must occur only up to t_{DATA} and, because this time is limited, the host must use a fast SCK.

The required SCK frequency is calculated by

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA} - t_{CNVH} - t_{EN}}$$

To determine the minimum SCK frequency, follow these examples to read data from conversion (n − 1).

For turbo mode (2.5 MSPS),

Number_SCK_Edges = 16; t_{DATA} = 190 ns; t_{CNVH} = 10 ns; t_{EN} = 5 ns

f_{SCK} = 16/(190 ns − 10 ns − 5 ns) = 91.5 MHz

For normal mode (2.0 MSPS),

Number_SCK_Edges = 16; t_{DATA} = 290 ns; t_{CNVH} = 10 ns; t_{EN} = 5 ns

f_{SCK} = 16/(290 ns − 10 ns − 5 ns) = 58.2 MHz

The time between t_{DATA} and t_{CONV} is an input/output quiet time during which digital activity must not occur, or sensitive bit decisions may be corrupted.

Split-Reading, Any Speed Host (Turbo or Normal Mode)

To allow for a slower SCK, there is the option of a split read, where data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n − 1) conversion.

Similar to reading during conversion, split-reading must occur only up to t_{DATA}. For the maximum throughput, the only time restriction is that split-reading take place during the t_{ACQ} (minimum) + (t_{DATA} − t_{QUIET}) time. The time between the falling edge of SCK and CNV rising is an acquisition quiet time, t_{QUIET}.

To determine how to split the read for a particular SCK frequency, follow these examples to read data from conversion (n − 1).

For turbo mode (2.5 MSPS),

f_{SCK} = 75 MHz; t_{DATA} = 190 ns; t_{CNVH} = 10 ns; t_{EN} = 5 ns

Number_SCK_Edges = 75 MHz × (190 ns − 10 ns − 5 ns) = 13.1

Thirteen bits are read during conversion (n), and three bits are read during acquisition (n).

For normal mode (2.0 MSPS),

f_{SCK} = 50 MHz; t_{DATA} = 290 ns; t_{CNVH} = 10 ns; t_{EN} = 5 ns

Number_SCK_Edges = 50 MHz × (290 ns − 10 ns − 5 ns) = 13.75

Thirteen bits are read during conversion (n), and three bits are read during acquisition (n).

For slow throughputs, the time restriction is dictated by the throughput required by the user; the host is free to run at any speed. Similar to reading during acquisition, data access for slow hosts must take place during the acquisition phase with additional time into the conversion.

Note that data access spanning conversion requires the CNV pin to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Thus, the host must perform two bursts of data access when using this method.

Reading During Acquisition, Any Speed Host (Turbo or Normal Mode)

When reading during acquisition (n), conversion results are for the previous (n − 1) conversion. Maximum throughput is achievable in normal mode (2.0 MSPS); however, in turbo mode, 2.5 MSPS throughput is not achievable.

For the maximum throughput, the only time restriction is that reading take place during the t_{ACQ} (minimum) time. For slow throughputs, the time restriction is dictated by the throughput required by the user; the host is free to run at any speed. Thus, for slow hosts, data access must take place during the acquisition phase.

$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 26, and the corresponding timing is given in Figure 27.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. When a conversion is initiated, it continues until completion, irrespective of the state of CNV.

This can be useful, for example, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD7985 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

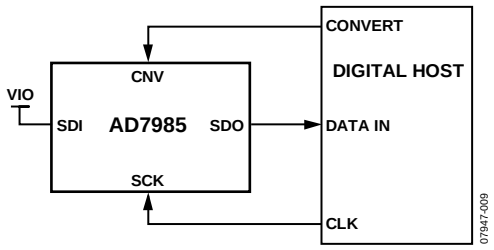

Figure 26. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

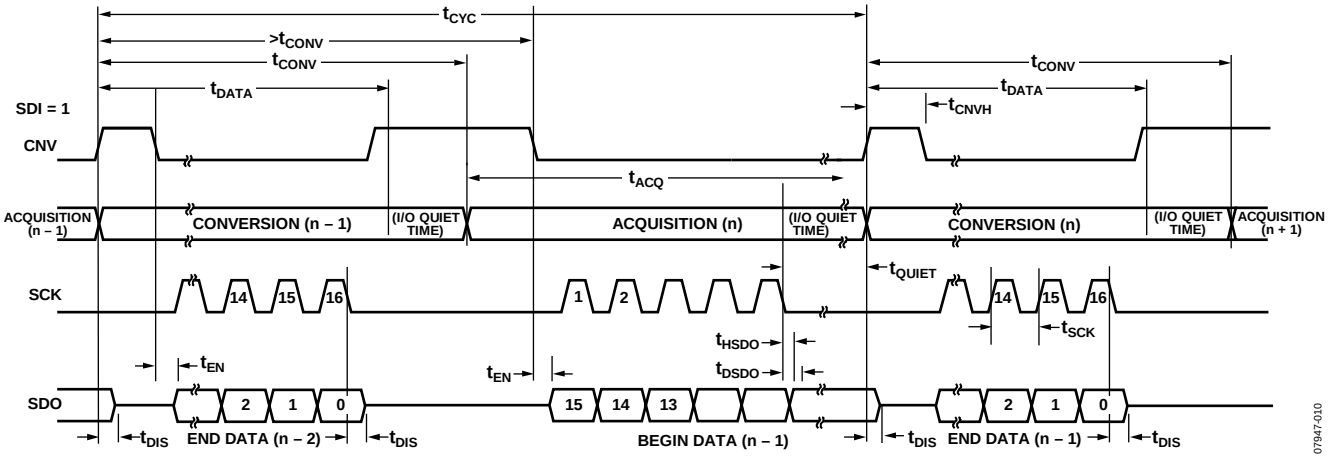

Figure 27. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host that has an interrupt input. It is available only in normal conversion mode (TURBO is low). The connection diagram is shown in Figure 28, and the corresponding timing is given in Figure 29.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion, irrespective of the state of CNV. Prior to the minimum conversion time, CNV can select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the optional 17th SCK falling edge, SDO returns to high impedance.

If multiple AD7985 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended that this contention be kept as short as possible to limit extra power dissipation.

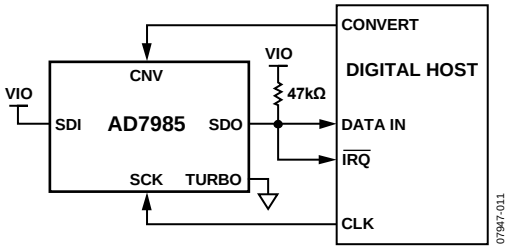

Figure 28. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

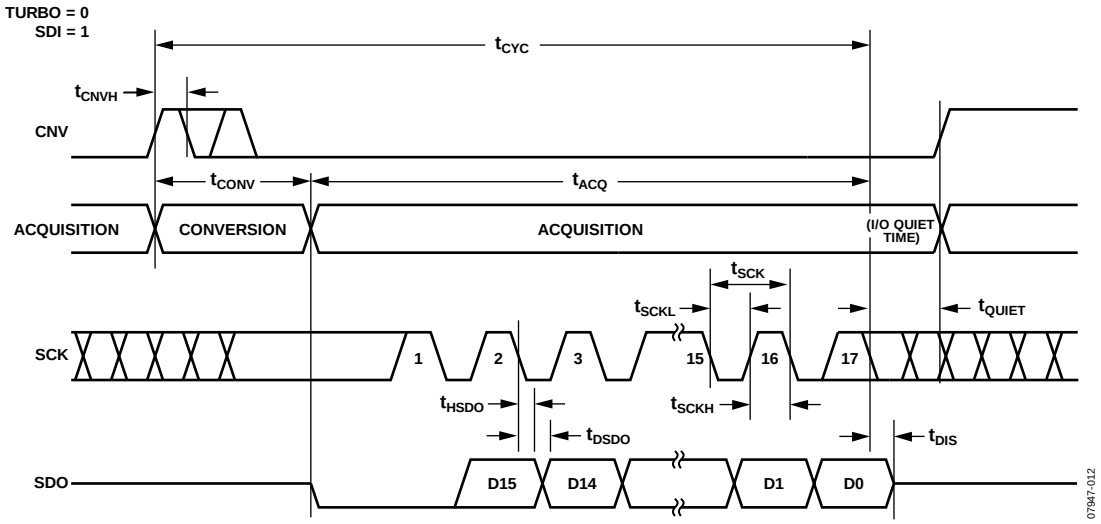

Figure 29. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7985 devices are connected to an SPI-compatible digital host. A connection diagram example using two AD7985 devices is shown in Figure 30, and the corresponding timing is given in Figure 31.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multi-plexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD7985 enters the acquisition phase and powers down. Each ADC result can be read by bringing the SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCK falling edge, SDO returns to high impedance and another AD7985 can be read.

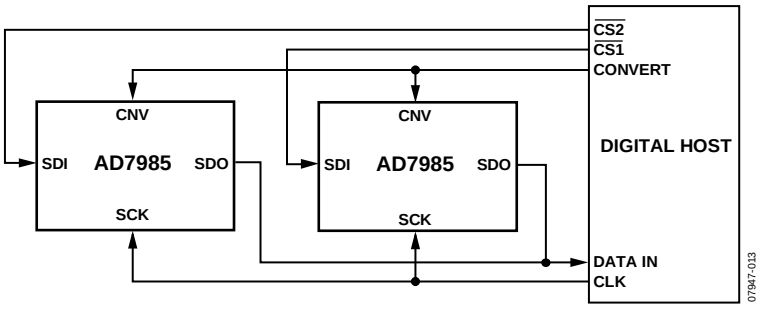

Figure 30. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

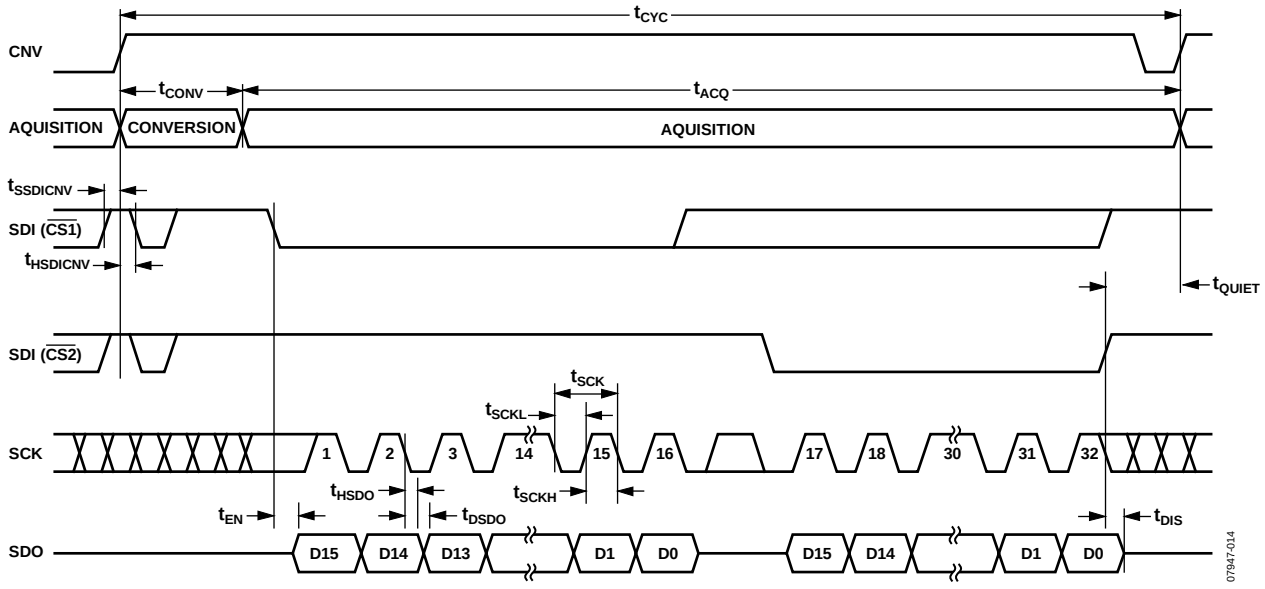

Figure 31. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host with an interrupt input and when it is desired to keep CNV, which samples the analog input, independent of the signal that selects the data reading. This independence is particularly important in applications where low jitter on CNV is desired. This mode is available only in normal conversion mode (TURBO is low). The connection diagram is shown in Figure 32, and the corresponding timing is given in Figure 33.

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.)

Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that it has an accept-able hold time. After the optional 17th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

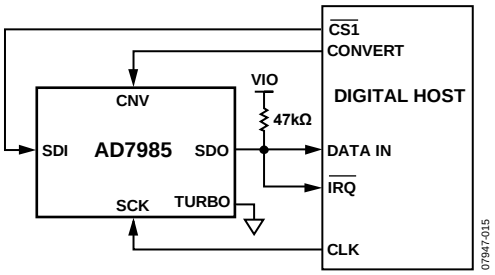

Figure 32. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Connection Diagram

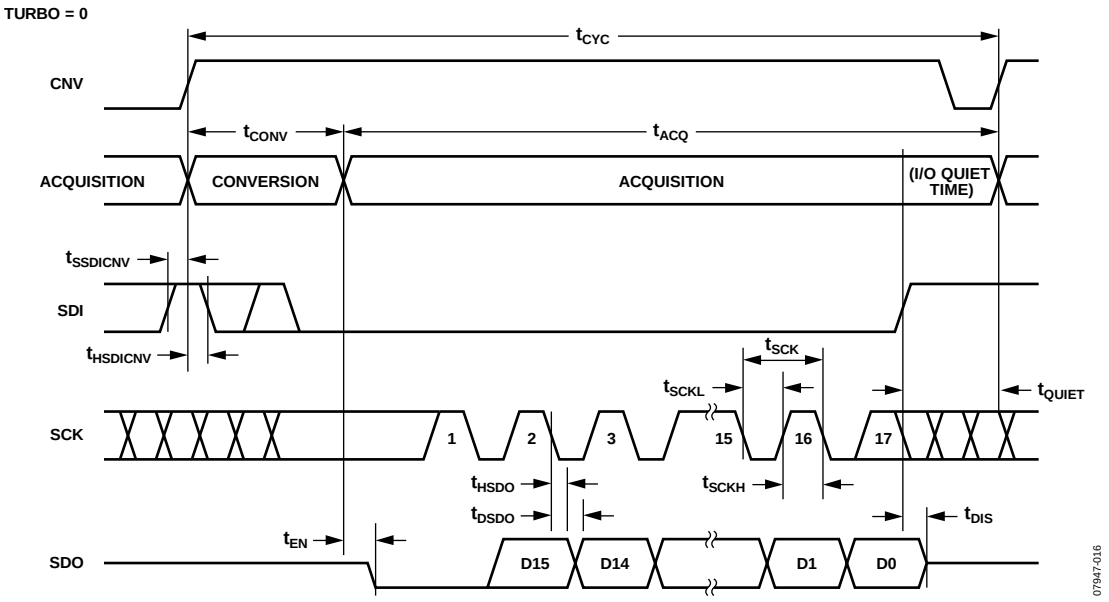

Figure 33. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

This mode can daisy-chain multiple AD7985 devices on a 3-wire serial interface. It is available only in normal conversion mode (TURBO is low). This feature is useful for reducing component count and wiring connections, for example, in isolated multi-converter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using two AD7985 devices is shown in Figure 34, and the corresponding timing is given in Figure 35.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback.

When the conversion is complete, the MSB is output onto SDO, and the AD7985 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs the data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7985 devices in the chain, provided that the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

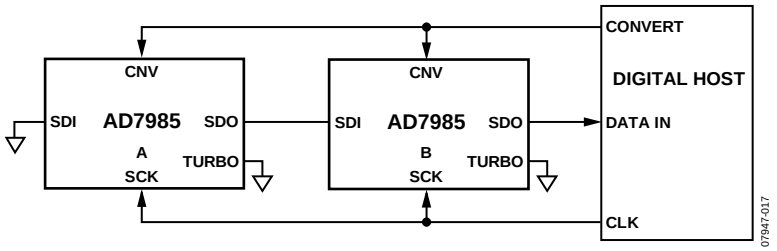

Figure 34. Chain Mode Without Busy Indicator Connection Diagram

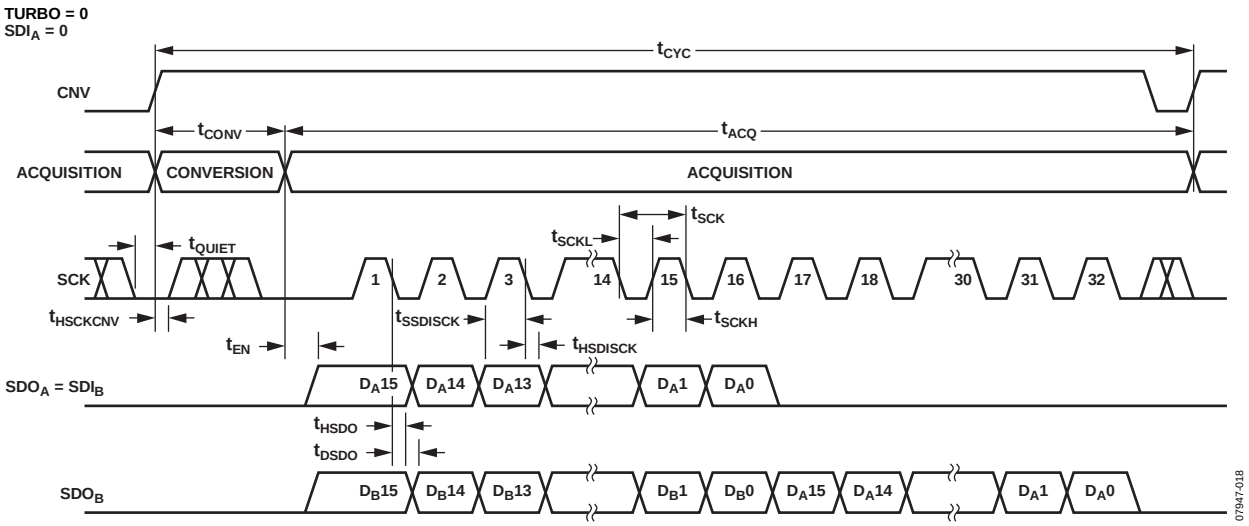

Figure 35. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can daisy-chain multiple AD7985 devices on a 3-wire serial interface while providing a busy indicator. It is available only in normal conversion mode (TURBO is low). This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using three AD7985 devices is shown in Figure 36, and the corresponding timing is given in Figure 37.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback.

When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7985 ADC labeled C in Figure 36) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs the data MSB first, and 16 × N + 1 clocks are required to read back the N ADCs. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7985 devices in the chain, provided that the digital host has an acceptable hold time.

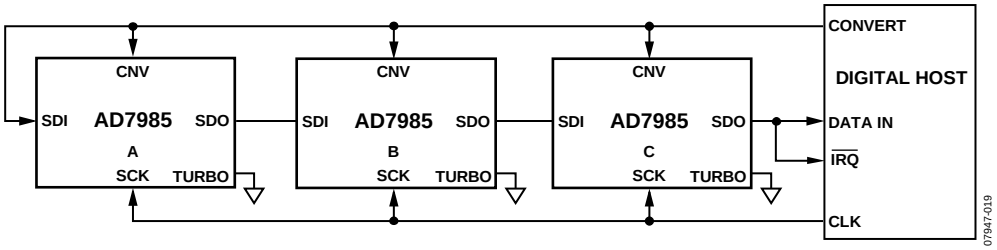

Figure 36. Chain Mode with Busy Indicator Connection Diagram

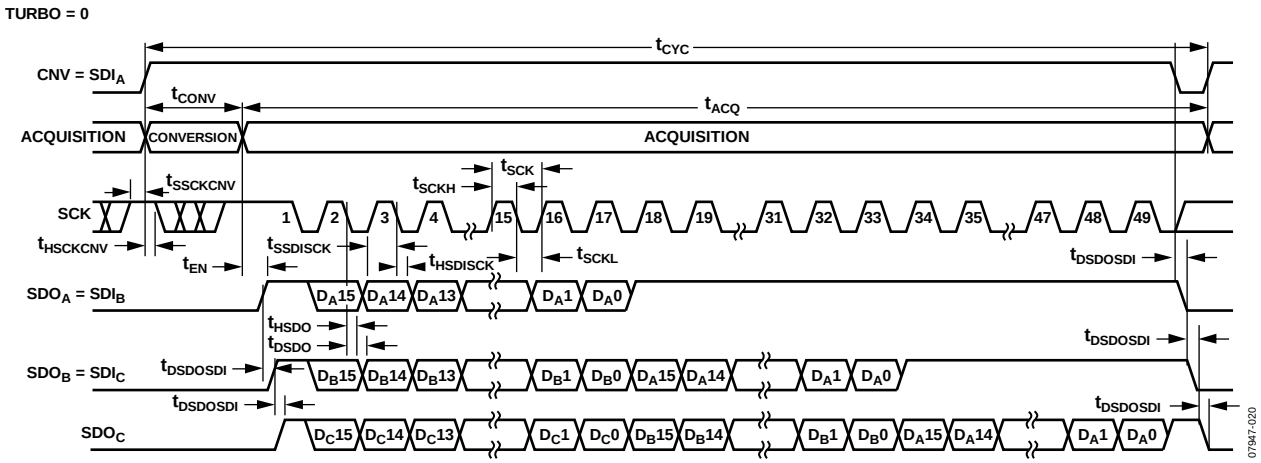

Figure 37. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATIONS INFORMATION

LAYOUT

Design the printed circuit board (PCB) that houses the AD7985 so the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7985, with the analog signals on the left side and the digital signals on the right side, eases this task.

Avoid running digital lines under the device because they couple noise onto the die, unless a ground plane under the AD7985 is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Crossover of digital and analog signals must be avoided.

At least one ground plane must be used. It can be common or split between the digital and analog sections. In the latter case, the planes must be joined underneath the AD7985 devices.

The AD7985 voltage reference inputs (REF) have a dynamic input impedance and must be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right against, the REF and REFGND pins and connecting them with wide, low impedance traces.

Finally, the power supplies, VDD and VIO of the AD7985, must be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7985 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

EVALUATING THE AD7985 PERFORMANCE

Other recommended layouts for the AD7985 are outlined in the documentation for the AD7985 evaluation board (EVAL-AD7985FMCZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CH1Z board.

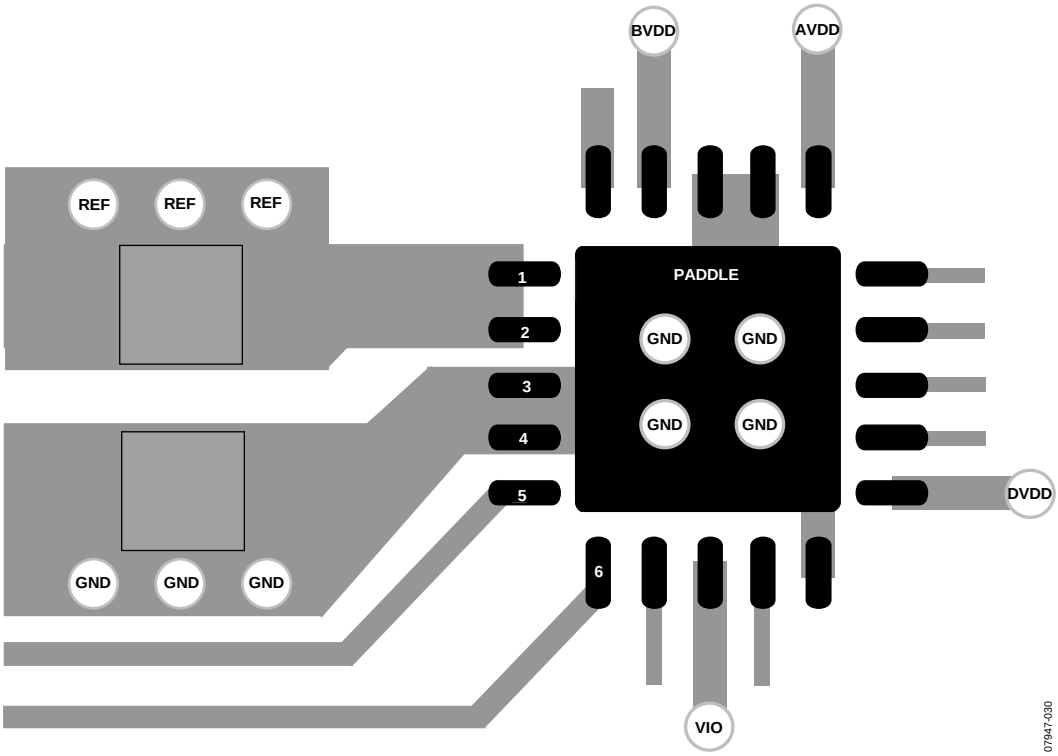

Figure 38. Example Layout of the AD7985 (Top Layer)

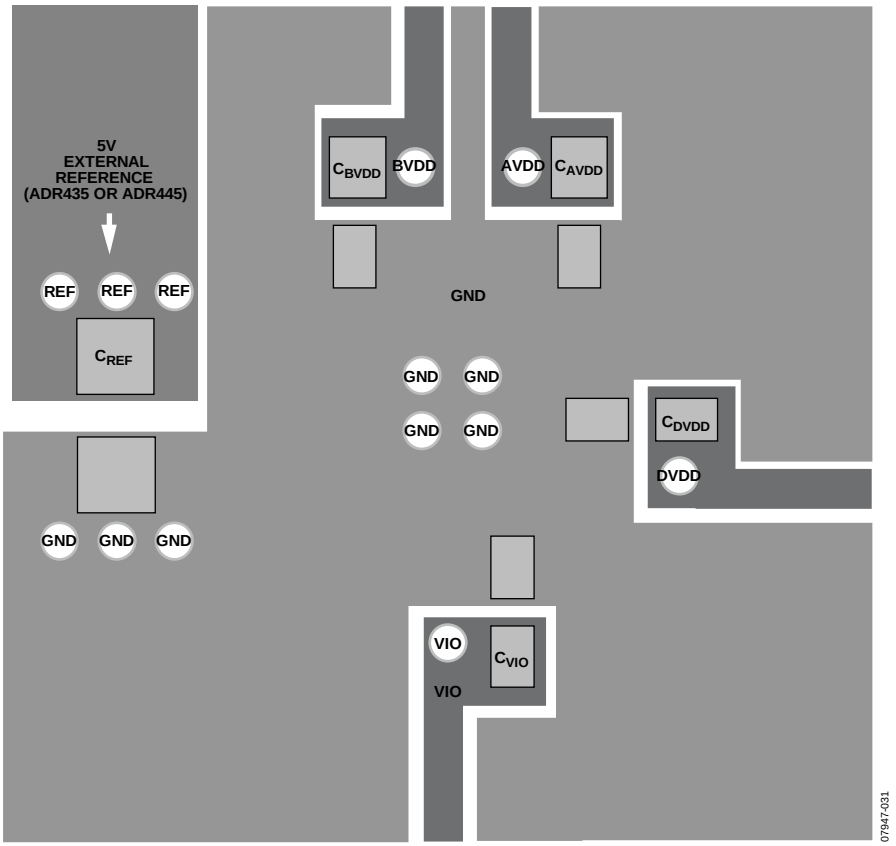

Figure 39. Example Layout of the AD7985 (Bottom Layer)

OUTLINE DIMENSIONS

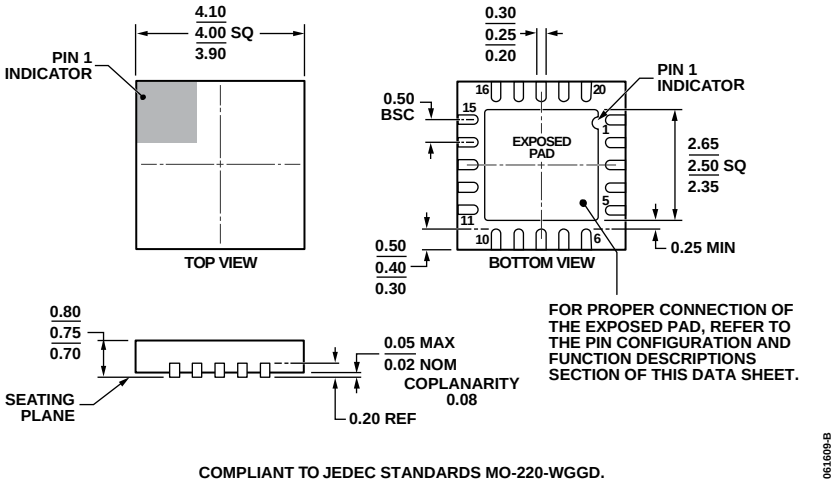

Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD7985BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP], Tray	CP-20-10	490
AD7985BCPZ-RL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-20-10	1,500
EVAL-AD7985FMCZ		Evaluation Board		
EVAL-SDP-CH1Z		Controller Board		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7985FMCZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CH1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CH1Z allows a PC to control and communicate with all Analog Devices evaluation boards ending in the FMC designator.

NOTES