# AD5662* PRODUCT PAGE QUICK LINKS

**Last Content Update: 12/18/2017**

## COMPARABLE PARTS

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## EVALUATION KITS

- AD5662 Evaluation Board

## DOCUMENTATION

**Application Notes**

- AN-1412: 4 mA to 20 mA Process Control Loop Using the AD5662 DAC

**Data Sheet**

- AD5662: 2.7 V to 5.5 V, 250 µA, Rail-to-Rail Output 16-Bit *nano*DAC™ in SOT-23 Data Sheet

**User Guides**

- UG-444: Evaluating the AD5750 Industrial Current/Voltage Output Driver

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5446 IIO DAC Linux Driver
- AD5791 IIO DAC Linux Driver
- AD5620/AD5640/AD5660/AD5662 Evaluation Software
- BeMicro FPGA Project for CN0202 with Nios driver
- BeMicro FPGA Project for CN0204 with Nios driver
- CN0202 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- CN0204 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design

## REFERENCE DESIGNS

- CN0063
- CN0064
- CN0202
- CN0204

## REFERENCE MATERIALS

**Solutions Bulletins & Brochures**

- Digital to Analog Converters ICs Solutions Bulletin

## DESIGN RESOURCES

- AD5662 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

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## SAMPLE AND BUY

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**1/05—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.5 V; $R_L$ = 2 kΩ to GND; $C_L$ = 200 pF to GND; $V_{REF}$ = $V_{DD}$; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| | A Grade | | | B Grade | | | | Y Version[1] |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Conditions/Comments** |
| STATIC PERFORMANCE[2] | | | | | | | | |
| Resolution | 16 | | | 16 | | | Bits | |
| Relative Accuracy | | ±8 | ±32 | | ±8 | ±16 | LSB | See Figure 4 |
| Differential Nonlinearity | | | ±1 | | | ±1 | LSB | Guaranteed monotonic by design<br>See Figure 5 |
| Zero Code Error | | 2 | 10 | | 2 | 10 | mV | All 0s loaded to DAC register |
| Full-Scale Error | | −0.2 | −1 | | −0.2 | −1 | % FSR | All 1s loaded to DAC register |
| Offset Error | | | ±10 | | | ±10 | mV | |
| Gain Error | | | ±1.5 | | | ±1.5 | % FSR | |
| Zero Code Error Drift[3] | | ±2 | | | ±2 | | µV/°C | |
| Gain Temperature Coefficient[3] | | ±2.5 | | | ±2.5 | | ppm | Of FSR/°C |
| DC Power Supply Rejection Ratio[3] | | −100 | | | −100 | | dB | DAC code = midscale; $V_{DD}$ = 5 V/3 V ±10% |
| OUTPUT CHARACTERISTICS[3] | | | | | | | | |
| Output Voltage Range | 0 | | $V_{DD}$ | 0 | | $V_{DD}$ | V | |
| Output Voltage Settling Time | | 8 | 10 | | 8 | 10 | µs | ¼ to ¾ scale change settling to ±2 LSB<br>$R_L$ = 2 kΩ; 0 pF < $C_L$ < 200 pF |
| Slew Rate | | 1.5 | | | 1.5 | | V/µs | ¼ to ¾ scale |
| Capacitive Load Stability | | 2 | | | 2 | | nF | $R_L$ = ∞ |
| | | 10 | | | 10 | | nF | $R_L$ = 2 kΩ |
| Output Noise Spectral Density[4] | | 100 | | | 100 | | nV/√Hz | DAC code = midscale,10 kHz |
| Output Noise (0.1 Hz to 10 Hz)[4] | | 10 | | | 10 | | µV p-p | DAC code = midscale |
| Total Harmonic Distortion (THD)[4] | | −80 | | | −80 | | dB | $V_{REF}$ = 2 V ± 300 mV p-p, f = 5 kHz |
| Digital-to-Analog Glitch Impulse | | 5 | | | 5 | | nV-s | 1 LSB change around major carry |
| Digital Feedthrough | | 0.1 | | | 0.1 | | nV-s | |
| DC Output Impedance | | 0.5 | | | 0.5 | | Ω | |
| Short-Circuit Current[4] | | 30 | | | 30 | | mA | $V_{DD}$ = 5 V, 3 V |
| Power-Up Time | | 4 | | | 4 | | µs | Coming out of power-down mode<br>$V_{DD}$ = 5 V, 3 V |
| REFERENCE INPUT[3] | | | | | | | | |
| Reference Current | | 40 | 75 | | 40 | 75 | µA | $V_{REF}$ = $V_{DD}$ = 5 V |
| | | 30 | 50 | | 30 | 50 | µA | $V_{REF}$ = $V_{DD}$ = 3.6 V |
| Reference Input Range[5] | 0.75 | | $V_{DD}$ | 0.75 | | $V_{DD}$ | V | |
| Reference Input Impedance | | 125 | | | 125 | | kΩ | |
| LOGIC INPUTS[3] | | | | | | | | |
| Input Current | | | ±2 | | | ±2 | µA | All digital inputs |
| $V_{INL}$, Input Low Voltage | | | 0.8 | | | 0.8 | V | $V_{DD}$ = 5 V, 3 V |
| $V_{INH}$, Input High Voltage | 2 | | | | 2 | | V | $V_{DD}$ = 5 V, 3 V |
| Pin Capacitance | | 3 | | | 3 | | pF | |

| Parameter | A Grade Min | A Grade Typ | A Grade Max | B Grade Min | B Grade Typ | B Grade Max | Unit | Y Version[1] Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | | | | |
| $V_{DD}$ | 2.7 | | 5.5 | 2.7 | | 5.5 | V | All digital inputs at 0 V or $V_{DD}$ |
| $I_{DD}$ (Normal Mode) | | | | | | | | DAC active and excluding load current |
| $V_{DD}$ = 4.5 V to 5.5 V | | 150 | 250 | | 150 | 250 | µA | $V_{IH} = V_{DD}$ and $V_{IL}$ = GND |
| $V_{DD}$ = 2.7 V to 3.6 V | | 140 | 225 | | 140 | 225 | µA | $V_{IH} = V_{DD}$ and $V_{IL}$ = GND |
| $I_{DD}$ (All Power-Down Modes) | | | | | | | | |
| $V_{DD}$ = 4.5 V to 5.5 V | | 0.48 | 1 | | 0.48 | 1 | µA | $V_{IH} = V_{DD}$ and $V_{IL}$ = GND |
| $V_{DD}$ = 2.7 V to 3.6 V | | 0.1 | 0.375 | | 0.1 | 0.375 | µA | $V_{IH} = V_{DD}$ and $V_{IL}$ = GND |
| POWER EFFICIENCY | | | | | | | | |
| $I_{OUT}/I_{DD}$ | | 90 | | | 90 | | % | $I_{LOAD}$ = 2 mA. $V_{DD}$ = 5 V |

[1] Temperature range is as follows: Y version: −40°C to +125°C, typical at +25°C.
[2] DC specifications tested with the outputs unloaded, unless otherwise stated. Linearity calculated using a reduced code range of 512 to 65024.
[3] Guaranteed by design and characterization; not production tested.
[4] Output unloaded.
[5] Reference input range at ambient where ±1 LSB max DNL specification is achievable.

# TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of $V_{DD}$) and timed from a voltage level of ($V_{IL}$ + $V_{IH}$)/2. See Figure 2. $V_{DD}$ = 2.7 V to 5.5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| | Limit at $T_{MIN}$, $T_{MAX}$ | | | |
|---|---|---|---|---|
| **Parameter** | **$V_{DD}$ = 2.7 V to 3.6 V** | **$V_{DD}$ = 3.6 V to 5.5 V** | **Unit** | **Conditions/Comments** |
| $t_1$[1] | 50 | 33 | ns min | SCLK cycle time |
| $t_2$ | 13 | 13 | ns min | SCLK high time |
| $t_3$ | 13 | 13 | ns min | SCLK low time |
| $t_4$ | 13 | 13 | ns min | $\overline{SYNC}$ to SCLK falling edge setup time |
| $t_5$ | 5 | 5 | ns min | Data setup time |
| $t_6$ | 4.5 | 4.5 | ns min | Data hold time |
| $t_7$ | 0 | 0 | ns min | SCLK falling edge to $\overline{SYNC}$ rising edge |
| $t_8$ | 50 | 33 | ns min | Minimum $\overline{SYNC}$ high time |
| $t_9$ | 13 | 13 | ns min | $\overline{SYNC}$ rising edge to SCLK fall ignore |
| $t_{10}$ | 0 | 0 | ns min | SCLK falling edge to $\overline{SYNC}$ fall ignore |

[1] Maximum SCLK frequency is 30 MHz at $V_{DD}$ = 3.6 V to 5.5 V, and 20 MHz at $V_{DD}$ = 2.7 V to 3.6 V.

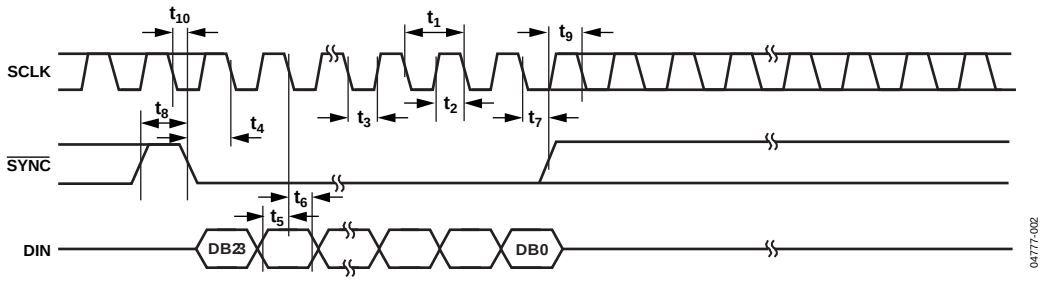



*Figure 2. Serial Write Operation*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{OUT}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{FB}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{REF}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Operating Temperature Range | |
| Industrial (Y Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 150°C |
| Power Dissipation | ($T_J$ max − $T_A$)/$\theta_{JA}$ |
| SOT-23 Package (4-Layer Board) | |
| $\theta_{JA}$ Thermal Impedance | 119°C/W |
| MSOP Package (4-Layer Board) | |
| $\theta_{JA}$ Thermal Impedance | 141°C/W |
| $\theta_{JC}$ Thermal Impedance | 44°C/W |
| Reflow Soldering Peak Temperature | |
| SnPb | 240°C |
| Pb-free | 260°C |
| ESD | 2 kV |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTION

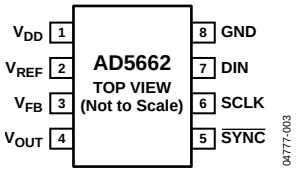



*Figure 3. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 | $V_{DD}$ | Power Supply Input. These parts can be operated from 2.7 V to 5.5 V. $V_{DD}$ should be decoupled to GND. |
| 2 | $V_{REF}$ | Reference Voltage Input. |
| 3 | $V_{FB}$ | Feedback Connection for the Output Amplifier. $V_{FB}$ should be connected to $V_{OUT}$ for normal operation. |
| 4 | $V_{OUT}$ | Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation. |
| 5 | $\overline{SYNC}$ | Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC. |
| 6 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz. |
| 7 | DIN | Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. |
| 8 | GND | Ground Reference Point for All Circuitry on the Part. |

# TYPICAL PERFORMANCE CHARACTERISTICS

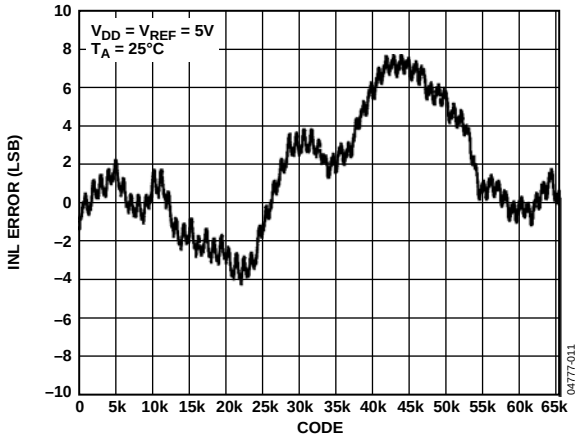



*Figure 4. Typical INL Plot*

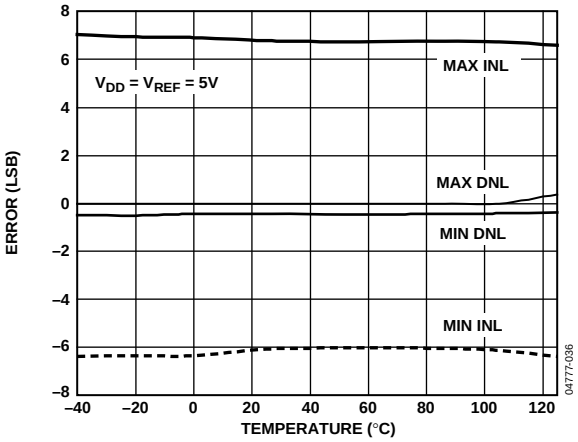



*Figure 7. INL Error and DNL Error vs. Temperature*

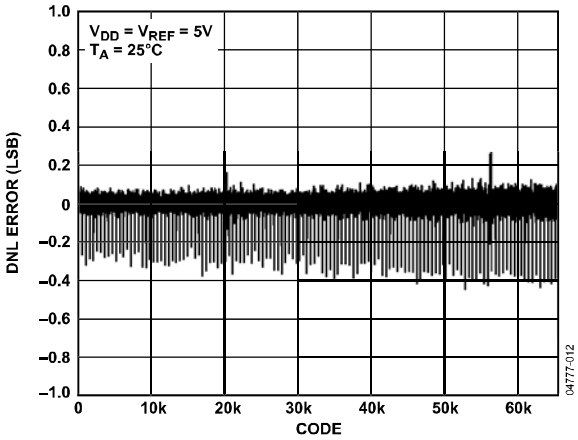



*Figure 5. Typical DNL Plot*

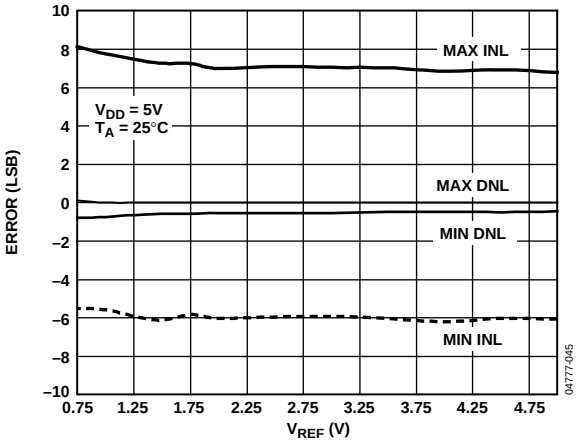



*Figure 8. INL and DNL Error vs. $V_{REF}$*

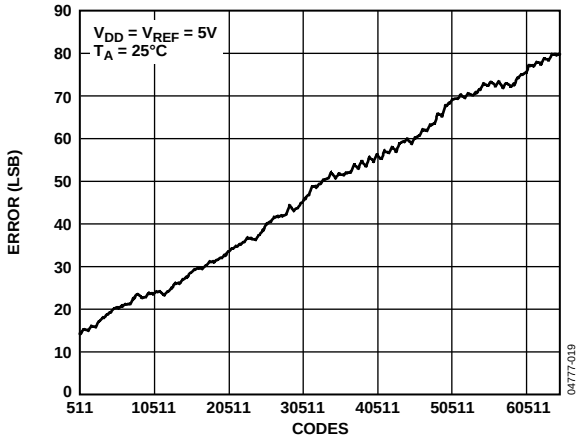



*Figure 6. Typical Total Unadjusted Error Plot*

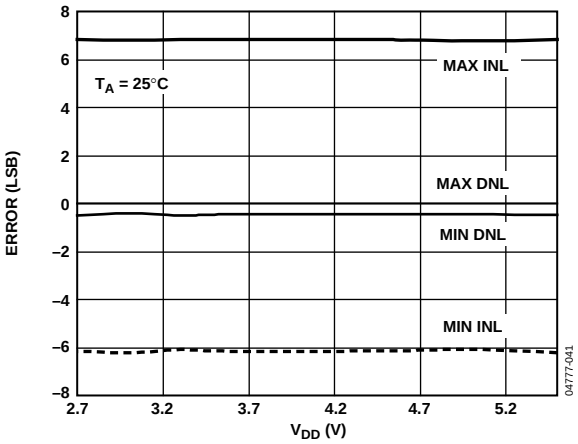



*Figure 9. INL and DNL Error vs. Supply*

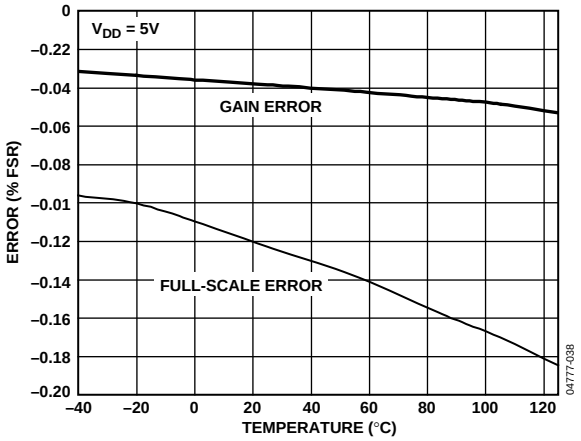



Figure 10. Gain Error and Full-Scale Error vs. Temperature

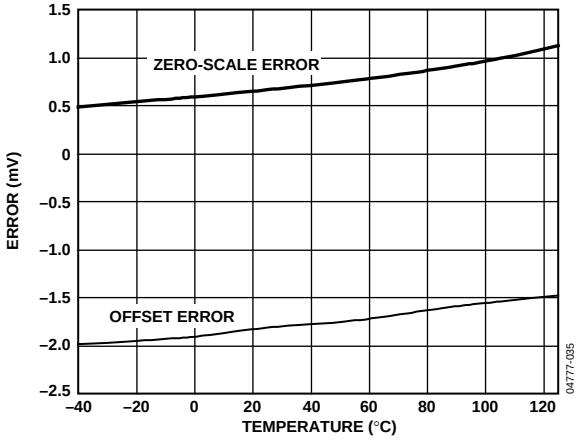



Figure 11. Zero-Scale and Offset Error vs. Temperature

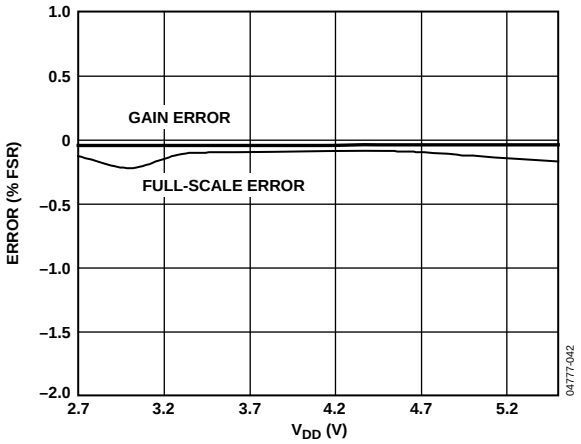



Figure 12. Gain Error and Full-Scale Error vs. Supply

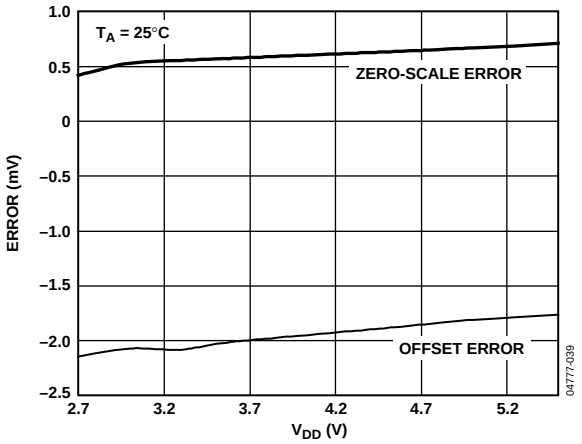



Figure 13. Zero-Scale and Offset Error vs. Supply

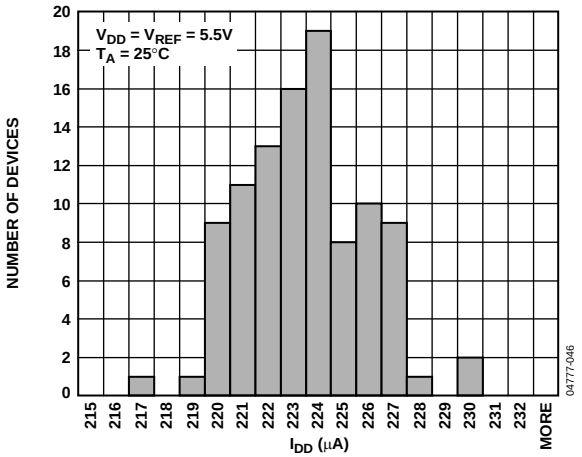



Figure 14. $I_{DD}$ Histogram with $V_{DD}$ = 5.5 V

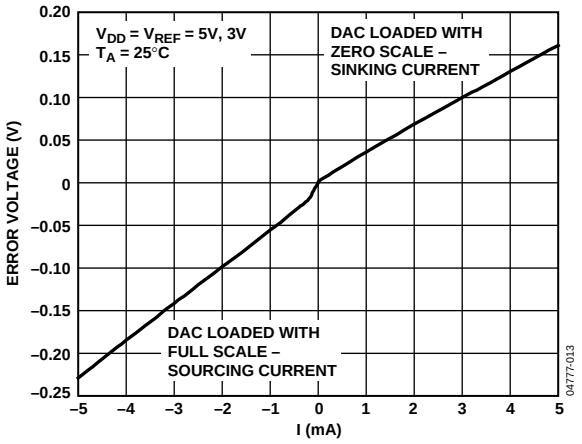



Figure 15. Headroom at Rails vs. Source and Sink Current

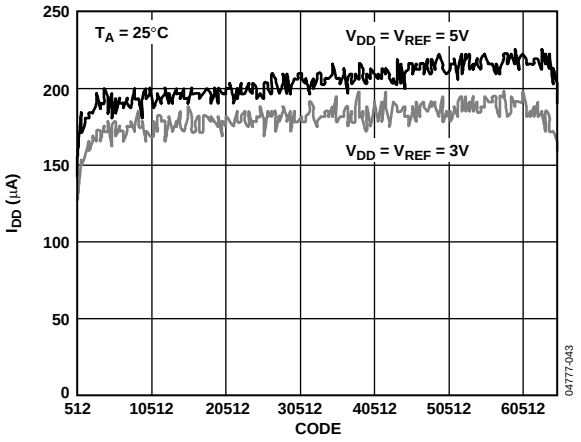



Figure 16. Supply Current vs. Code

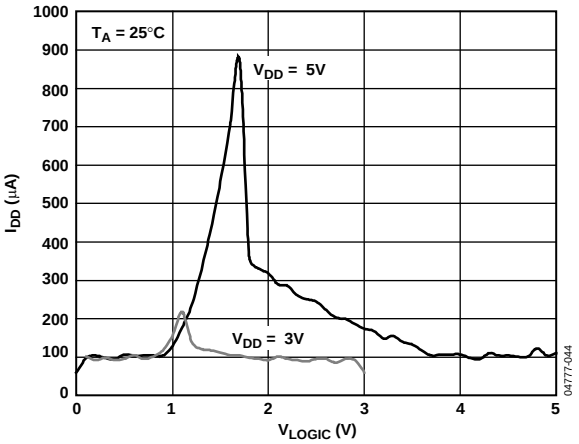



Figure 19. Supply Current vs. Logic Input Voltage

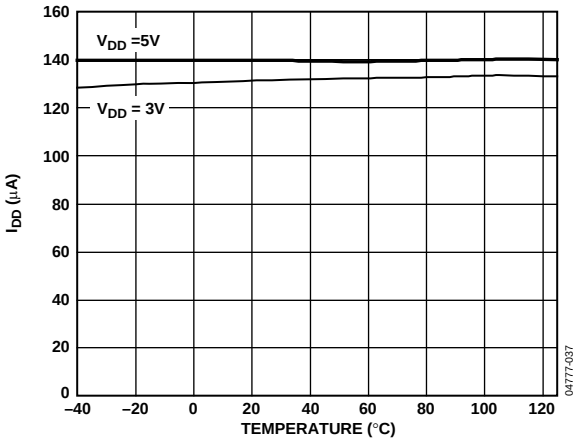



Figure 17. Supply Current vs. Temperature

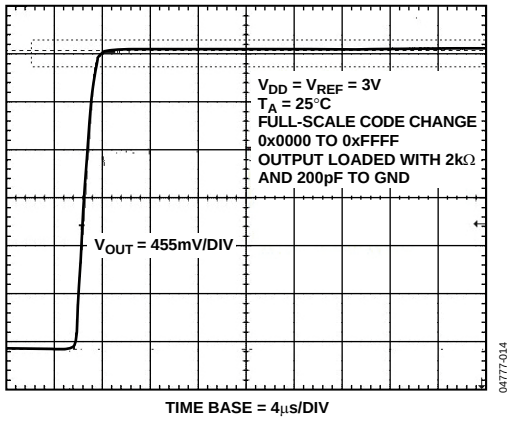



Figure 20. Full-Scale Settling Time, 3 V

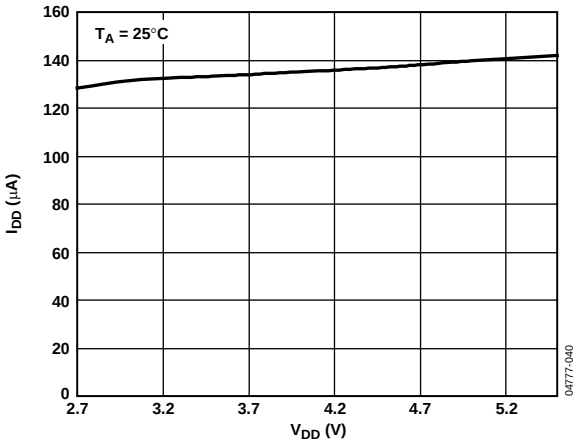



Figure 18. Supply Current vs. Supply Voltage

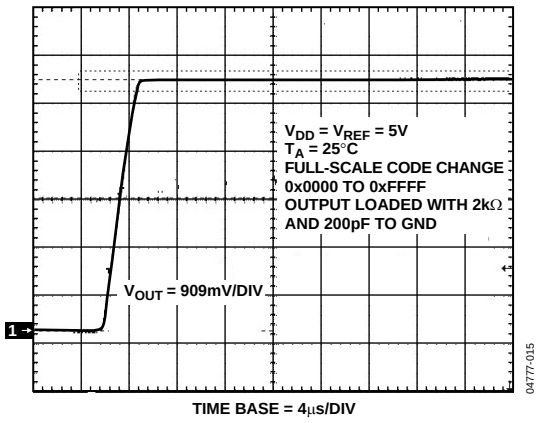



Figure 21. Full-Scale Settling Time, 5 V

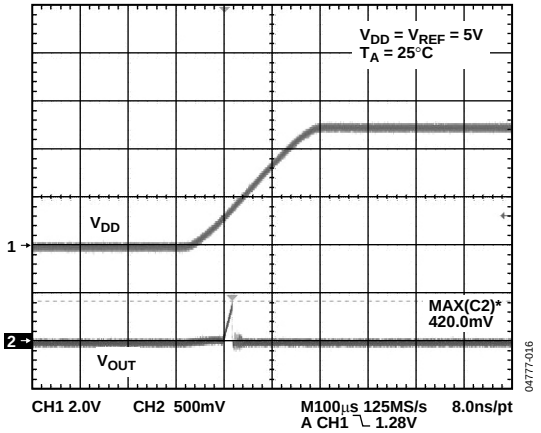



Figure 22. Power-On Reset to 0 V

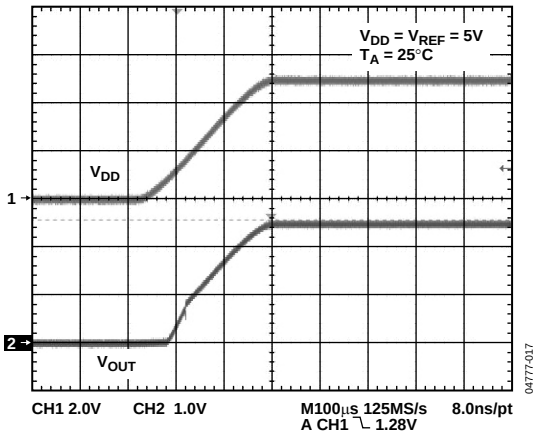



Figure 23. Power-On Reset to Midscale

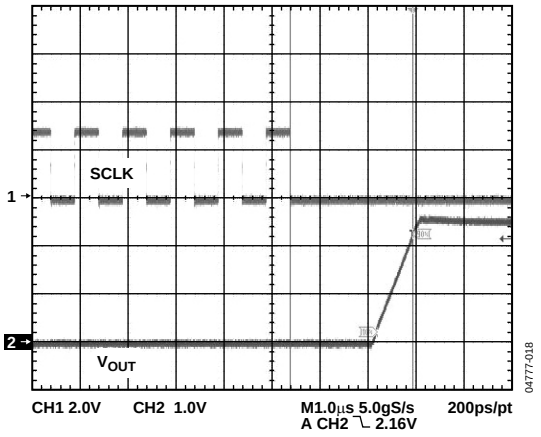



Figure 24. Exiting Power-Down to Midscale

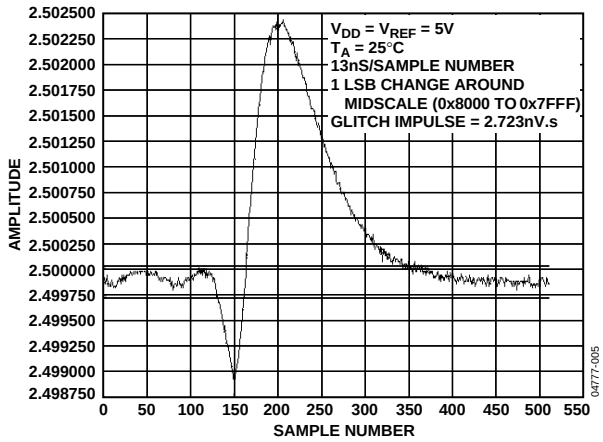



Figure 25. Digital-to-Analog Glitch Impulse (Negative)

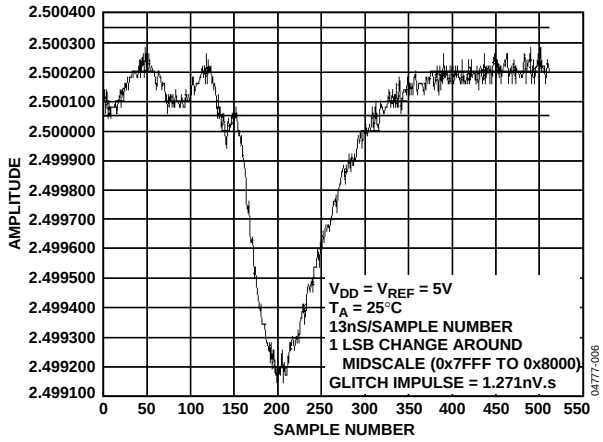



Figure 26. Digital-to-Analog Glitch Impulse (Positive)

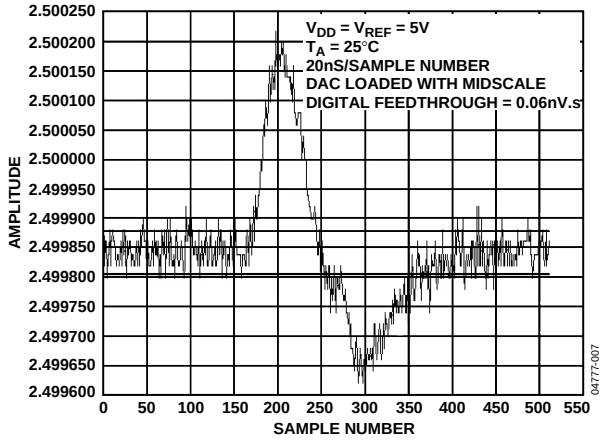



Figure 27. Digital Feedthrough

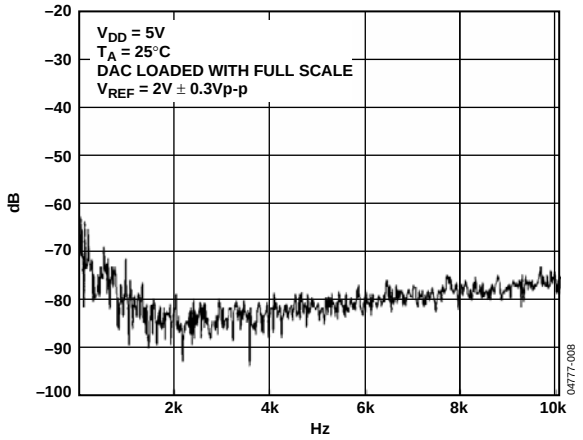



Figure 28. Total Harmonic Distortion

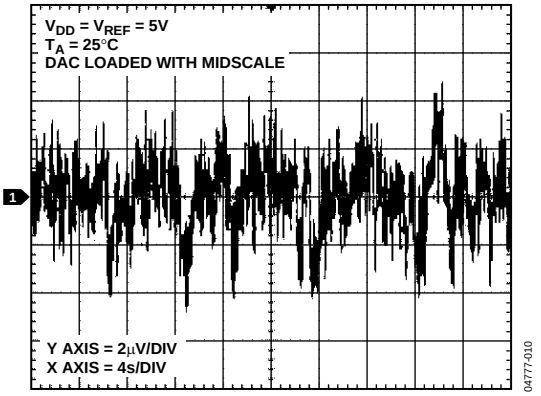



Figure 30. 0.1 Hz to 10 Hz Output Noise Plot

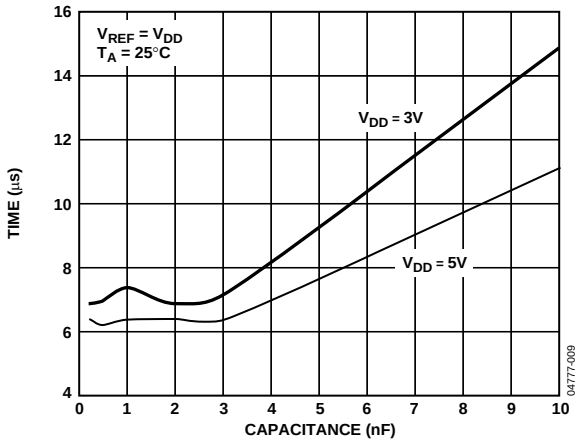



Figure 29. Settling Time vs. Capacitive Load

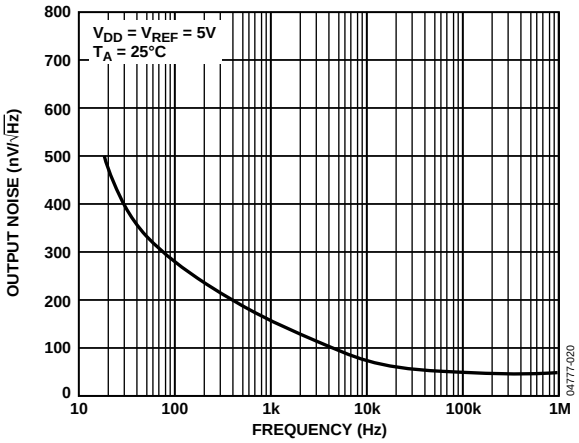



Figure 31. Noise Spectral Density

# TERMINOLOGY

**Relative Accuracy or Integral Nonlinearity (INL)**
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 4.

**Differential Nonlinearity (DNL)**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 5.

**Zero-Code Error**
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5662 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 11.

**Full-Scale Error**
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD}$ − 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 10.

**Gain Error**
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

**Total Unadjusted Error (TUE)**
Total unadjusted error is a measurement of the output error, taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 6.

**Zero-Code Error Drift**
This is a measurement of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

**Gain Temperature Coefficient**
This is a measurement of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

**Offset Error**
Offset error is a measure of the difference between $V_{OUT}$ (actual) and $V_{OUT}$ (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5662 with Code 512 loaded in the DAC register. It can be negative or positive.

**DC Power Supply Rejection Ratio (PSRR)**
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. It is measured in dB. $V_{REF}$ is held at 2 V, and $V_{DD}$ is varied by ±10%.

**Output Voltage Settling Time**
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the 24th falling edge of SCLK.

**Digital-to-Analog Glitch Impulse**
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 25 and Figure 26.

**Digital Feedthrough**
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

**Total Harmonic Distortion (THD)**
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

**Noise Spectral Density**
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density can be seen in Figure 31.

# THEORY OF OPERATION

## DAC SECTION

The AD5662 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 32 shows a block diagram of the DAC architecture.

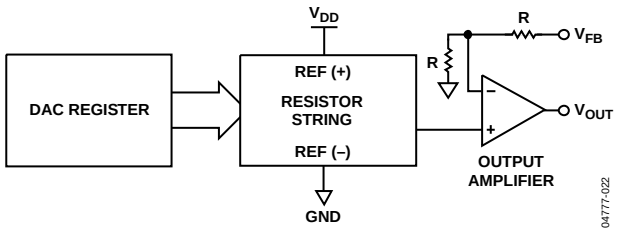



*Figure 32. DAC Architecture*

Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times \left( \frac{D}{65{,}536} \right)$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 65,535.

## RESISTOR STRING

The resistor string section is shown in Figure 33. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

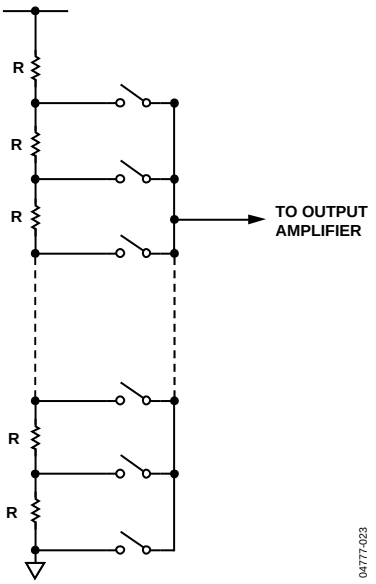



*Figure 33. Resistor String*

## OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to $V_{DD}$. This output buffer amplifier has a gain of 2 derived from a 50 kΩ resistor divider network in the feedback path. The output amplifier's inverting input is available to the user, allowing for remote sensing. This $V_{FB}$ pin must be connected to $V_{OUT}$ for normal operation. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 15. The slew rate is 1.5 V/μs with a ¼ to ¾ full-scale settling time of 10 μs.

## SERIAL INTERFACE

The AD5662 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as with most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5662 compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Since the $\overline{\text{SYNC}}$ buffer draws more current when $V_{IN}$ = 2.4 V than it does when $V_{IN}$ = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation. As mentioned previously it must, however, be brought high again just before the next write sequence.

## INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 34). The first six bits are don't cares. The next two are control bits that control the part's mode of operation (normal mode or any one of three power-down modes). See the Power-Down Modes section for a more complete description of the various modes. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

## $\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 35).

## POWER-ON RESET

The AD5662 family contains a power-on reset circuit that controls the output voltage during power-up. The AD5662x-1 DAC output powers up to 0 V, and the AD5662x-2 DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

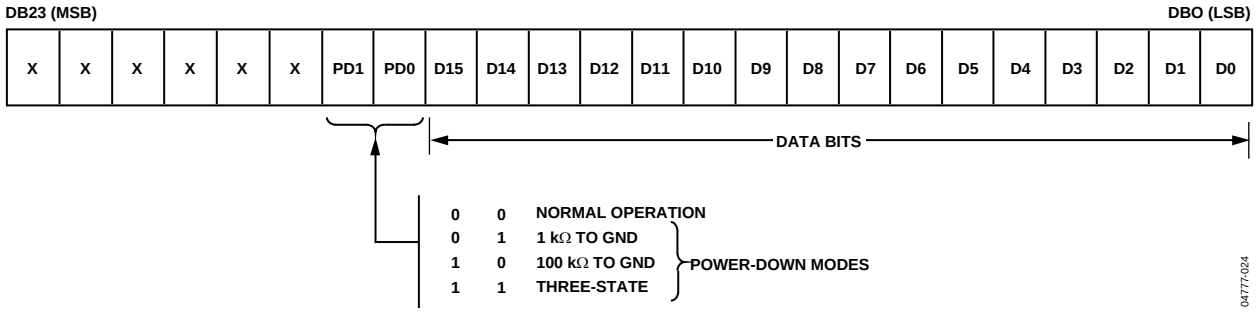



*Figure 34. Input Register Contents*

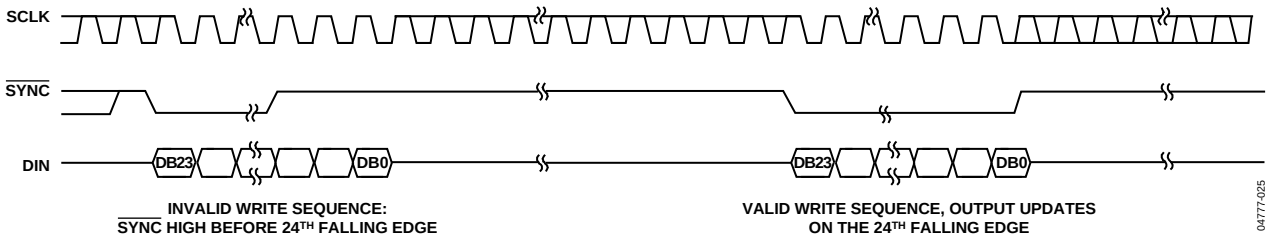



*Figure 35. $\overline{\text{SYNC}}$ Interrupt Facility*

## POWER-DOWN MODES

The AD5662 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Table 5 shows how the state of the bits corresponds to the device's mode of operation.

**Table 5. Modes of Operation for the AD5662**

| DB17 | DB16 | Operating Mode |
|---|---|---|
| 0 | 0 | Normal Operation |
| | | Power-Down Modes |
| 0 | 1 | 1 kΩ to GND |
| 1 | 0 | 100 kΩ to GND |
| 1 | 1 | Three-State |

When both bits are set to 0, the part works normally with its normal power consumption of 250 μA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V (100 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ resistor, or left open-circuited (three-state) (see Figure 36).

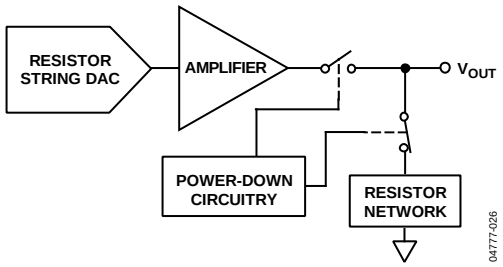


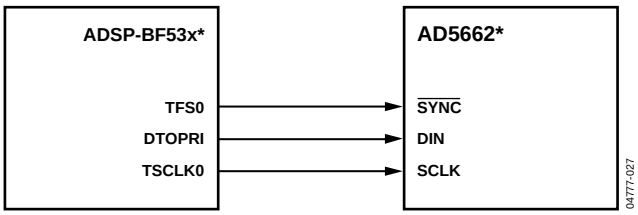

*Figure 36. Output Stage During Power-Down*

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 μs for $V_{DD}$ = 5 V and for $V_{DD}$ = 3 V (see Figure 24).

## MICROPROCESSOR INTERFACING

### *AD5662 to Blackfin® ADSP-BF53x Interface*

Figure 37 shows a serial interface between the AD5662 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5662, the setup for the interface is as follows. DT0PRI drives the DIN pin of the AD5662, while TSCLK0 drives the SCLK of the part. The $\overline{\text{SYNC}}$ is driven from TFS0.



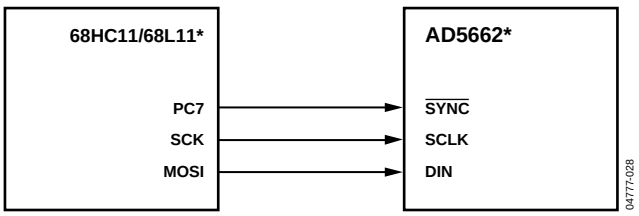

*ADDITIONAL PINS OMITTED FOR CLARITY

*Figure 37. AD5662 to Blackfin ADSP-BF53x Interface*

### *AD5662 to 68HC11/68L11 Interface*

Figure 38 shows a serial interface between the AD5662 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5662, while the MOSI output drives the serial data line of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows. The 68HC11/68L11 is configured with its CPOL bit as a 0 and its CPHA bit as a 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/ 68L11 is configured as described above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5662, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.




*ADDITIONAL PINS OMITTED FOR CLARITY

*Figure 38. AD5662 to 68HC11/68L11 Interface*

### AD5662 to 80C51/80L51 Interface

Figure 39 shows a serial interface between the AD5662 and the 80C51/80L51 microcontroller. The setup for the interface is as follows. TxD of the 80C51/80L51 drives SCLK of the AD5662, while RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5662, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes only; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5662 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

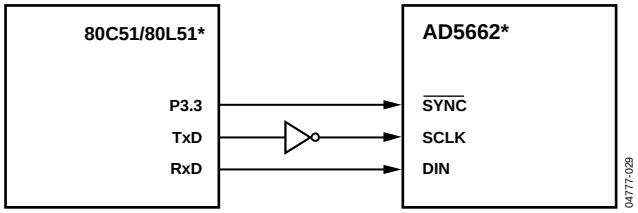



*Figure 39. AD5662 to 80C51/80L51 Interface*

### AD5662 to MICROWIRE Interface

Figure 40 shows an interface between the AD5662 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5662 on the rising edge of the SK.

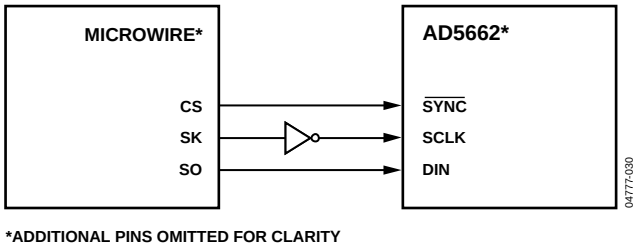



*Figure 40. AD5662 to MICROWIRE Interface*

# APPLICATIONS

## CHOOSING A REFERENCE FOR THE AD5662

To achieve the optimum performance from the AD5662, thought should be given to the choice of a precision voltage reference. The AD5662 has only one reference input, $V_{REF}$. The voltage on the reference input is used to supply the positive input to the DAC. Therefore any error in the reference is reflected in the DAC.

When choosing a voltage reference for high accuracy applications, the sources of error are initial accuracy, ppm drift, long-term drift, and output voltage noise. Initial accuracy on the output voltage of the DAC leads to a full-scale error in the DAC. To minimize these errors, a reference with high initial accuracy is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR423, allows a system designer to trim system errors out by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measurement of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable during its entire lifetime.

The temperature coefficient of a reference's output voltage effect INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce temperature dependence of the DAC output voltage in ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. It is important to choose a reference with as low an output noise voltage as practical for the system noise resolution required. Precision voltage references such as the ADR425 produce low output noise in the 0.1 Hz to10 Hz range. Examples of recommended precision references for use as supply to the AD5662 are shown in the Table 6.

## USING A REFERENCE AS A POWER SUPPLY FOR THE AD5662

Because the supply current required by the AD5662 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 41). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5662; see Table 6 for a suitable reference. If the low dropout REF195 is used, it must supply 250 μA of current to the AD5662, with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

$$250\ \mu A + (5\ V/5\ k\Omega) = 1.25\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 2.5 ppm (12.5 μV) error for the 1.25 mA current drawn from it. This corresponds to a 0.164 LSB error.

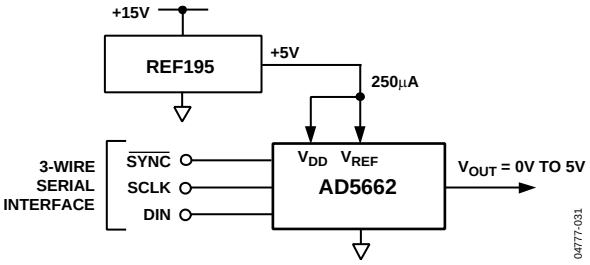



*Figure 41. REF195 as Power Supply to the AD5662*

**Table 6. Partial List of Precision References for Use with the AD5662**

| Part No. | Initial Accuracy (mV max) | Temp Drift (ppm°C max) | 0.1 Hz to 10 Hz Noise (μV p-p typ) | $V_{OUT}$ (V) |
|---|---|---|---|---|
| ADR425 | ±2 | 3 | 3.4 | 5 |
| ADR395 | ±6 | 25 | 5 | 5 |
| REF195 | ±2 | 5 | 50 | 5 |
| AD780 | ±2 | 3 | 4 | 2.5/3 |
| ADR423 | ±2 | 3 | 3.4 | 3 |

## BIPOLAR OPERATION USING THE AD5662

The AD5662 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 42. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[ V_{DD} \times \left( \frac{D}{65{,}536} \right) \times \left( \frac{R1 + R2}{R1} \right) - V_{DD} \times \left( \frac{R2}{R1} \right) \right]$$

where $D$ represents the input code in decimal (0 to 65,535). With $V_{DD}$ = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left( \frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

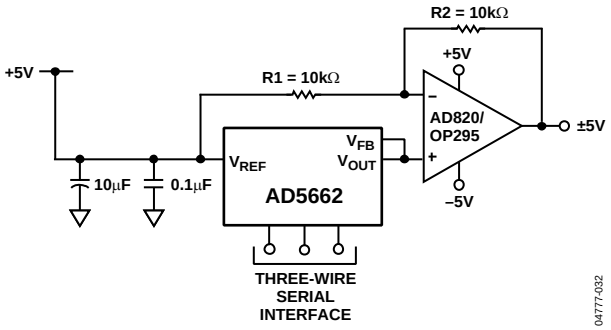



*Figure 42. Bipolar Operation with the AD5662*

## USING THE AD5662 AS AN ISOLATED, PROGRAMMABLE, 4-20 mA PROCESS CONTROLLER

In many process control system applications, 2-wire current transmitters are used to transmit analog signals through noisy environments. These current transmitters use a zero-scale signal current of 4 mA that can power the transmitter's signal conditioning circuitry. The full-scale output signal in these transmitters is 20 mA. The converse approach to process control can also be used; a low-power, programmable current source can be used to control remotely located sensors or devices in the loop.

A circuit that performs this function is shown in Figure 43. Using the AD5662 as the controller, the circuit provides a programmable output current of 4 mA to 20 mA, proportional to the DAC's digital code. Biasing for the controller is provided by the ADR02 and requires no external trim for two reasons: (1) the ADR02's tight initial output voltage tolerance and (2) the low supply current consumption of both the AD8627 and the AD5662. The entire circuit, including opto-couplers, consumes less than 3 mA from the total budget of 4 mA. The AD8627 regulates the output current to satisfy the current summation at the noninverting node of the AD8627.

$$I_{OUT} = 1/R7 \, (V_{DAC} \times R3/R1 + V_{REF} \times R3/R2)$$

For the values shown in Figure 43,

$$I_{OUT} = 0.2435 \text{ µA} \times D + 4 \text{ mA}$$

where $D = 0 \le D \le 65535$, giving a full-scale output current of 20 mA when the AD5662's digital code equals 0xFFFF. Offset trim at 4 mA is provided by P2, and P1 provides the circuit's gain trim at 20 mA. These two trims do not interact because the noninverting input of the AD8627 is at virtual ground. The Schottky diode, D1, is required in this circuit to prevent loop supply power-on transients from pulling the noninverting input of the AD8627 more than 300 mV below its inverting input. Without this diode, such transients could cause phase reversal of the AD8627 and possible latch-up of the controller. The loop supply voltage compliance of the circuit is limited by the maximum applied input voltage to the ADR02 and is from 12 V to 40 V.

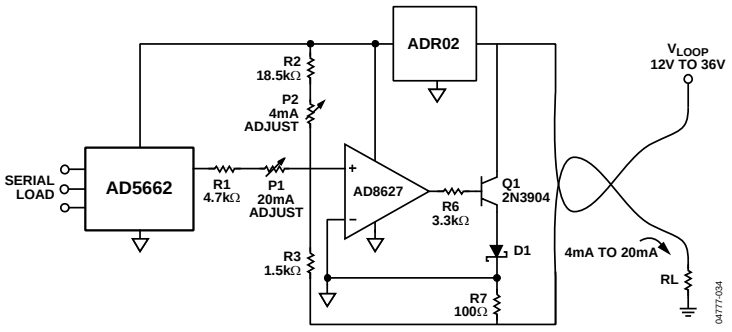



*Figure 43. Programmable 4–20 mA Process Controller*

## USING AD5662 WITH A GALVANICALLY ISOLATED INTERFACE

In process-control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur in the area where the DAC is functioning. Isocouplers provide isolation in excess of 3 kV. The AD5662 uses a 3-wire serial logic interface, so the ADuM130x 3-channel digital isolator provides the required isolation (see Figure 44). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5662.

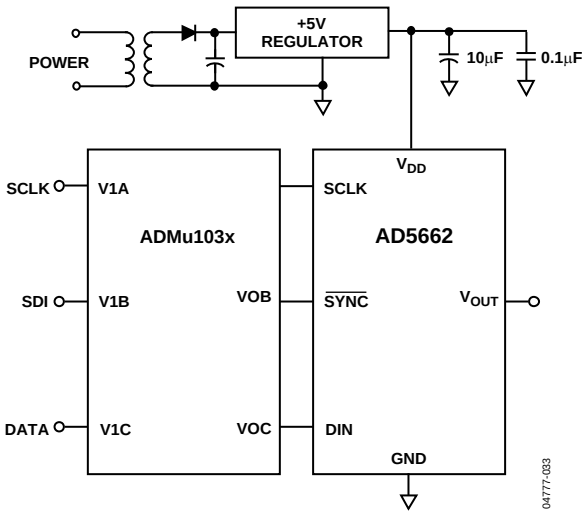



*Figure 44. AD5662 with a Galvanically Isolated Interface*

## POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5662 should have separate analog and digital sections, each having its own area of the board. If the AD5662 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5662.

The power supply to the AD5662 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

# OUTLINE DIMENSIONS

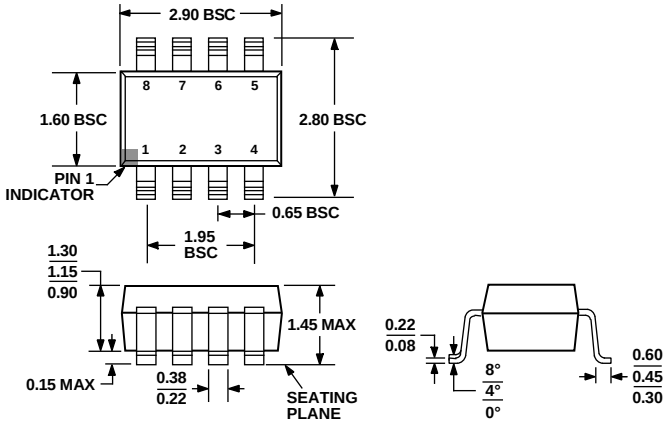



*Figure 45. 8-Lead SOT-23*
*(RJ-8)*
*Dimensions shown in millimeters*

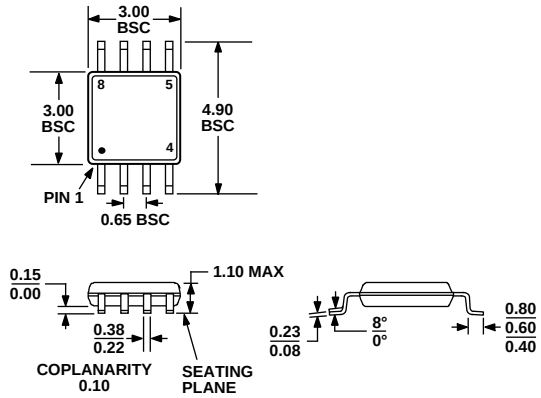



*Figure 46. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Temperature Range | Package Description | Package Option | Branding | Power-On Reset to Code | Acurracy |
|---|---|---|---|---|---|---|
| AD5662ARJ-1500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D38 | Zero | ±32 LSB INL |
| AD5662ARJZ-1500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9P | Zero | ±32 LSB INL |
| AD5662ARJ-1REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D38 | Zero | ±32 LSB INL |
| AD5662ARJZ-1REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9P | Zero | ±32 LSB INL |
| AD5662ARJ-2500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D39 | Midscale | ±32 LSB INL |
| AD5662ARJ-2REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D39 | Midscale | ±32 LSB INL |
| AD5662ARJZ-2REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9Q | Midscale | ±32 LSB INL |
| AD5662ARM-1 | −40°C to +125°C | 8-lead MSOP | RM-8 | D38 | Zero | ±32 LSB INL |
| AD5662ARMZ-1 | −40°C to +125°C | 8-lead MSOP | RM-8 | D9P | Zero | ±32 LSB INL |
| AD5662ARM-1REEL7 | −40°C to +125°C | 8-lead MSOP | RM-8 | D38 | Zero | ±32 LSB INL |
| AD5662ARMZ-1REEL7 | −40°C to +125°C | 8-lead MSOP | RM-8 | D9P | Zero | ±32 LSB INL |
| AD5662BRJ-1500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D36 | Zero | ±16 LSB INL |
| AD5662BRJZ-1500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9T | Zero | ±16 LSB INL |
| AD5662BRJ-1REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D36 | Zero | ±16 LSB INL |
| AD5662BRJZ-1REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9T | Zero | ±16 LSB INL |
| AD5662BRJ-2500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D37 | Midscale | ±16 LSB INL |
| AD5662BRJZ-2500RL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9R | Midscale | ±16 LSB INL |
| AD5662BRJ-2REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D37 | Midscale | ±16 LSB INL |
| AD5662BRJZ-2REEL7 | −40°C to +125°C | 8-lead SOT-23 | RJ-8 | D9R | Midscale | ±16 LSB INL |
| AD5662BRM-1 | −40°C to +125°C | 8-lead MSOP | RM-8 | D36 | Zero | ±16 LSB INL |
| AD5662BRMZ-1 | −40°C to +125°C | 8-lead MSOP | RM-8 | D9T | Zero | ±16 LSB INL |
| AD5662BRM-1REEL7 | −40°C to +125°C | 8-lead MSOP | RM-8 | D36 | Zero | ±16 LSB INL |
| AD5662BRMZ-1REEL7 | −40°C to +125°C | 8-lead MSOP | RM-8 | D9T | Zero | ±16 LSB INL |
| AD5662WARMZ-1REEL7 | −40°C to +125°C | 8-lead MSOP | RM-8 | D9P | Zero | ±32 LSB INL |
| EVAL-AD5662EBZ | | Evaluation Board | | | | |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The AD5662WARMZ-1REEL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability report for this model.

## NOTES

## NOTES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