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1 Block diagram and pin configuration

Figure 1. Block diagram

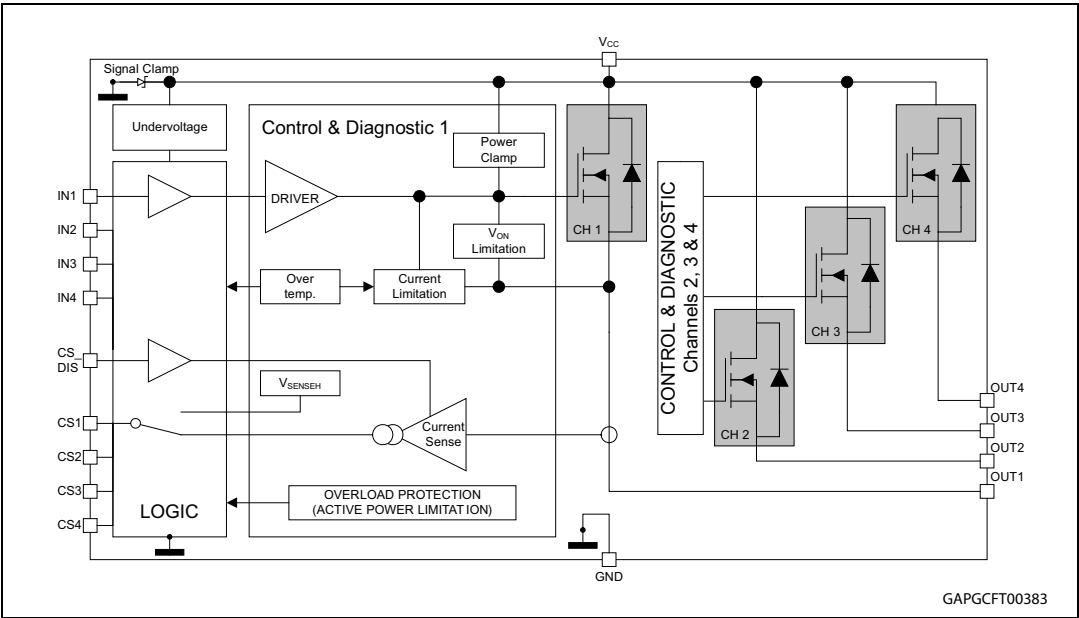


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection
OUTPUT _n	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT _n	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE _n	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

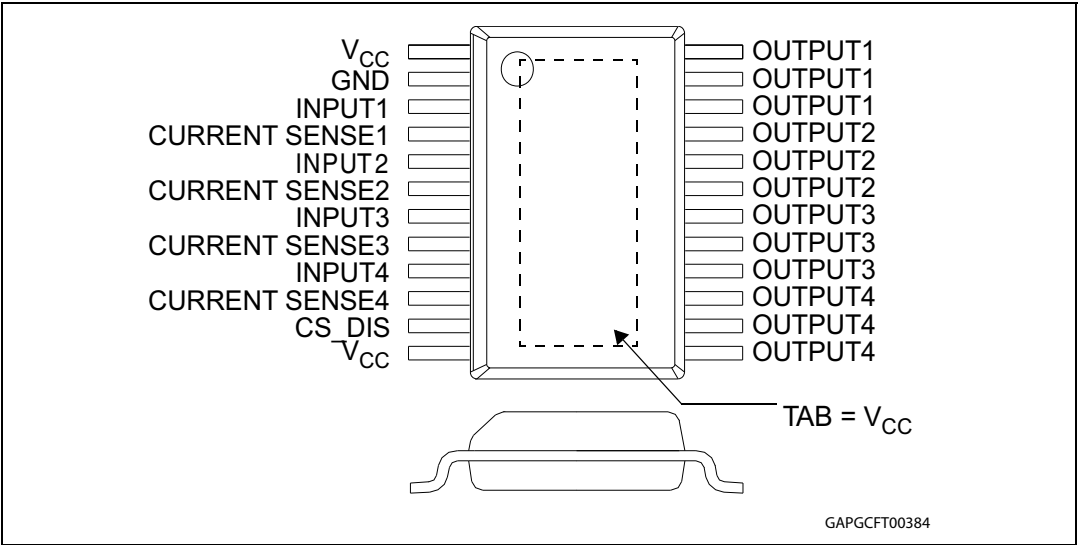
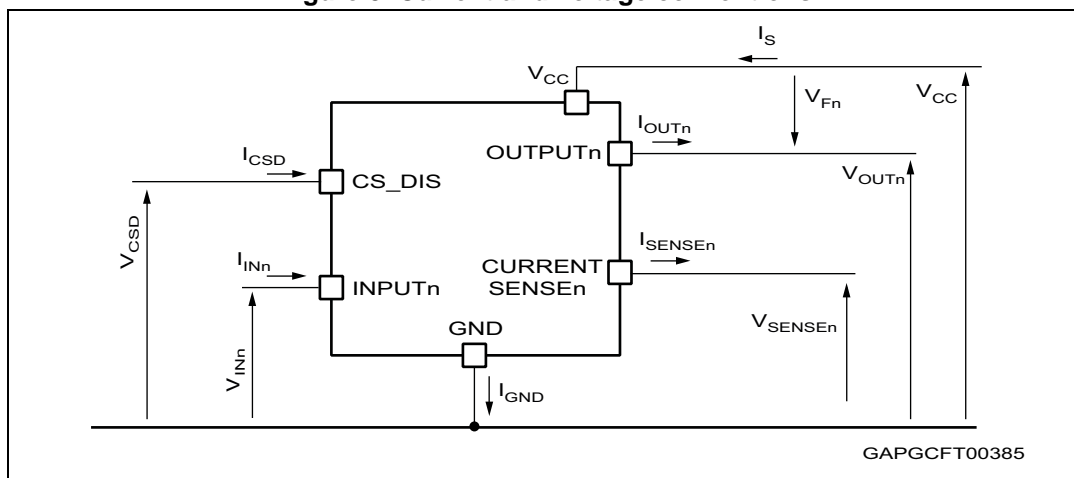


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 k Ω resistor	X	Not allowed	Through 10 k Ω resistor	Through 10 k Ω resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 12 \text{ mH}$; $R_L = 0 \Omega$; $V_{bat} = 13.5 \text{ V}$; $T_{jstart} = 150 \text{ }^\circ\text{C}$; $I_{OUT} = I_{limL}(Typ.)$)	34	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5\text{ K}\Omega$; $C = 100\text{ pF}$)		
	– INPUT	4000	V
	– CURRENT SENSE	2000	V
	– CS_DIS	4000	V
	– OUTPUT	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	8	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 33 in the thermal section	°C/W

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 28\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance ⁽²⁾	$I_{OUT} = 1\text{ A}$; $T_j = 25\text{ °C}$			160	mΩ
		$I_{OUT} = 1\text{ A}$; $T_j = 150\text{ °C}$			320	mΩ
		$I_{OUT} = 1\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ °C}$			210	mΩ
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 ⁽¹⁾	5 ⁽¹⁾	μA
		On-state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		8	14	mA
$I_{L(off1)}$	Off-state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		5	μA
V_F	Output - V_{CC} diode voltage ⁽²⁾	$-I_{OUT} = 1\text{ A}$; $T_j = 150\text{ °C}$			0.7	V

1. PowerMOS leakage included.

2. For each channel.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 13\text{ Ω}$ (see Figure 5)	—	20	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 13\text{ Ω}$ (see Figure 5)	—	10	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 13\text{ Ω}$	—	See Figure 23	—	V/μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 13\text{ Ω}$	—	See Figure 25	—	V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 13\text{ Ω}$ (see Figure 5)	—	0.05	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 13\text{ Ω}$ (see Figure 5)	—	0.03	—	mJ

Table 7. Logic Inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1\text{ mA}$	5.5		7	V
		$I_{CSD} = -1\text{ mA}$		-0.7		V

Table 8. Protections and diagnostics ⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC} = 13\text{ V}$	7	10	14	A
		$5\text{ V} < V_{CC} < 28\text{ V}$			14	A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V}; T_R < T_j < T_{TSD}$		2.5		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 1\text{ A}; V_{IN} = 0; L = 20\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.03\text{ A}; T_j = -40\text{ }^{\circ}\text{C} \dots 150\text{ }^{\circ}\text{C}$ (see Figure 6)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	330	600	870	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.35 A; V _{SENSE} = 0.5 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	337 395	475 475	642 555	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.35 A; V _{SENSE} = 0.5 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	- 12		12	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 0.5 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	375 407	470 470	583 544	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.5 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	- 8		8	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 1.5 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C T _j = 25 °C to 150 °C	425 435	465 465	505 495	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 1.5 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	- 6		6	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{CSD} = 5 V; V _{IN} = 0 V; T _j = -40 °C to 150 °C	0		1	μA
		V _{CSD} = 0 V; V _{IN} = 5 V; T _j = -40 °C to 150 °C	0		2	μA
		I _{OUT} = 1 A; V _{SENSE} = 0 V; V _{CSD} = 5 V; V _{IN} = 5 V; T _j = -40 °C to 150 °C	0		1	μA
I _{OL}	Openload ON-state current detection threshold	V _{IN} = 5 V; I _{SENSE} = 5 μA	1		5	mA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 1.5 A; V _{CSD} = 0 V	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} = 13 V; R _{SENSE} = 3.9 KΩ;		8		V
I _{SENSEH} ⁽²⁾	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 13 V; V _{SENSE} = 5 V;		9		mA
t _{DSSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} < 4 V; 0.025 A < I _{OUT} < 1.5 A; I _{SENSE} = 90 % of I _{SENSE} max (see Figure 4)		40	100	μs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} < 4 V; 0.025 A < I _{OUT} < 1.5 A; I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V; 0.025 A < I _{OUT} < 1.5 A; I _{SENSE} = 90 % of I _{SENSE max} (see Figure 4)		120	300	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V; I _{SENSE} = 90% of I _{SENSEMAX} ; I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 1.5 A (see Figure 7)			110	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4 V; 0.025 A < I _{OUT} < 1.5 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		80	250	μs

1. Parameter guaranteed by design; it is not tested
2. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

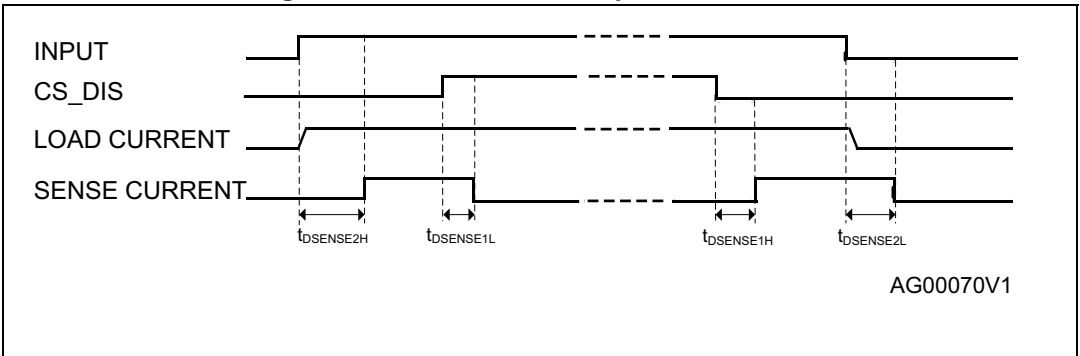


Figure 5. Switching characteristics

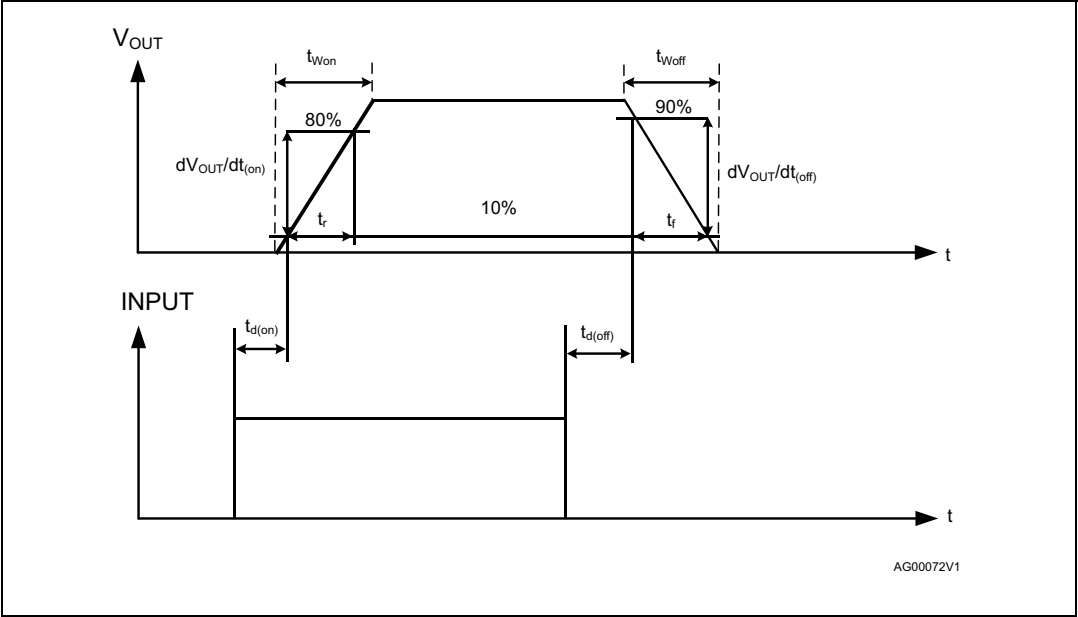


Figure 6. Output voltage drop limitation

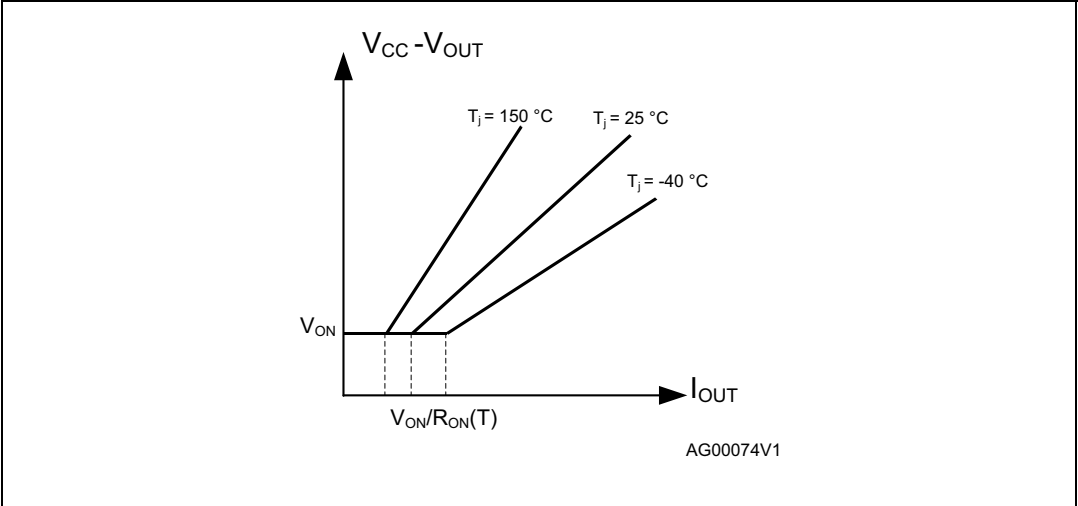


Figure 7. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

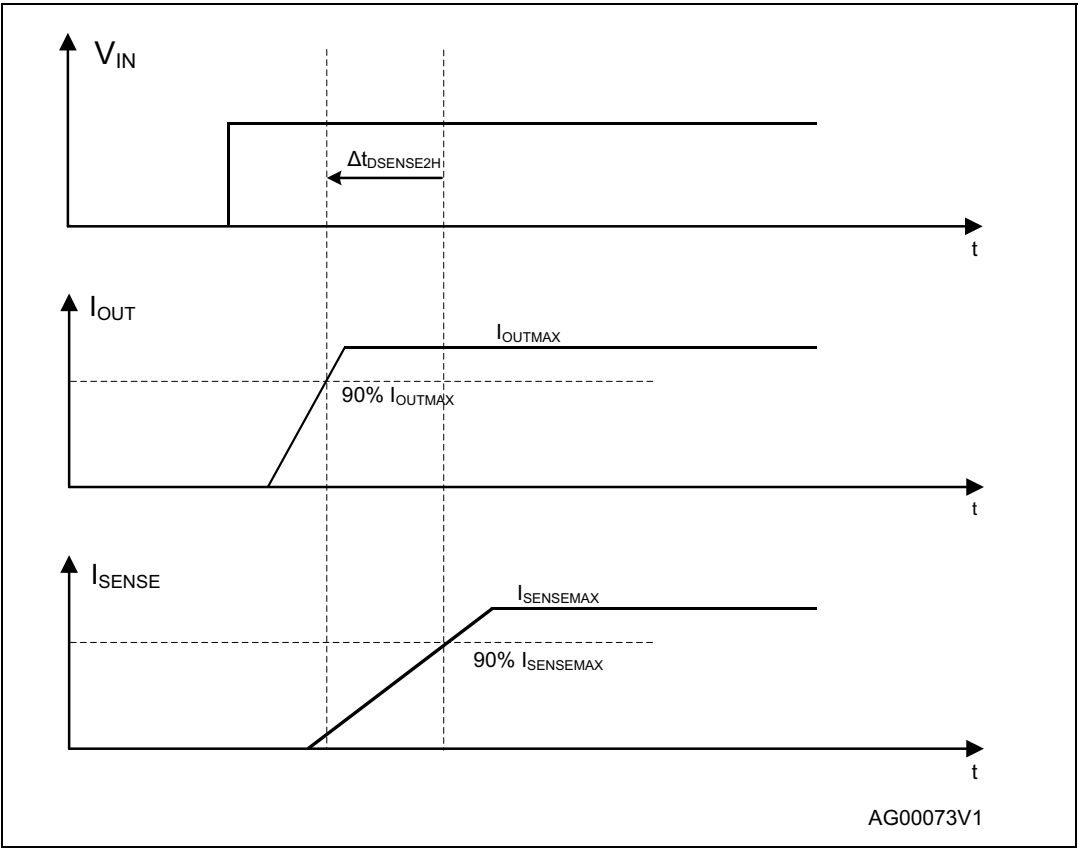


Figure 8. I_{OUT}/I_{SENSE} vs I_{OUT}

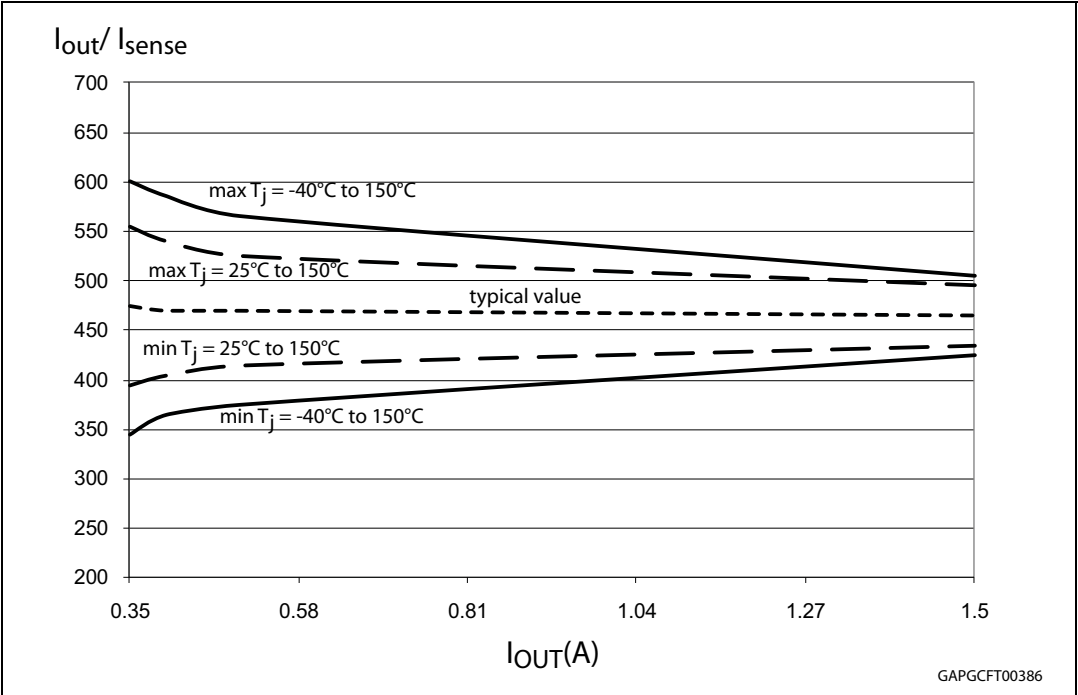
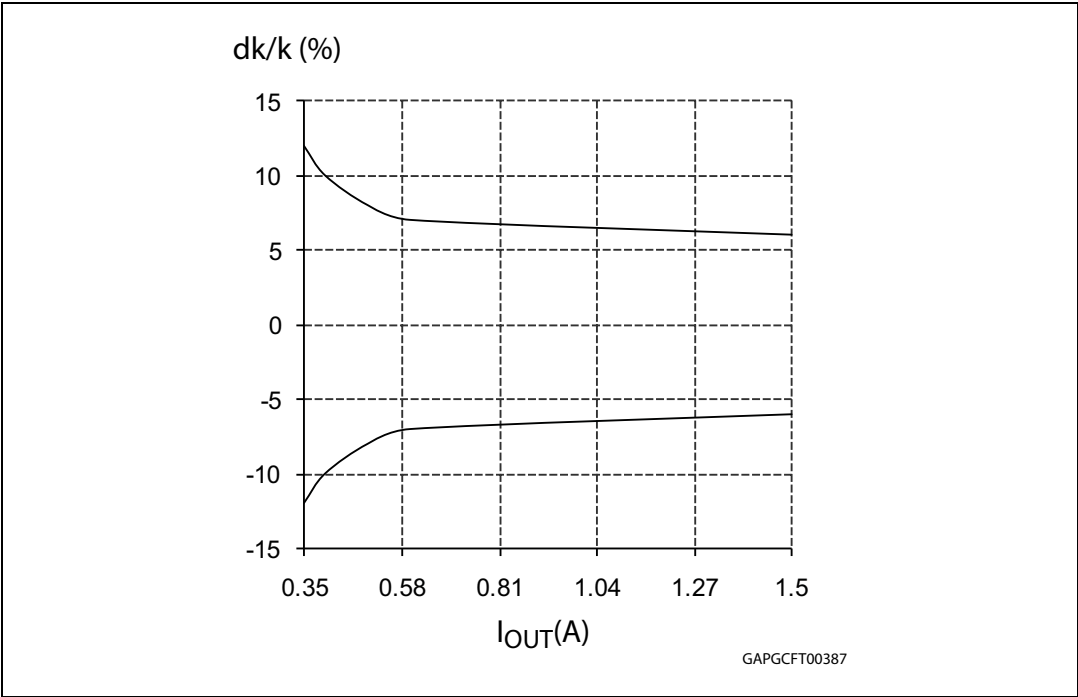


Figure 9. Maximum current sense ratio drift vs load current⁽¹⁾



1. Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense ($V_{CSD} = 0\text{ V}$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X	Nominal
	H	(no power limitation) Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	L	L	0
	H	L	V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽¹⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

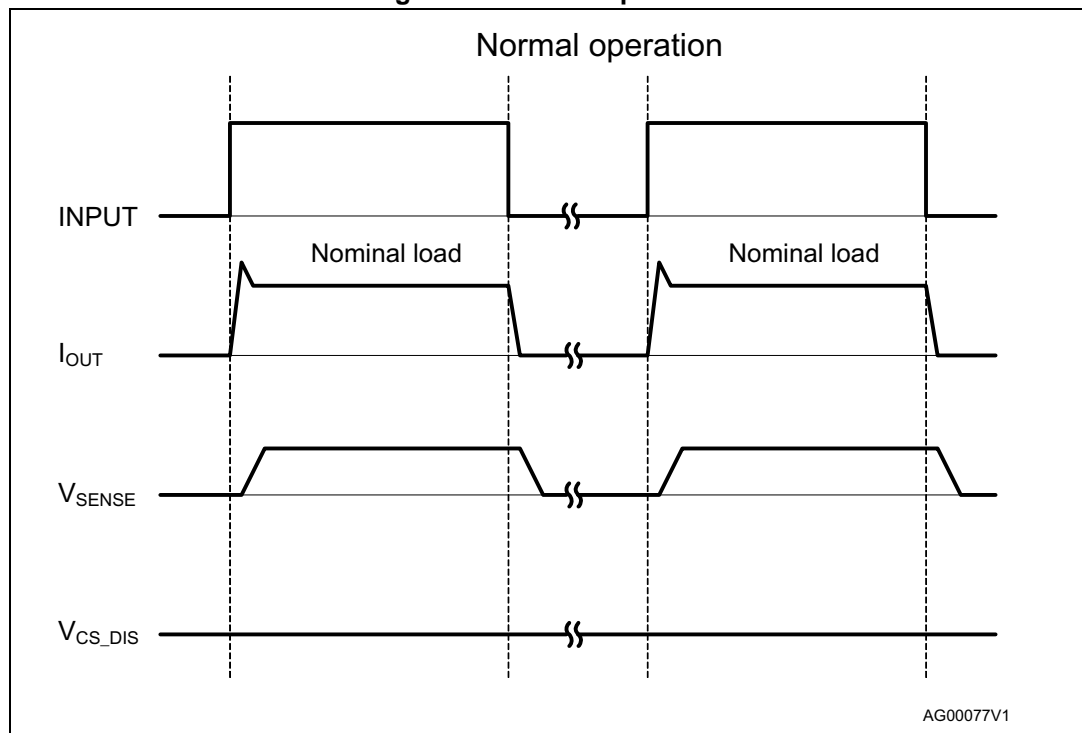
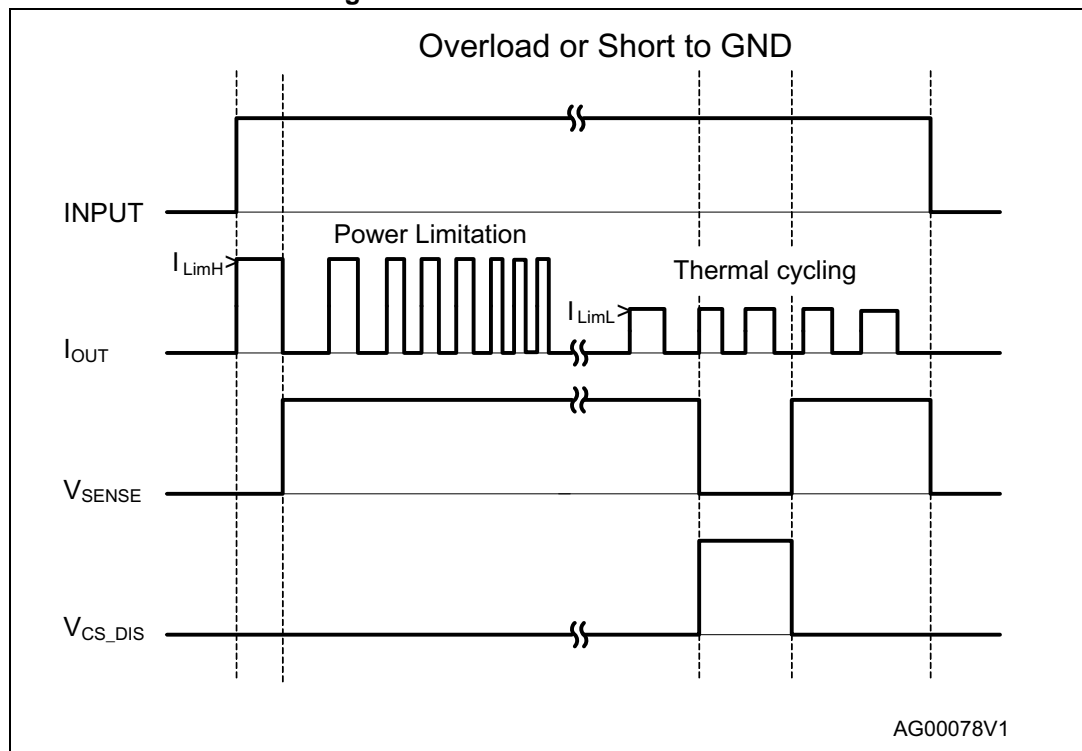
Figure 10. Normal operation**Figure 11. Overload or short to GND**

Figure 12. Intermittent overload

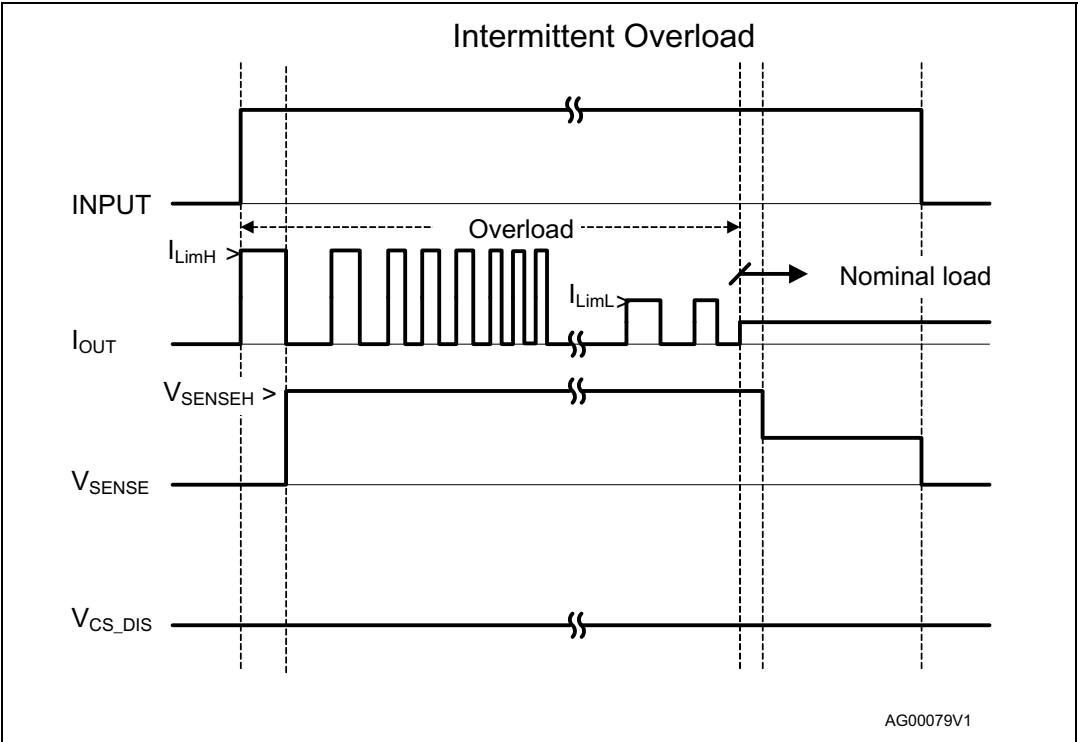
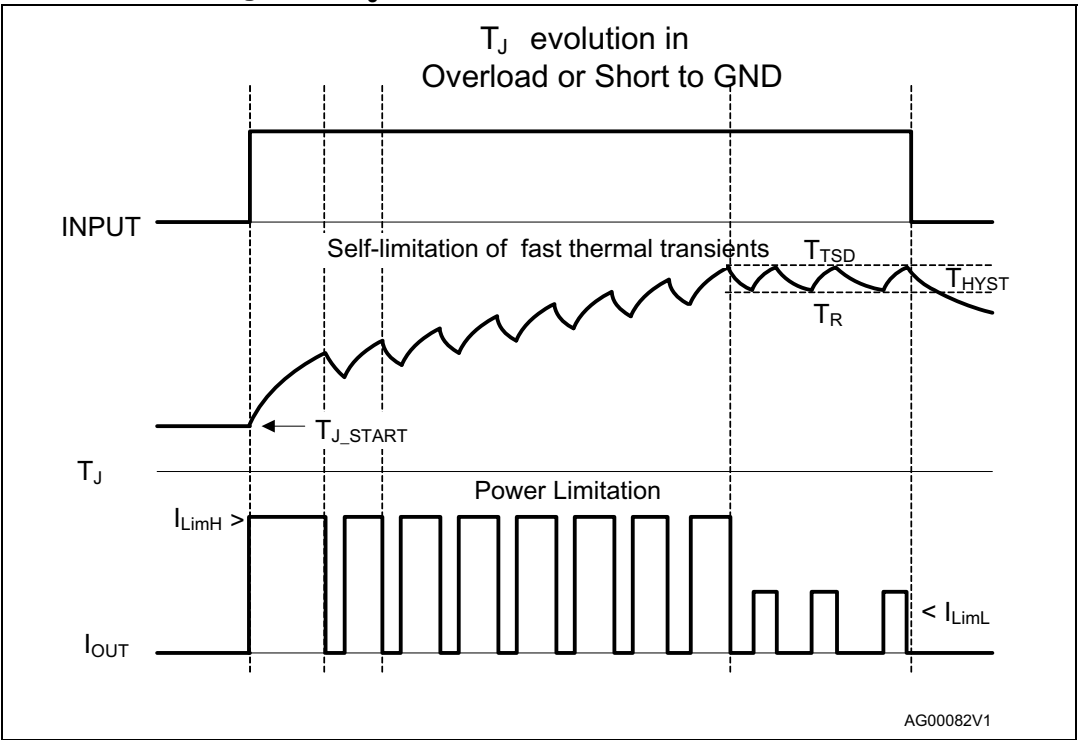


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

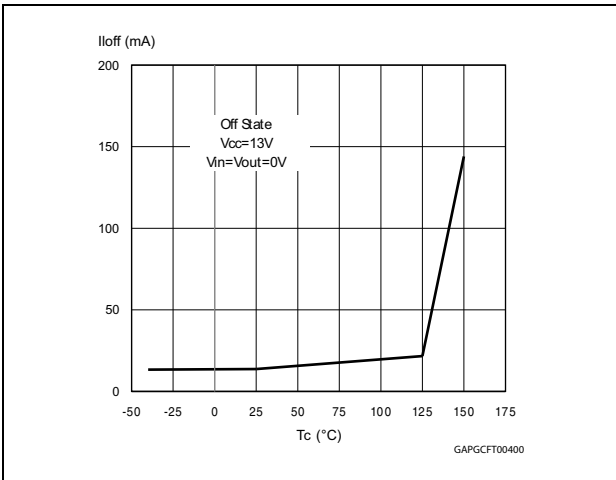


Figure 15. High level input current

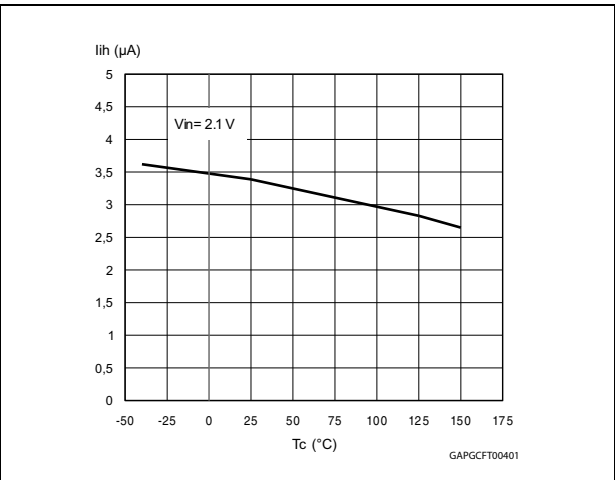


Figure 16. Input clamp voltage

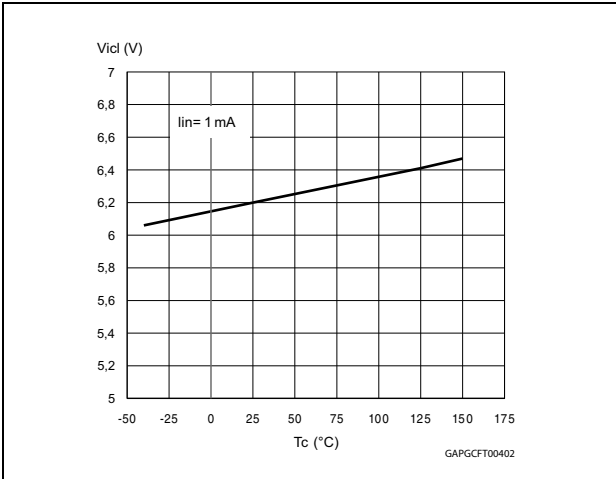


Figure 17. Input low level voltage

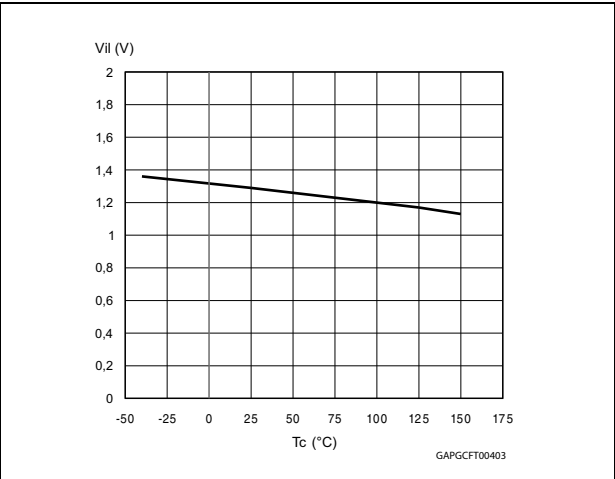


Figure 18. Input high level voltage

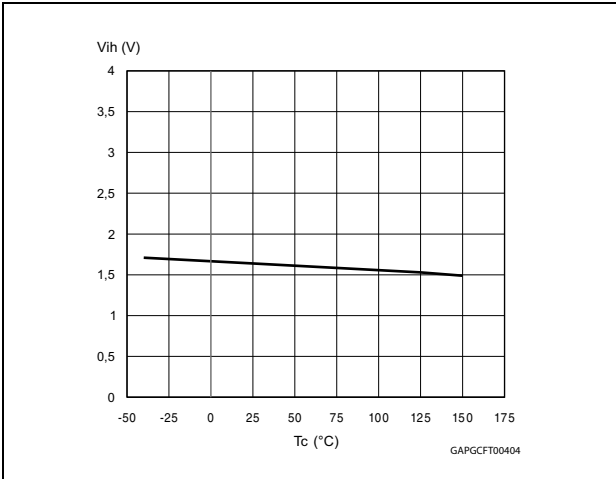


Figure 19. Input hysteresis voltage

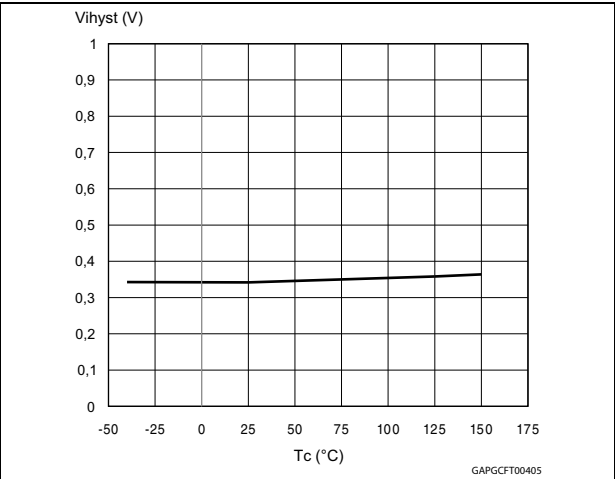


Figure 20. On-state resistance vs T_{case}

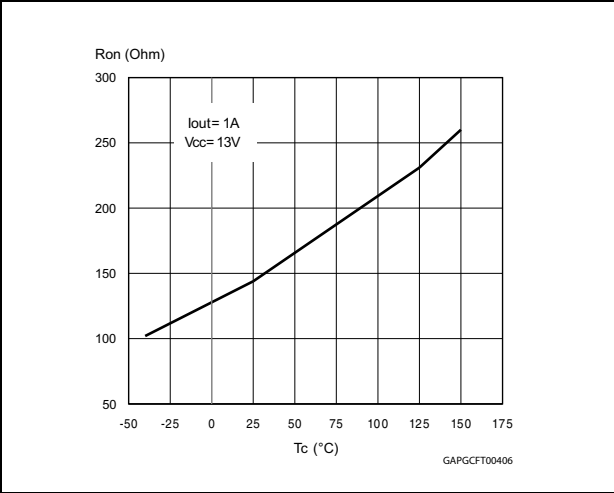


Figure 21. On-state resistance vs V_{cc}

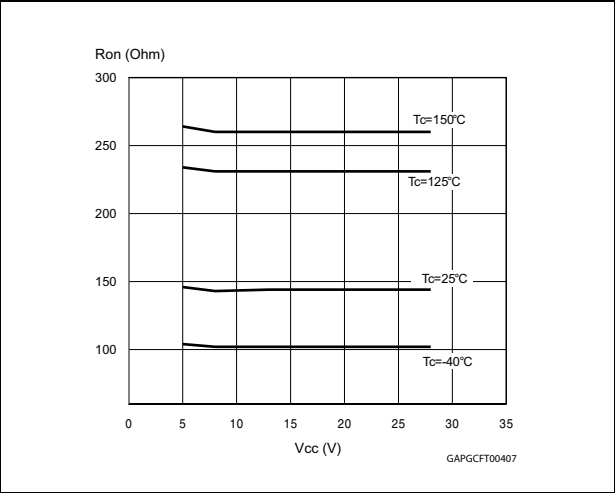


Figure 22. Undervoltage shutdown

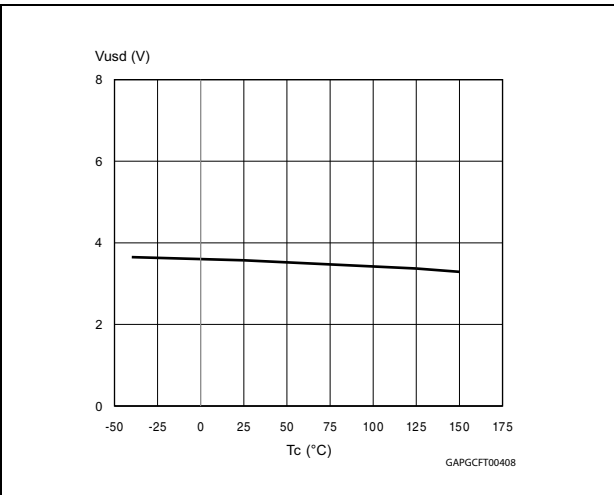


Figure 23. Turn-on voltage slope

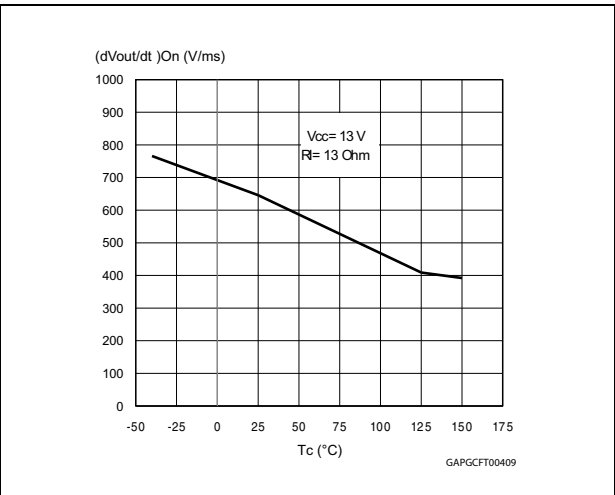


Figure 24. I_{limH} vs T_{case}

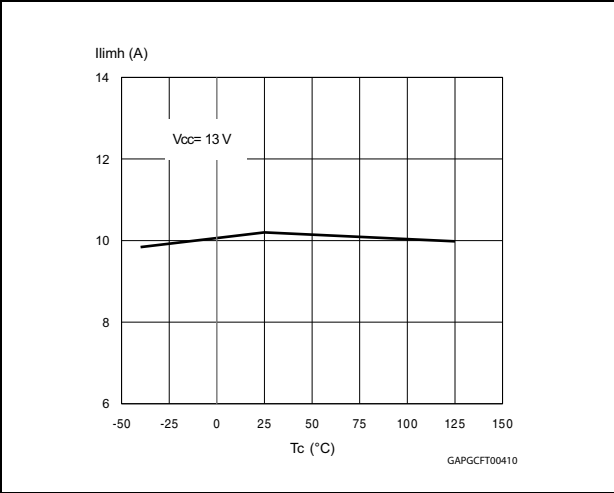


Figure 25. Turn-off voltage slope

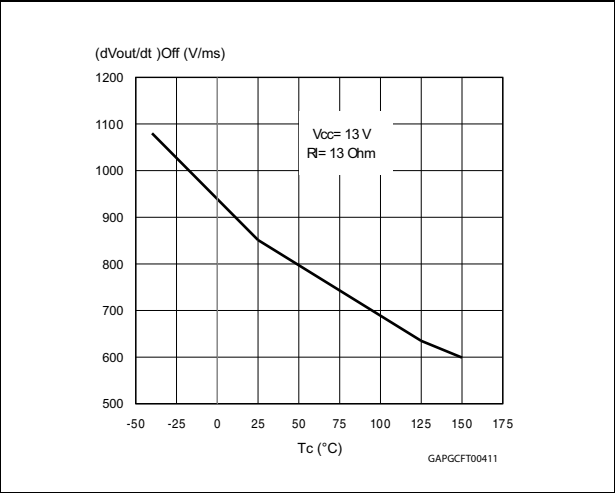


Figure 26. CS_DIS high level voltage

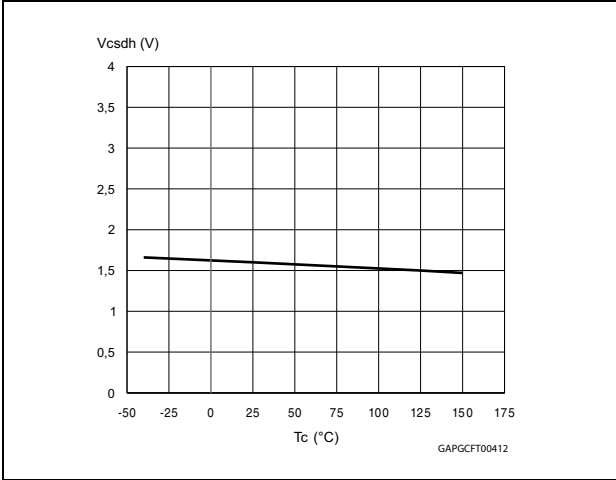


Figure 27. CS_DIS clamp voltage

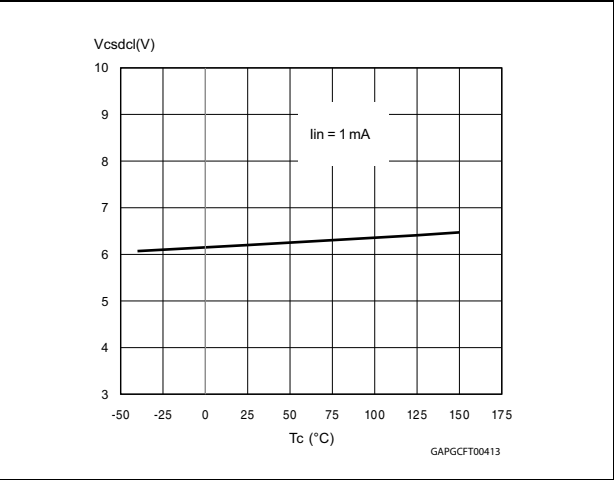
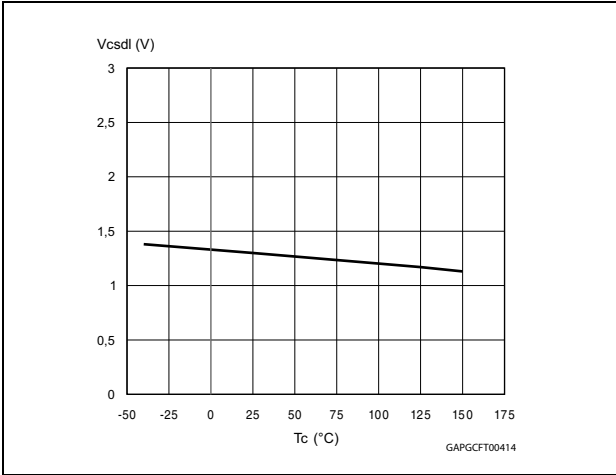
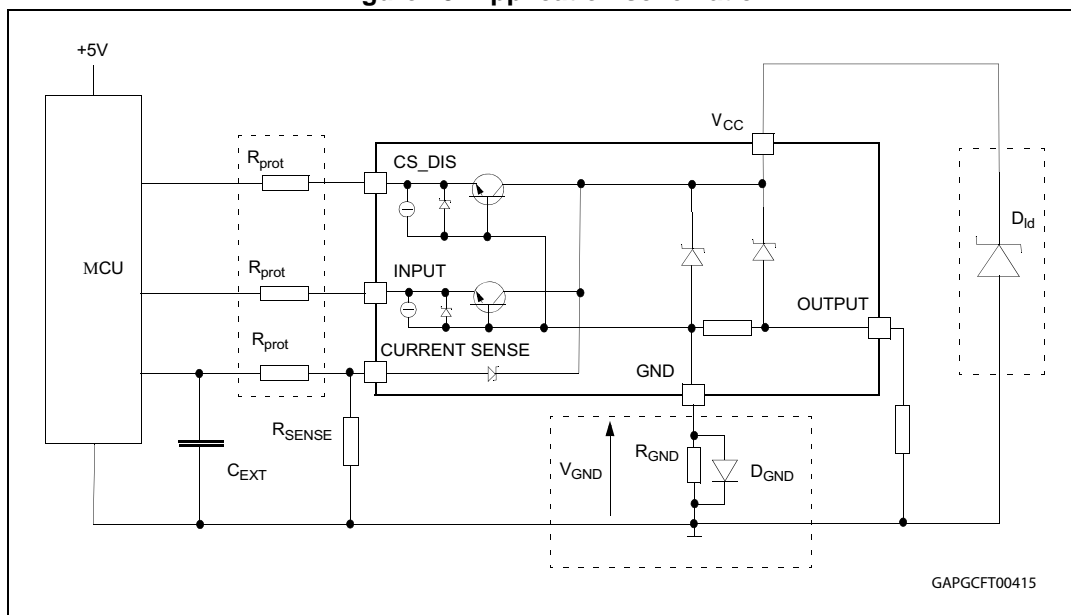


Figure 28. CS_DIS low level voltage



3 Application information

Figure 29. Application schematic



1. Channel 2, 3, 4 have the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum On-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2 : diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1\text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600\text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{ V}$ and $I_{latchup} \geq 20\text{ mA}$; $V_{OH\mu C} \geq 4.5\text{ V}$

$$5\text{ k}\Omega \leq R_{prot} \leq 180\text{ k}\Omega$$

Recommended values: $R_{prot} = 10\text{ k}\Omega$, $C_{EXT} = 10\text{ nF}$.

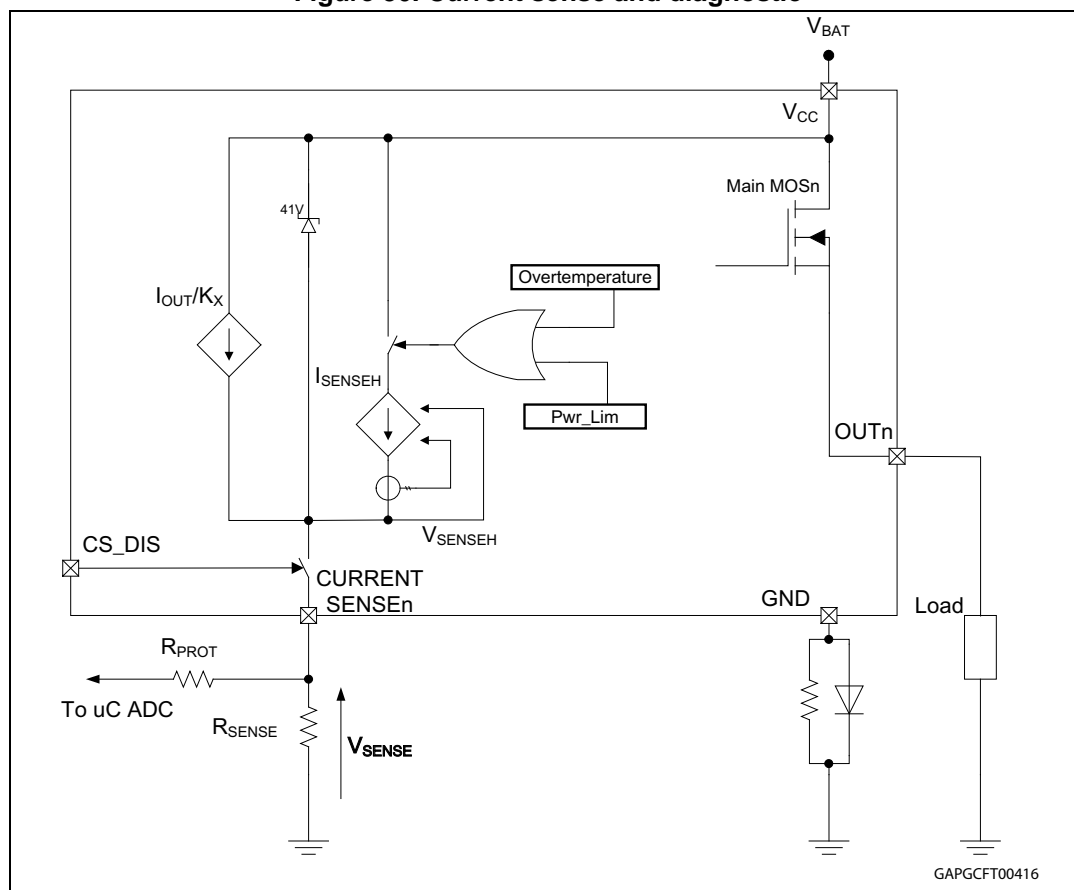
3.4 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 30: Current sense and diagnostic](#)):

- Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X .
 The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)).
- Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to):
 - Power limitation activation
 - Over-temperature

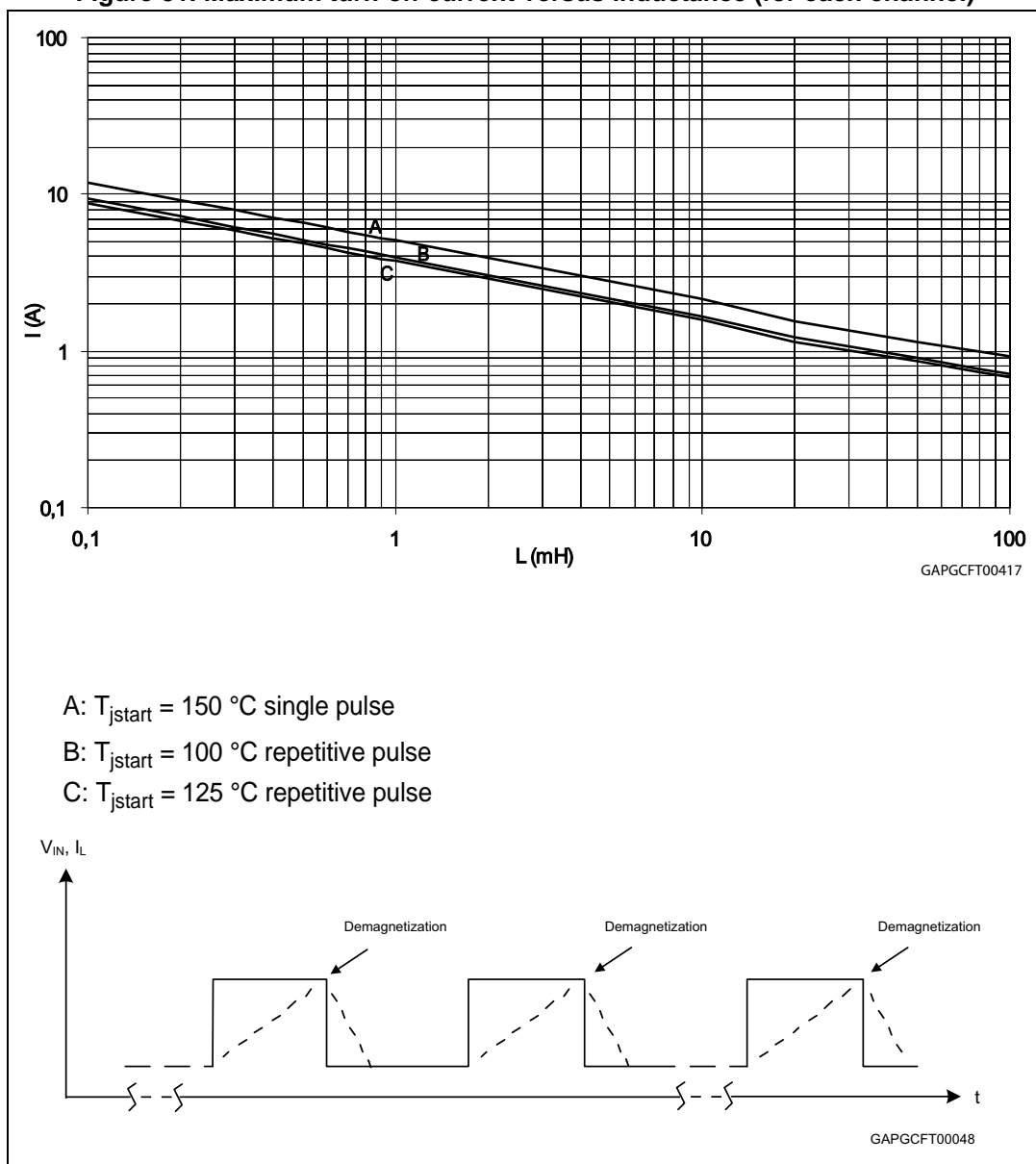
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.5 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 31. Maximum turn-off current versus inductance (for each channel)

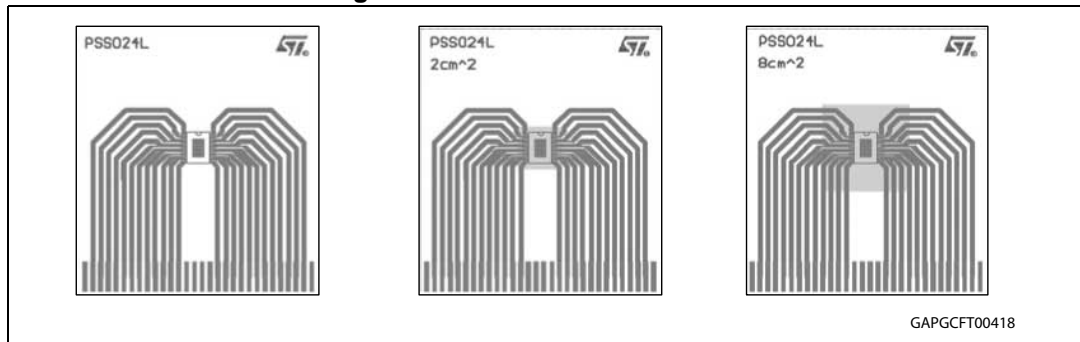


1. Values are generated with $R_L = 0\text{ }\Omega$.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-24 thermal data

Figure 32. PowerSSO-24 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 mm (front and back side), Copper areas: from minimum pad lay-out to 8 cm²).

Figure 33. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

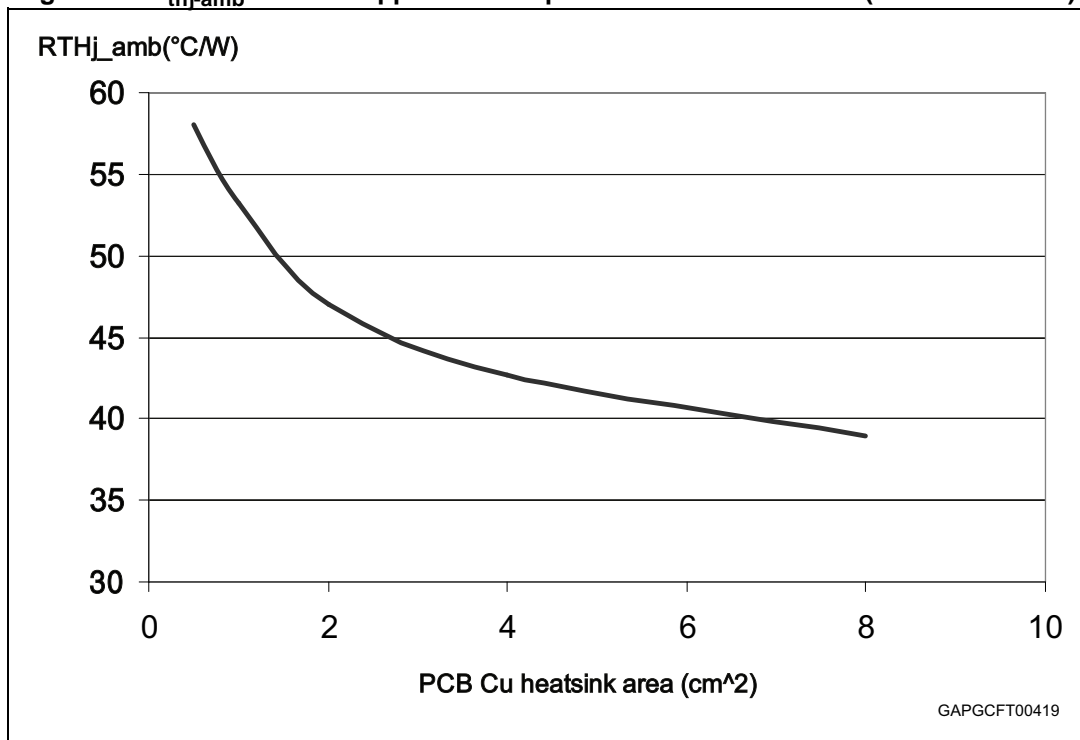


Figure 34. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

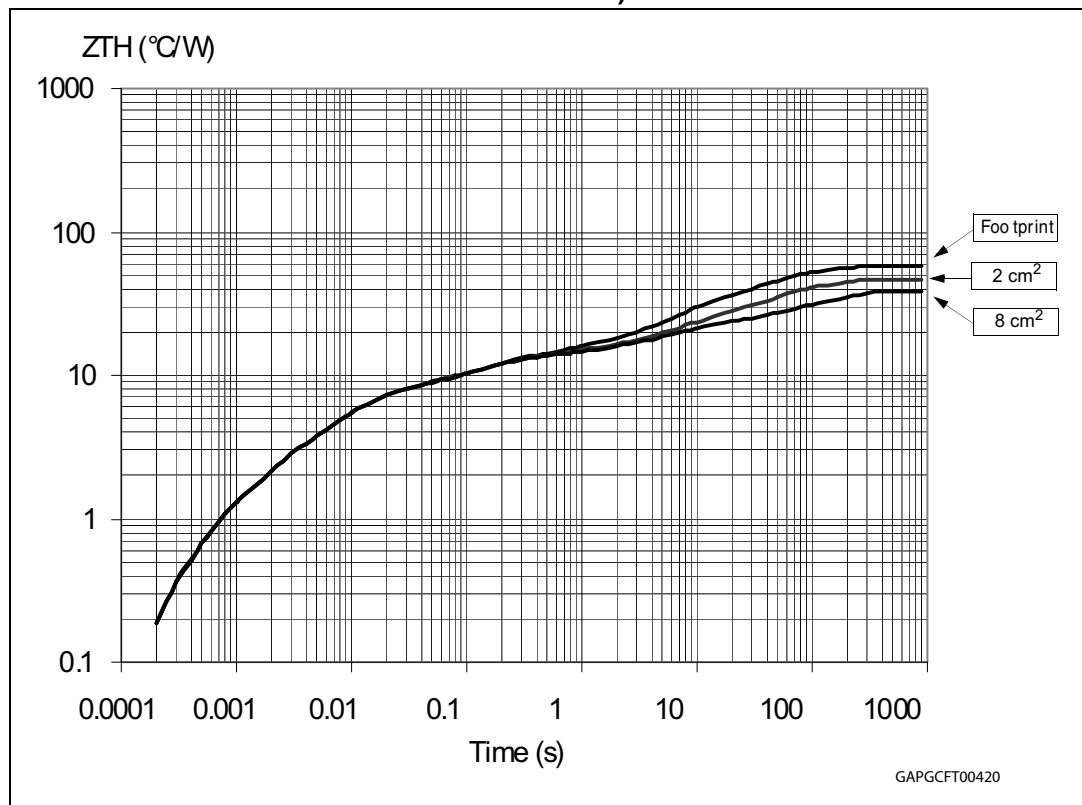
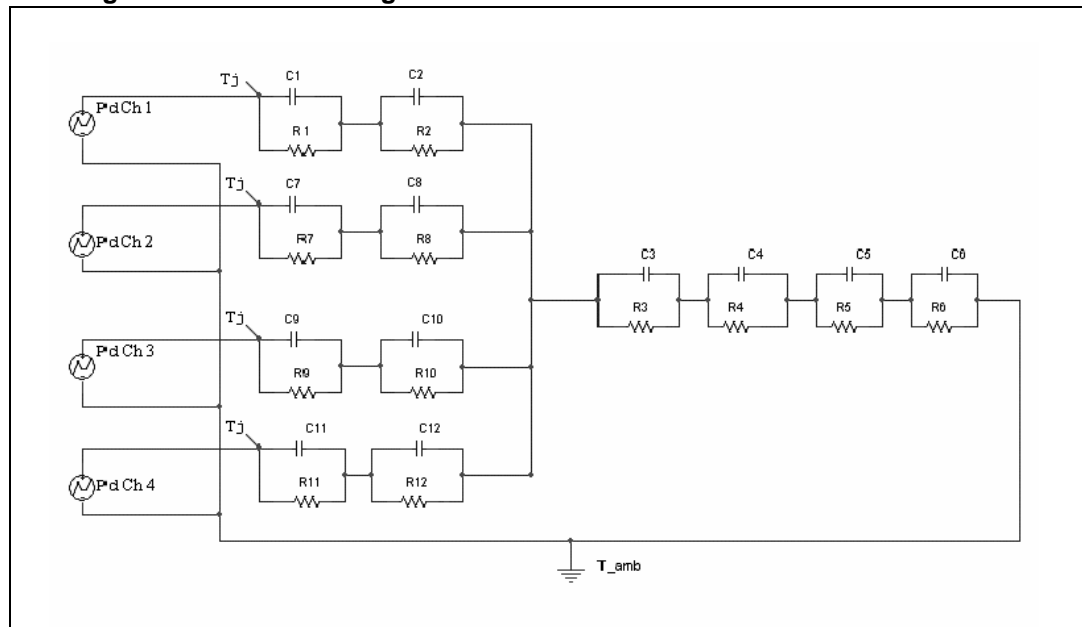


Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-24



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Table 14. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1 = R7 = R9 = R11 (°C/W)	1.2		
R2 = R8 = R10 = R12 (°C/W)	6		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 = C9 = C11 (W.s/°C)	0.0008		
C2 = C8 = C10 = C12 (W.s/°C)	0.0016		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

5.2 PowerSSO-24 mechanical data

Figure 36. PowerSSO-24 package dimensions

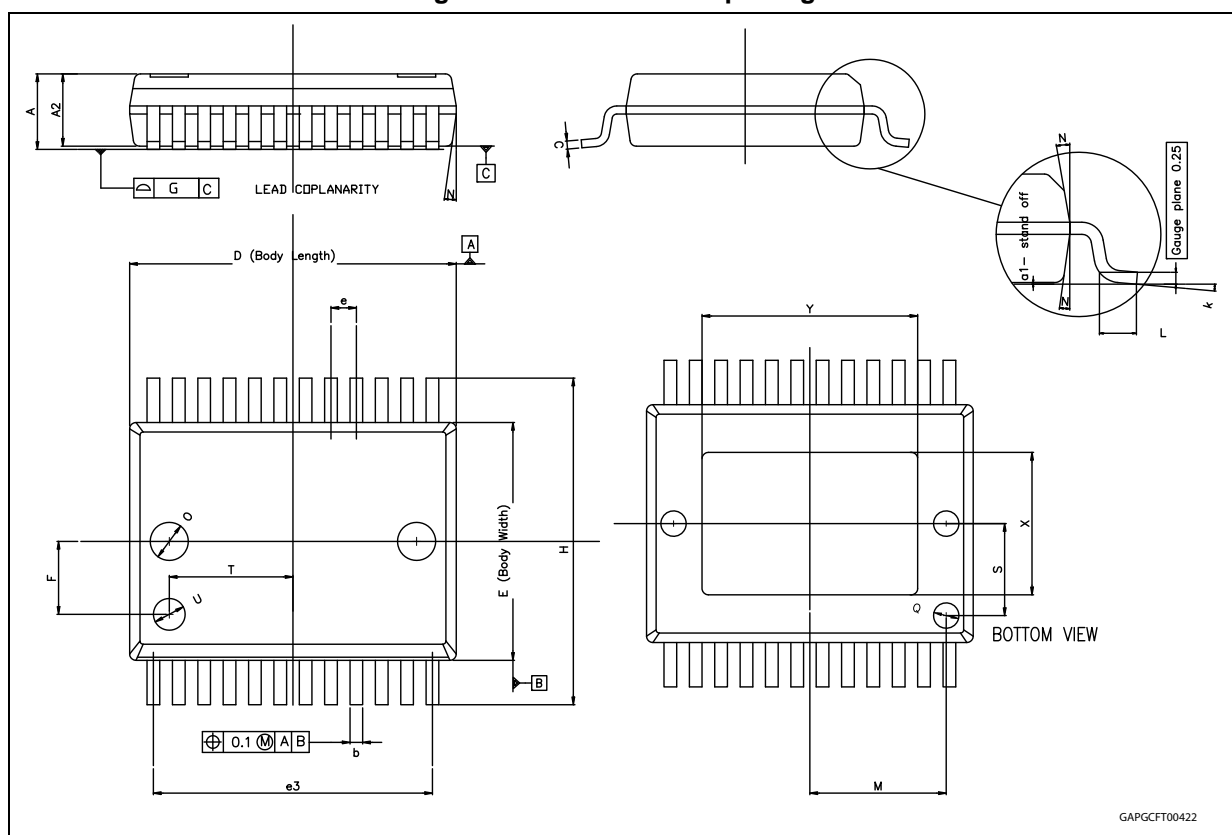


Table 15. PowerSSO-24 mechanical data⁽¹⁾⁽²⁾

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.50
A2	2.15		2.40
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D ⁽³⁾	10.10		10.50
E ⁽³⁾	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k		5°	
L	0.6		1
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10°
X	4.1		4.7
Y	6.5 4.9 ⁽⁴⁾		7.1 5.5 ⁽⁴⁾

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. "D and E" do not include mold flash or protusions. Mold flash or protusions shall not exceed 0.15 mm.
4. Variations for small window leadframe option.

5.3 Packing information

Figure 37. PowerSSO-24 tube shipment (no suffix)

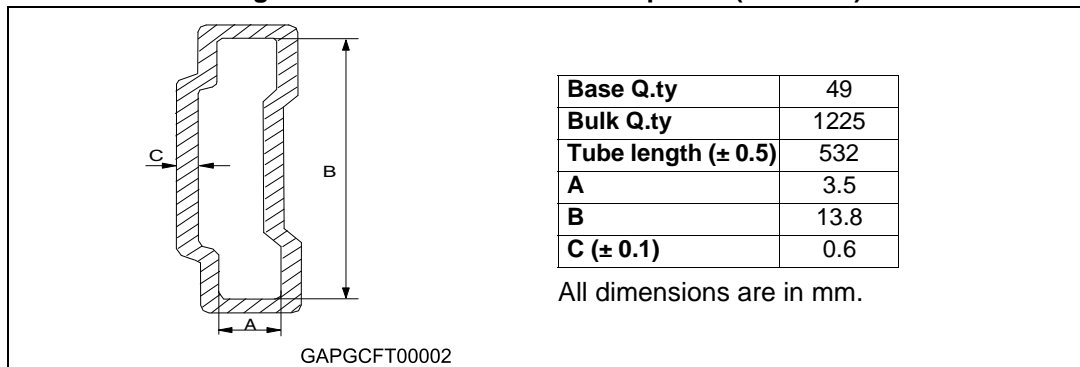
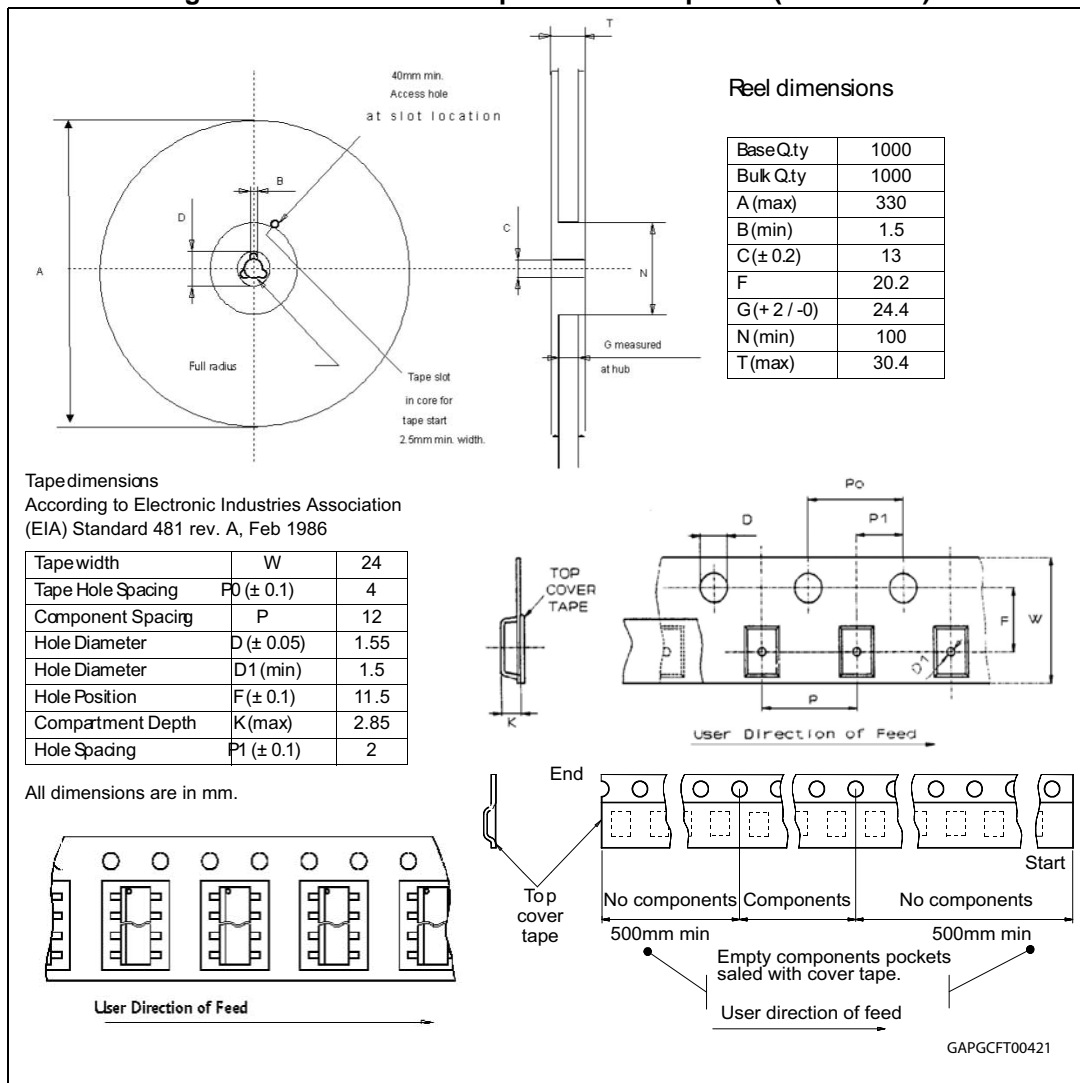


Figure 38. PowerSSO-24 tape and reel shipment (suffix "TR")



6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VNQ5E160MK-E	VNQ5E160MKTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
25-May-2011	1	Initial release.
04-Nov-2013	2	Updated disclaimer.

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