

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	$I_{DR}^{\dagger}$	$I_{DRM}$
TO-92	190mA	1.7A	1.0W	190mA	1.7A

**Notes:**
<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

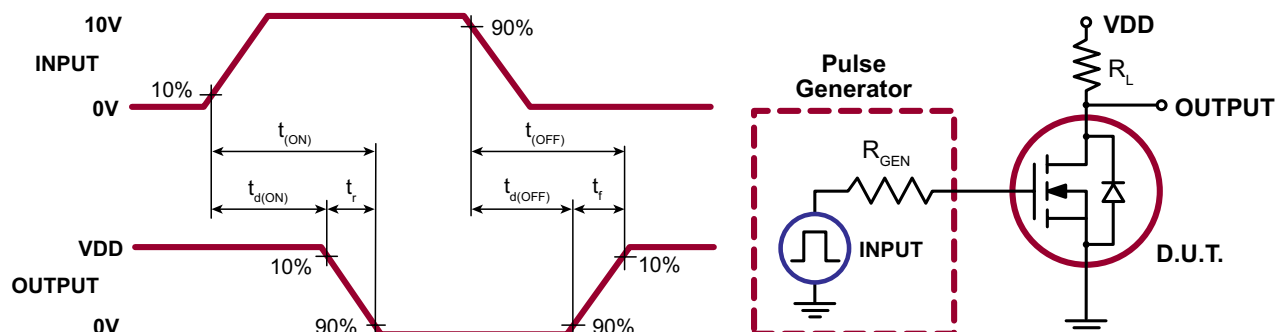
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	240	-	-	V	$V_{GS} = 0V, I_D = 100\mu A$
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.0	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$I_{GSS}$	Gate body leakage	-	-	100	nA	$V_{GS} = 20V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	10	$\mu A$	$V_{GS} = 0V, V_{DS} = 120V$
		-	-	500		$V_{GS} = 0V, V_{DS} = 120V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	1.0	-	-	A	$V_{GS} = 10V, V_{DS} = 15V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	10	$\Omega$	$V_{GS} = 2.5V, I_D = 100mA$
		-	-	6.0		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	1.0	1.4	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 500mA$
$G_{FS}$	Forward transductance	300	-	-	mmho	$V_{DS} = 10V, I_D = 500mA$
$C_{ISS}$	Input capacitance	-	-	125	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	-	50		
$C_{RSS}$	Reverse transfer capacitance	-	-	20		
$t_r$	Rise time	-	-	8.0	ns	$V_{DD} = 60V, I_D = 400mA, R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-on delay time	-	-	8.0		
$t_f$	Fall time	-	-	24		
$t_{d(OFF)}$	Turn-off delay time	-	-	23		
$V_{SD}$	Diode forward voltage drop	-	1.2	-	V	$V_{GS} = 0V, I_{SD} = 800mA$

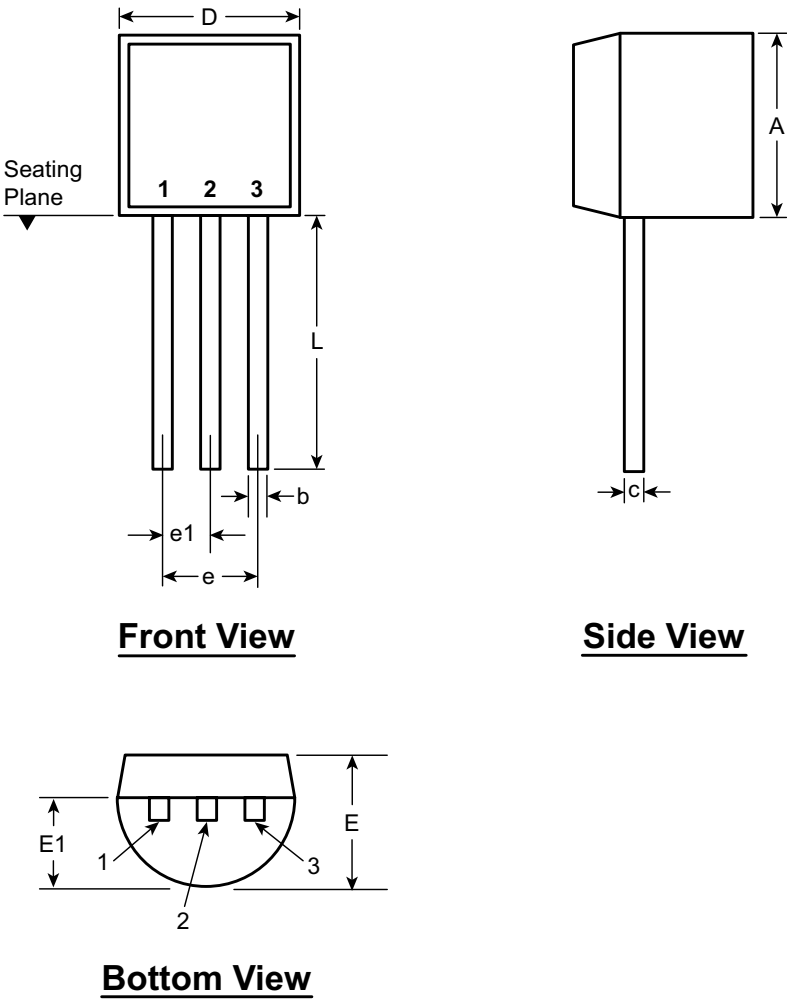
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu s$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit



3-Lead TO-92 Package Outline (L)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.  
\* This dimension is not specified in the JEDEC drawing.  
† This dimension differs from the JEDEC drawing.  
**Drawings not to scale.**  
**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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