

# Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>pk</sub>	100	Watts
Maximum Peak Pulse Current (tp = 8/20μs)	I <sub>pp</sub>	7	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>PP</sub>	+/- 20 +/- 12	kV
Lead Soldering Temperature	T <sub>L</sub>	260 (10 sec.)	°C
Operating Temperature	T,	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

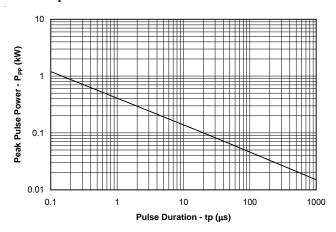
# Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>				5	V
Reverse Breakdown Voltage	$V_{BR}$	I <sub>t</sub> = 1mA	6	7.8	9	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, T=25°C		0.100	1	μΑ
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3V, T=25°C		0.050	0.500	μΑ
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 1A, t_p = 8/20 \mu s$			9	V
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 7A, t_p = 8/20 \mu s$			12	V
Junction Capacitance	C <sub>j</sub>	Between I/O Pins and Gnd V <sub>R</sub> = OV, f = 1MHz		30	40	pF

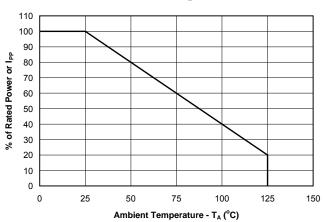


## **Typical Characteristics**

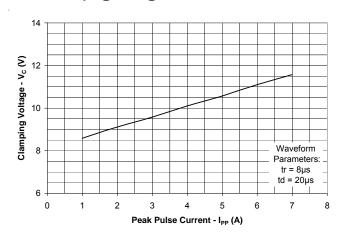
### Non-Repetitive Peak Pulse Power vs. Pulse Time



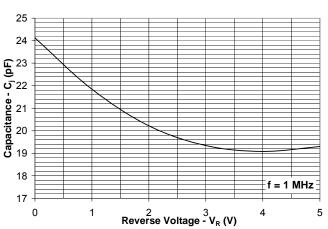
### **Power Derating Curve**



### Clamping Voltage vs. Peak Pulse Current



### Junction Capacitance vs. Reverse Voltage



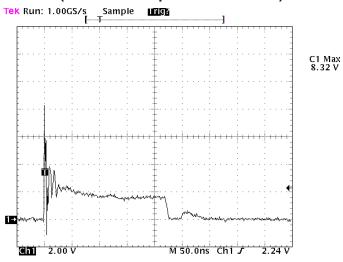
### **Insertion Loss S21**



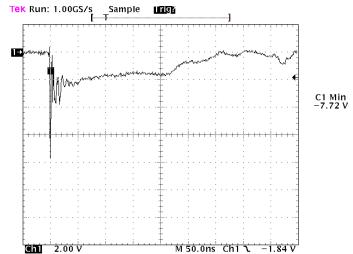


## Typical Characteristics (Con't.)

# ESD Clamping (+8kV Contact per IEC 61000-4-2)



# ESD Clamping (-8kV Contact per IEC 61000-4-2)





### **Applications Information**

### **Device Connection for Protection of Five Data Lines**

These devices are designed to protect up to five bildirectional data lines. The device is connected as follows:

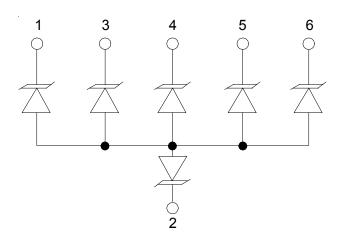
1. Bidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

# Circuit Board Layout Recommendations for Suppression of ESD.

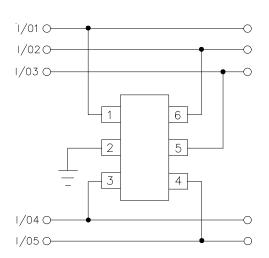
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

### **Circuit Diagram**

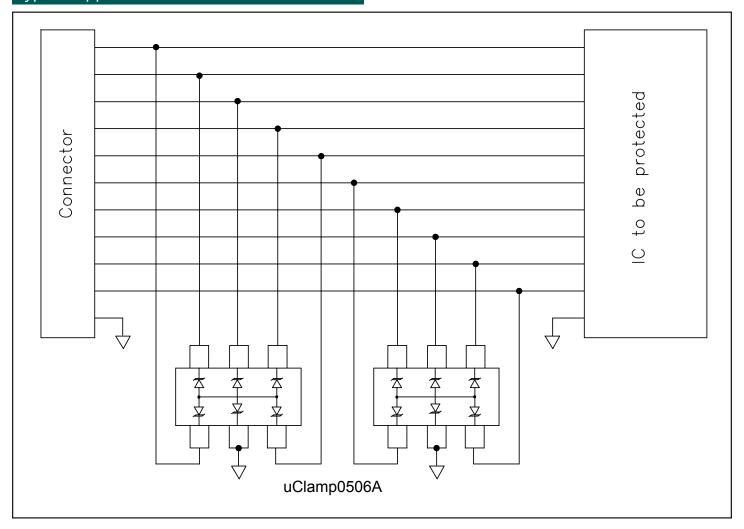


#### **Protection of Five Bidirectional Lines**



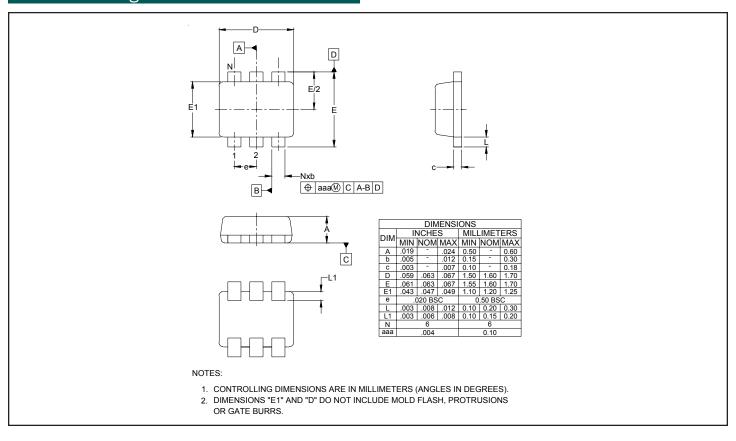


# Typical Applications

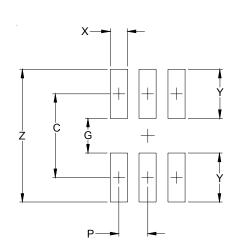




## Outline Drawing - SC-89



# Land Pattern - SC89



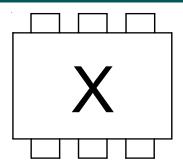
DIMENSIONS				
DIM	INCHES	MILLIMETERS		
С	(.057)	(1.45)		
Р	.020	0.50		
G	.024	0.60		
Χ	.012	0.30		
Υ	.033	0.85		
Z	.090	2.30		

### NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.



# Marking Code



## **Ordering Information**

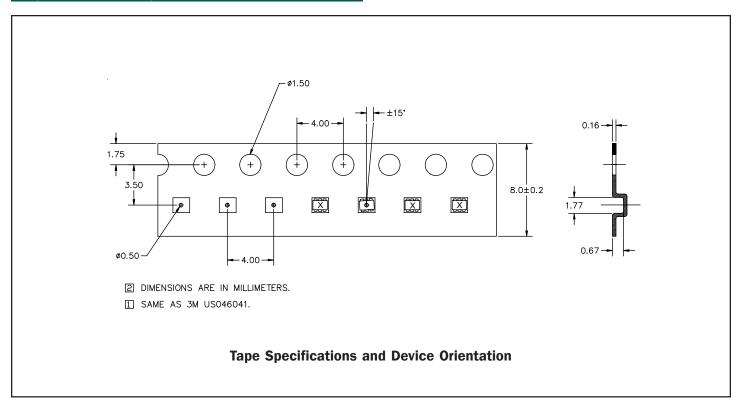
Part N	Number	Working Voltage	Device Marking	Qty per Reel	Reel Size
uClamp(	)506A.TCT	5V	Х	3,000	7 Inch

MicroClamp, uClamp and  $\mu$ Clamp are trademarks of Semtech Corporation

#### Note:

- (1) Device is symmetrical so there is no pin 1 identifier
- (2) Lead finish is matte tin

## Tape and Reel Specification



### **Contact Information**

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