

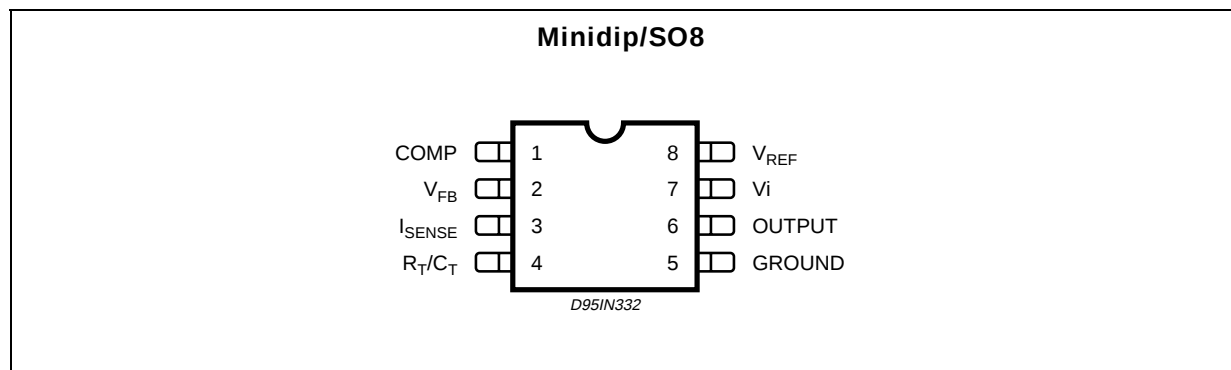
UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage ($I_i < 30\text{mA}$)	Self Limiting	
I_o	Output Current	± 1	A
E_o	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	-0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (Minidip)	1.25	W
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO8)	800	mW
T_{stg}	Storage Temperature Range	-65 to 150	$^\circ\text{C}$
T_j	Junction Operating Temperature	-40 to 150	$^\circ\text{C}$
T_L	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTION (top view)



PIN FUNCTIONS

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T .

ORDERING NUMBERS

SO8	Minidip
UC2842BD1; UC3842BD1 UC2843BD1; UC3843BD1 UC2844BD1; UC3844BD1 UC2845BD1; UC3845BD1	UC2842BN; UC3842BN UC2843BN; UC3843BN UC2844BN; UC3844BN UC2845BN; UC3845BN

THERMAL DATA

Symbol	Description	Minidip	SO8	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient. max.	100	150	°C/W

ELECTRICAL CHARACTERISTICS ([note 1] Unless otherwise stated, these specifications apply for $-25 \leq T_{amb} \leq 85^\circ\text{C}$ for UC284XB; $0 \leq T_{amb} \leq 70^\circ\text{C}$ for UC384XB; $V_i = 15\text{V}$ (note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

Symbol	Parameter	Test Conditions	UC284XB			UC384XB			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V _{REF}	Output Voltage	T _J = 25°C I _o = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV _{REF}	Line Regulation	12V ≤ V _i ≤ 25V		2	20		2	20	mV
ΔV _{REF}	Load Regulation	1 ≤ I _o ≤ 20mA		3	25		3	25	mV
ΔV _{REF} /ΔT	Temperature Stability	(Note 2)		0.2			0.2		mV/°C
	Total Output Variation	Line, Load, Temperature	4.9		5.1	4.82		5.18	V
e _N	Output Noise Voltage	10Hz ≤ f ≤ 10KHz T _J = 25°C (note 2)		50			50		μV
	Long Term Stability	T _{amb} = 125°C, 1000Hrs (note 2)		5	25		5	25	mV
I _{SC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f _{osc}	Frequency	T _J = 25°C T _A = T _{low} to T _{high} T _J = 25°C (R _T = 6.2k, C _T = 1nF)	49 48 225	52 – 250	55 56 275	49 48 225	52 – 250	55 56 275	KHz KHz KHz
Δf _{osc} /ΔV	Frequency Change with Volt.	V _{CC} = 12V to 25V	–	0.2	1	–	0.2	1	%
Δf _{osc} /ΔT	Frequency Change with Temp.	T _A = T _{low} to T _{high}	–	1	–	–	0.5	–	%
V _{OSC}	Oscillator Voltage Swing	(peak to peak)	–	1.6	–	–	1.6	–	V
I _{dischg}	Discharge Current (V _{OSC} =2V)	T _J = 25°C T _A = T _{low} to T _{high}	7.8 7.5	8.3 –	8.8 8.8	7.8 7.6	8.3 –	8.8 8.8	mA mA
ERROR AMP SECTION									
V ₂	Input Voltage	V _{PIN1} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
I _b	Input Bias Current	V _{FB} = 5V		-0.1	-1		-0.1	-2	μA
	A _{VOL}	2V ≤ V _o ≤ 4V	65	90		65	90		dB
BW	Unity Gain Bandwidth	T _J = 25°C	0.7	1		0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	12V ≤ V _i ≤ 25V	60	70		60	70		dB
I _o	Output Sink Current	V _{PIN2} = 2.7V V _{PIN1} = 1.1V	2	12		2	12		mA
I _o	Output Source Current	V _{PIN2} = 2.3V V _{PIN1} = 5V	-0.5	-1		-0.5	-1		mA
	V _{OUT} High	V _{PIN2} = 2.3V; R _L = 15KΩ to Ground	5	6.2		5	6.2		V
	V _{OUT} Low	V _{PIN2} = 2.7V; R _L = 15KΩ to Pin 8		0.8	1.1		0.8	1.1	V
CURRENT SENSE SECTION									
G _V	Gain	(note 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
V ₃	Maximum Input Signal	V _{PIN1} = 5V (note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	12 ≤ V _i ≤ 25V (note 3)		70			70		dB
I _b	Input Bias Current			-2	-10		-2	-10	μA
	Delay to Output			150	300		150	300	ns

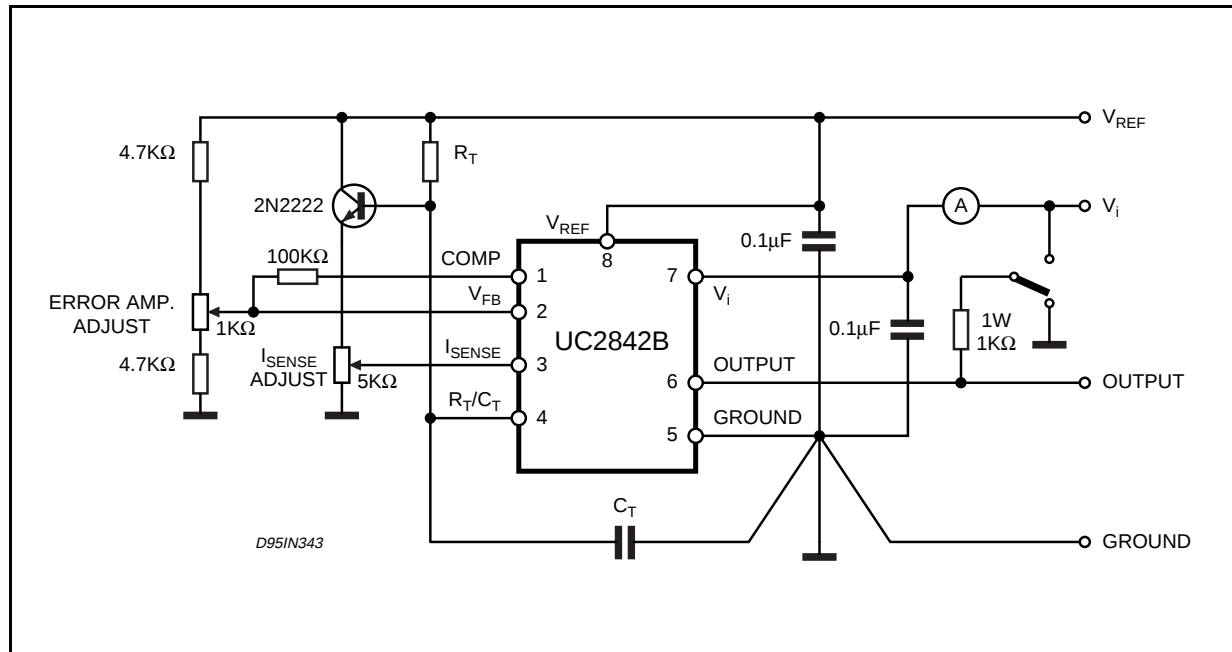
UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC284XB			UC384XB			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT SECTION									
V _{OL}	Output Low Level	I _{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I _{SINK} = 200mA		1.6	2.2		1.6	2.2	V
V _{OH}	Output High Level	I _{SOURCE} = 20mA	13	13.5		13	13.5		V
		I _{SOURCE} = 200mA	12	13.5		12	13.5		V
V _{OLS}	UVLO Saturation	V _{CC} = 6V; I _{SINK} = 1mA		0.1	1.1		0.1	1.1	V
t _r	Rise Time	T _J = 25°C C _L = 1nF (2)		50	150		50	150	ns
t _f	Fall Time	T _J = 25°C C _L = 1nF (2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842B/4B	15	16	17	14.5	16	17.5	V
		X843B/5B	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	X842B/4B	9	10	11	8.5	10	11.5	V
		X843B/5B	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM SECTION									
	Maximum Duty Cycle	X842B/3B	94	96	100	94	96	100	%
		X844B/5B	47	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I _{st}	Start-up Current	V _i = 6.5V for UCX843B/45B		0.3	0.5		0.3	0.5	mA
		V _i = 14V for UCX842B/44B		0.3	0.5		0.3	0.5	mA
I _i	Operating Supply Current	V _{PIN2} = V _{PIN3} = 0V		12	17		12	17	mA
V _{iz}	Zener Voltage	I _i = 25mA	30	36		30	36		V

- Notes :**
1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_j as close to T_{amb} as possible.
 2. These parameters, although guaranteed, are not 100% tested in production.
 3. Parameter measured at trip point of latch with V_{PIN2} = 0.
 4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8 \text{ V}$$
 5. Adjust V_i above the start threshold before setting at 15 V.

Figure 1: Open Loop Test Circuit.

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close

to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

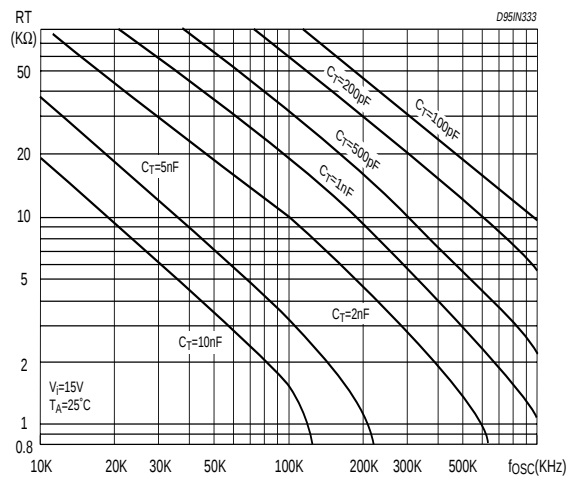
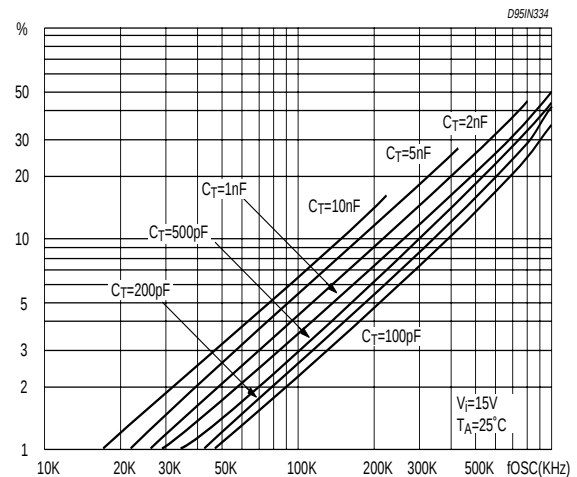
Figure 2: Timing Resistor vs. Oscillator Frequency**Figure 3:** Output Dead-Time vs. Oscillator Frequency

Figure 4: Oscillator Discharge Current vs. Temperature.

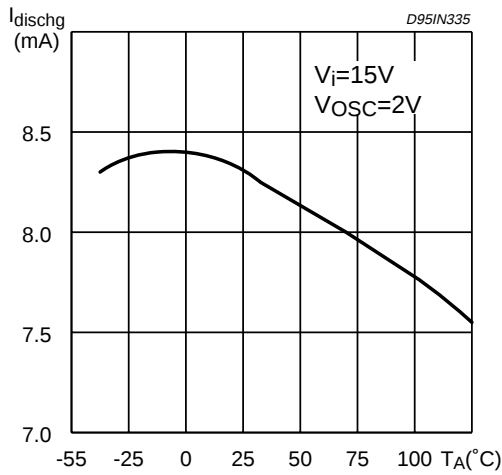


Figure 5: Maximum Output Duty Cycle vs. Timing Resistor.

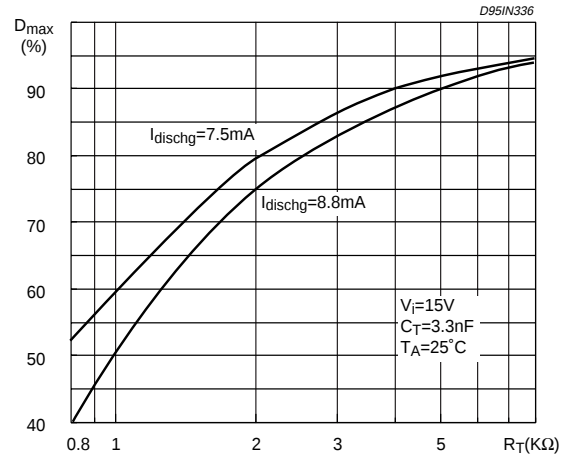


Figure 6: Error Amp Open-Loop Gain and Phase vs. Frequency.

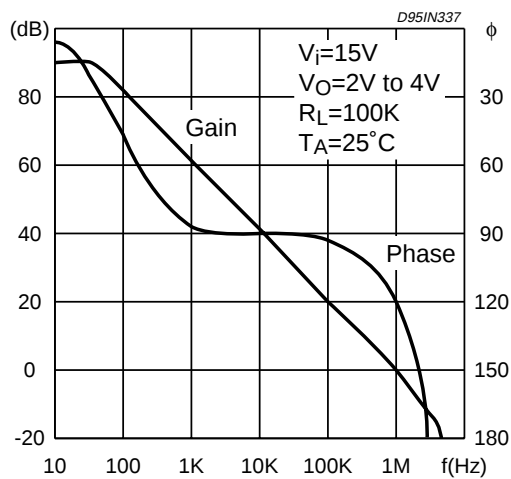


Figure 7: Current Sense Input Threshold vs. Error Amp Output Voltage.

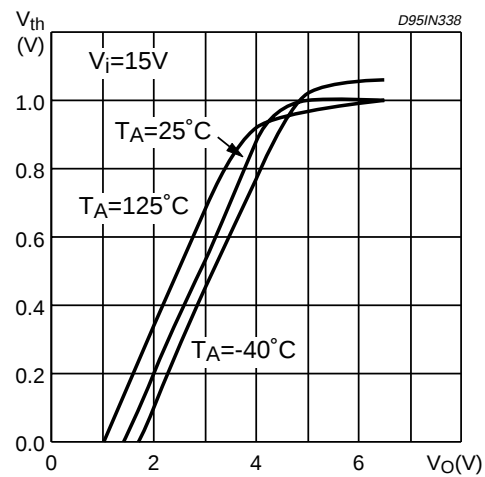


Figure 8: Reference Voltage Change vs. Source Current.

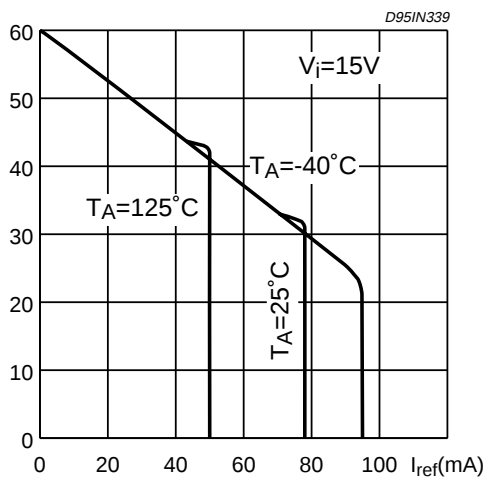


Figure 9: Reference Short Circuit Current vs. Temperature.

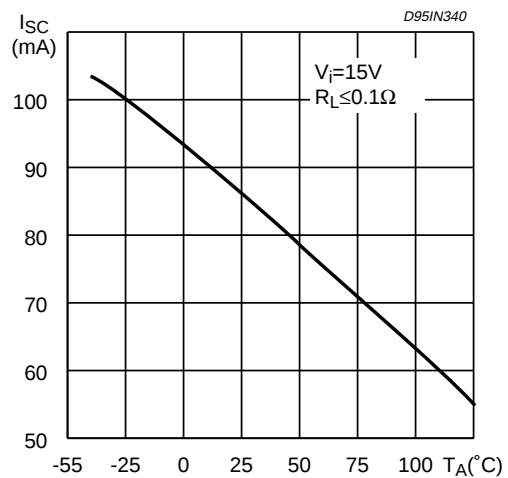


Figure 10: Output Saturation Voltages vs. Load Current.

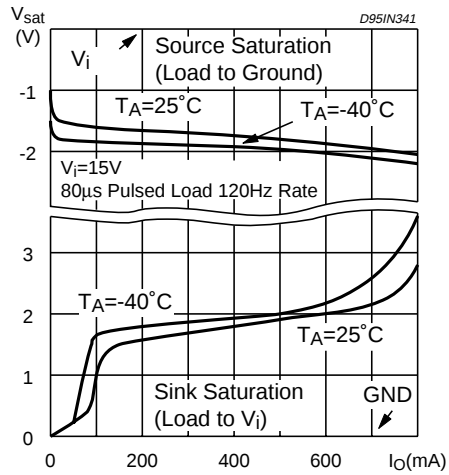


Figure 12: Output Waveform.

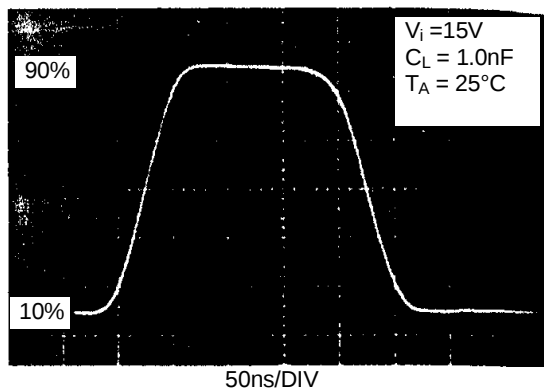


Figure 14: Oscillator and Output Waveforms.

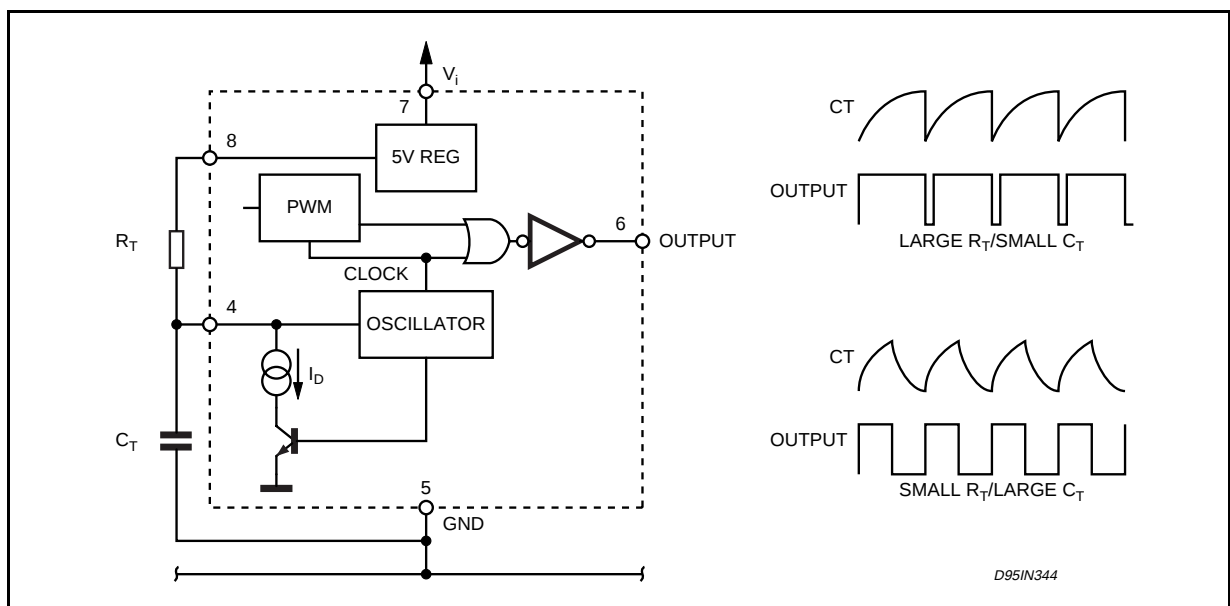


Figure 11: Supply Current vs. Supply Voltage.

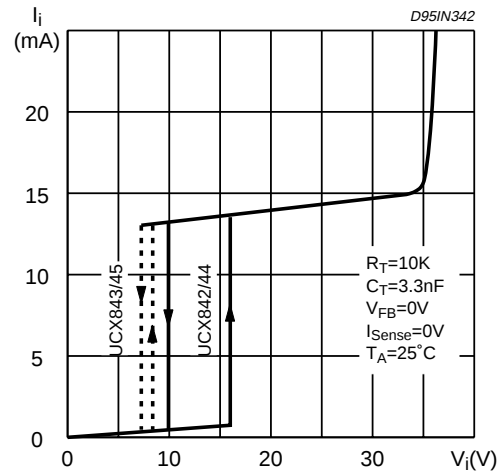


Figure 13: Output Cross Conduction

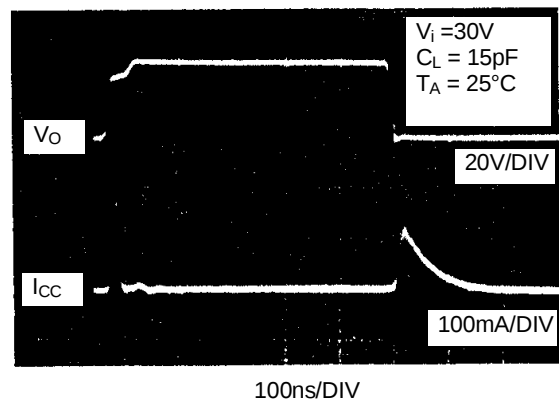


Figure 15 : Error Amp Configuration.

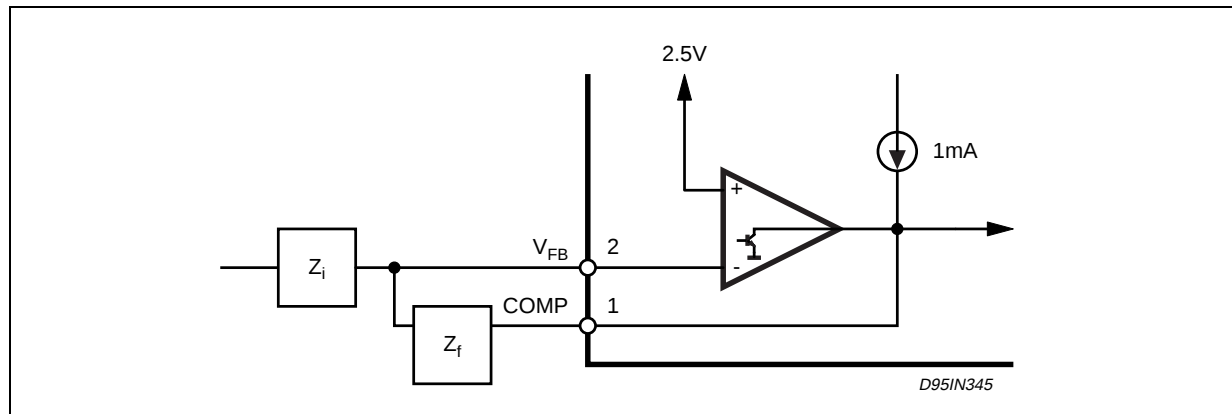


Figure 16 : Under Voltage Lockout.

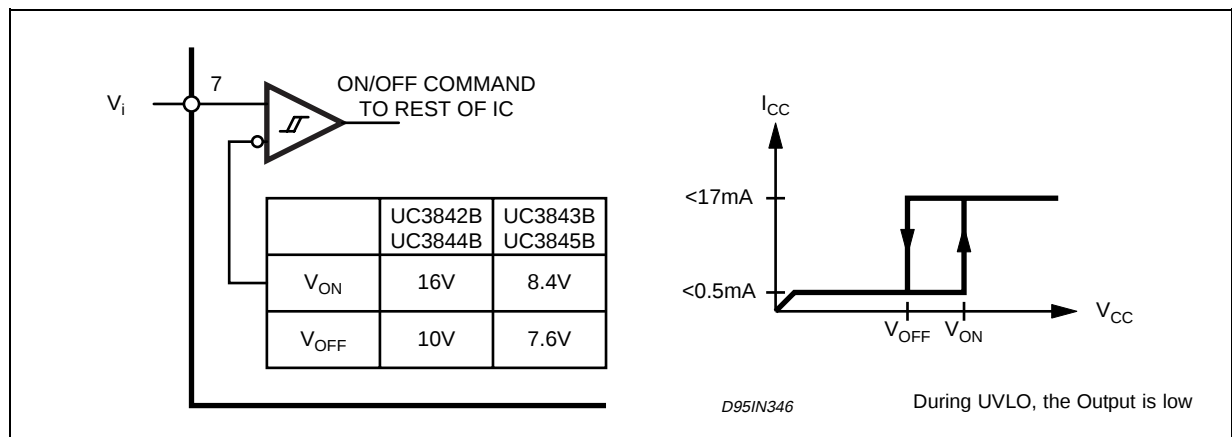
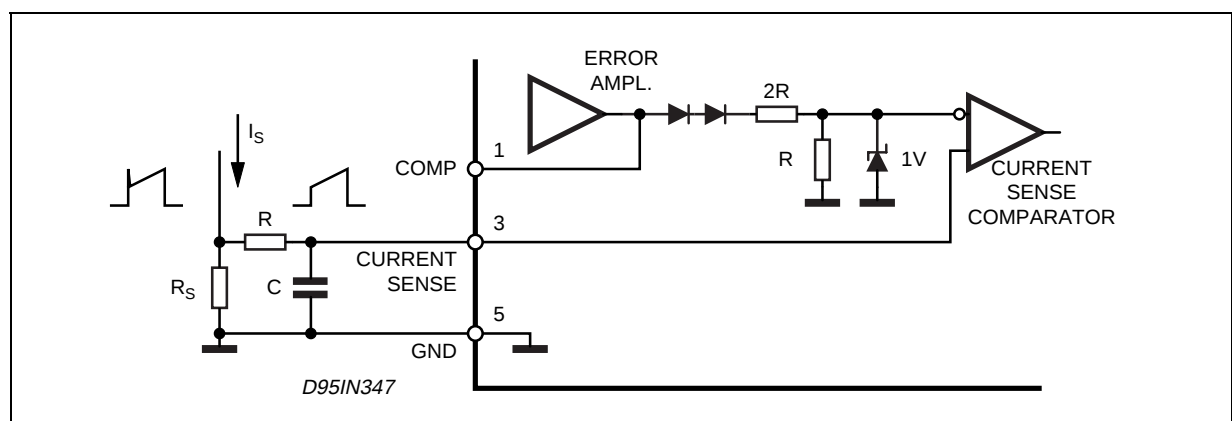


Figure 17 : Current Sense Circuit .



Peak current (i_s) is determined by the formula

$$I_{S \text{ max}} \approx \frac{1.0 \text{ V}}{R_s}$$

A small RC filter may be required to suppress switch transients.

Figure 20 : Latched Shutdown.

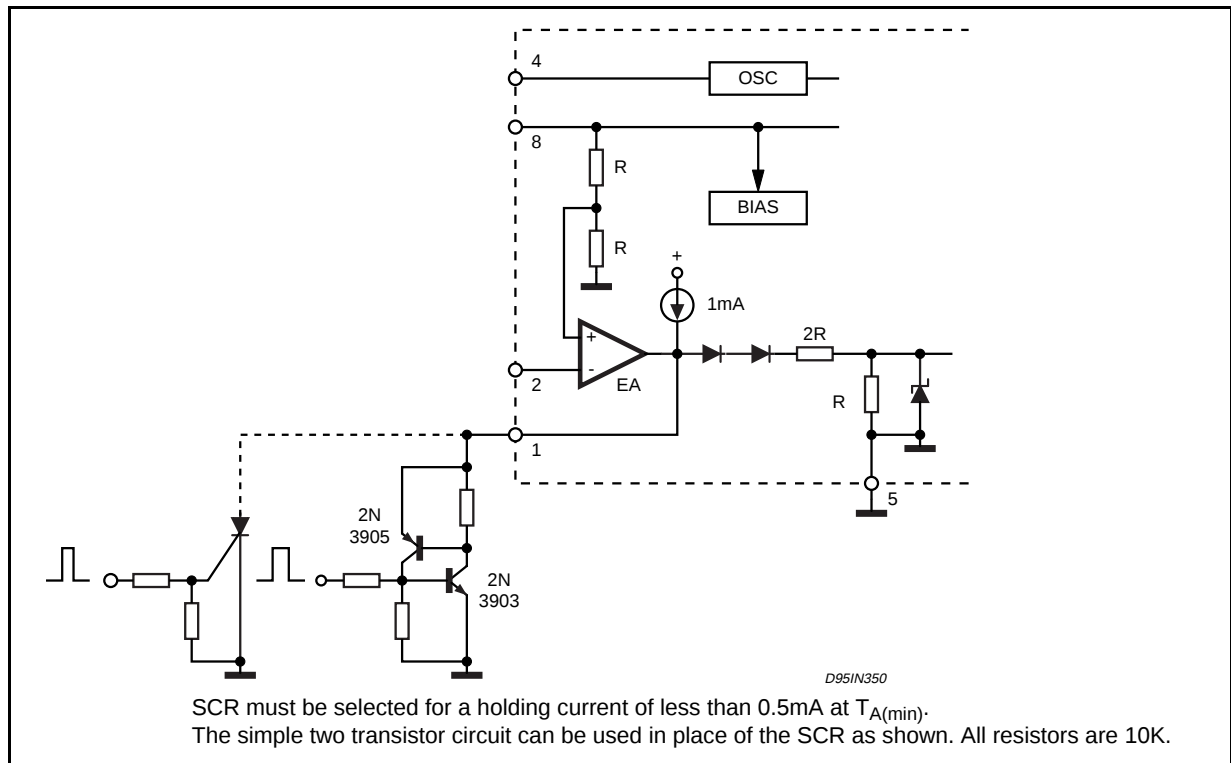


Figure 21: Error Amplifier Compensation

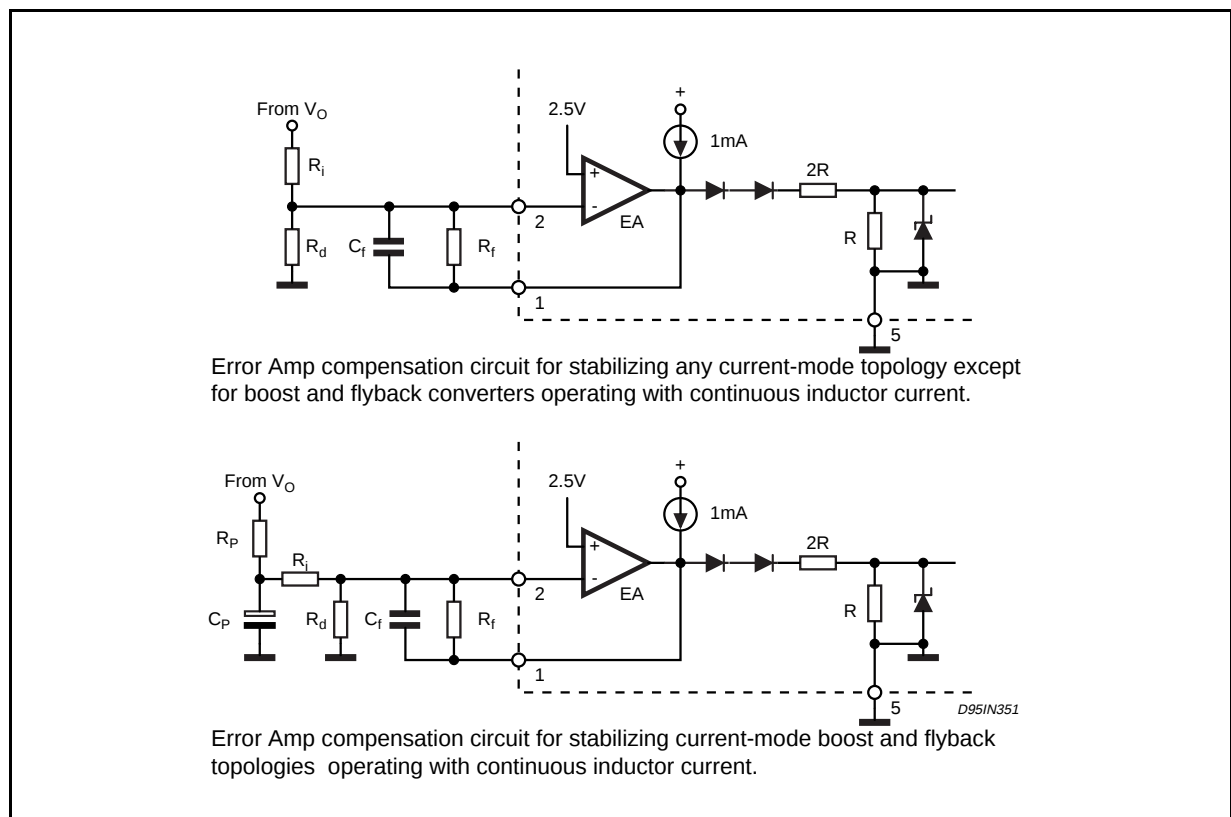
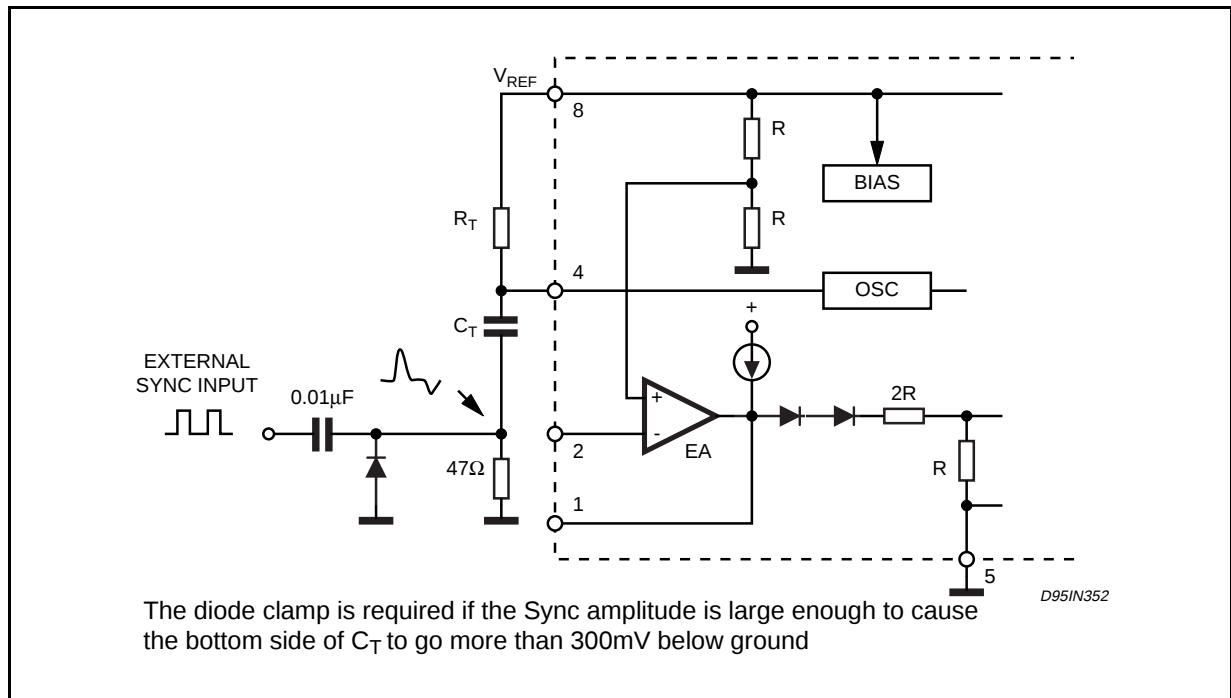
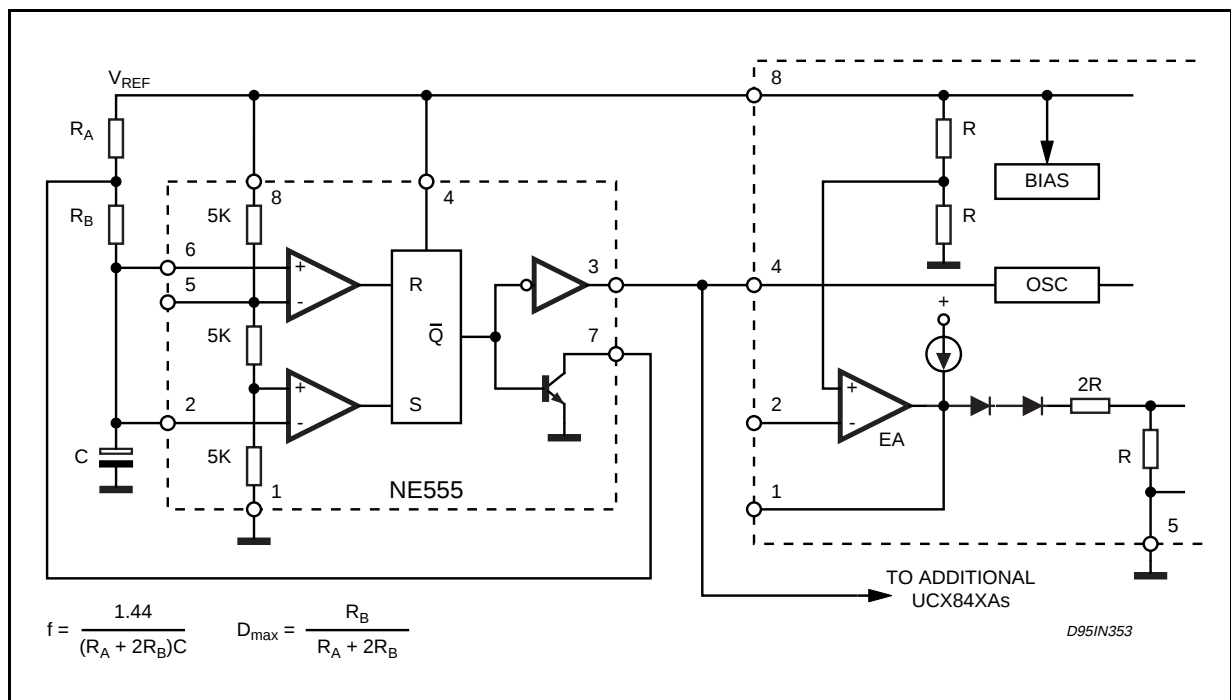


Figure 22: External Clock Synchronization.**Figure 23:** External Duty Cycle Clamp and Multi Unit Synchronization.

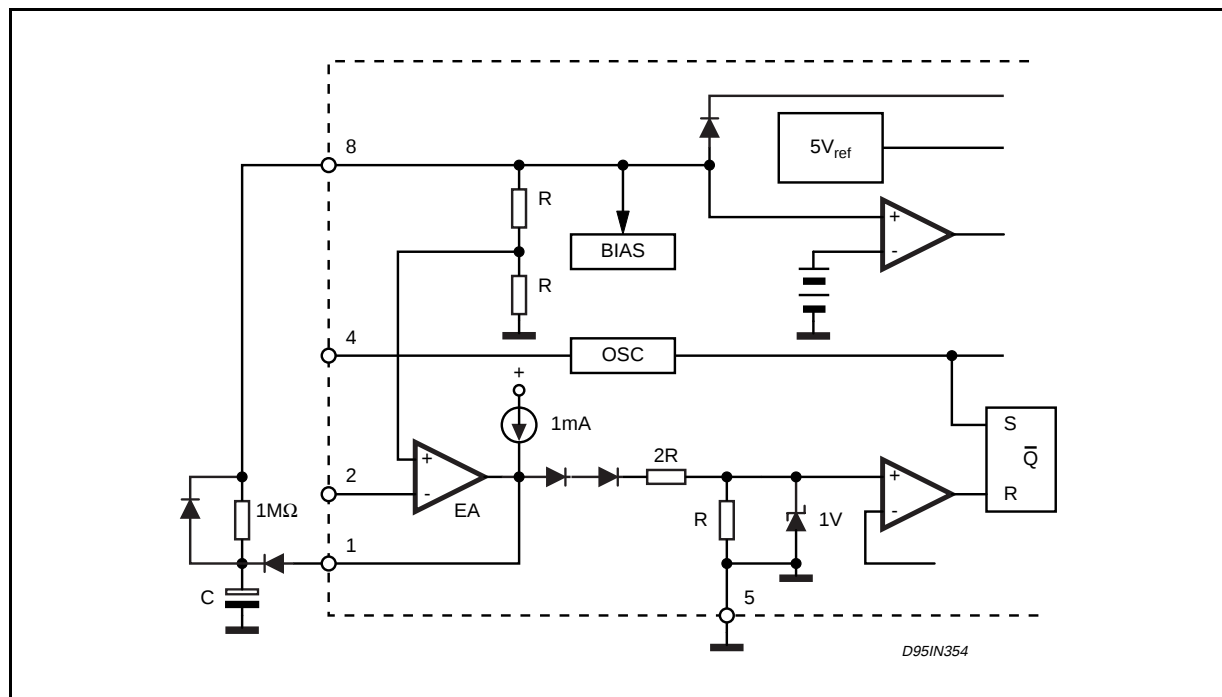
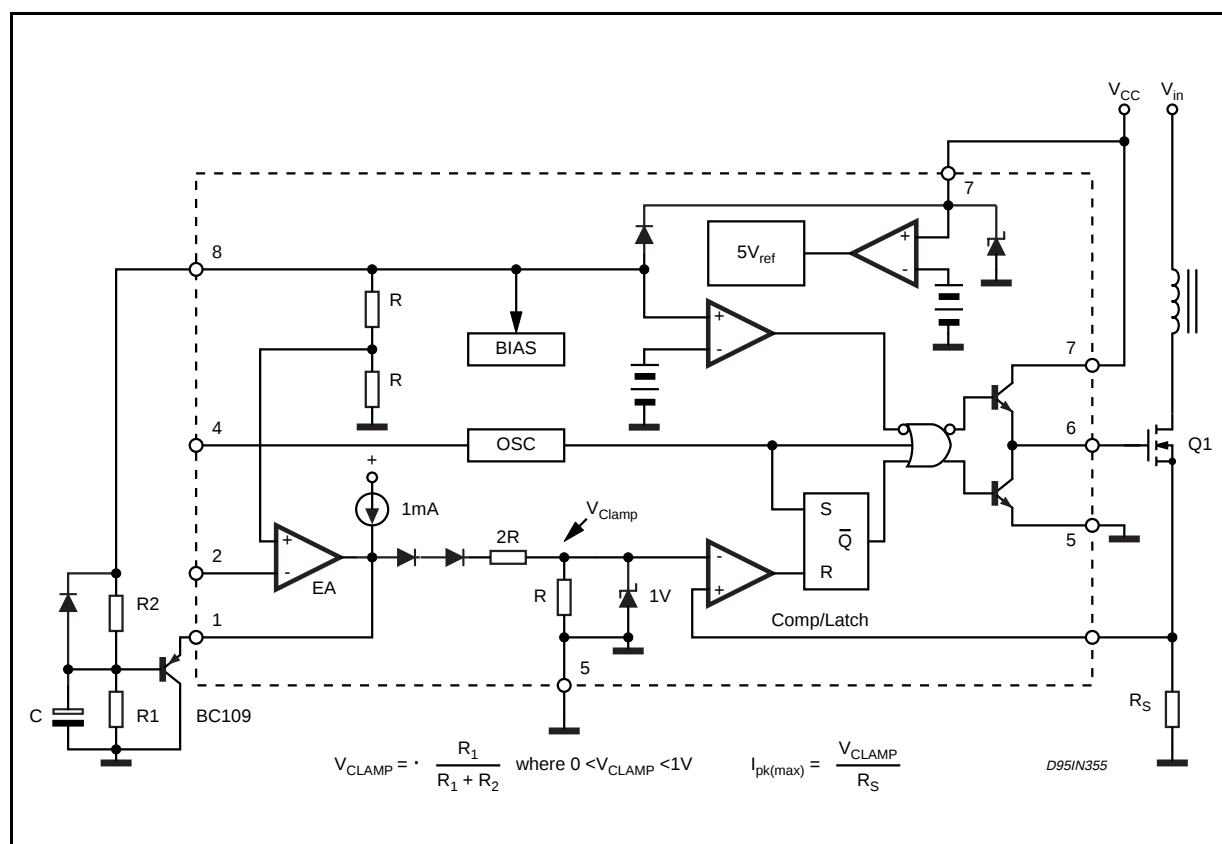


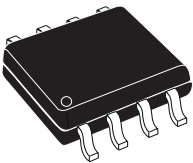
Figure 25: Soft-Start and Error Amplifier Output Duty Cycle Clamp.



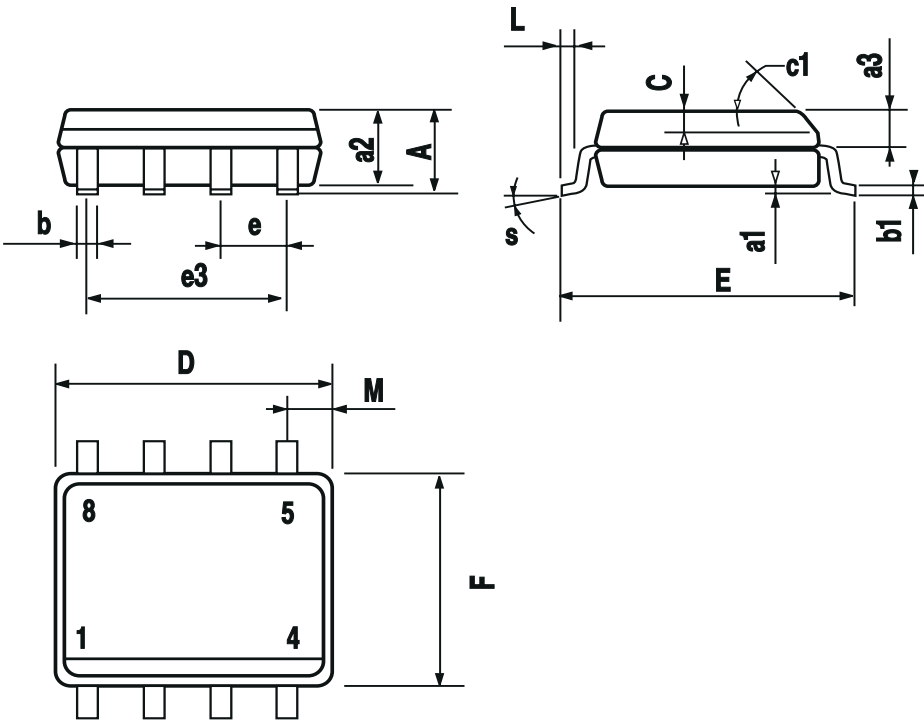
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND
MECHANICAL DATA



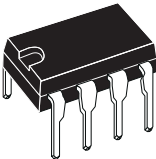
SO8



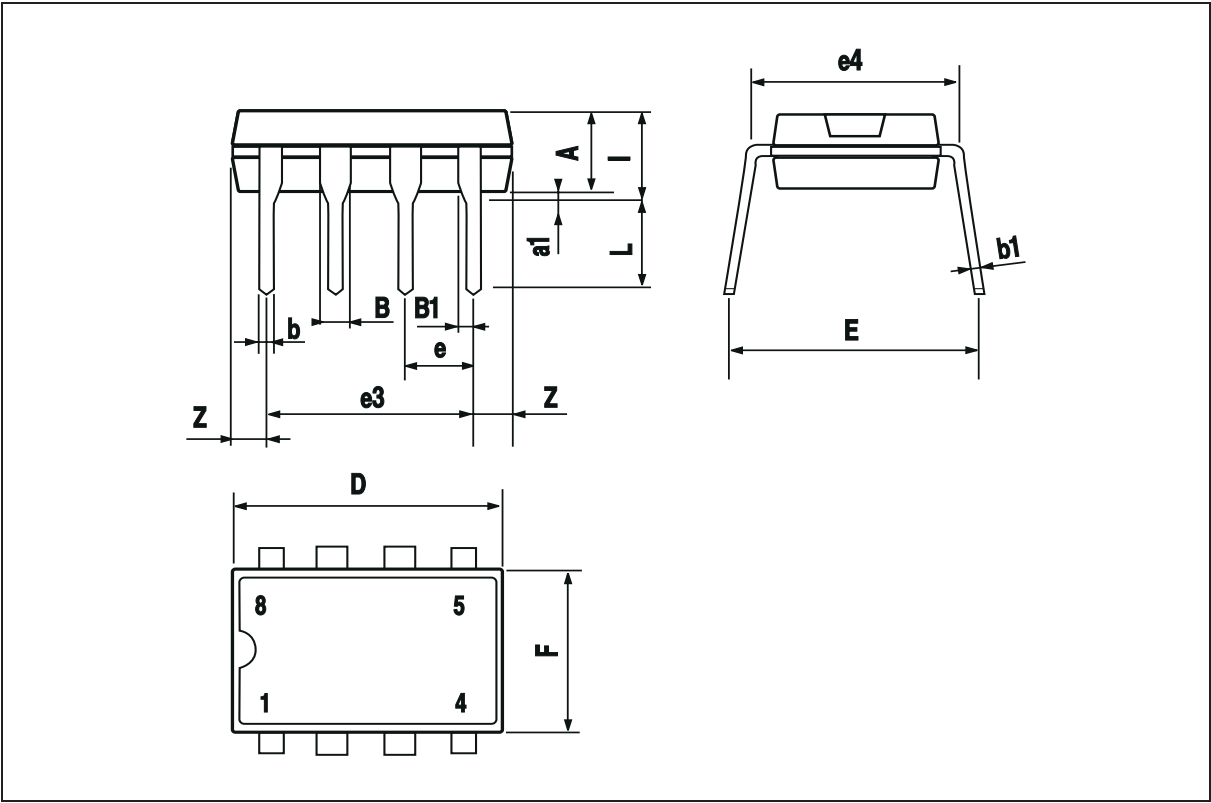
UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



Minidip



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