TISP4A250H3BJ Overvoltage Protector

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Absolute Maximum Ratings, TA = 25 °C (Unless Otherwise Noted)

Rating		Value	Unit
Repetitive peak off-state voltage (see Note 1)		+100 -200	V
Non-repetitive peak impulse current (see Notes 2 and 3)			
2/10 μs (GR-1089-CORE, 2/10 μs voltage wave shape)		±500	
8/20 μs (IEC 61000-4-5, 1.2/50 μs voltage, 8/20 μs current combination wave generator)		±300	
10/160 μs (TIA-968-A, 10/160 μs voltage wave shape)		±250	
5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45)	I _{PPSM}	±200	A
5/320 μs (TIA-968-A, 9/720 μs voltage wave shape)		±200	
10/560 μs (TIA-968-A, 10/560 μs voltage wave shape)		±160	
10/1000 μs (GR-1089-CORE, 10/1000 μs voltage wave shape)			
Non-repetitive peak on-state current (see Notes 2, 3 and 4)			
20 ms, 50 Hz (full sine wave)		55	
16.7 ms, 60 Hz (full sine wave)		60	Α
1000 s, 50 Hz or 60 Hz a.c.		2.2	
Initial rate of rise of on-state currrent, exponential current ramp. Maximum ramp value < 200 A	di _T /dt	400	A/μs
Junction temperature	TJ	-40 to +150	°C
Storage temperature range	T _{stg}	-65 to +150	°C

- NOTES: 1. See Figure 6 for voltages at other temperatures.
 - 2. Initially the device must be in thermal equilibrium with $T_J = 25$ °C.
 - 3. The surge may be repeated after the device returns to its initial conditions.
 - 4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 5 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz or 60 Hz a.c. (see note 5)	I _{T(OV)M}		
0.03 s		60	
0.07 s		40	\ A rmo
1.6 s		8	A rms
5.0 s		7	
1000 s		2.2	

NOTE: 5. Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A250H3BJ silicon die. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short-circuit fault mode. In the short-circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open-circuit fault mode developed.

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Electrical Characteristics, $T_A = 25$ °C (Unless Otherwise Noted)

	Parameter	Test Conditions		Min	Тур	Max	Unit
I _{DRM}	Repetitive peak off-state current	V _D = V _{DRM}	T _A = 25 °C T _A = 85 °C	1		±5 ±10	μA
V _(BO)	Breakover voltage	$dv/dt = \pm 250 \text{ V/ms}, \text{ R}_{SOURCE} = 300 \Omega$				+125 -250	V
I _(BO)	Breakover current	$dv/dt = \pm 250 \text{ V/ms}, \text{ R}_{SOURCE} = 300 \Omega$		±150		±600	mA
V _T	On-state voltage	$I_T = \pm 5 \text{ A, t}_w = 100 \mu \text{s}$				±3	V
I _H	Holding current	$I_T = \pm 5 \text{ A, di/dt} = \pm 30 \text{ mA/ms}$		±150		±600	mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp Maximum ramp value < 0.85V _{DRM}		±5			kV/µs
Co	Off-state capacitance	$f = 1 \text{ MHz}, V_d = 1 \text{ V rms}$ $V_D =$	2 V			72	pF

Thermal Characteristics

	Parameter	Test Conditions	Min	Тур	Max	Unit
$R_{ heta JA}$	Junction to ambient thermal resistance	EIA/JESD51-3 PCB, I _T = I _{TSM(1000)} (see Note 6)			113	- °C/W
		265 mm x 210 mm populated line card, 4-layer PCB, I _T = I _{TSM(1000)}		50		

NOTE: 6. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

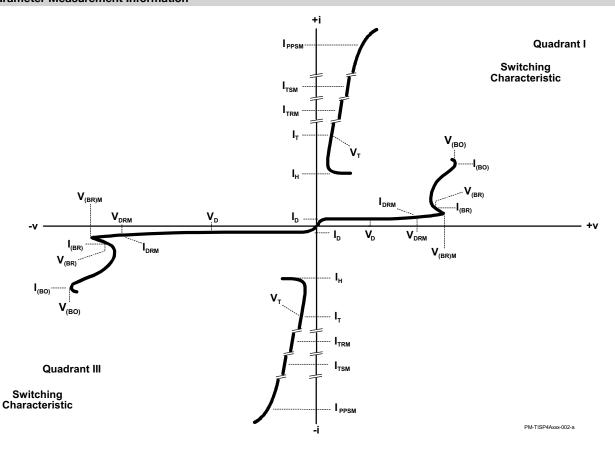
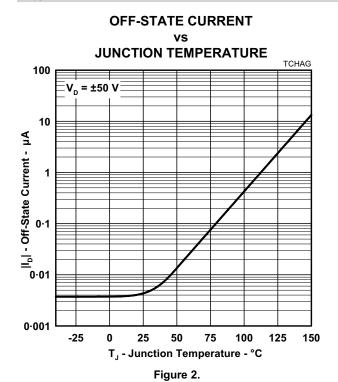


Figure 1. Voltage-Current Characteristic for the Ring and Ground Terminals All Measurements are Referenced to the Ground Terminal

Typical Characteristics



NORMALIZED BREAKOVER VOLTAGE **JUNCTION TEMPERATURE**

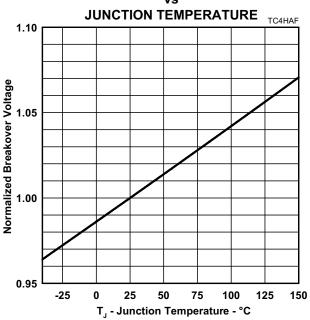
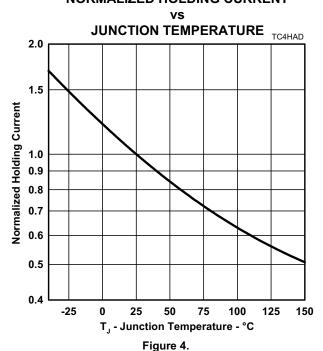


Figure 3.

NORMALIZED HOLDING CURRENT



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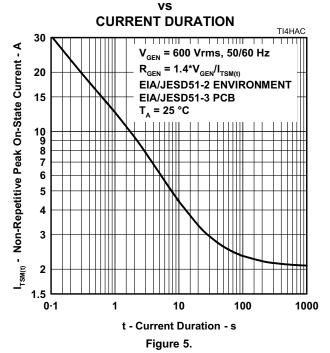
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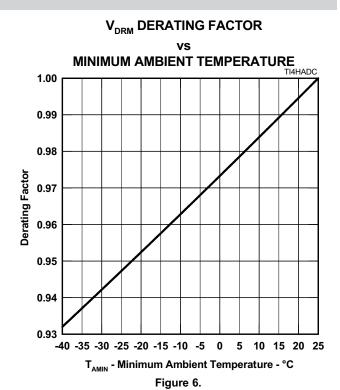
TISP4A250H3BJ Overvoltage Protector

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Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT





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Applications Information

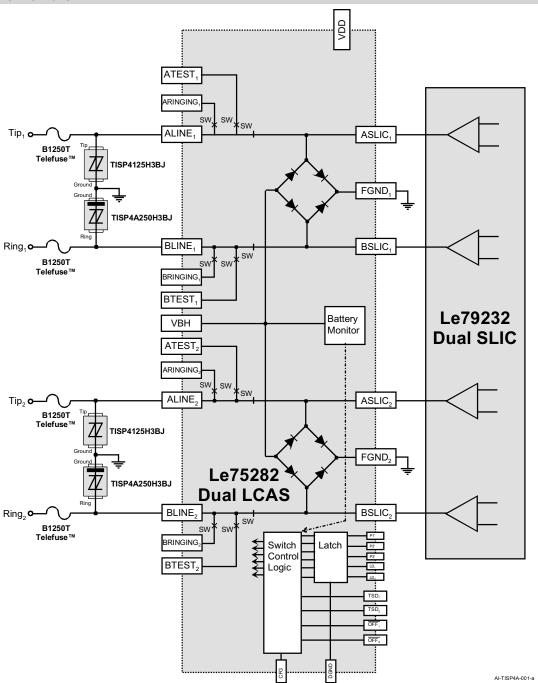


Figure 7. Typical Application Circuit

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